TLV320AIC33EVM and TLV320AIC33EVM-PDK User's Guide

This user's guide describes the characteristics, operation, and use of the TLV320AIC33EVM, both by itself and as part of the TLV320AIC33EVM-PDK. This evaluation module (EVM) is a complete stereo audio codec with several inputs and outputs, extensive audio routing, mixing and effects capabilities. A complete circuit description, schematic diagram and bill of materials are also included.

The following related documents are available through the Texas Instruments web site at www.ti.com.

EVM-Compatible Device Data Sheets

Device	Literature Number
TLV320AIC33	SLAS480
TAS1020B	SLES025
REG1117-3.3	SBVS001
TPS767D318	SLVS209
SN74LVC125A	SCAS290
SN74LVC1G125	SCES223
SN74LVC1G07	SCES296

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1 EVM Overview

1.1 Features

- Full-featured evaluation board for the TLV320AIC33 stereo audio codec.
- Modular design for use with a variety of digital signal processor (DSP) and microcontroller interface boards.

The TLV320AIC33EVM-PDK is a complete evaluation kit, which includes a universal serial bus (USB)-based motherboard and evaluation software for use with a personal computer running the Microsoft Windows™ operating system (Win2000 or XP).

1.2 Introduction

The TLV320AIC33EVM is in Texas Instruments' modular EVM form factor, which allows direct evaluation of the device performance and operating characteristics, and eases software development and system prototyping. This EVM is compatible with the 5-6K Interface Evaluation Module (SLAU104) and the HPA-MCUINTERFACE (SLAU106) from Texas Instruments and additional third-party boards which support TI's Modular EVM format.

The TLV320AIC33EVM-PDK is a complete evaluation/demonstration kit, which includes a USB-based motherboard called the USB-MODEVM Interface board and evaluation software for use with a personal computer running the Microsoft Windows operating systems.

2 Analog Interface

For maximum flexibility, the TLV320AIC33EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J13 and J14. These headers/sockets provide access to the analog input and output pins of the device. Consult Samtec at www.samtec.com or call 1-800-SAMTEC-9 for a variety of mating connector options. Table 1 summarizes the analog interface pinout for the TLV320AIC33EVM..

Table 1. Analog Interface Pin Out

PIN NUMBER	SIGNAL	DESCRIPTION
J13.1	HPLCOM	High Power Output Driver (Left Minus or Multifunctional)
J13.2	HPLOUT	High Power Output Driver (Left Plus)
J13.3	HPRCOM	High Power Output Driver (Right Minus or Multifunctional)
J13.4	HPROUT	High Power Output Driver (Right Plus)
J13.5	LINE1LM	MIC1 or LINE1 Analog Input (Left Minus or Multifunctional)
J13.6	LINE1LP	MIC1 or LINE1 Analog Input (Left Plus or Multifunctional)
J13.7	LINE1RM	MIC1 or LINE1 Analog Input (Right Minus or Multifunctional)
J13.8	LINE1RP	MIC1 or LINE1 Analog Input (Right Plus or Multifunctional)
J13.9	AGND	Analog Ground
J13.10	MIC3L	MIC3 Input (Left or Multifunctional)
J13.11	AGND	Analog Ground
J13.12	MIC3R	MIC3 Input (Right or Multifunctional)
J13.13	AGND	Analog Ground
J13.14	MICBIAS	Microphone Bias Voltage Output
J13.15	NC	Not Connected
J13.16	MICDET	Microphone Detect
J13.17	AGND	Analog Ground
J13.18	NC	Not Connected
J13.19	AGND	Analog Ground
J13.20	NC	Not Connected
J14.1	LINE2RM	MIC2 or LINE2 Analog Input (Right Minus or Multifunctional)
J14.2	LINE2RP	MIC2 or LINE2 Analog Input (Right Plus or Multifunctional)
J14.3	LINE2LM	MIC2 or LINE2 Analog Input (Left Minus or Multifunctional)
J14.4	LINE2RP	MIC2 or LINE2 Analog Input (Left Plus or Multifunctional)
J14.5	MONO_LOP	Mono Line Output (Plus)
J14.6	MONO_LOM	Mono Line Output (Minus)
J14.7	LEFT_LOP	Left Line Output (Plus)
J14.8	LEFT_LOM	Left Line Output (Minus)
J14.9	AGND	Analog Ground
J14.10	RIGHT_LOP	Right Line Output (Plus)
J14.11	AGND	Analog Ground
J14.12	RIGHT_LOM	Right Line Output (Minus)
J14.13	AGND	Analog Ground
J14.14	NC	Not Connected
J14.15	NC	Not Connected
J14.16	NC	Not Connected
J14.17	AGND	Analog Ground
J14.18	NC	Not Connected
J14.19	AGND	Analog Ground
J14.20	NC	Not Connected

In addition to the analog headers, the analog inputs and outputs may also be accessed through alternate connectors, either screw terminals or audio jacks. The stereo microphone input is also tied to J6 and the stereo headphone output (the HP set of outputs) is available at J7.

Table 2 summarizes the screw terminals available on the TLV320AIC33EVM.

Table 2. Alternate Analog Connectors

DESIGNATOR	PIN 1	PIN 2	PIN3
J1	LINE1LP	LINE1LM	
J2	LINE1RP	LINE1RM	
J3	LINE2LP	LINE2LM	
J4	LINE2RP	LINE2RM	
J5	MIC3 IN LEFT	MIC3 IN RIGHT	AGND
J11	(+) HPLOUT	(-) HPLCOM	
J12	(+) HPROUT	(-) HPRCOM	

3 Digital Interface

The TLV320AIC33EVM is designed to easily interface with multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J16 and J17. These headers/sockets provide access to the digital control and serial data pins of the device. Consult Samtec at www.samtec.com or call 1-800- SAMTEC-9 for a variety of mating connector options. Table 3 summarizes the digital interface pinout for the TLV320AIC33EVM.

Table 3. Digital Interface Pin Out

PIN NUMBER	SIGNAL	DESCRIPTION
J16.1	NC	Not Connected
J16.2	GPIO1	General Purpose Input/Output #1
J16.3	SCLK	SPI Serial Clock
J16.4	DGND	Digital Ground
J16.5	NC	Not Connected
J16.6	GPIO2	General Purpose Input/Output #2
J16.7	/SS	SPI Chip Select
J16.8	RESET INPUT	Reset signal input to AIC33EVM
J16.9	NC	Not Connected
J16.10	DGND	Digital Ground
J16.11	MOSI	SPI MOSI Slave Serial Data Input
J16.12	SPI SELECT	Select Pin (SPI vs I^2C Control Mode)
J16.13	MISO	SPI MISO Slave Serial Data Output
J16.14	AIC33 $\overline{\text{RESET}}$	Reset
J16.15	NC	Not Connected
J16.16	SCL	I^2C Serial Clock
J16.17	NC	Not Connected
J16.18	DGND	Digital Ground
J16.19	NC	Not Connected
J16.20	SDA	I^2C Serial Data Input/Output
J17.1	NC	Not Connected
J17.2	NC	Not Connected
J17.3	BCLK	Audio Serial Data Bus Bit Clock (Input/Output)
J17.4	DGND	Digital Ground

Table 3. Digital Interface Pin Out (continued)

PIN NUMBER	SIGNAL	DESCRIPTION
J17.5	NC	Not Connected
J17.6	NC	Not Connected
J17.7	WCLK	Audio Serial Data Bus Word Clock (Input/Output)
J17.8	NC	Not Connected
J17.9	NC	Not Connected
J17.10	DGND	Digital Ground
J17.11	DIN	Audio Serial Data Bus Data Input (Input)
J17.12	NC	Not Connected
J17.13	DOUT	Audio Serial Data Bus Data Output (Output)
J17.14	NC	Not Connected
J17.15	NC	Not Connected
J17.16	SCL	I^2C Serial Clock
J17.17	MCLK	Master Clock Input
J17.18	DGND	Digital Ground
J17.19	NC	Not Connected
J17.20	SDA	I^2C Serial Data Input/Output

Note that J17 comprises the signals needed for an I^2S™ serial digital audio interface; the control interface (I^2C™ and $\overline{\text{RESET}}$) signals are routed to J16. I^2C is actually routed to both connectors; however, the device is connected only to J16.

4 Power Supplies

J15 provides connection to the common power bus for the TLV320AIC33EVM. Power is supplied on the pins listed in Table 4.

Table 4. Power Supply Pin Out

SIGNAL	PIN NUMBER		SIGNAL
NC	J15.1	J15.2	NC
+5VA	J15.3	J15.4	NC
DGND	J15.5	J15.6	AGND
DVDD (1.8V)	J15.7	J15.8	NC
IOVDD (3.3V)	J15.9	J15.10	NC

The TLV320AIC33EVM-PDK motherboard (the USB-MODEVM Interface board) supplies power to J15 of the TLV320AIC33EVM. Power for the motherboard is supplied either through its USB connection or via terminal blocks on that board.

4.1 Stand-Alone Operation

When used as a stand-alone EVM, power can be applied to J15 directly, making sure to reference the supplies to the appropriate grounds on that connector.

CAUTION

Verify that all power supplies are within the safe operating limits shown on the TLV320AIC33 data sheet before applying power to the EVM.

4.2 USB-MODEVM Interface Power

The USB-MODEVM Interface board can be powered from several different sources:

- USB
- 6VDC-10VDC AC/DC external wall supply (not included)
- Lab power supply

When powered from the USB connection, JMP6 should have a shunt from pins 1–2 (this is the default factory configuration). When powered from 6V-10VDC, either through the J8 terminal block or J9 barrel jack, JMP6 should have a shunt installed on pins 2–3. If power is applied in any of these ways, onboard regulators generate the required supply voltages and no further power supplies are necessary.

If lab supplies are used to provide the individual voltages required by the USB-MODEVM Interface, JMP6 should have no shunt installed. Voltages are then applied to J2 (+5VA), J3 (+5VD), J4 (+1.8VD), and J5 (+3.3VD). The +1.8VD and +3.3VD can also be generated on the board by the onboard regulators from the +5VD supply; to enable this configuration, the switches on SW1 need to be set to enable the regulators by placing them in the ON position (lower position, looking at the board with text reading right-side up). If +1.8VD and +3.3VD are supplied externally, disable the onboard regulators by placing SW1 switches in the OFF position.

Each power supply voltage has an LED (D1-D7) that lights when the power supplies are active.

5 EVM Operation

This section provides information on the analog input and output, digital control, and general operating conditions of the TLV320AIC33EVM.

5.1 Analog Input

The analog input sources can be applied directly to J13 (top or bottom side) or through signal conditioning modules available for the modular EVM system.

The analog inputs may also be accessed through J6 and and screw terminals J1, J2, and J3.

5.2 Analog Output

The analog outputs from the TLV320AIC33 are available on J13 and J14 (top or bottom). They also may be accessed through J4, J5, J7, J11,and J12.

5.3 Digital Control

The digital control signals can be applied directly to J16 and J17 (top or bottom side). The modular TLV320AIC33EVM can also be connected directly to a DSP interface board, such as the 5-6KINTERFACE or HPA-MCUINTERFACE, or to the USB-MODEVM Interface board if purchased as part of the TLV320AIC33EVM-PDK. See the product folder for this EVM or the TLV320AIC33 for a current list of compatible interface and/or accessory boards.

5.4 Default Jumper Locations

Table 5 provides a list of jumpers found on the EVM and their factory default conditions.

Table 5. List of Jumpers

JUMPER	DEFAULT POSITION	JUMPER DESCRIPTION
JMP1	2-3	When connecting 2-3, mic bias comes from the MICBIAS pin on the device; when connecting 1-2, mic bias is supplied from the power supply through a resistor, which the user must install.
JMP2	Installed	Connects on-board Mic to Left Microphone Input.
JMP3	Installed	Connects on-board Mic to Right Microphone Input.
JMP4	Installed	Provides a means of measuring IOVDD current.
JMP5	Installed	Provides a means of measuring AVDD_ADC current.
JMP6	Installed	Provides a means of measuring DVDD current.
JMP7	Installed	Provides a means of measuring DRVDD current.
JMP8	Installed	Provides a means of measuring AVDD_DAC current.
JMP9	Installed	Connects Analog and Digital Grounds.
JMP10	3-5	When connecting 3 to 5, I^2C is selected as control mode; when connecting 1 to 3, SPI is selected as control mode. When connecting 3 to 4, mode selection can be made by a logic level at J16.12
JMP11	3-5	In I^2C control mode, this jumper sets the state of A0. When connecting 3 to 5, A0 = 0; when connecting 1 to 3, A0 = 1. In SPI control mode, connecting 3 to 4, SPI /SS is provided from J16.2
JMP12	3-5	In I^2C control mode, this jumper sets the state of A1. When connecting 3 to 5, A1 = 0; when connecting 1 to 3, A1 = 1. In SPI control mode, connecting 3 to 4, SPI SCLK is provided from J16.3
JMP13	Installed	When installed, shorts across the output capacitor on HPLOUT; remove this jumper if using AC-coupled output drive
JMP14	Installed	When installed, shorts across the output capacitor on HPLCOM; remove this jumper if using AC-coupled output drive
JMP15	Installed	When installed, shorts across the output capacitor on HPROUT; remove this jumper if using AC-coupled output drive
JMP16	Installed	When installed, shorts HPLCOM and HPRCOM. Use only if these signals are set to constant VCM.
JMP17	Installed	When installed, shorts across the output capacitor on HPRCOM; remove this jumper if using AC-coupled output drive
JMP18	Open	Selects on-board EEPROM as Firmware Source.
JMP19	Open	When installed, allows the USB-MODEVM to hardware reset the device under user control

6 Kit Operation

The following section provides information on using the TLV320AIC33EVM-PDK, including set up, program installation, and program usage.

6.1 TLV320AIC33EVM-PDK Block Diagram

A block diagram of the TLV320AIC33EVM-PDK is shown in Figure 1. The evaluation kit consists of two circuit boards connected together. The motherboard is designated as the USB-MODEVM Interface board, while the daughtercard is the TLV320AIC33EVM described previously in this manual.

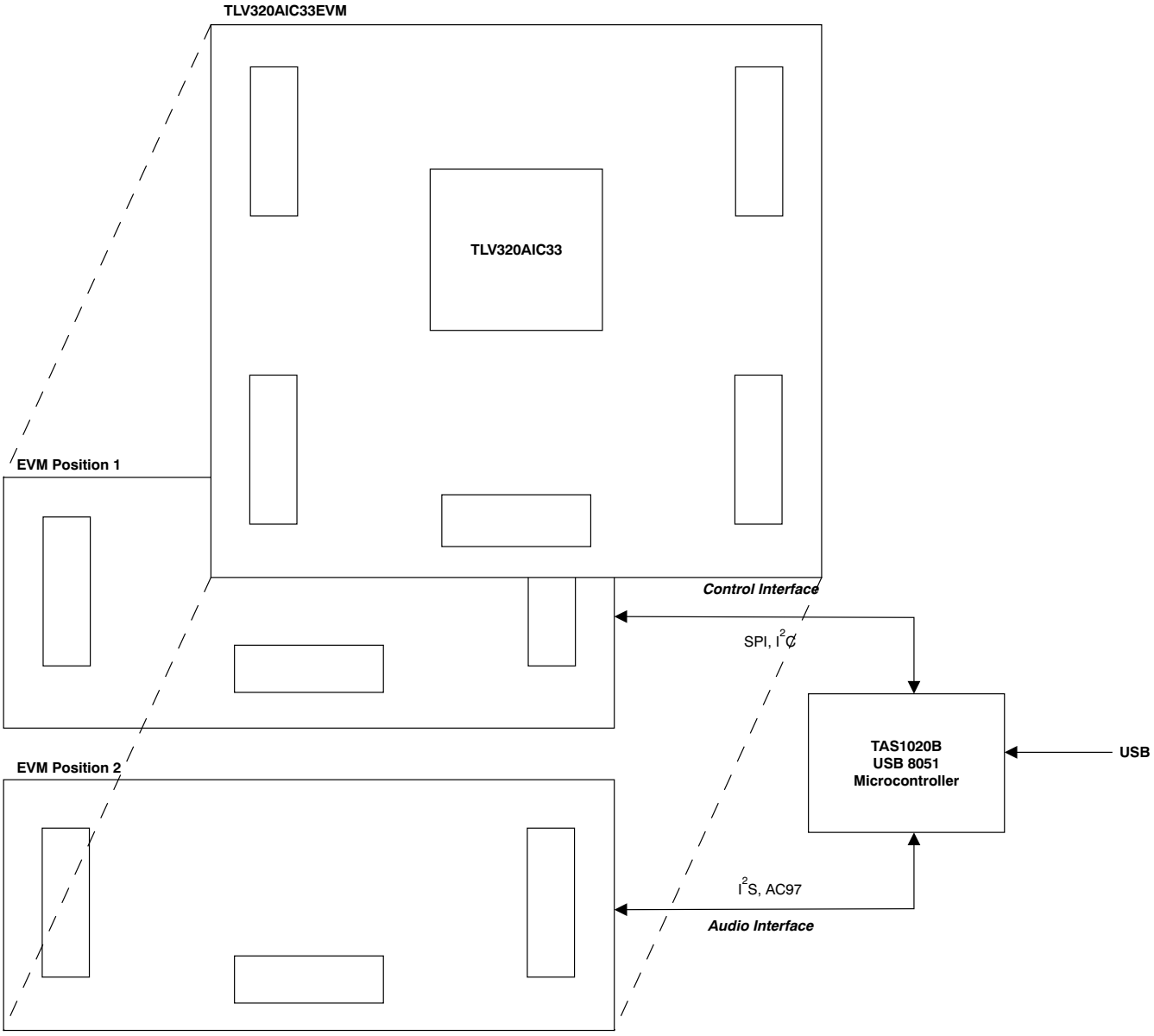


Figure 1. TLV320AIC33EVM-PDK Block Diagram

The USB-MODEVM Interface board is intended to be used in USB mode, where control of the installed EVM is accomplished using the onboard USB controller device. Provision is made, however, for driving all the data buses (I^2C, SPI™, I^2S/AC97) externally. The source of these signals is controlled by SW2 on the USB-MODEVM. Refer to Table 6 for details on the switch settings.

Table 6. USB-MODEVM SW2 Settings

SW-2 SWITCH NUMBER	LABEL	SWITCH DESCRIPTION
1	A0	USB-MODEVM EEPROM I²C Address A0 ON: A0 = 0 OFF: A0 = 1
2	A1	USB-MODEVM EEPROM I²C Address A1 ON: A1 = 0 OFF: A1 = 1
3	A2	USB-MODEVM EEPROM I²C Address A2 ON: A2 = 0 OFF: A2 = 1
4	USB I²S	I²S Bus Source Selection ON: I²S Bus connects to TAS1020 OFF: I²S Bus connects to USB-MODEVM J14
5	USB MCK	I²S Bus MCLK Source Selection ON: MCLK connects to TAS1020 OFF: MCLK connects to USB-MODEVM J14
6	USB SPI	SPI Bus Source Selection ON: SPI Bus connects to TAS1020 OFF: SPI Bus connects to USB-MODEVM J15
7	USB RST	RST Source Selection ON: EVM Reset Signal comes from TAS1020 OFF: EVM Reset Signal comes from USB-MODEVM J15
8	EXT MCK	External MCLK Selection ON: MCLK Signal is provided from USB-MODEVM J10 OFF: MCLK Signal comes from either selection of SW2-5

For use with the TLV320AIC33EVM, SW-2 positions 1 through 7 should be set to ON, while SW-2.8 should be set to OFF.

6.2 Installation

Ensure that the TLV320AIC33EVM is installed on the USB-MODEVM Interface board, aligning J13, J14, J15, J16, J17 with the corresponding connectors on the USB-MODEVM.

Place the CD-ROM into your PC CD-ROM drive. Locate the **Setup** program on the disk, and run it. The Setup program will install the TLV320AIC33 Evaluation software on your PC.

After the main program is installed, the NI-VISA Runtime installer will automatically run. This software allows the program to communicate with USB.

When the installation completes, click *Finish* on the TLV320AIC33EVM installer window. You may be prompted to restart your computer.

When installation is complete, attach a USB cable from your PC to the USB-MODEVM Interface board. As configured at the factory, the board will be powered from the USB interface, so the power indicator LEDs on the USB-MODEVM should light. Once this connection is established, launch the TLV320AIC33 Evaluation software on your PC.

The software should automatically find the TLV320AIC33EVM, and a screen similar to the one in Figure 2 should appear.

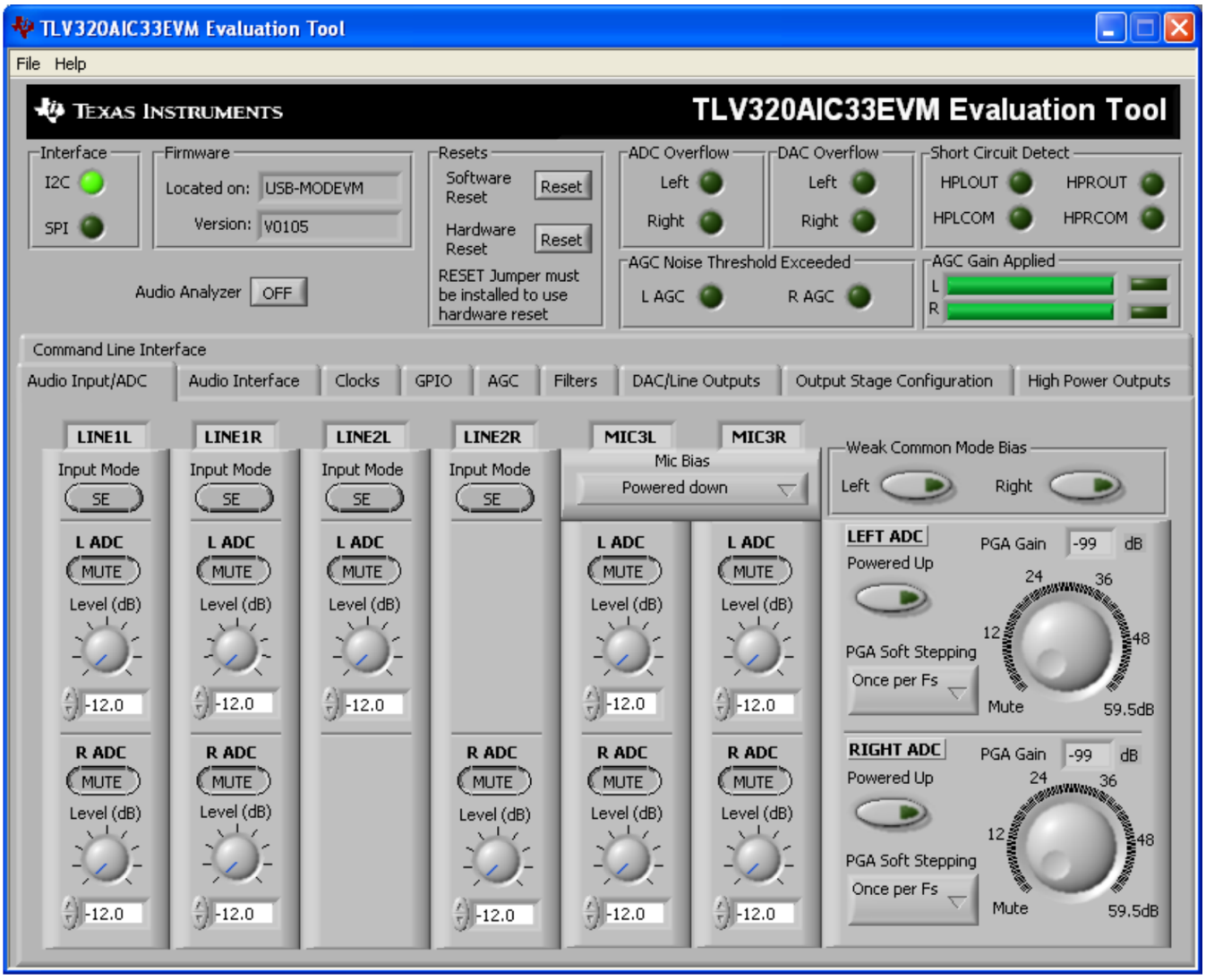


Figure 2. Default Software Screen

6.3 USB-MODEVM Interface Board

The simple diagram shown in Figure 1 shows only the basic features of the USB-MODEVM Interface board. The board is built around a TAS1020B streaming audio USB controller with an 8051-based core. The board features two positions for modular EVMs, or one double-wide serial modular EVM may be installed.

Since the TLV320AIC33EVM is a double-wide modular EVM, it is installed with connections to both EVM positions, which connects the TLV320AIC33 digital control interface to the I^2C port realized using the TAS1020B, as well as the TAS1020B digital audio interface..

In the factory configuration, the board is ready to use with the TLV320AIC33EVM. To view all the functions and configuration options available on the USB-MODEVM board, see the USB-MODEVM Interface Board schematic in Appendix B.

6.4 Program Description

After the TLV320AIC33EVM-PDK software installation (described in Section 6.2) is complete, evaluation and development with the TLV320AIC33 can begin.

6.5 Interface Selection

When the program first starts up, a small window (Figure 3) appears that gives two choices for the control interface: I^2C or SPI. Click on the interface that will be used by the EVM, as selected by the jumper settings detailed in Table 5.

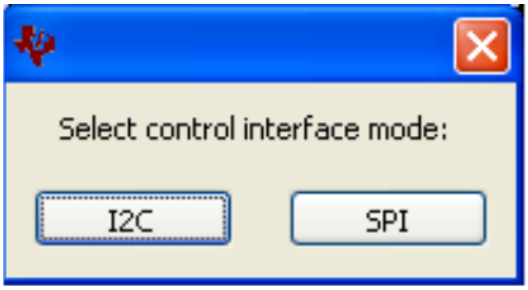


Figure 3. Interface Selection Window

If the I^2C interface is selected, a second window then appears which allows for selecting the address of the TLV320AIC33. This window (see Figure 4) has two checkboxes for setting the state of **A0** and **A1**. Note that this address should correspond to the jumper settings selected as described in Table 5.

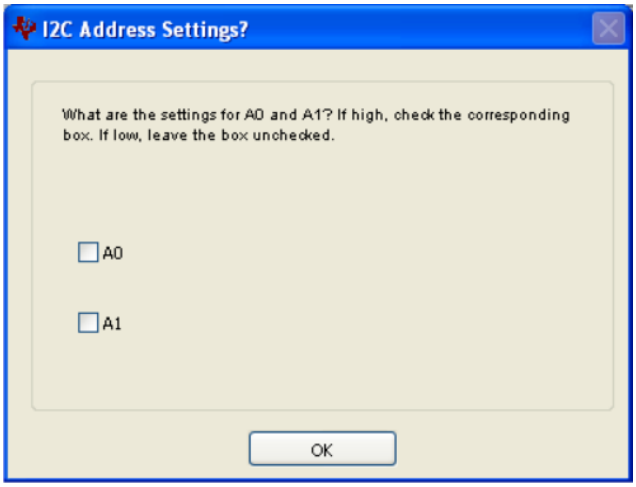


Figure 4. I^2C Address Selection Window

6.6 Indicators and Main Screen Controls

Figure 2 illustrates the indicators and controls near the top of the screen, and a large tabbed interface below. This section will discuss the controls above this tabbed section.

At the top left of the screen is an **Interface** indicator. This indicator shows which interface is selected for controlling the TLV320AIC33 , either I^2C or SPI; it is lit after the program begins.

To the right of the Interface indicator is a group box called **Firmware**. This box indicates where the firmware being used is operating from—in this release, the firmware is on the USB-MODEVM, so you should see *USB-MODEVM* in the box labeled **Located On:**. The version of the firmware appears in the **Version** box below this.

To the right, the next group box contains controls for resetting the TLV320AIC33. A software reset can be done by writing to a register in the TLV320AIC33, and this is accomplished by pushing the button labeled **Software Reset**. The TLV320AIC33 also may be reset by toggling a pin on the TLV320AIC33, which is done by pushing the **Hardware Reset** button.

CAUTION

In order to perform a hardware reset, the RESET jumper (JMP19) must be installed and SW2-7 on the USB-MODEVM must be turned OFF. Failure to do either of these steps results in not generating a hardware reset or causing unstable operation of the EVM, which may require cycling power to the USB-MODEVM.

The **ADC Overflow** and **DAC Overflow** indicators light when the overflow flags are set in the TLV320AIC33. These indicators, as well as the other indicators on this panel, are updated only when the software's front panel is inactive, once every 20ms. Below these indicators are other indicators that show when the AGC noise threshold is exceeded. To the far right on this screen, the short-circuit indicators show when a short-circuit condition is detected, if this feature has been enabled. Below the short-circuit indicators is a bar graph that shows the amount of gain which has been applied by the AGC, and indicators that light when the AGC is saturated.

6.6.1 Audio Analyzer

Near the left side of the screen is a button labeled **Audio Analyzer**, and this button can be set to ON or OFF. Pressing the button to turn it *ON* opens another window (see Figure 5). This feature provides the ability to generate signals to send to the TLV320AIC33 DACs as well as viewing and analyzing signals read by the TLV320AIC33 ADCs. This ability to view and process the real-time streaming USB audio is a demanding task. Use of the Audio Analyzer feature requires a computer with at least 512MB of memory and reasonable processor speed (> 1GHz); computers with inadequate resources could still use the Audio Analyzer to generate signals for the DACs, but will be unable to process signals from the ADCs because the FFT, distortion analysis, and signal-to-noise ratio analysis will not be able to keep up with the data processing requirements.

The Audio Analyzer features two tabs. The front tab, shown in Figure 5 and titled *Generator*, creates digital waveforms to send to the DACs. When first started, the function will be set to *SNR (Output Zeros)* which feeds only zero codes to the DAC. This is commonly done to test for the noise floor of the DAC.

The second function available is *THD (-1dB sinewave)*. This function sends a sinewave at a coherent frequency to the 44.1kHz sample rate to the DACs; this is commonly used for testing THD+N.

These first two functions do not require any further settings; therefore, the frequency and amplitude knobs below the function selector are not used. Selecting a function of *Function Generator* allows the choice of waveform shape by using the pull-down menu next to the function selector, and the frequency and amplitude of that signal can be varied using the knobs below.

The output waveforms for both left and right channels are displayed in the graph at the bottom of this screen.

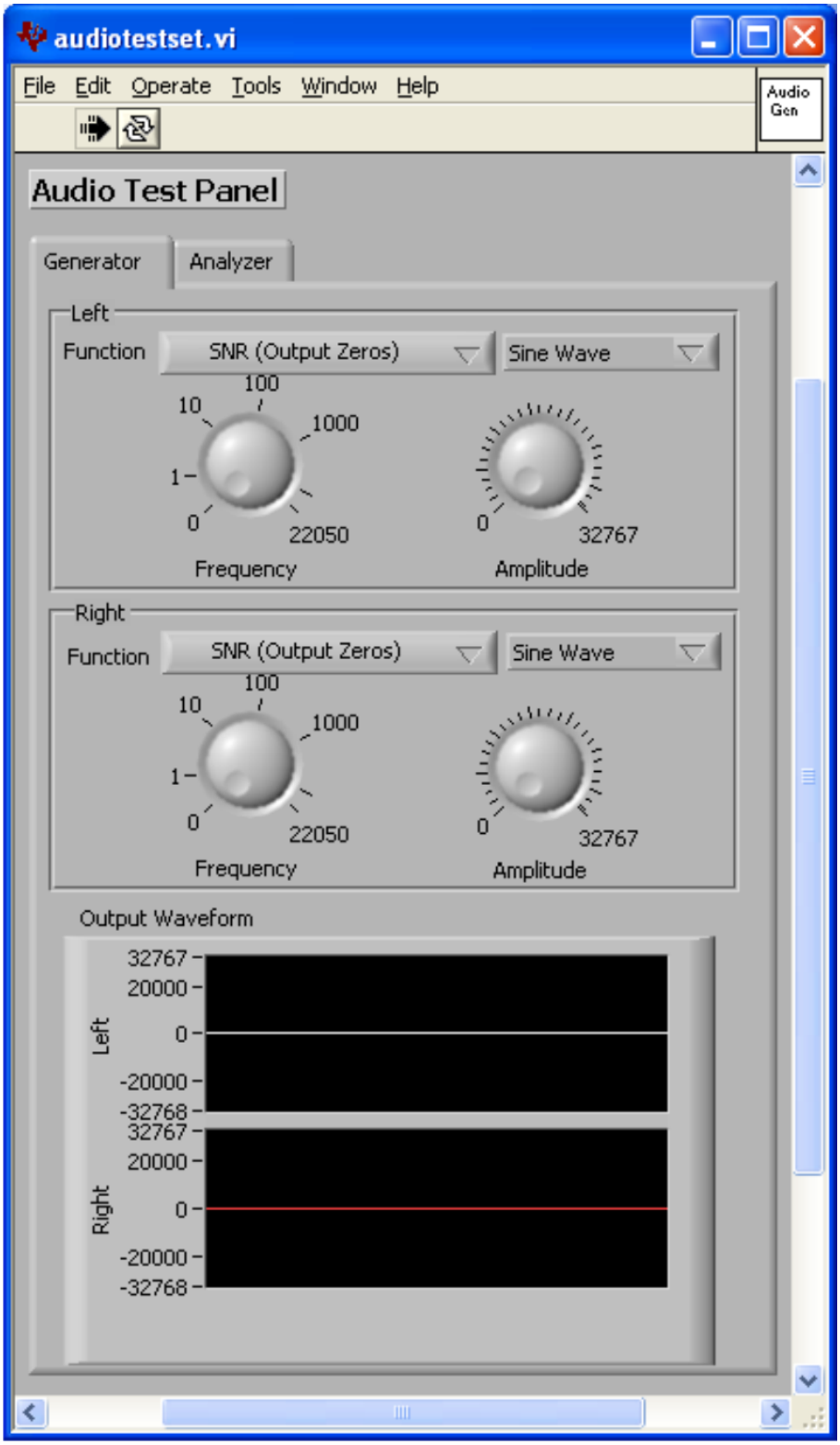


Figure 5. Audio Generator Screen

The second tab, titled **Analyzer** (Figure 6), handles the display and analysis of data from the ADCs.

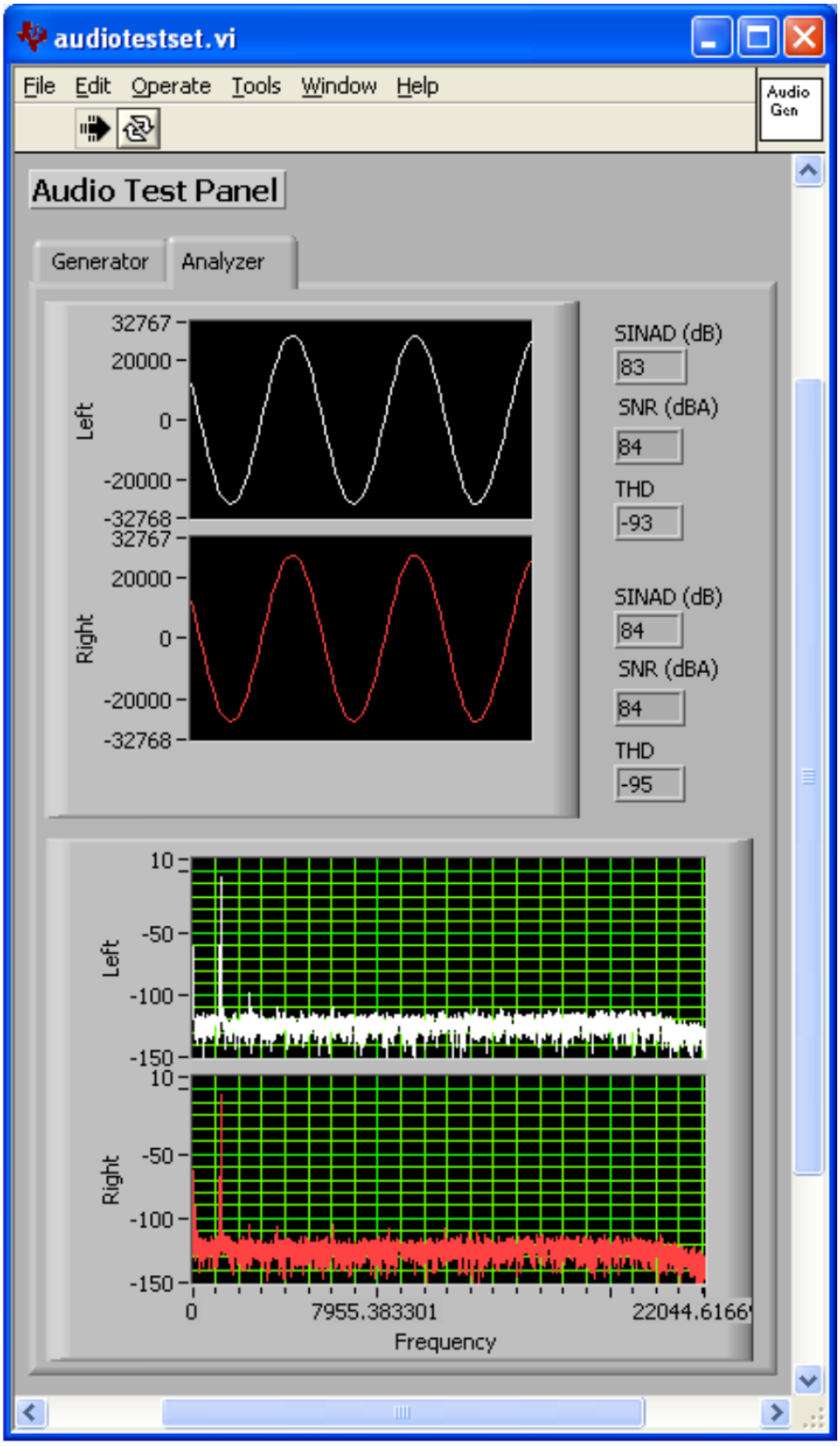


Figure 6. Audio Analyzer Screen

The analyzer screen features a graph of the input signals, both left and right channels, in a time domain display at the top of the screen, and in the frequency domain (FFT) at the bottom of the screen.

Next to the time domain plots, calculated values of SINAD, SNR, and THD are shown. These values are all expressed in dB relative to the full-scale of the TLV320AIC33. Note that the SNR number shown is A-weighted.

In Figure 6, a sine wave generated by the TLV320AIC33 DACs is fed through the high power drivers and back into the ADC and the resulting FFTs can be seen. Note that this is a full analog loopback test case, so the measured numbers show the combined performance of the DAC, drivers, and ADC. There is also no post-DAC filtering; as noted in the data sheet, this may degrade measurements even though there is no audible noise.

6.7 Audio Input/ADC Tab

The Audio Input/ADC Tab is laid out like an audio mixing console. Each input channel has a vertical strip that corresponds to that channel. *LINE1L* and *LINE1R* input strips have controls to route that input to either the left or right ADC input; by default, all inputs are muted when the TLV320AIC33 is powered up. To route an input to the ADC, first click on the **MUTE** button in the input channel strip which corresponds to the ADC input channel you want that input to go to—the caption on the button will change to *ACTIVE*. The level of the input channel routed to that particular ADC channel can then be adjusted using the **Level** knob below the **MUTE/ACTIVE** button. See Figure 7.

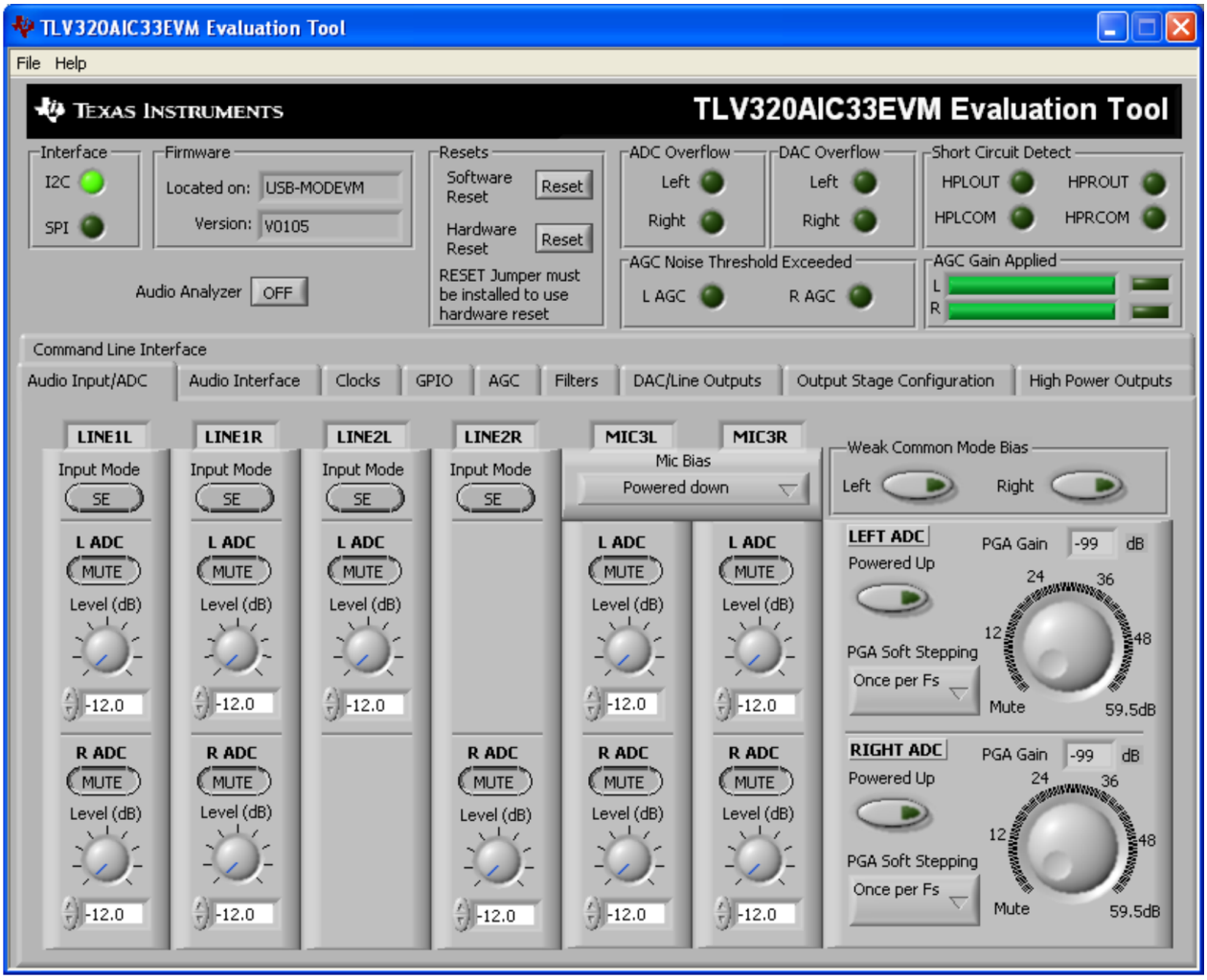


Figure 7. Audio Input Tab

Similarly, the *LINE2L* and *LINE2R* inputs can be routed to the ADC. However, note that these inputs do not have the choice to route to either ADC channel; they can only be configured to connect to the corresponding ADC input.

The *MIC3L* and *MIC3R* inputs are similar to the *LINE1L* and *LINE1R* inputs in that they can be routed to either ADC input channel. Control of the mic bias is accomplished by using the pull-down menu at the top of these channel strips. The mic bias can either be powered down or set to 2.0V, 2.5V, or the power supply voltage of the ADC (AVDD_ADC).

To use the on-board microphone, JMP2 and JMP3 must be installed and nothing should be plugged into J6. In order for the mic bias settings in the software to take effect, JMP1 should be set to connect positions 2 and 3, so that mic bias is controlled by the TLV320AIC33.

In the upper right of this tab are controls for **Weak Common Mode Bias**. Enabling these controls will result in unselected inputs to the ADC channels to be weakly biased to the ADC common mode voltage.

Below these controls are the controls for the ADC PGA—the master volume controls for the ADC inputs. Each channel of the ADC can be powered up or down as needed using the **Powered Up** buttons. PGA soft-stepping for each channel is selected using the control below this. The large knobs set the actual **ADC PGA Gain**; at the extreme counterclockwise rotation, the channel is muted. Rotating the knob clockwise increases the PGA gain.

6.8 Audio Interface Tab

The Audio Interface tab (Figure 8) sets up the audio data interface to the TLV320AIC33. For use with the PC software and the USB-MODEVM, the default settings should be used. If using an external I^2S source, or other data source, the interface mode may be selected using the **Transfer Mode** control—selecting either I^2S mode, DSP mode, or Right- or Left-Justified modes. Word length can be selected using the **Word Length** control, and the bit clock rate can also be selected using the **Bit Clock** rate control. The **Data Word Offset**, used in TDM mode (see the product datasheet) can also be selected on this tab.

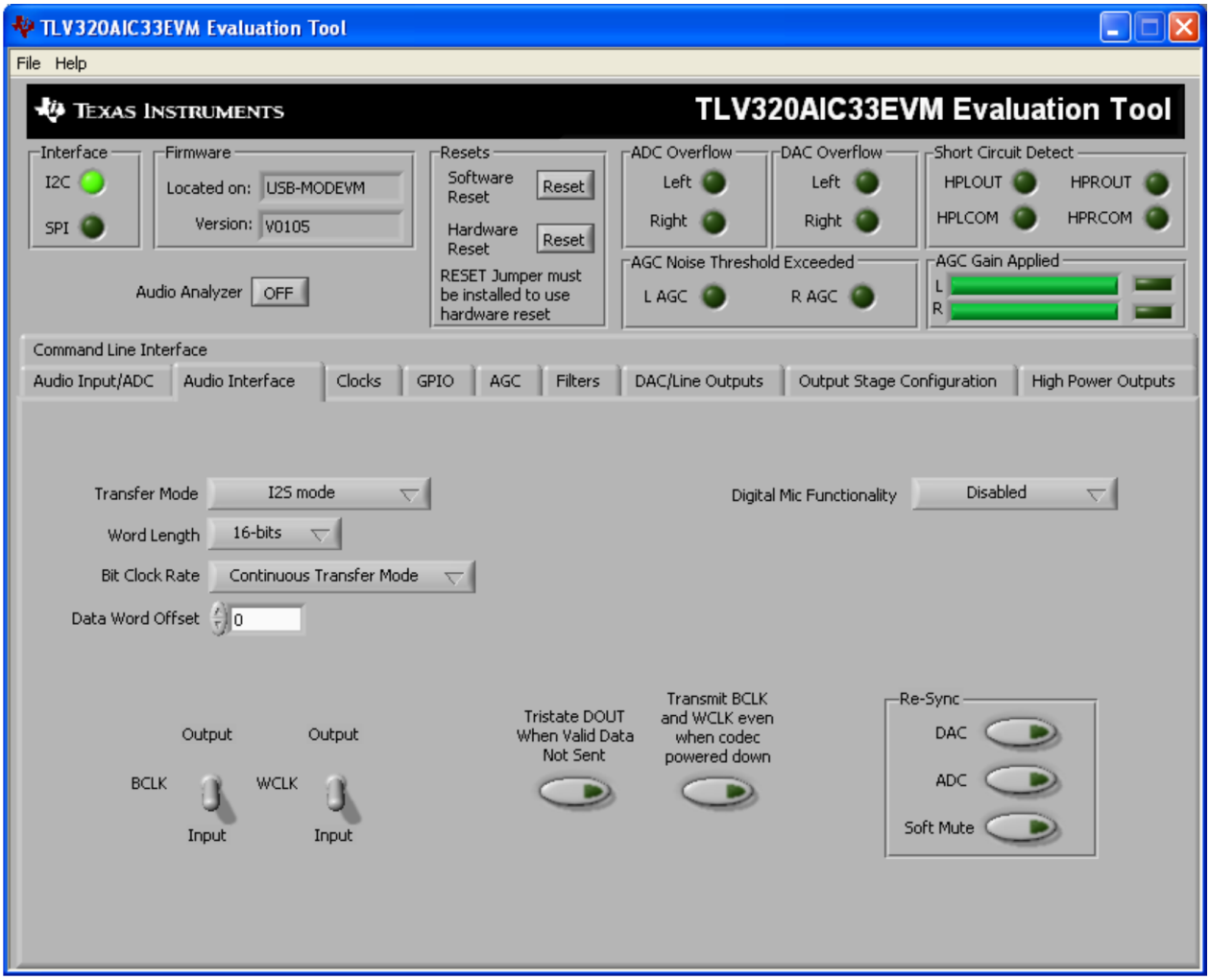


Figure 8. Audio Interface Tab

Along the bottom of this tab are controls for choosing the **BLCK** and **WCLK** as being either inputs or outputs, as well as options for tristating the DOUT line when there is not valid data and transmitting BLCK and WCLK when the codec is powered down.

Re-sync of the audio bus is enabled using the controls in the lower right corner of this screen. Re-sync is done if the group delay changes by more than ±FS/4 for the ADC or DAC sample rates (see the TLV320AIC33 datasheet). The channels can be soft muted when doing the re-sync if the **Soft Mute** button is enabled.

In the upper right corner of this tab is the **Digital Mic Functionality** control. The TLV320AIC33 can accept a data stream from a digital microphone, which would have its clock pin connected to the TLV320AIC33 GPIO1 pin, and the mic data connected to the GPIO2 pin. Refer to section Section 6.10 for a discussion of setting the GPIO pin options. The TLV320AIC33 can provide a modulator clock to the digital microphone with oversampling ratios (OSR) of 128, 64, or 32. For a detailed discussion of how to connect a digital microphone on this platform, refer to the application note *Using the Digital Microphone Function on TLV320AIC33 with AIC33EVM/USB-MODEVM System* (literature number SLAA275), available for download at www.ti.com.

6.9 Clocks Tab

The TLV320AIC33 has a very flexible scheme for generating the clock sources for ADC and DAC sample rates. The Clocks tab allows access to set the different options for setting up these clocks. Refer to the Audio Clock Generation Processing figure in the TLV320AIC33 datasheet.

For use with the PC software and the USB-MODEVM, the clock settings must be set a certain way. These settings are not the default settings of the TLV320AIC33. The EVM-required settings can be loaded automatically by pushing the **Load EVM Clock Settings** button at the bottom of this tab. Note that changing any of the clock settings from the values loaded when this button is pushed may result in the EVM not working properly with the PC software or USB interface. If an external audio bus is used (audio not driven over the USB bus), then settings may be changed to any valid combination. See Figure 9.

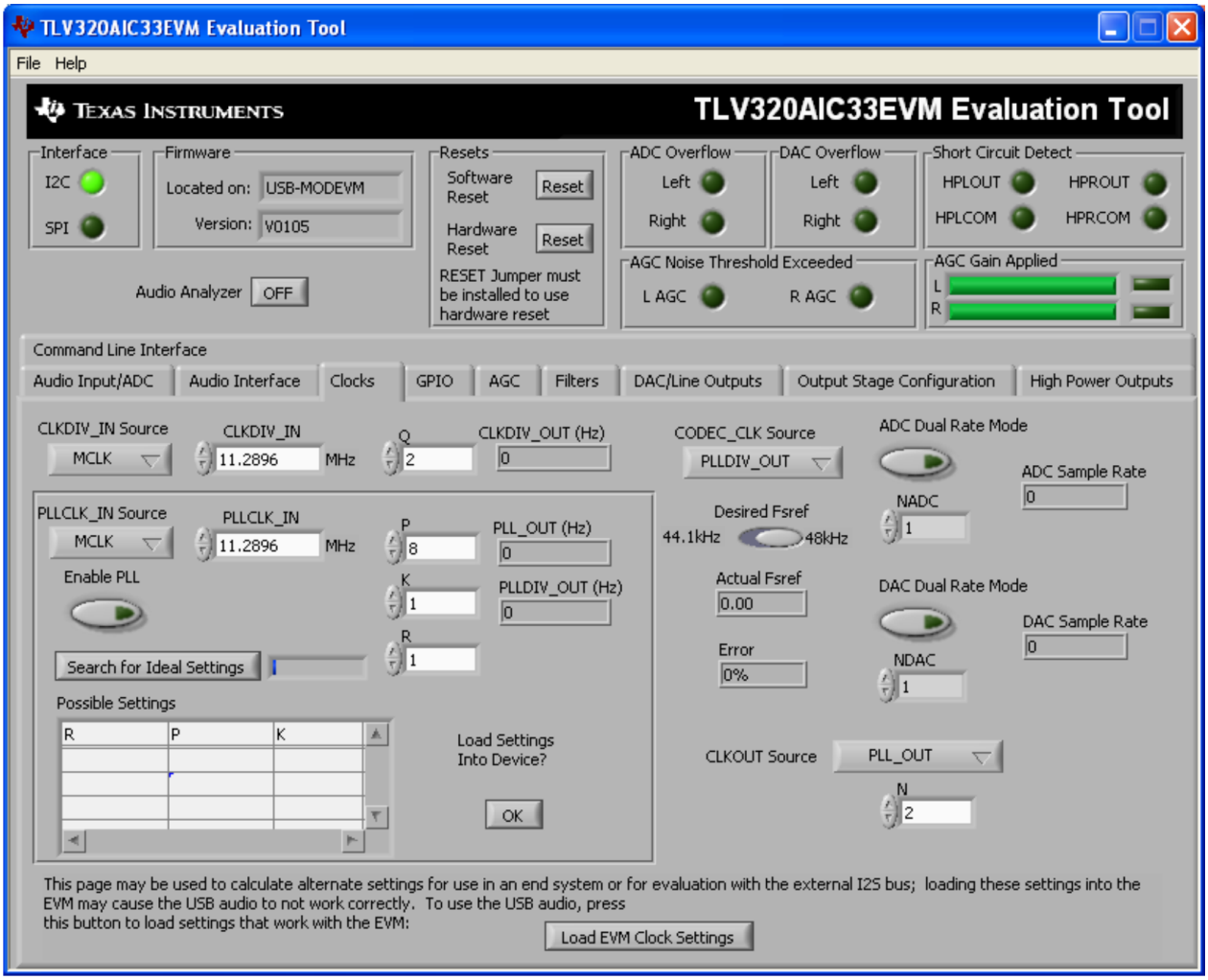


Figure 9. Clocks Tab

The codec clock source is chosen by by the **CODEC_CLK Source** control. When this control is set to *CLKDIV_OUT*, the PLL is not used; when set to *PLLDIV_OUT*, the PLL is used to generate the clocks.

6.9.1 Use Without PLL

Setting up the TLV320AIC33 for clocking without using the PLL is straightforward. The **CLKDIV_IN** source can be selected as either *MCLK* or *BCLK*, the default is MCLK. The CLKDIV_IN frequency is then entered into the **CLKDIV_IN** box, in megahertz (MHz). The default value shown, 11.2896MHz, is the frequency used on the USB-MODEVM board. This value is then divided by the value of Q, which can be set from 2 to 17; the resulting *CLKDIV_OUT* frequency is shown in the indicator next to the **Q** control.

This frequency will then be used to calculate the actual Fsref frequency, and the ADC and DAC sample rates, after the **NADC** and **NDAC** factors are applied to the Fsref. If dual rate mode is desired, this option can be enabled for either the ADC or DAC by pressing the corresponding **Dual Rate Mode** button.

6.9.2 Use With The PLL

When PLLDIV_OUT is selected as the codec clock source, the PLL will be used. The PLL clock source is chosen using the **PLLCLK_IN** control, and may be set to either *MCLK* or *BCLK*. The PLLCLK_IN frequency is then entered into the **PLLCLK_IN Source** box.

The *PLL_OUT* and *PLLDIV_OUT* indicators show the resulting PLL output frequencies with the values set for the P, K, and R parameters of the PLL. Refer to the the TLV320AIC33 datasheet for an explanation of these parameters. The parameters can be set by clicking on the up/down arrows of the **P**, **K**, and **R** combo boxes, or they can be typed into these boxes. The values can also be calculated by the PC software.

To use the PC software to find the ideal values of P, K, and R for a given PLL input frequency and desired Fsref, the desired **Fsref** must be set using the switch on this tab; it can be set to either 44.1kHz or 48kHz. Once the desired Fsref and PLLCLK_IN values are correctly set, pushing the **Search for Ideal Settings** button starts the software searching for ideal combinations of P, K, and R which achieve the desired Fsref. The possible settings for these parameters are displayed in the spreadsheet-like table labeled *Possible Settings*. Clicking on a row in this table sets the P, K, and R values in the software and updates the PLL_OUT and PLLDIV_OUT readings, as well as the *Actual Fsref* and Error displays. This process does not actually load the values into the TLV320AIC33, however; it only updates the displays in the software. This allows for different possible solutions to be selected and the error evaluated before loading into the device.

When a suitable combination of P,K, and R have been chosen, pressing the **Load Settings into Device?** button will download these values into the appropriate registers on the TLV320AIC33.

6.10 GPIO Tab

The GPIO tab (see Figure 10) selects options for the general-purpose inputs and outputs (GPIO) of the TLV320AIC33. Many pins on the TLV320AIC33 are denoted as *multifunction* pins, meaning they may be used for many different purposes.

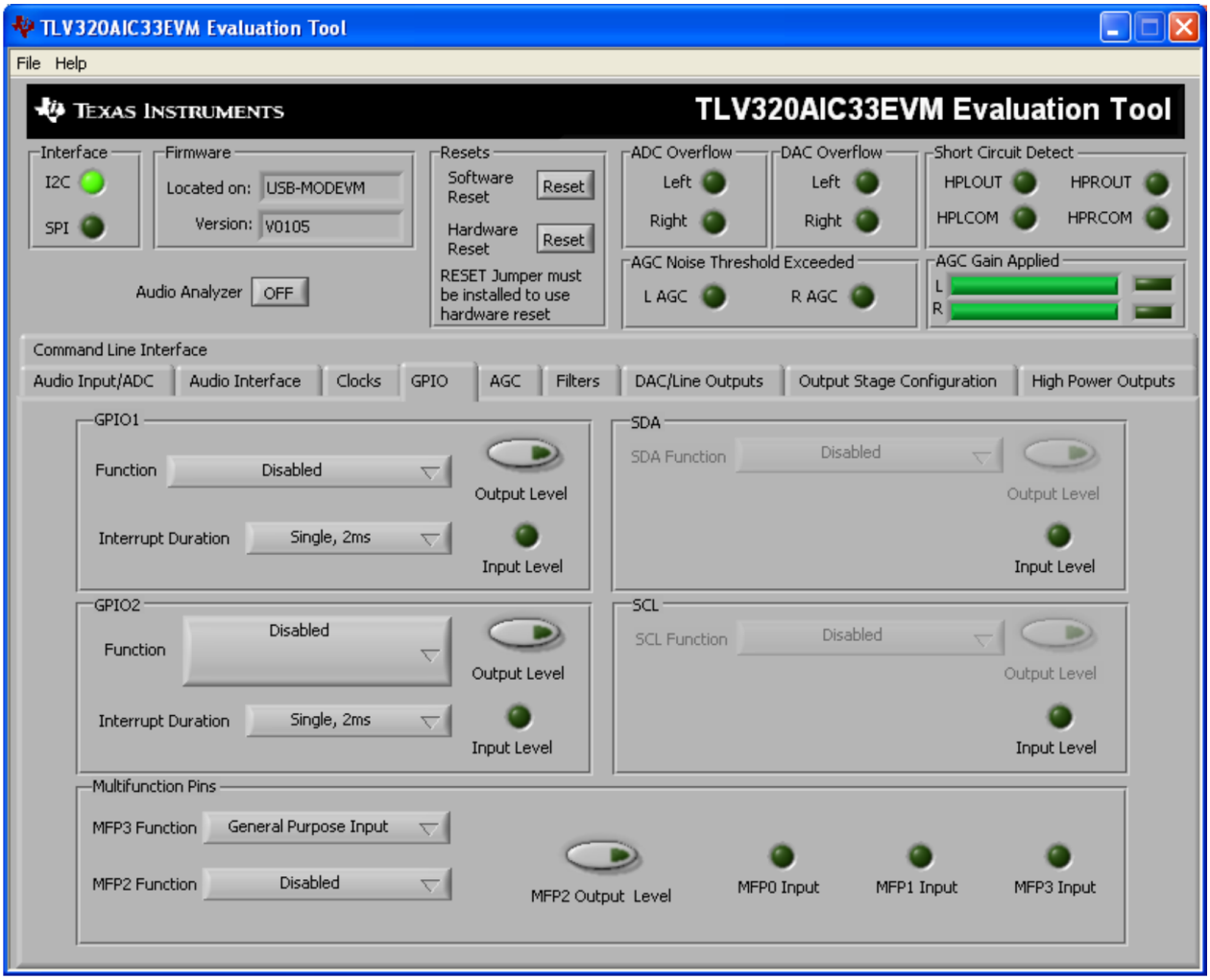


Figure 10. GPIO Tab

The **GPIO1** groupbox contains controls for setting options for the GPIO1 pin. The **Function** control selects the function that GPIO1 will be used for—it can be used as the ADC Word Clock, as an output clock, as interrupt pins to signal Short Circuit or AGC Noise Threshold detection, or Button Press or Headset detection. It may also be used for the alternate I^2S Word Clock or provide a modulator clock for use with a digital microphone (see Section 6.8 and the TLV320AIC33 datasheet). In addition, it can also be used as a general-purpose I/O pin.

If selected as a *General Purpose Input*, the state of the GPIO1 pin is reflected by the **Input Level** indicator. If selected as a *General Purpose Output*, the state of the GPIO1 pin can be set by using the **Output Level** button.

For use as an interrupt output, the behavior of the interrupt can be selected using the **Interrupt Duration** control. A *Single, 2ms* pulse can be delivered when the selected interrupt occurs, or *Continuous Pulses* can be generated signaling the interrupt.

In similar fashion, the GPIO2 pin can also be used for an alternate I^2S bus, provide interrupt outputs, or be used with a digital microphone. These options are selected using the **Function** control in the **GPIO2** groupbox. The other controls in this groupbox work the same as the corresponding controls for GPIO1.

When the control interface for the TLV320AIC33 is selected to be I^2C, the **SDA** and **SCL** groupboxes and controls within them are disabled. If SPI mode is selected, however, the SDA and SCL pins can be used as GPIO, and selected as either inputs or outputs using the **SDA Function** and **SCL Function** controls. The **Output Level** and **Input Level** controls function for these pins in the same way that they do for GPIO1 or GPIO2.

When the control interface for the TLV320AIC33 is selected to be SPI, the **Multifunction Pins** groupbox and controls within it are disabled, because these pins are used by the SPI bus. When in I^2C mode, however, these controls are enabled. The **MFP3 Function** control selects MFP3 to be used either as a *General Purpose Input* or as the data input line for the alternate I^2S bus. The **MFP2 Function** control selects MFP2 as either *Disabled* or as a *General Purpose Output*. When used as an output, the **MFP2 Output Level** control sets the output state of the MFP2 pin either high or low. The states of the MFP0, MFP1 and MP3 inputs are indicated by the three indicator lights on the right-hand side of this groupbox.

6.11 AGC Tab

The AGC tab (see Figure 11) consists of two identical sets of controls, one for the left channel and the other for the right channel. The AGC function is described in the TLV320AIC33 datasheet.

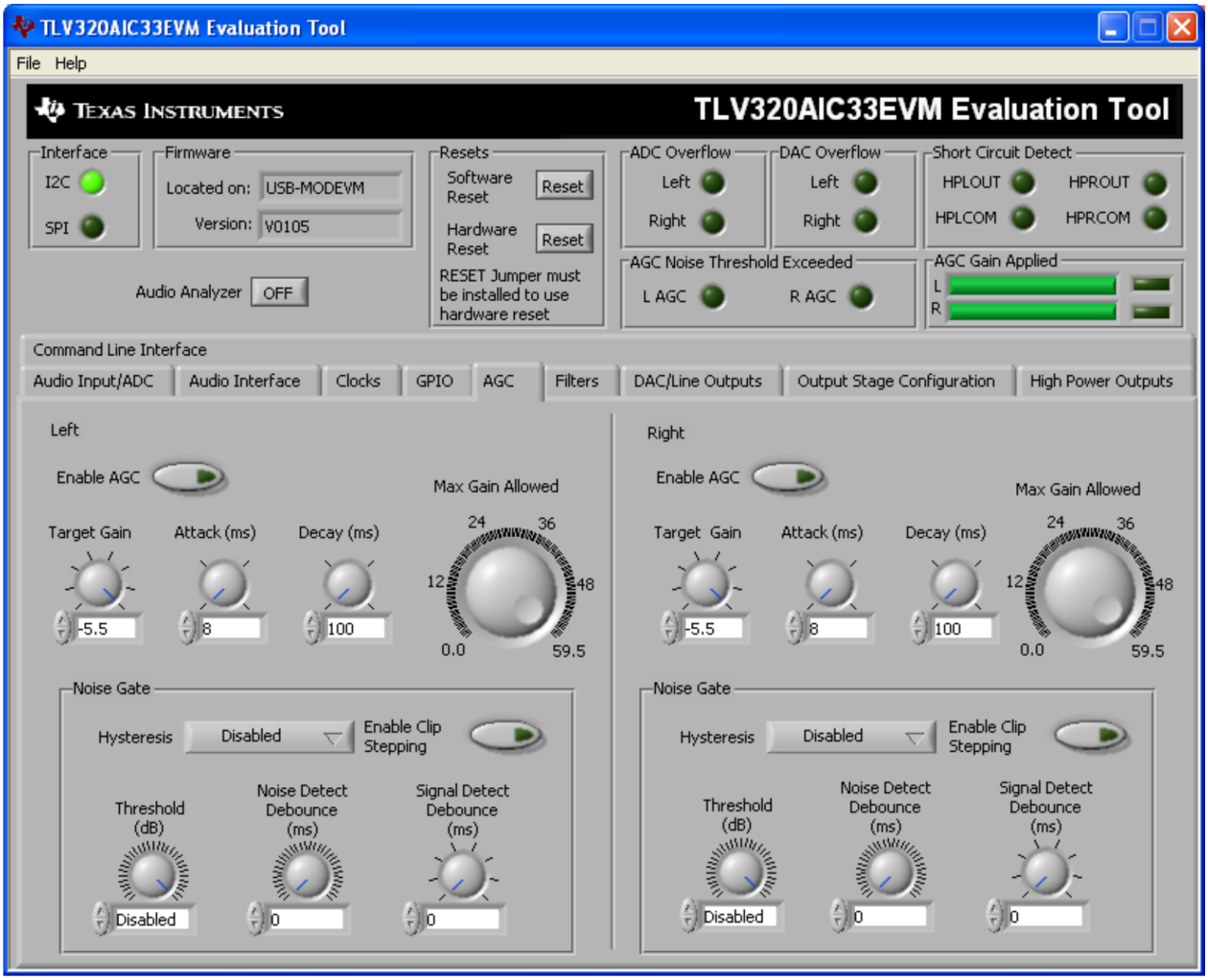


Figure 11. AGC Tab

The AGC can be enabled for each channel using the **Enable AGC** button. *Target* gain, *Attack* time in milliseconds, *Decay* time in milliseconds, and the *Maximum PGA Gain Allowed* can all be set, respectively, using the four corresponding knobs in each channel.

Noise gate functions, such as *Hysteresis*, *Clip stepping*, *Threshold*, and *Signal and Noise Detect* debouncing are set using the corresponding controls in the **Noise Gate** groupbox for each channel.

6.12 Filters Tab

The TLV320AIC33 has a very rich feature set for applying digital filtering to audio signals. This tab controls all of the filter features of the TLV320AIC33. In order to use this tab and have plotting of filter responses correct, the DAC sample rate must be set correctly. Therefore, the clocks must be set up correctly in the software following the discussion in Section 6.9. See Figure 12.

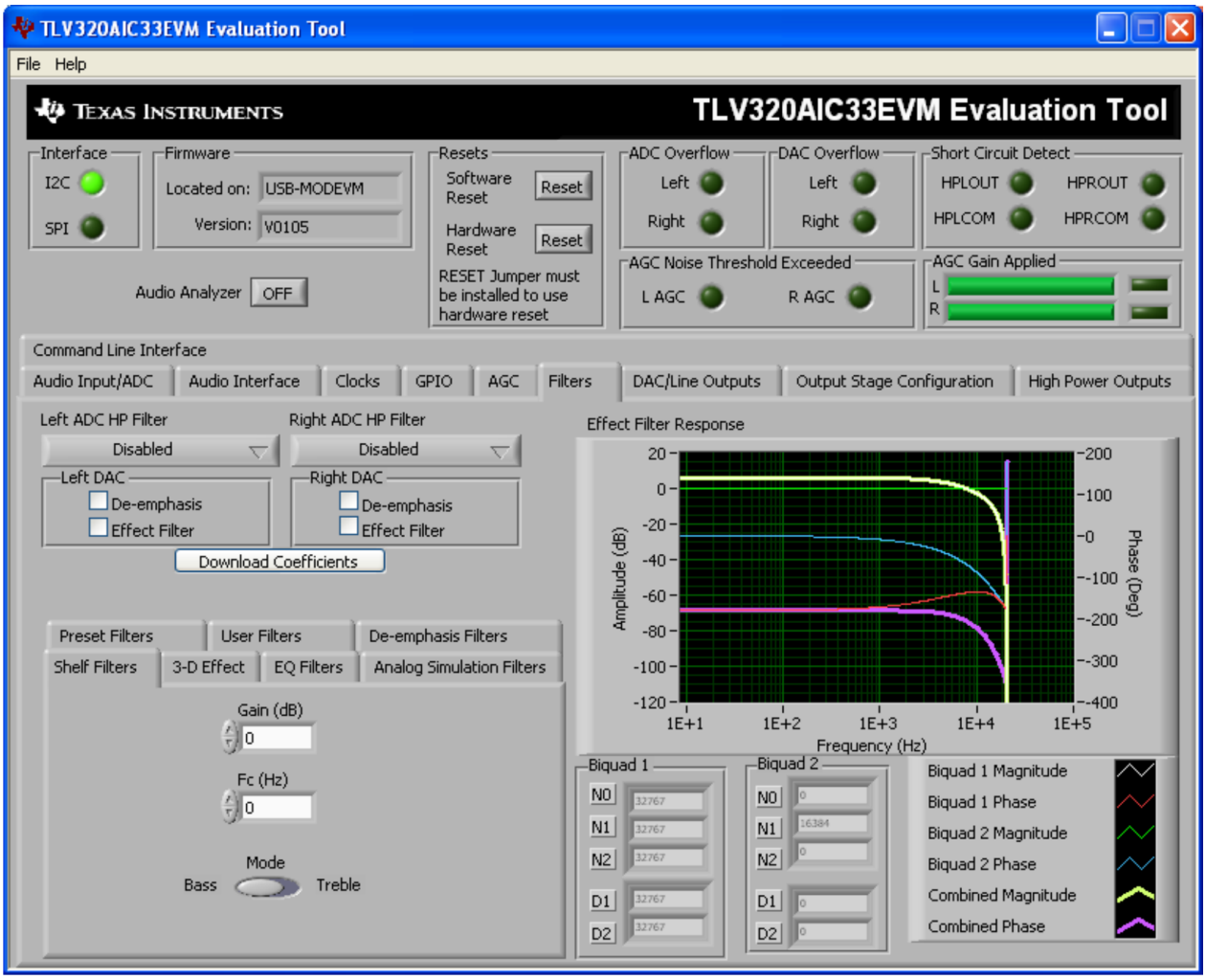


Figure 12. Filters Tab

The right-hand side of this tab shows a display that plots the magnitude and phase response of each biquad section, plus the combined responses of the two biquad sections. The coefficients used for the plotted responses are shown below the graph for both Biquad 1 and Biquad 2. Note that the plot shows only the responses of the effect filters, not the combined response of those filter along with the de-emphasis and ADC high-pass filters.

6.12.1 ADC Highpass Filters

The ADC of the TLV320AIC33 can have a high-pass filter enabled, which helps to reduce the effects of DC offsets in the system. This function is enabled as shown in Figure 13. The four options for this setting are disabled, or three different corner frequencies which are based on the ADC sample rate.

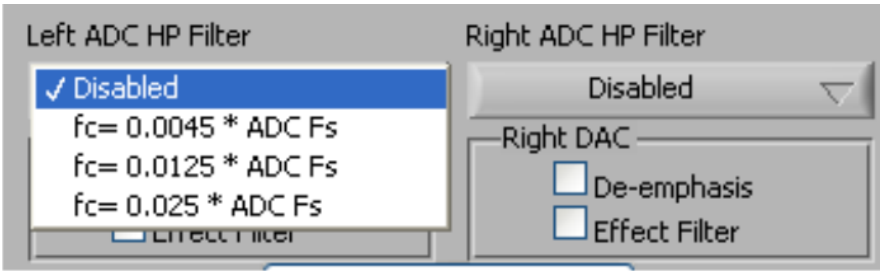


Figure 13. ADC Highpass Filter Settings

6.12.2 Enabling Filters

The de-emphasis and effect filters (the biquad filters) of the TLV320AIC33 are selected using the checkboxes shown in Figure 14. The De-emphasis filters are described in the TLV320AIC33 datasheet, and their coefficients may be changed (see Section 6.12.7).

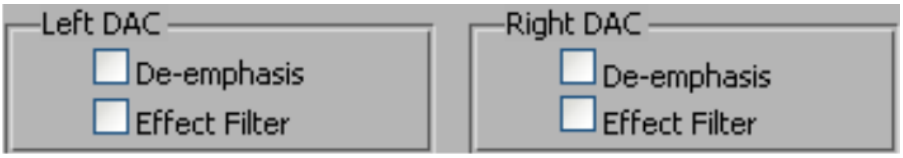


Figure 14. Enabling Filters

When designing filters for use with TLV320AIC33, the software allows for several different filter types to be used. These options are shown on a tab control in the lower left corner of the screen. When a filter type is selected, and suitable input parameters defined, the response will be shown in the *Effect Filter Response* graph. Regardless of the setting for enabling the Effect Filter, the filter coefficients are not loaded into the TLV320AIC33 until the **Download Coefficients** button is pressed. To avoid noise during the update of coefficients, it is recommended that you uncheck the **Effect Filter enable** checkboxes before downloading coefficients. Once the desired coefficients are in the TLV320AIC33, enable the Effect Filters by checking the boxes again.

6.12.3 Shelf Filters

A shelf filter is a simple filter that applies a gain (positive or negative) to frequencies above or below a certain corner frequency. As shown in Figure 15, in *Bass* mode a shelf filter applies a gain to frequencies below the corner frequency; in *Treble* mode the gain is applied to frequencies above the corner frequency.

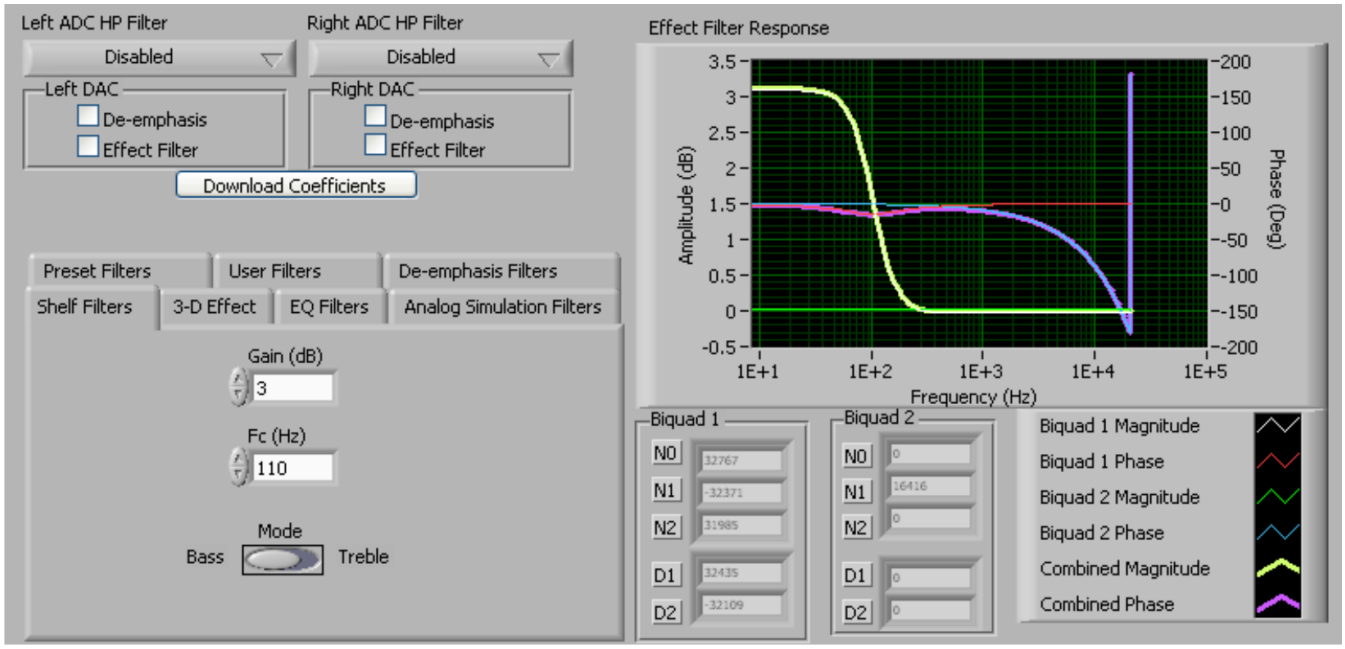


Figure 15. Shelf Filters

To use these filters, enter the gain desired and the corner frequency. Choose the mode to use (*Bass* or *Treble*); the response will be plotted on the *Effect Filter Response* graph.

6.12.4 EQ Filters

EQ, or parametric, filters can be designed on this tab (see Figure 16). Enter a gain, bandwidth, and a center frequency (Fc). Either bandpass (positive gain) or band-reject (negative gain) filters can be created

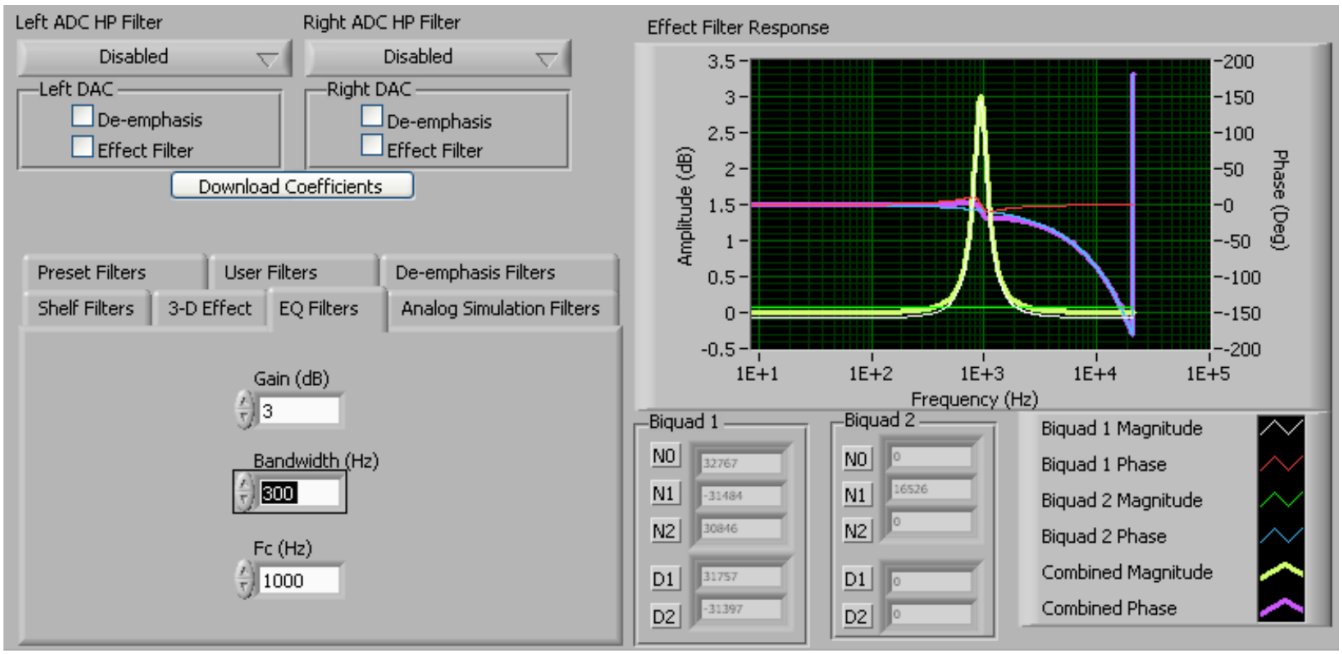


Figure 16. EQ Filters

6.12.5 Analog Simulation Filters

Biquads are quite good at simulating analog filter designs. For each biquad section on this tab, enter the desired analog filter type to simulate (Butterworth, Chebyshev, Inverse Chebyshev, Elliptic or Bessel). Parameter entry boxes appropriate to the filter type will be shown (ripple, for example, with Chebyshev filters, etc.). Enter the desired design parameters and the response will be shown. (See Figure 17.)

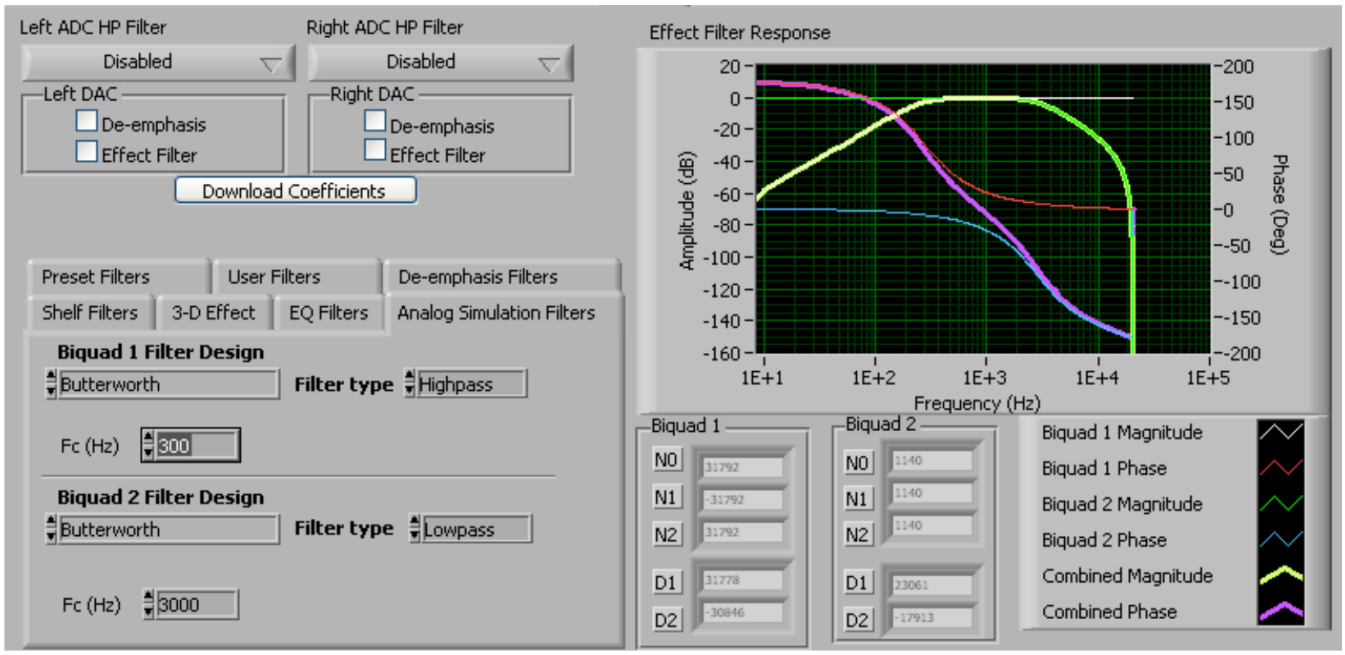


Figure 17. Analog Simulation Filters

6.12.6 Preset Filters

Many applications are designed to provide preset filters common for certain types of program material. This tab (see Figure 18) allows selection of one of four preset filter responses - Rock, Jazz, Classical, or Pop.

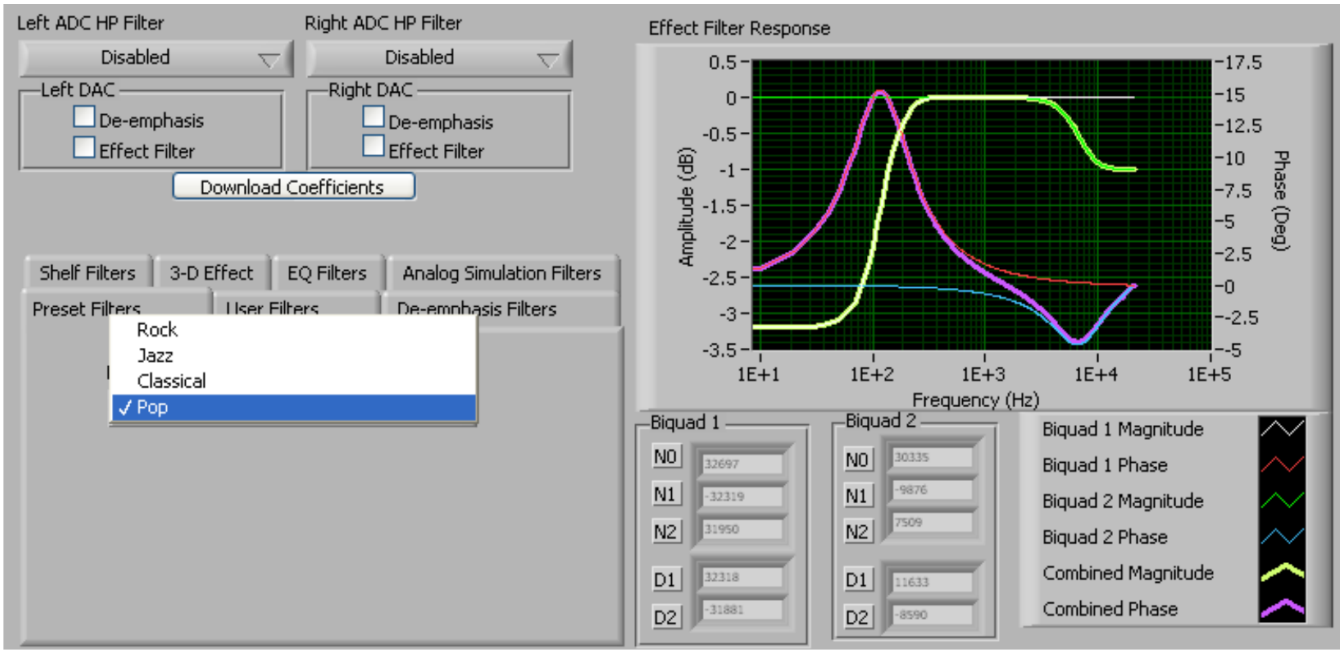


Figure 18. Preset Filters

6.12.7 De-emphasis Filters

The de-emphasis filters used in the TLV320AIC33 can be programmed as described in the TLV320AIC33 datasheet, using this tab (Figure 19). Enter the coefficients for the de-emphasis filter response desired. While on this tab, the de-emphasis response will be shown on the *Effect Filter Response* graph; however, note that this response is not included in graphs of other effect responses when on the other filter design tabs.

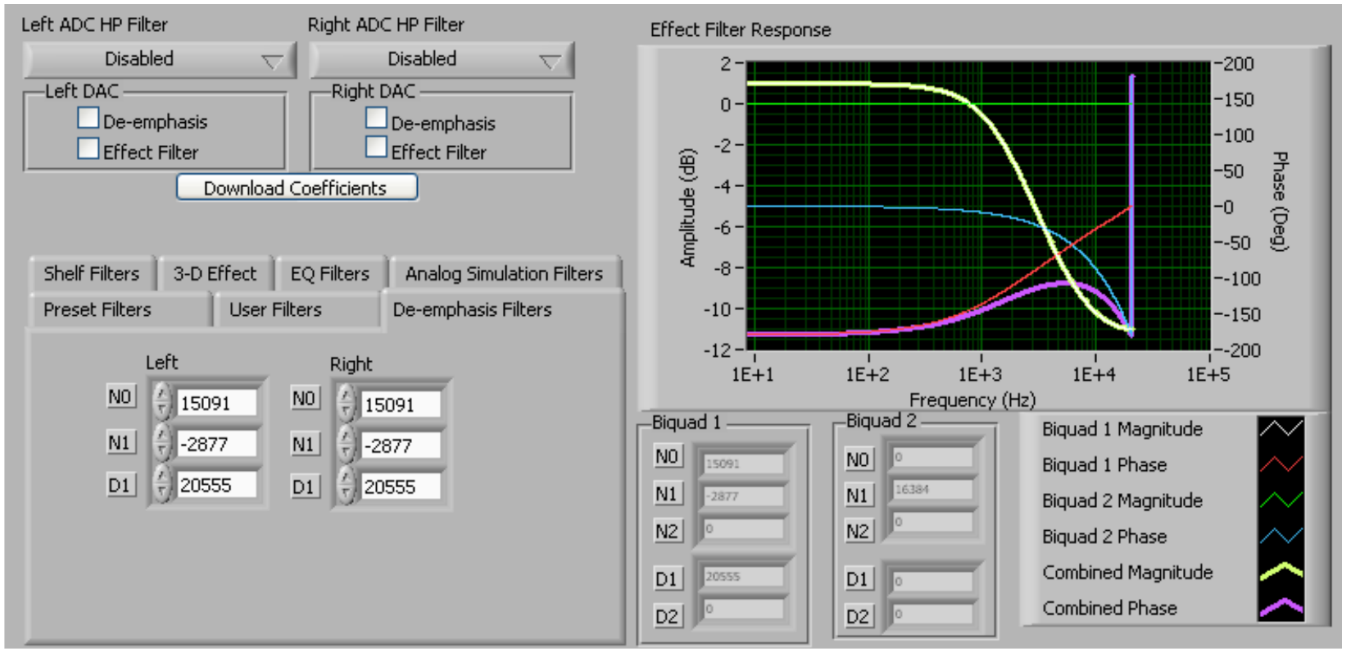


Figure 19. De-emphasis Filters

6.12.8 User Filters

If filter coefficients are known, they can be entered directly on this tab (see Figure 20) for both biquads for both left and right channels. The filter response will ***not*** be shown on the *Effect Filter Response* graph for user filters.

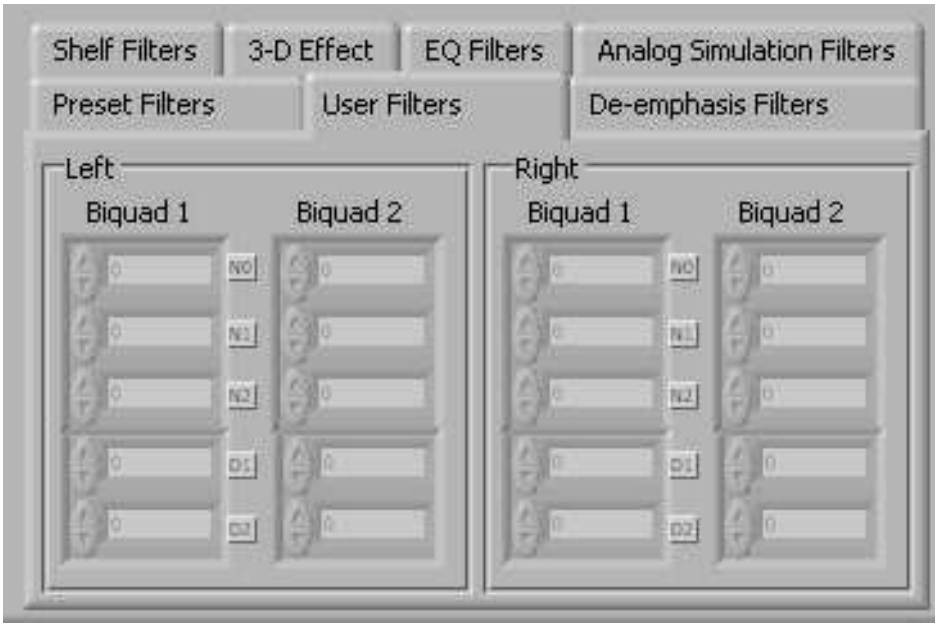


Figure 20. User Filters

6.12.9 3D Effect

The 3D effect is described in the TLV320AIC33 datasheet. It uses the two biquad sections differently than most other effect filter settings. To use this effect properly, make sure the appropriate coefficients are already loaded into the two biquad sections. The User Filters tab may be used to load the coefficients. See Figure 21.

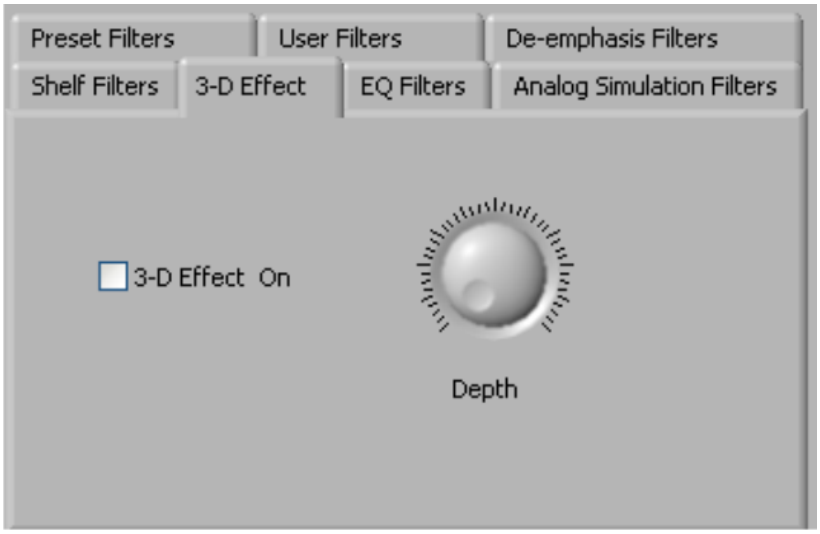


Figure 21. 3D Effect Settings

To enable the 3D effect, check the **3D Effect On** box. The **Depth** knob controls the value of the 3D Attenuation Coefficient.

6.13 DAC/Line Outputs Tab

The DAC/Line Outputs tab controls the DAC power and volume, as well as routing of digital data to the DACs and the analog output from the DACs. (See Figure 22.)

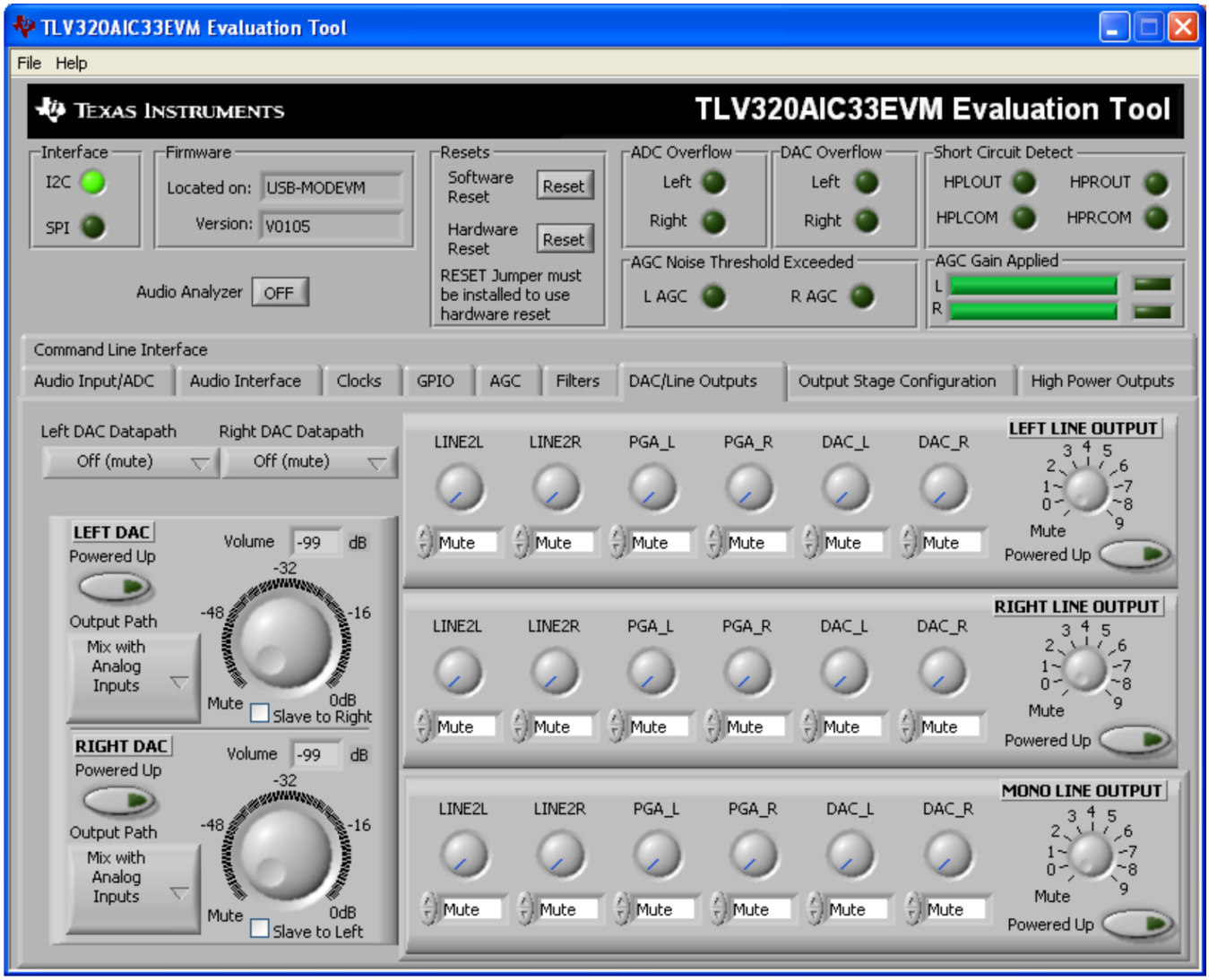


Figure 22. DAC/Line Outputs Tab

6.13.1 DAC Controls

On the left side of this tab are controls for the left and right DACs.

In similar fashion as the ADC, the DAC controls are set up to allow powering of each DAC individually, and setting the output level. Each channel's level can be set independently using the corresponding **Volume** knob. Alternately, by checking the **Slave to Right** box, the left channel Volume can be made to track the right channel Volume knob setting; checking the **Slave to Left** box causes the right channel Volume knob to track the left Volume knob setting.

Data going to the DACs is selected using the drop-down boxes under the **Left and Right Datapath**. Each DAC channel can be selected to be off, use left channel data, use right channel data, or use a mono mix of the left and right data.

Analog audio coming from the DACs is routed to outputs using the **Output Path** controls in each DAC control panel. The DAC output can be mixed with the analog inputs (LINE2L, LINE2R, PGA_L, PGA_R) and routed to the Line or High Power outputs using the mixer controls for these outputs on this tab (for the line outputs) or on the High Power Outputs tab (for the high power outputs). If the DAC is to be routed directly to either the Line or HP outputs, these can be selected as choices in the Output Path control. Note that if the Line or HP outputs are selected as the Output Path, the mixer controls on this tab and the High Power Output tabs have no effect.

6.13.2 Line Output Mixers

On the right side of this tab are horizontal panels which house the mixing functions for the line outputs.

Each line output master volume is controlled by the knob at the far right of these panels. The output can be muted, or gain up to 9dB can be applied. Power for the line output can also be controlled using the button below this master output knob.

If the DAC output path is set to *Mix with Analog Inputs*, the six knobs in each panel can be used to set the individual level of signals routed and mixed to the line output. LINE2L, LINE2R, PGA_L, PGA_R, and DAC_L and DAC_R levels can each be set to create a custom mix of signals presented to that particular line output. **Note:** if the DAC output path is set to anything other than *Mix with Analog Inputs*, these controls have no effect.

6.14 Output Stage Configuration Tab

The Output Stage Configuration tab (Figure 23) allows for setting several features of the output drivers. The **Configuration** may be set as either *Fully-Differential* or *Pseudo-Differential*. The output coupling can be chosen as either capless or AC-coupled. This setting should correspond to the setting of the hardware switch (SW1) on the TLV320AIC33EVM.

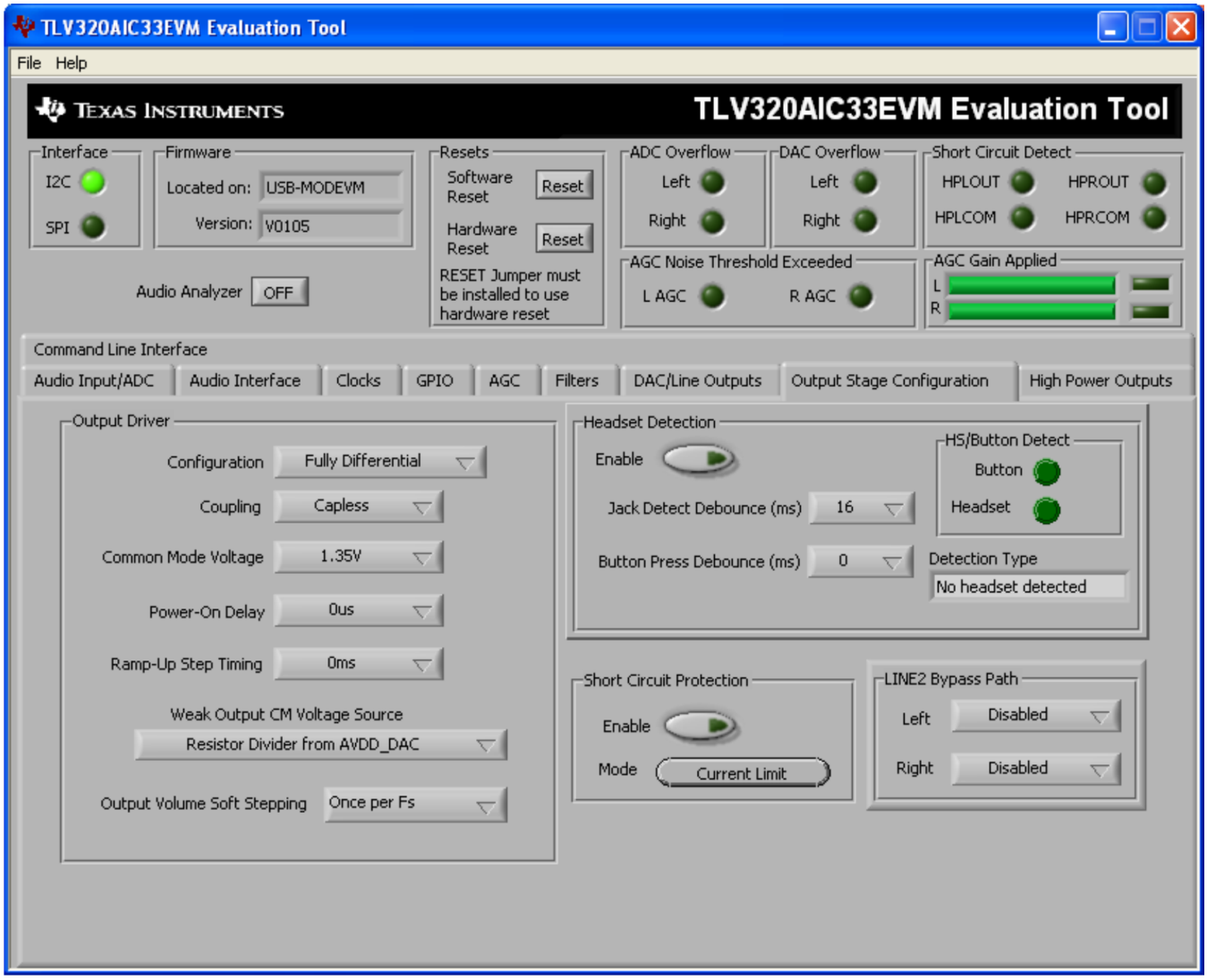


Figure 23. Output Stage Configuration Tab

The Common Mode Voltage of the outputs may be set to 1.35V, 1.5V, 1.65V, or 1.8V using the **Common Mode Voltage** control. The **Power-On Delay** of the output drivers can be set using the corresponding control from 0µs up to 4 seconds. **Ramp-Up Step Timing** can also be adjusted from 0ms to 4ms.

The high power outputs of the TLV320AIC33 can be configured to go to a weak common-mode voltage when powered down. The source of this weak common-mode voltage can be set on this tab with the **Weak Output CM Voltage Source** drop-down. Choices for the source are either a resistor divider off the AVDD_DAC supply, or a bandgap reference. See the datasheet for more details on this option.

The outputs can be set to soft-step their volume changes, using the **Output Volume Soft Stepping** control, and set to step once per Fs period, once per two Fs periods, or soft-stepping can be disabled altogether.

Headset detection features are enabled using the **Enable** button in the **Headset Detection** groupbox. When enabled, the indicators in the **HS/Button Detect** groupbox will light when either a button press or headset is detected. When a headset is detected, the type of headset is displayed in the **Detection Type** indicator. Debounce times for detection are set using the **Jack Detect Debounce** and **Button Press Debounce** controls, which offer debounce times in varying numbers of milliseconds. See the TLV320AIC33 datasheet for a discussion of headset detection.

Output short-circuit protection can be enabled in the **Short Circuit Protection** groupbox. Short Circuit Protection can use a current-limit mode, where the drivers will limit current output if a short-circuit condition is detected, or in a mode where the drivers will power down when such a condition exists.

The LINE2 Bypass Path groupbox has controls that allow disabling or routing the LINE2 input to the output stage directly.

6.15 High Power Outputs Tab

This tab contains four horizontal groupings of controls, one for each of the high power outputs. Each output has a mixer to mix the LINE2L, LINE2R, PGA_L, PGA_R, DAC_L and DAC_R signals, assuming that the DACs are not routed directly to the high power outputs (see Section 6.13).

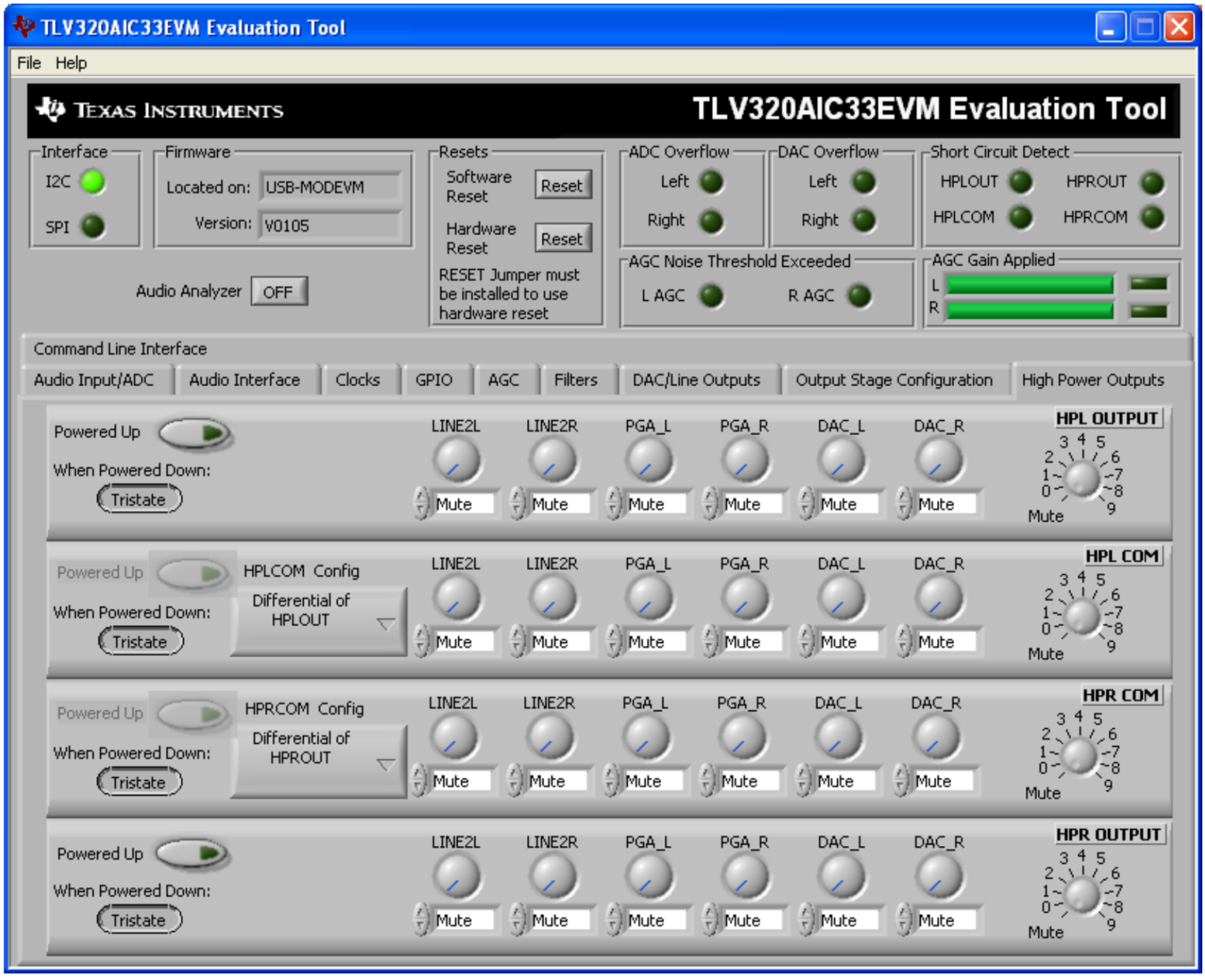


Figure 24. High Power Outputs Tab

At the left of each output strip is a power button that controls whether the corresponding output is powered up or not. When powered down, the outputs can be tri-stated or driven weakly to a the output common mode voltage; this option is selected using the button below the power button.

The **COM** outputs (*HPLCOM* and *HPRCOM*) can be used as independent output channels or can be used

as complementary signals to the HPL and HPR outputs. In these complementary configurations, the COM outputs can be selected as differential signals to the corresponding outputs or may be set to be a common mode voltage. When used in these configurations, the power button for the COM output is disabled, as the power mode for that output will track the power status of the HPL or HPR output that the COM output is tracking.

At the right side of the output strip is a master volume knob for that output, which allows muting the output or applying gain up to 9dB.

6.16 Command Line Interface Tab

A simple scripting language controls the TAS1020 on the USB-MODEVM from the LabView™-based PC software. The main program controls, described previously, do nothing more than write a script which is then handed off to an interpreter that sends the appropriate data to the correct USB endpoint. Because this system is script-based, provision is made in this tab for the user to view the scripting commands created as the controls are manipulated, as well as load and execute other scripts that have been written and saved (see Figure 25). This design allows the software to be used as a quick test tool or to help provide troubleshooting information in the rare event that the user encounters problem with this EVM.

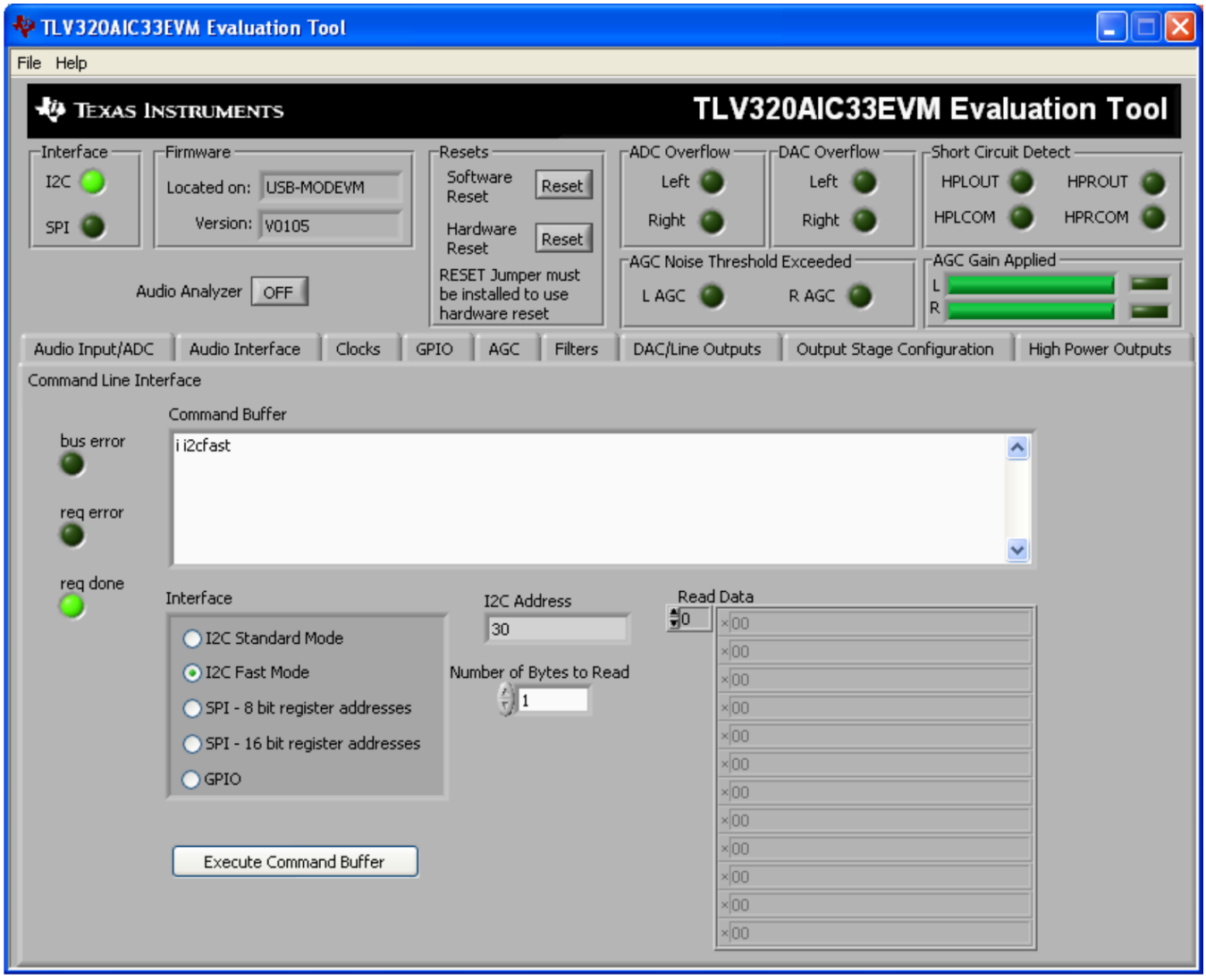


Figure 25. Command Line Interface Tab

A script is loaded into the command buffer, either by operating the controls on the other tabs or by loading a script file. When executed, the return packets of data which result from each command will be displayed in the **Read Data** array control. When executing several commands, the Read Data control shows only the results of the last command. If you want to see the results after every executed command, use the logging function described below.

The File menu (Figure 26) provides some options for working with scripts. The first option, *Open Command File...*, loads a command file script into the command buffer. This script can then be executed by pressing the **Execute Command Buffer** button.

The second option is *Log Script and Results...*, which opens a file save dialog box. Choose a location for a log file to be written using this file save dialog. When the Execute Command Buffer button is pressed, the script will run and the script, along with resulting data read back during the script, will be saved to the file specified. The log file is a standard text file that can be opened with any text editor, and looks much like the source script file, but with the additional information of the result of each script command executed.

The third menu item is a submenu of *Recently Opened Files*. This is simply a list of script files that have previously been opened, allowing fast access to commonly-used script files. The final menu item is *Exit*, which terminates the TLV320AIC33EVM software.

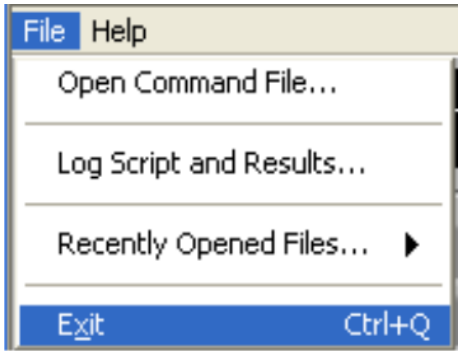


Figure 26. File Menu

Under the Help menu is an *About...* menu item which displays information about the TLV320AIC33EVM software.

The actual USB protocol used as well as instructions on writing scripts are detailed in the following subsections. While it is not necessary to understand or use either the protocol or the scripts directly, understanding them may be helpful to some users.

6.16.1 USB-MODEVM Protocol

The USB-MODEVM is defined to be a Vendor-Specific class, and is identified on the PC system as an NI-VISA device. Because the TAS1020 has several routines in its ROM which are designed for use with HID-class devices, HID-like structures are used, even though the USB-MODEVM is not an HID-class device. Data is passed from the PC to the TAS1020 using the control endpoint.

Data is sent in an HIDSETREPORT (see Table 7):

Table 7. USB Control Endpoint HIDSETREPORT Request

Part	Value	Description
bmRequestType	0x21	00100001
bRequest	0x09	SET_REPORT
wValue	0x00	don't care
wIndex	0x03	HID interface is index 3
wLength	calculated by host	
Data		Data packet as described below

The data packet consists of the following bytes, shown in Table 8:

Table 8. Data Packet Configuration

BYTE NUMBER	TYPE	DESCRIPTION
0	Interface	Specifies serial interface and operation. The two values are logically OR'd. Operation: READ 0x00 WRITE 0x10 Interface: GPIO 0x08 SPI_16 0x04 I2C_FAST 0x02 I2C_STD 0x01 SPI_8 0x00
1	I^2C Slave Address	Slave address of I^2C device or MSB of 16-bit reg addr for SPI
2	Length	Length of data to write/read (number of bytes)
3	Register address	Address of register for I^2C or 8-bit SPI; LSB of 16-bit address for SPI
4..64	Data	Up to 60 data bytes could be written at a time. EP0 maximum length is 64. The return packet is limited to 42 bytes, so advise only sending 32 bytes at any one time.

Example usage:
Write two bytes (AA, 55) to device starting at register 5 of an I^2C device with address A0:

```
[0] 0x11
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

Do the same with a fast mode I²C device:

```
[0] 0x12
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

Now with an SPI device which uses an 8-bit register address:

```
[0] 0x10
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

Now let's do a 16-bit register address, as found on parts like the TSC2101. Assume the register address (command word) is **0x10E0**:

```
[0] 0x14
[1] 0x10 --> Note: the I²C address now serves as MSB of reg addr.
[2] 0x02
[3] 0xE0
[4] 0xAA
[5] 0x55
```

In each case, the TAS1020 will return, in an HID interrupt packet, the following:

[0] interface byte | status

status:

`REQ_ERROR 0x80`

`INTF_ERROR 0x40`

`REQ_DONE 0x20`

[1] for I²C interfaces, the I²C address as sent

for SPI interfaces, the read back data from SPI line for transmission of the corresponding byte

[2] length as sent

[3] for I²C interfaces, the reg address as sent

for SPI interfaces, the read back data from SPI line for transmission of the corresponding byte

[4..60] echo of data packet sent

If the command is sent with no problem, the returning byte [0] should be the same as the sent one logically or'd with 0x20 - in our first example above, the returning packet should be:

```
[0] 0x31
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

If for some reason the interface fails (for example, the I^2C device does not acknowledge), it would come back as:

```
[0] 0x51 --> interface | INTF_ERROR
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

If the request is malformed, that is, the interface byte (byte [0]) takes on a value which is not described above, the return packet would be:

```
[0] 0x93 --> you sent 0x13, which is not valid, so 0x93 returned
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

Examples above used writes. Reading is similar:
Read two bytes from device starting at register 5 of an I^2C device with address A0:

```
[0] 0x01
[1] 0xA0
[2] 0x02
[3] 0x05
```

The return packet should be

```
[0] 0x21
[1] 0xA0
[2] 0x02
[3] 0x05
[4] 0xAA
[5] 0x55
```

assuming that the values we wrote above starting at Register 5 were actually written to the device.

6.16.1.1 GPIO Capability

The USB-MODEVM has seven GPIO lines. You can access them by specifying the interface to be 0x08, and then using the standard format for packets—but addresses are unnecessary. The GPIO lines are mapped into one byte (see Table 9):

Table 9. GPIO Pin Assignments

7	6	5	4	3	2	1	0
x	P3.5	P3.4	P3.3	P1.3	P1.2	P1.1	P1.0

Example: write P3.5 to a 1, set all others to 0:

```
[0] 0x18 --> write, GPIO
[1] 0x00 --> this value is ignored
[2] 0x01 --> length - ALWAYS a 1
[3] 0x00 --> this value is ignored
[4] 0x40 --> 01000000
```

You may also read back from the GPIO to see the state of the pins. Let's say we just wrote the previous example to the port pins.

Example: read the GPIO

```
[0] 0x08 --> read, GPIO
[1] 0x00 --> this value is ignored
[2] 0x01 --> length - ALWAYS a 1
[3] 0x00 --> this value is ignored
```

The return packet should be:

```
[0] 0x28
[1] 0x00
[2] 0x01
[3] 0x00
[4] 0x40
```

6.16.2 Writing Scripts

A script is simply a text file that contains data to send to the serial control buses. The scripting language is quite simple, as is the parser for the language. Therefore, the program is not very forgiving about mistakes made in the source script file, but the formatting of the file is simple. Consequently, mistakes should be rare.

Each line in a script file is one command. There is no provision for extending lines beyond one line. A line is terminated by a carriage return.

The first character of a line is the command. Commands are:

i Set interface bus to use
r Read from the serial control bus
w Write to the serial control bus
Comment
b Break
d Delay

The first command, **i**, sets the interface to use for the commands to follow. This command must be followed by one of the following parameters:

i2cstd	Standard mode I^2C Bus
i2cfast	Fast mode I^2C bus
spi8	SPI bus with 8-bit register addressing
spi16	SPI bus with 16-bit register addressing
gpio	Use the USB-MODEVM GPIO capability

For example, if a fast mode I^2C bus is to be used, the script would begin with:

i i2cfast

No data follows the break command. Anything following a comment command is ignored by the parser, provided that it is on the same line. The delay command allows the user to specify a time, in milliseconds, that the script will pause before proceeding.

Note: UNLIKE ALL OTHER NUMBERS USED IN THE SCRIPT COMMANDS, THE DELAY TIME IS ENTERED IN A DECIMAL FORMAT. Also, note that because of latency in the USB bus as well as the time it takes the processor on the USB-MODEVM to handle requests, the delay time may not be precise.

A series of byte values follows either a read or write command. Each byte value is expressed in hexadecimal, and each byte must be separated by a space. Commands are interpreted and sent to the TAS1020 by the program using the protocol described in Section 6.16.1.

The first byte following a read or write command is the I^2C slave address of the device (if I^2C is used) or the first data byte to write (if SPI is used—note that SPI interfaces are not standardized on protocols, so the meaning of this byte will vary with the device being addressed on the SPI bus). The second byte is the starting register address that data will be written to (again, with I^2C; SPI varies—see Section 6.16.1 for additional information about what variations may be necessary for a particular SPI mode). Following these two bytes are data, if writing; if reading, the third byte value is the number of bytes to read, (expressed in hexadecimal).

For example, to write the values 0xAA 0x55 to an I^2C device with a slave address of 0x90, starting at a register address of 0x03, one would write:

```
#example script
i i2cfast
w 90 03 AA 55
r 90 03 2
```

This script begins with a comment, specifies that a fast I^2C bus will be used, then writes *0xAA 0x55* to the I^2C slave device at address 0x90, writing the values into registers 0x03 and 0x04. The script then reads back two bytes from the same device starting at register address 0x03. Note that the slave device value does not change. It is not necessary to set the R/$\overline{W}$ bit for I^2C devices in the script; the read or write commands will do that for you.

Here is an example of using an SPI device that requires 16-bit register addresses:

```
# setup TSC2101 for input and output
# uses SPI16 interface
# this script sets up DAC and ADC at full volume, input from onboard mic
#
# Page 2: Audio control registers
w 10 00 00 00 80 00 00 00 45 31 44 FD 40 00 31 C4
w 13 60 11 20 00 00 00 80 7F 00 C5 FE 31 40 7C 00 02 00 C4 00 00 00 23 10 FE 00 FE 00
```

Note that blank lines are allowed. However, be sure that your script does not end with a blank line. While ending with a blank line will not cause the script to fail, the program will execute that line, and therefore may prevent you from seeing data that was written or read back on the previous command.

In this example, the first two bytes of each command are the command word to send to the TSC2101 (0x1000, 0x1360); these are followed by data to write to the device starting at the address specified in the command word. The second line may wrap in the viewer you are using to look like more than one line; careful examination will show, however, that there is only one carriage return on that line, following the last **00**.

Any text editor may be used to write these scripts; Jedit is an editor that is highly recommended for general usage. For more information, go to: http://www.jedit.org.

Once the script is written, it can be used in the command window by running the program, and then selecting *Open Command File...* from the File menu. Locate your script and open it. The script will then be displayed in the command buffer. You may also edit the script once it is in the buffer, but saving of the command buffer is not possible at this time (this feature may be added at a later date).

Once the script is in the command buffer, it may be executed by pressing the *Execute Command Buffer* button. If you have placed breakpoints in your script, the script will execute to that point, and you will be presented with a dialog box with a button to press to continue executing the script. When you are ready to proceed, push that button and the script will continue.

Here an example of a (partial) script with breakpoints:

```
# setup AIC33 for input and output
# uses I2C interface
i i2cfast
# reg 07 - codec datapath
w 30 07 8A
r 30 07 1
d 1000
# regs 15/16 - ADC volume, unmute and set to 0dB
w 30 0F 00 00
r 30 0F 2
b
```

This script writes the value 8A at register 7, then reads it back to verify that the write was good. A delay of 1000ms (one second) is placed after the read to pause the script operation. When the script continues, the values **00 00** will be written starting at register 0F. This output is verified by reading two bytes, and pausing the script again, this time with a break. The script would not continue until the user allows it to by pressing *OK* in the dialog box that will be displayed due to the break.

7 EVM Bill of Materials

Table 10 and Table 11 contain a complete bill of materials for the modular TLV320AIC33EVM and the USB-MODEVM Interface Board (included only in the TLV320AIC33EVM-PDK).

Table 10. TLV320AIC33EVM Bill of Materials

REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	MFGPART NUMBER
R8, R9	0Ω 1/4W 5% Chip Resistor	Panasonic	ERJ-8GEY0R00V
R6, R7	2.2KΩ 1/4W 5% Chip Resistor	Panasonic	ERJ-8GEYJ222V
R11, R12, R13	2.7KΩ 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ272V
R10	100KΩ 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ104V
R1, R2, R3, R4, R5	Chip Resistor	Not Installed	
C12-C17, C34	0.1µF 25V Ceramic Chip Capacitor, +/ - 10%, X7R	TDK	C1608X7R1E104K
C4-C11, C21, C22	0.1µF 250V Ceramic Chip Capacitor, +/ - 10%, X7R	TDK	C3216X7R2E104K
C1-C3, C23-C27	10µF 6.3V Ceramic Chip Capacitor, +/ - 10%, X5R	TDK	C3216X5R0J106K
C28-C33	47µF 6.3V Ceramic Chip Capacitor, +/ - 20%, X5R	TDK	C3225X5R0J476M
C19, C20	Ceramic Chip Capacitor	Not Installed	
C18	Ceramic Chip Capacitor	Not Installed	
U1	Audio Codec	Texas Instruments	TLV320AIC33IRGZ
U2	3.3V LDO Voltage Regulator	Texas Instruments	REG1117-3.3
U3	64K I2C EEPROM	MicroChip	24LC64-I/SN
J1-J4, J8-J10	Screw Terminal Block, 2 Position	On Shore Technology	ED555/2DS
J5, J11, J12	Screw Terminal Block, 3 Position	On Shore Technology	ED555/3DS
J6, J7	3.5mm Audio Jack, T-R-S, SMD	CUI Inc.	SJ1-3515-SMT
	or alternate	KobiConn	161-3335
J13A, J14A, J16A, J17A	20 Pin SMT Plug	Samtec	TSM-110-01-L-DV-P
J13B, J14B, J16B, J17B	20 pin SMT Socket	Samtec	SSW-110-22-F-D-VS-K
J15A	10 Pin SMT Plug	Samtec	TSM-105-01-L-DV-P
J15B	10 pin SMT Socket	Samtec	SSW-105-22-F-D-VS-K
N/A	TLV320AIC33EVM PWB	Texas Instruments	6465235
JMP2, JMP3, JMP9, JMP13-JMP19	2 Position Jumper , 0 .1" spacing	Samtec	TSW-102-07-L-S
JMP4-JMP8	Bus Wire		
JMP1	3 Position Jumper , 0 .1" spacing	Samtec	TSW-103-07-L-S
JMP10-JMP12	3 X 2 Position Header , 0 .1" spacing	Samtec	TSW-103-07-L-D
MK1	Omnidirectional Microphone Cartridge	Knowles Acoustics	MD9745APZ-F
SW1	4PDT Right Angle Switch	E-Switch	EG4208
TP1-TP39	Miniature Test Point Terminal	Keystone Electronics	5000
TP40, TP41	Multipurpose Test Point Terminal	Keystone Electronics	5011
N/A	Header Shorting Block	Samtec	SNT-100-BK-T

Table 11. USB-MODEVM Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
R4	10Ω 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ1300V
R10, R11	27.4Ω 1/16W 1% Chip Resistor	Panasonic	ERJ-3EKF27R4V
R20	75Ω 1/4W 1% Chip Resistor	Panasonic	ERJ-14NF75R0U
R19	220Ω 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ221V
R14, R21, R22	390Ω 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ391V
R13	649Ω 1/16W 1% Chip Resistor	Panasonic	ERJ-3EKF6490V
R9	1.5KΩ 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ1352V
R1, R2, R3, R5, R6, R7, R8	2.7KΩ 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ272V
R12	3.09KΩ 1/16W 1% Chip Resistor	Panasonic	ERJ-3EKF3091V
R15, R16	10KΩ 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ1303V
R17, R18	100kΩ 1/10W 5% Chip Resistor	Panasonic	ERJ-3GEYJ1304V
RA1	10KΩ 1/8W Octal Isolated Resistor Array	CTS Corporation	742C163103JTR
C18, C19	33pF 50V Ceramic Chip Capacitor, ±5%, NPO	TDK	C1608C0G1H330J
C13, C14	47pF 50V Ceramic Chip Capacitor, ±5%, NPO	TDK	C1608C0G1H470J
C20	100pF 50V Ceramic Chip Capacitor, ±5%, NPO	TDK	C1608C0G1H101J
C21	1000pF 50V Ceramic Chip Capacitor, ±5%, NPO	TDK	C1608C0G1H102J
C15	0.1µF 16V Ceramic Chip Capacitor, ±10%,X7R	TDK	C1608X7R1C104K
C16, C17	0.33µF 16V Ceramic Chip Capacitor, +/-20%,Y5V	TDK	C1608X5R1C334K
C9, C10, C11, C12, C22, C23, C24, C25, C26, C27, C28	1µF 6.3V Ceramic Chip Capacitor, ±10%, X5R	TDK	C1608X5R0J1305K
C1, C2, C3, C4, C5, C6, C7, C8	10µF 6.3V Ceramic Chip Capacitor, ±10%, X5R	TDK	C3216X5R0J1306K
D1	50V, 1A, Diode MELF SMD	Micro Commercial Components	DL4001
D2	Yellow Light Emitting Diode	Lumex	SML-LX0603YW-TR
D3, D4, D6, D7	Green Light Emitting Diode	Lumex	SML-LX0603GW-TR
D5	Red Light Emitting Diode	Lumex	SML-LX0603IW-TR
Q1, Q2	N-Channel MOSFET	Zetex	ZXMN6A07F
X1	6MHz Crystal SMD	Epson	MA-505 6.000M-C0
U8	USB Streaming Controller	Texas Instruments	TAS1020BPFB
U2	5V LDO Regulator	Texas Instruments	REG1117-5
U9	3.3V/1.8V Dual Output LDO Regulator	Texas Instruments	TPS767D318PWP
U3, U4	Quad, Tri-State Buffers	Texas Instruments	SN74LVC125APW
U5, U6, U7	Single IC Buffer Driver with Open Drain o/p	Texas Instruments	SN74LVC1G07DBVR
U10	Single Tri-State Buffer	Texas Instruments	SN74LVC1G125DBVR
U1	64K 2-Wire Serial EEPROM I^2C	Microchip	24LC64I/SN
	USB-MODEVM PCB	Texas Instruments	6463995

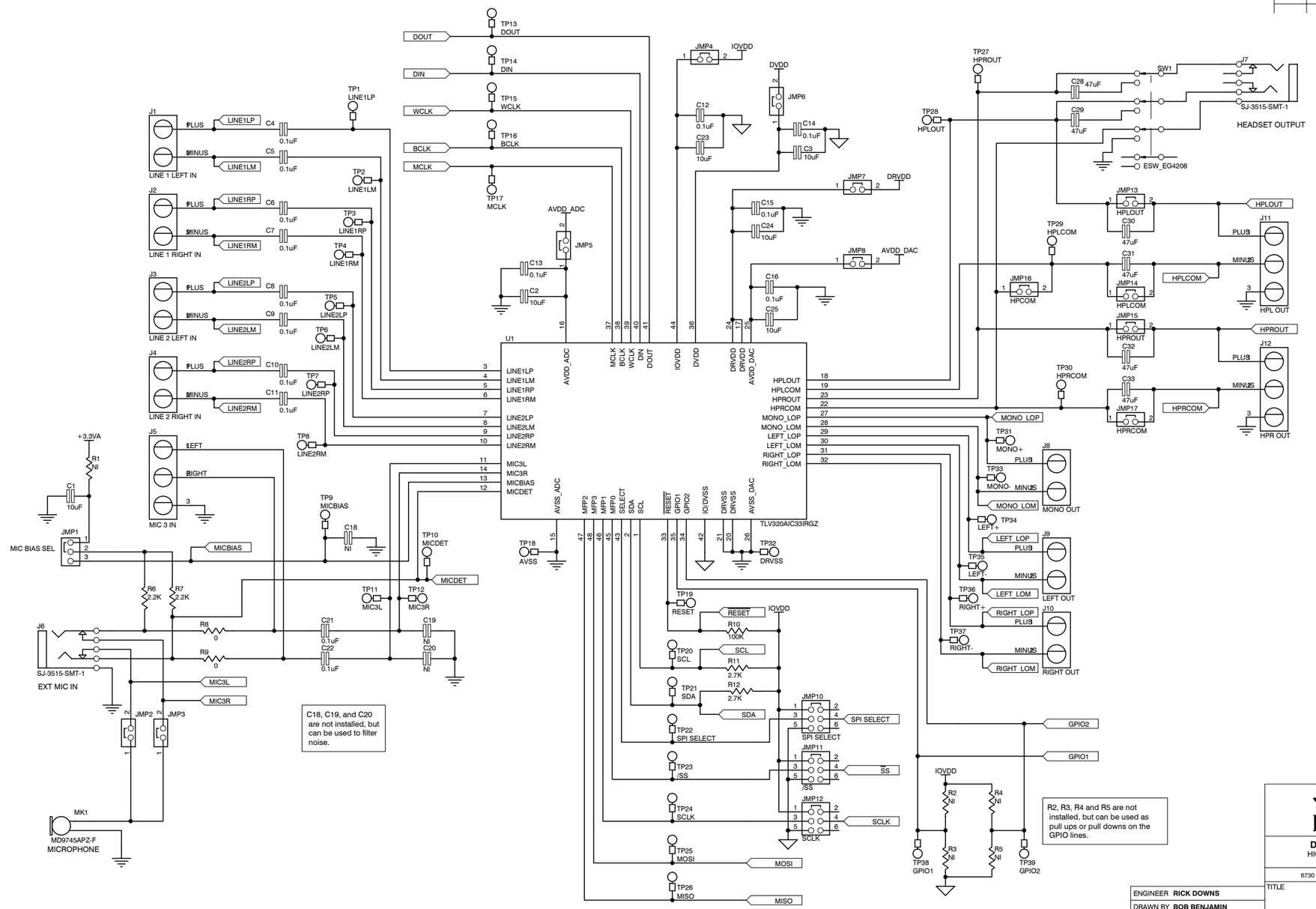
Table 11. USB-MODEVM Bill of Materials (continued)

Designators	Description	Manufacturer	Mfg. Part Number
TP1, TP2, TP3, TP4, TP5, TP6, TP9, TP10, TP11	Miniature test point terminal	Keystone Electronics	5000
TP7, TP8	Multipurpose test point terminal	Keystone Electronics	5011
J7	USB Type B Slave Connector Thru-Hole	Mill-Max	897-30-004-90-000000
J13, J2, J3, J4, J5, J8	2-position terminal block	On Shore Technology	ED555/2DS
J9	2.5mm power connector	CUI Stack	PJ-102B
J130	BNC connector, female, PC mount	AMP/Tyco	414305-1
J131A, J132A, J21A, J22A	20-pin SMT plug	Samtec	TSM-110-01-L-DV-P
J131B, J132B, J21B, J22B	20-pin SMT socket	Samtec	SSW-110-22-F-D-VS-K
J133A, J23A	10-pin SMT plug	Samtec	TSM-105-01-L-DV-P
J133B, J23B	10-pin SMT socket	Samtec	SSW-105-22-F-D-VS-K
J6	4-pin double row header (2x2) 0.1"	Samtec	TSW-102-07-L-D
J134, J135	12-pin double row header (2x6) 0.1"	Samtec	TSW-106-07-L-D
JMP1-JMP4	2-position jumper, 0.1" spacing	Samtec	TSW-102-07-L-S
JMP8-JMP14	2-position jumper, 0.1" spacing	Samtec	TSW-102-07-L-S
JMP5, JMP6	3-position jumper, 0.1" spacing	Samtec	TSW-103-07-L-S
JMP7	3-position dual row jumper, 0.1" spacing	Samtec	TSW-103-07-L-D
SW1	SMT, half-pitch 2-position switch	C&K Division, ITT	TDA02H0SK1
SW2	SMT, half-pitch 8-position switch	C&K Division, ITT	TDA08H0SK1
	Jumper plug	Samtec	SNT-100-BK-T

Appendix A TLV320AIC33EVM Schematic

The schematic diagram is provided as a reference.

Revision History		
REV	ECN Number	Approved



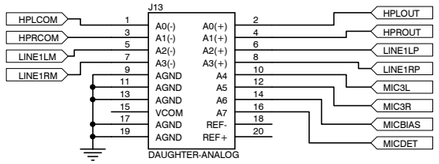
TEXAS INSTRUMENTS

DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

ENGINEER **RICK DOWNS**	TITLE **TLV320AIC33EVM**		
DRAWN BY **BOB BENJAMIN**			
DOCUMENT CONTROL NO. **6465236**	SIZE **A**	DATE **28-Oct-2004**	REV **B**
SHEET **1** OF **2**	FILE:C:\Work\AIC33\Edge\TLV320AIC33EVM.ddb - Documents\AIC33		

REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED



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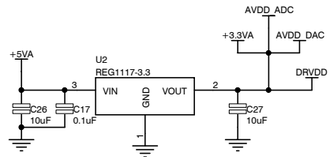
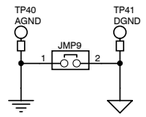
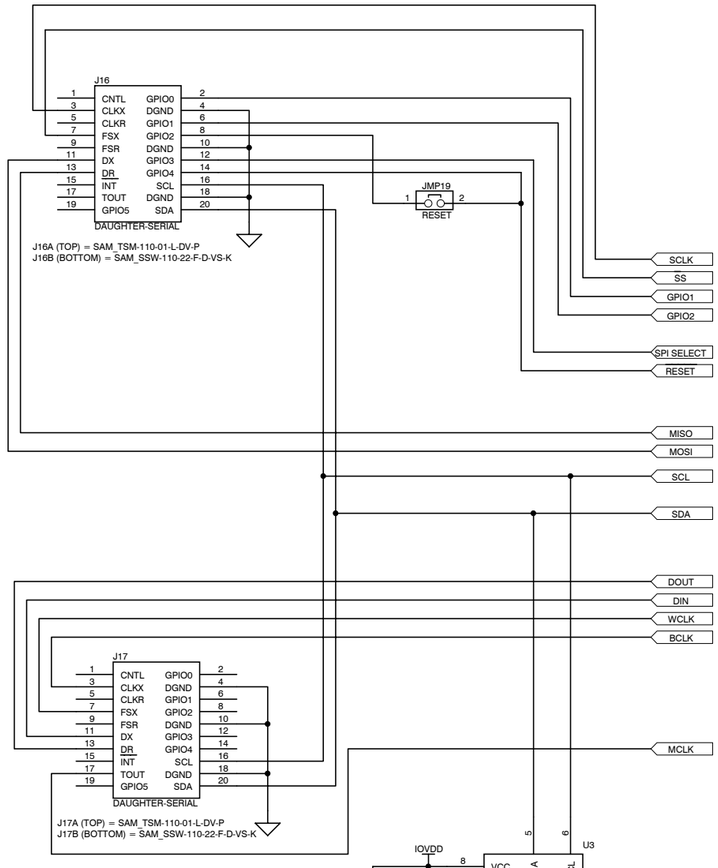
J13B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K







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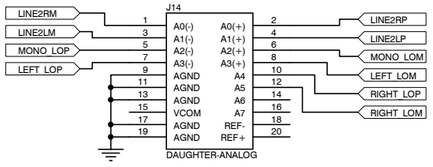
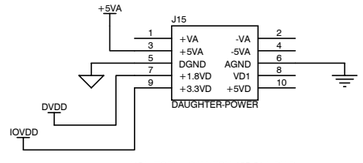
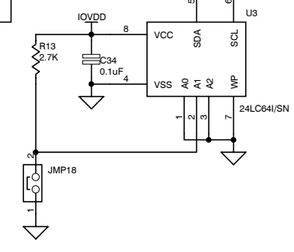


J14A (TOP) = SAM_TSM-110-01-L-DV-P
J14B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K



J15A (TOP) = SAM_TSM-105-01-L-DV-P
J15B (BOTTOM) = SAM_SSW-105-22-F-D-VS-K

J17A (TOP) = SAM_TSM-110-01-L-DV-P
J17B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K



TEXAS INSTRUMENTS

DATA ACQUISITION PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

ENGINEER **RICK DOWNS**	TITLE **TLV320AIC33EVM INTERFACE**		
DRAWN BY **BOB BENJAMIN**			
DOCUMENT CONTROL NO. **6465236**	SIZE **B**	DATE **28-Oct-2004**	REV **B**
SHEET **2** OF **2**	FILE **C:\Work\AIC33\Edge\TLV320AIC33EVM.ddb - Documents\Daughtercard Interface**		

Appendix B USB-MODEVM Schematic

The schematic diagram is provided as a reference.

REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED

IOVDD
Q1 ZXMN6A07F
SDA
J6
EXTERNAL I2C
SCL
Q2 ZXMN6A07F
TP10
+3.3VD
TP9
R3 2.7K
R5 2.7K
+3.3VD
U1
VCC SDA SCL
VSS A0 A1 A2 WP
C9 1uF
24LC64I/SN
C18 33pF
X1
MA-505 6.000M-C0
6.00 MHZ
C19 33pF
J7 USB SLAVE CONN
GND D+ D- VCC
897-30-004-90-000000
R9 1.5K
R10 27.4
R11 27.4
C13 47pF
C14 47pF
C20 100pF
C21 .001uF
R12 3.09K
U8
TAS1020BPFB
SCL SDA VREN RESET MCLKO2 MCLKO1 CSCLK CDATO CDATI CSYNC CRESET CSCHNE
XTALO XTALI PLLFILI PLLFILO MCLKI PUR DP DM DVSS DVSS DVSS AVSS
P1.7 P1.6 P1.5 P1.4 P1.3 P1.2 P1.1 P1.0 DVDD DVDD DVDD AVDD
MRESET TEST EXTEN RSTO P3.0 P3.1 P3.2/XINT P3.3 P3.4 P3.5 NC NC
TP11 MRESET
+3.3VD
R13 649
USB ACTIVE
D2 SML-LX0603YW-TR YELLOW
JMP8 P1.3
JMP9 P1.2
JMP10 P1.1
JMP11 P1.0
JMP12 P3.5
JMP13 P3.4
JMP14 P3.3
C24 1uF
C10 1uF
C11 1uF
C12 1uF
+3.3VD
U3
SN74LVC125APW
1A 2A 3A 4A 1OE 2OE 3OE 4OE VCC 1Y 2Y 3Y 4Y GND
USB MCK
USB I2S
C22 1uF
IOVDD
C28 1uF
U10
SN74LVC1G125DBV
J10 EXT MCLK
R20 75
MCLK
I2SDIN
BCLK
LRCLK
I2SDOUT
+3.3VD
RA1 10K
SW2
A0 A1 A2 USB I2S USB MCK USB SPI USB RST EXT MCK
SW DIP-8
+3.3VD
R6 2.7K
U5
SN74LVC1G07DBV
C23 1uF
IOVDD
J14
EXTERNAL AUDIO DATA
PWR_DWN
+3.3VD
R7 2.7K
U7
SN74LVC1G07DBV
C26 1uF
IOVDD
MISO
MOSI
SS
SCLK
RESET
C27 1uF
IOVDD
U4
SN74LVC125APW
1A 2A 3A 4A 1OE 2OE 3OE 4OE VCC 1Y 2Y 3Y 4Y GND
J15
EXTERNAL SPI
USB RST
USB SPI
INT
+3.3VD
R8 2.7K
C25 1uF
IOVDD
U6
SN74LVC1G07DBV
J8
ED555/2DS
EXT PWR IN
6VDC-10VDC IN
JMP6
PWR SELECT
+5VD
R14 390
D3 SML-LX0603GW-TR GREEN
U2
REG1117-5
VIN GND VOUT
D1 DL4001
C15 0.1uF
C16 0.33uF
C6 10uF
J9
CUI-STACK PJ102-B
2.5 MM
SW1
1.8VD ENABLE
3.3VD ENABLE
REGULATOR ENABLE
R15 10K
R16 10K
U9
TPS767D318PWP
1IN 1IN 1EN 1GND 2GND 2EN 2IN 2IN 1RESET 1OUT 1OUT 2RESET 2OUT 2OUT
R17 100K
R18 100K
C7 10uF
C8 10uF
C17 0.33uF
+1.8VD
R4 10
D5 SML-LX0603IW-TR RED
+3.3VD
R19 220
D4 SML-LX0603GW-TR GREEN
+5VD
+3.3VD
+1.8VD
JMP7
IOVDD SELECT
IOVDD
TP6

ENGINEER	**RICK DOWNS**
DRAWN BY	**ROBERT BENJAMIN**
DOCUMENT CONTROL NO.	**6463996**
SHEET	**1** OF **2**

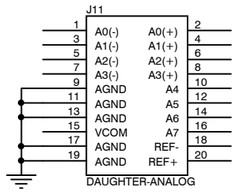
TEXAS INSTRUMENTS
DATA ACQUISITION PRODUCTS
HIGH PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP
6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

TITLE
USB-MODEVM INTERFACE

SIZE **B** | DATE **28-Oct-2004** | REV **B**

FILE **D:\USB-MODEVM\USB Motherboard - ModEvm.ddb - Documents\USB Interface**

REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED



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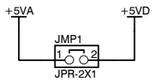
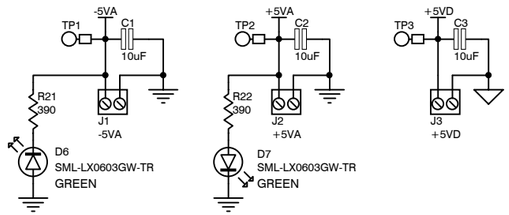
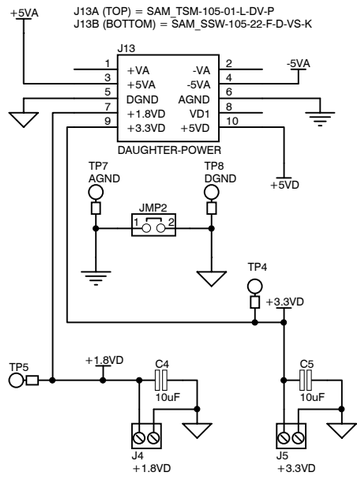
J11B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K







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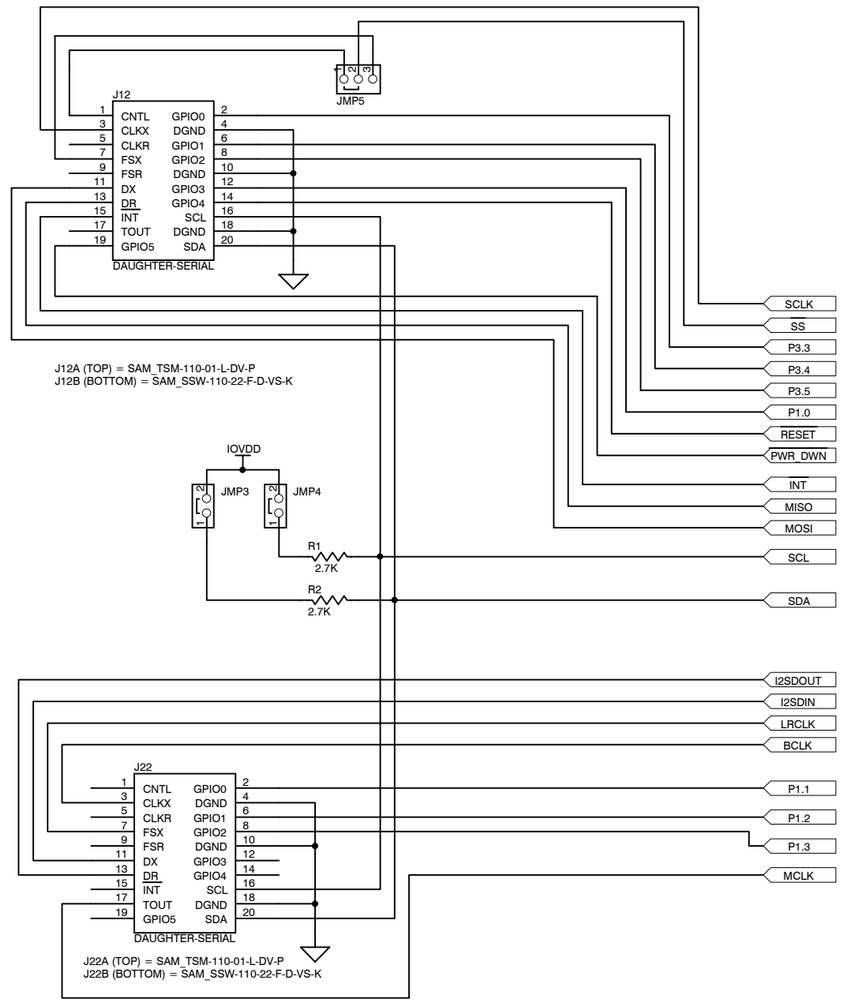

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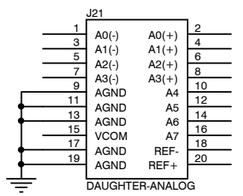
J12B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K

J22A (TOP) = SAM_TSM-110-01-L-DV-P
J22B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K



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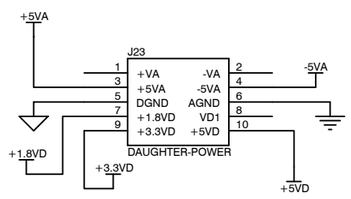
J21B (BOTTOM) = SAM_SSW-110-22-F-D-VS-K



J23A (TOP) = SAM_TSM-105-01-L-DV-P
J23B (BOTTOM) = SAM_SSW-105-22-F-D-VS-K

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DATA ACQUISITION PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

TITLE **USB-MODEVM INTERFACE**

ENGINEER **RICK DOWNS**			
DRAWN BY **ROBERT BENJAMIN**			
DOCUMENT CONTROL NO. **6463996**	SIZE **B**	DATE **28-Oct-2004**	REV **B**
SHEET **2** OF **2**	FILE **D:\USB-MODEVM\USB Motherboard - ModEvm.ddb - Documents\Daughtercard Interface**		

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During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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- Экспресс доставка в любую точку России;
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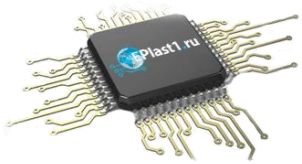
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
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