

### General Description

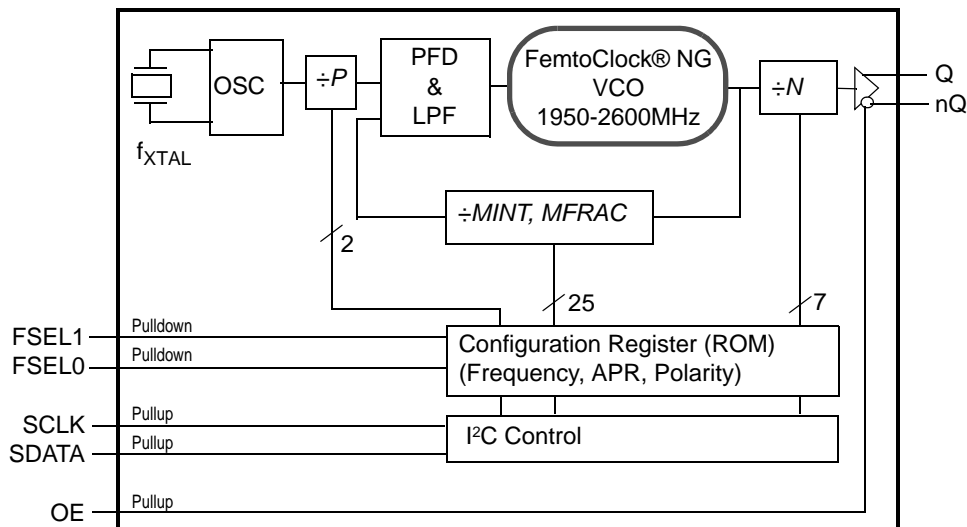
The IDT8N3Q001 is a Quad-Frequency Programmable Clock Oscillator with very flexible frequency programming capabilities. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency and low phase noise performance. The device accepts 2.5V or 3.3V supply and is packaged in a small, lead-free (RoHS 6) 10-lead Ceramic 5mm x 7mm x 1.55mm package.

Besides the four default power-up frequencies set by the FSEL0 and FSEL1 pins, the IDT8N3Q001 can be programmed via the I<sup>2</sup>C interface to output clock frequencies between 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz to a very high degree of precision with a frequency step size of  $435.9\text{Hz} \div N$  ( $N$  is the PLL output divider). Since the FSEL0 and FSEL1 pins are mapped to 4 independent PLL M and N divider registers (P, MINT, MFRAC and N), reprogramming those registers to other frequencies under control of FSEL0 and FSEL1 is supported. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

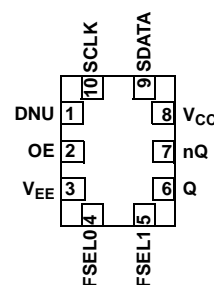
### Features

- Fourth generation FemtoClock® NG technology
- Programmable clock output frequency from 15.476MHz to 866.67MHz and from 975MHz to 1,300MHz
- Four power-up default frequencies (see part number order codes), re-programmable by I<sup>2</sup>C
- I<sup>2</sup>C programming interface for the output clock frequency and internal PLL control registers
- Frequency programming resolution is  $435.9\text{Hz} \div N$
- One 2.5V, 3.3V LVPECL clock output
- Two control inputs for the power-up default frequency
- LVCMOS/LVTTL compatible control inputs
- RMS phase jitter @ 156.25MHz (12kHz - 20MHz): 0.244ps (typical), integer PLL feedback configuration
- RMS phase jitter @ 156.25MHz (1kHz - 40MHz): 0.265ps (typical), integer PLL feedback configuration
- Full 2.5V or 3.3V supply modes
- -40°C to 85°C ambient operating temperature
- Available in Lead-free (RoHS 6) package

### Block Diagram



### Pin Assignment



**IDT8N3Q001**  
**10-lead Ceramic 5mm x 7mm x 1.55mm**  
**package body**  
**CD Package**  
**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	DNU	Unused		Do not use.
2	OE	Input	Pullup	Output enable pin. See Table 3 for function. LVCMOS/LVTTL interface levels.
3	V <sub>EE</sub>	Power		Negative power supply.
5, 4	FSEL1, FSEL0	Input	Pulldown	Default frequency select pins. See the Default Frequency Order Codes section. LVCMOS/LVTTL interface levels.
6, 7	Q, nQ	Output		Differential clock output. LVPECL interface levels.
8	V <sub>CC</sub>	Power		Power supply pin.
9	SDATA	Input/Output	Pullup	I <sup>2</sup> C Data Input/Output. Input: LVCMOS/LVTTL compatible interface levels. Output: Open drain.
10	SCLK	Input	Pullup	I <sup>2</sup> C Clock Input. LVCMOS/LVTTL compatible interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			5.5		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			50		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			50		kΩ

## Function Tables

**Table 3A. OE Configuration**

Input	Output Enable
0	Outputs Q, nQ are in high-impedance state.
1 (default)	Outputs are enabled.

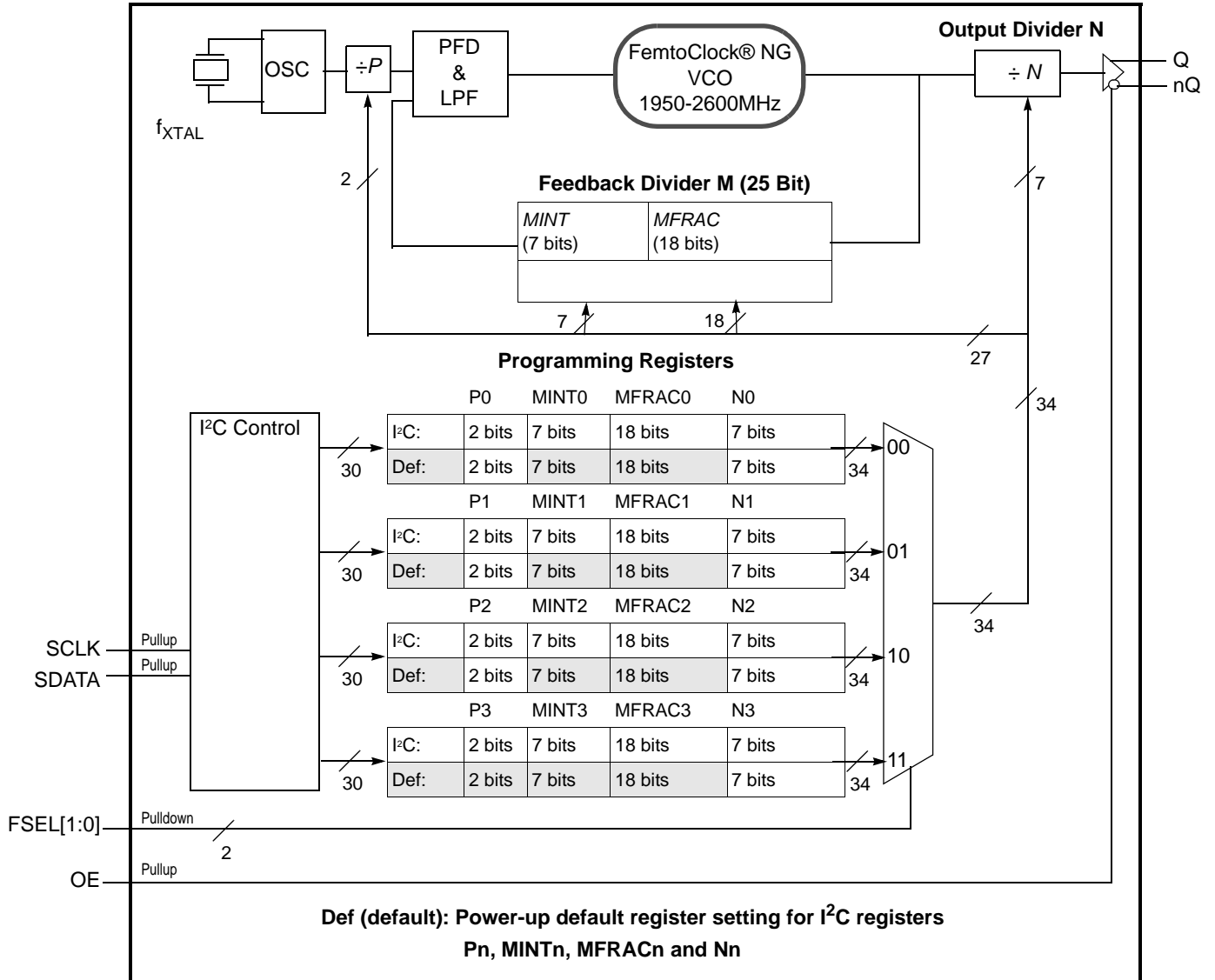
NOTE: OE is an asynchronous control.

**Table 3B. Output Frequency Range**

15.476MHz to 866.67MHz
975MHz to 1,300MHz

NOTE: Supported output frequency range. The output frequency can be programmed to any frequency in this range and to a precision of 218Hz or better.

### Block Diagram with Programming Registers



## Principles of Operation

The block diagram consists of the internal 3<sup>rd</sup> overtone crystal and oscillator which provide the reference clock  $f_{XTAL}$  of either 114.285 MHz or 100MHz. The PLL includes the FemtoClock NG VCO along with the Pre-divider ( $P$ ), the feedback divider ( $M$ ) and the post divider ( $N$ ). The  $P$ ,  $M$ , and  $N$  dividers determine the output frequency based on the  $f_{XTAL}$  reference and must be configured correctly for proper operation. The feedback divider is fractional supporting a huge number of output frequencies. The configuration of the feedback divider to integer-only values results in an improved output phase noise characteristics at the expense of the range of output frequencies. In addition, internal registers are used to hold up to four different factory pre-set  $P$ ,  $M$ , and  $N$  configuration settings. These default pre-sets are stored in the I<sup>2</sup>C registers at power-up. Each configuration is selected via the FSEL[1:0] pins and can be read back using the SCLK and SDATA pins.

The user may choose to operate the device at an output frequency different than that set by the factory. After power-up, the user may write new  $P$ ,  $N$  and  $M$  settings into one or more of the four configuration registers and then use the FSEL[1:0] pins to select the newly programmed configuration. Note that the I<sup>2</sup>C registers are volatile and a power supply cycle will reload the pre-set factory default conditions.

If the user does choose to write a different  $P$ ,  $M$ , and  $N$  configuration, it is recommended to write to a configuration which is not currently selected by FSEL[1:0] and then change to that configuration after the I<sup>2</sup>C transaction has completed. Changing the FSEL[1:0] controls results in an immediate change of the output frequency to the selected register values. The  $P$ ,  $M$ , and  $N$  frequency configurations support an output frequency range 15.476MHz to 866.67MHz and 975MHz to 1,300MHz.

The devices use the fractional feedback divider with a delta-sigma modulator for noise shaping and robust frequency synthesis capability. The relatively high reference frequency minimizes phase noise generated by frequency multiplication and allows more efficient shaping of noise by the delta-sigma modulator.

The output frequency is determined by the 2-bit pre-divider ( $P$ ), the feedback divider ( $M$ ) and the 7-bit post divider ( $N$ ). The feedback divider ( $M$ ) consists of both a 7-bit integer portion ( $MINT$ ) and an 18-bit fractional portion ( $MFRAC$ ) and provides the means for high-resolution frequency generation. The output frequency  $f_{OUT}$  is calculated by:

$$f_{OUT} = f_{XTAL} \cdot \frac{1}{P \cdot N} \cdot \left[ MINT + \frac{MFRAC + 0.5}{2^{18}} \right] \quad (1)$$

The four configuration registers for the  $P$ ,  $M$  ( $MINT$  &  $MFRAC$ ) and  $N$  dividers which are named  $P_n$ ,  $MINT_n$ ,  $MFRAC_n$  and  $N_n$  with  $n=0$  to 3. "n" denominates one of the four possible configurations.

As identified previously, the configurations of  $P$ ,  $M$  ( $MINT$  &  $MFRAC$ ) and  $N$  divider settings are stored in the I<sup>2</sup>C register, and the configuration loaded at power-up is determined by the FSEL[1:0] pins.

**Table 4. Frequency Selection**

Input		Selects	Register
FSEL1	FSEL0		
0 (def.)	0 (def.)	Frequency 0	P0, MINT0, MFRAC0, N0
0	1	Frequency 1	P1, MINT1, MFRAC1, N1
1	0	Frequency 2	P2, MINT2, MFRAC2, N2
1	1	Frequency 3	P3, MINT3, MFRAC3, N3

## Frequency Configuration

An order code is assigned to each frequency configuration programmed by the factory (default frequencies). For more information on the available default frequencies and order codes, please see the Ordering Information Section in this document. For available order codes, see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.

For more information and guidelines on programming of the device for custom frequency configurations, the register description, the selection of fractional and integer-feedback configurations and the serial interface description, see the *FemtoClock NG Ceramic 5x7 Module Programming Guide*.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{CC}$	3.63V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$ (SDATA) Outputs, $I_O$ (LVPECL) Continuous Current Surge Current	10mA 50mA 100mA
Package Thermal Impedance, $\theta_{JA}$	49.4°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 5A. Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				140	mA

**Table 5B. Power Supply DC Characteristics,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				136	mA

**Table 5C. LVCMOS/LVTTL DC Characteristic,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$V_{IH}$	Input High Voltage	FSEL[1:0], OE	$V_{CC} = 3.3V + 5\%$	1.7		$V_{CC} + 0.3$	V
		FSEL[1:0], OE	$V_{CC} = 2.5V + 5\%$	1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	FSEL[1:0]	$V_{CC} = 3.3V + 5\%$	-0.3		0.5	V
		OE	$V_{CC} = 3.3V + 5\%$	-0.3		0.8	V
		FSEL[1:0]	$V_{CC} = 2.5V + 5\%$	-0.3		0.5	V
		OE	$V_{CC} = 2.5V + 5\%$	-0.3		0.8	V
$I_{IH}$	Input High Current	OE	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			10	$\mu A$
		SDATA, SCLK	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu A$
		FSEL0, FSEL1	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
$I_{IL}$	Input Low Current	OE	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-500			$\mu A$
		SDATA, SCLK	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu A$
		FSEL0, FSEL1	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu A$

**Table 5D. LVPECL DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.8$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.5$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.55		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

## AC Electrical Characteristics

**Table 6. AC Characteristics,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency Q, nQ	Output Divider, $N = 3$ to 126	15.476		866.67	MHz
		Output Divider, $N = 2$	975		1,300	MHz
$f_I$	Initial Accuracy	Measured at $25^\circ C$			$\pm 10$	ppm
$f_S$	Temperature Stability	Option code = A or B			$\pm 100$	ppm
		Option code = E or F			$\pm 50$	ppm
		Option code = K or L			$\pm 20$	ppm
$f_A$	Aging	Frequency drift over 10 year life			$\pm 3$	ppm
		Frequency drift over 15 year life			$\pm 5$	ppm
$f_T$	Total Stability	Option code A or B (10 year life)			$\pm 113$	ppm
		Option code E or F (10 year life)			$\pm 63$	ppm
		Option code K or L (10 year life)			$\pm 33$	ppm
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1				20	ps
$f_{jit(per)}$	RMS Period Jitter; NOTE 1			2.85	4	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random); Fractional PLL feedback and $f_{XTAL} = 100.000MHz$ (2xxx order codes)	$17 MHz \leq f_{OUT} \leq 1300MHz$ , NOTE 2,3,4		0.440	0.995	ps
		$500 MHz \leq f_{OUT} \leq 1300MHz$ , NOTE 2,3,4		0.240	0.390	ps
	RMS Phase Jitter (Random); Integer PLL feedback and $f_{XTAL} = 100.00MHz$ (1xxx order codes)	$125 MHz \leq f_{OUT} < 500MHz$ , NOTE 2,3,4		0.245	0.425	ps
		$17 MHz \leq f_{OUT} < 125MHz$ , NOTE 2,3,4		0.350	0.555	ps
		$f_{OUT} = 156.25MHz$ , NOTE 2, 3, 4		0.244		ps
		$f_{OUT} = 156.25MHz$ , NOTE 2, 3, 5		0.265		ps
	RMS Phase Jitter (Random) Fractional PLL feedback and $f_{XTAL} = 114.285MHz$ (0xxx order codes)	$17 MHz \leq f_{OUT} \leq 1300 MHz$ , NOTE 2, 3, 4		0.475	0.990	ps
$\Phi_N(100)$	Single-side band phase noise, 100Hz from Carrier	156.25MHz		-94.7		dBc/Hz
$\Phi_N(1k)$	Single-side band phase noise, 1kHz from Carrier	156.25MHz		-121.3		dBc/Hz
$\Phi_N(10k)$	Single-side band phase noise, 10kHz from Carrier	156.25MHz		-131.1		dBc/Hz

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$\Phi_N(100k)$	Single-side band phase noise, 100kHz from Carrier	156.25MHz		-137.3		dBc/Hz
$\Phi_N(1M)$	Single-side band phase noise, 1MHz from Carrier	156.25MHz		-139.0		dBc/Hz
$\Phi_N(10M)$	Single-side band phase noise, 10MHz from Carrier	156.25MHz		-154.9		dBc/Hz
PSNR	Power Supply Noise Rejection	50mV Sinusoidal Noise 1kHz - 50kHz		-54		dB
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	100		425	ps
odc	Output Duty Cycle		45		55	%
$t_{STARTUP}$	Oscillator Start-Up Time				20	ms
$t_{SET}$	Output frequency settling time after FSEL0 and FSEL1 values are changed			470		$\mu$ s

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: XTAL parameters (initial accuracy, temperature stability, aging and total stability) are guaranteed by manufacturing.

NOTE 1: This parameter is defined in accordance with JEDEC standard 65.

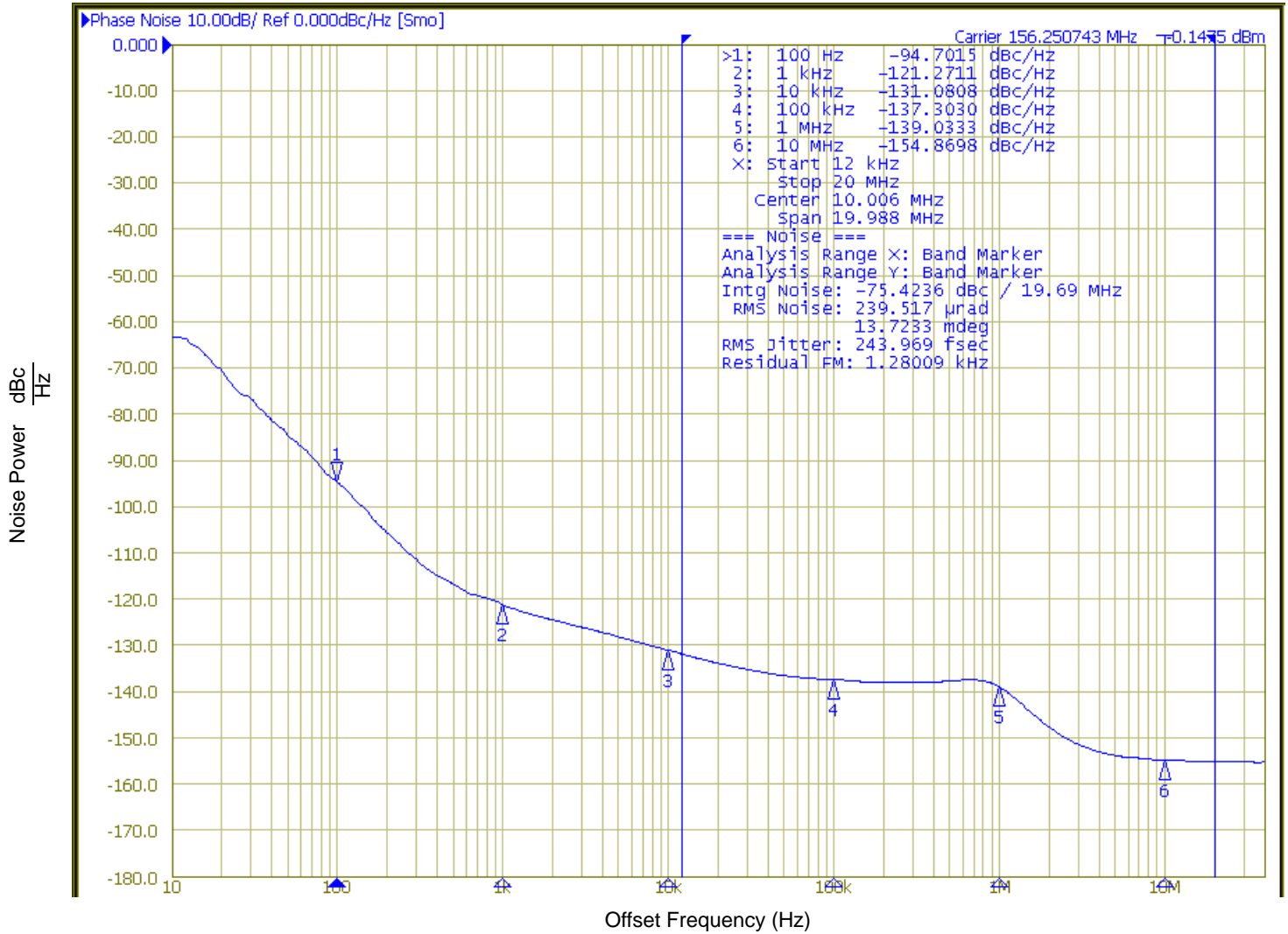
NOTE 2: Please refer to the phase noise plots.

NOTE 3: Please see the FemtoClockNG Ceramic 5x7 Modules Programming guide for more information on PLL feedback modes and the optimum configuration for phase noise. Integer PLL feedback is the default operation for the dddd = 1xxx order codes and configures  $DSM\_ENA = 0$  and  $ADC\_EN = 0$ .

NOTE 4: Integration range: 12kHz-20MHz.

NOTE 5: Integration range: 1kHz-40MHz.

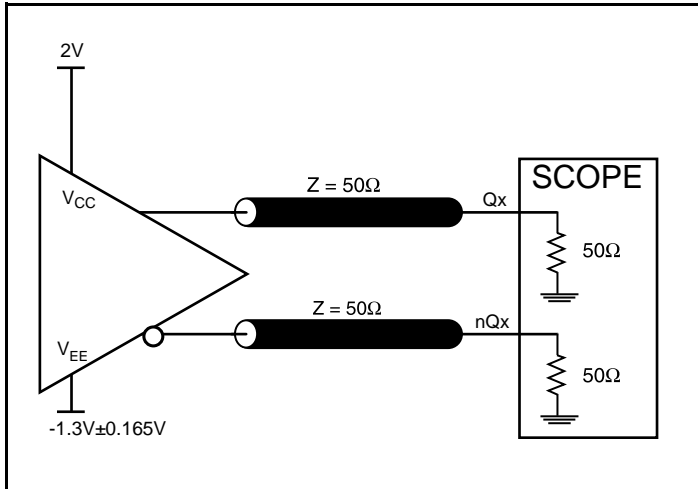
### Typical Phase Noise at 156.25MHz (12kHz - 20MHz)



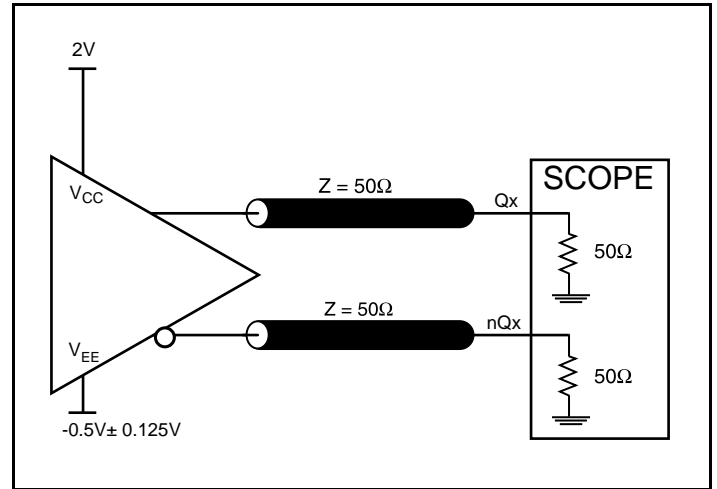
NOTE: RMS Phase Noise (Random) for Integer PLL Feedback and  $f_{\text{XTAL}}=100.000\text{MHz}$ .



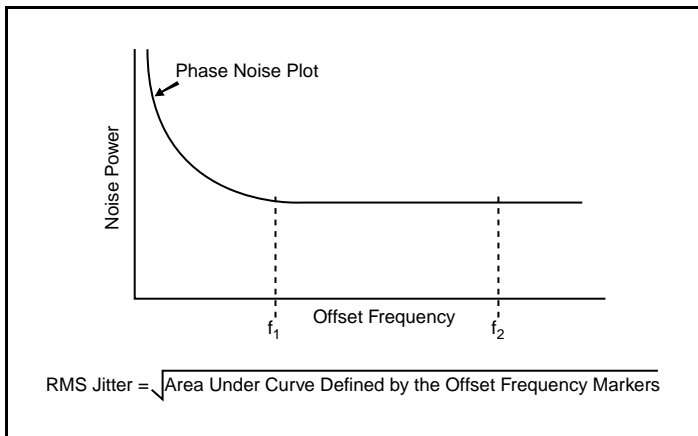
### Parameter Measurement Information



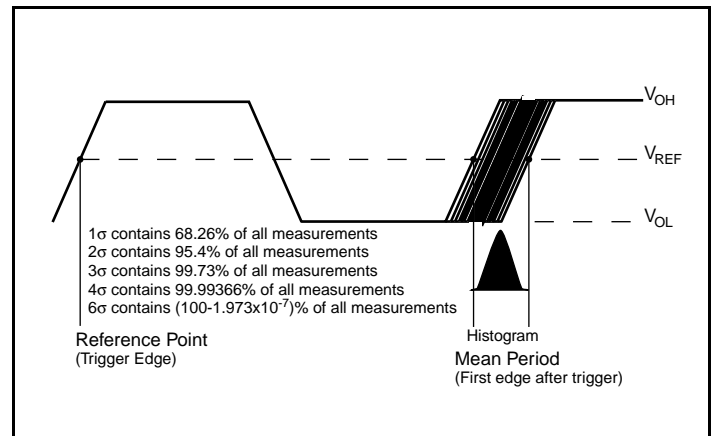
3.3V LVPECL Output Load AC Test Circuit



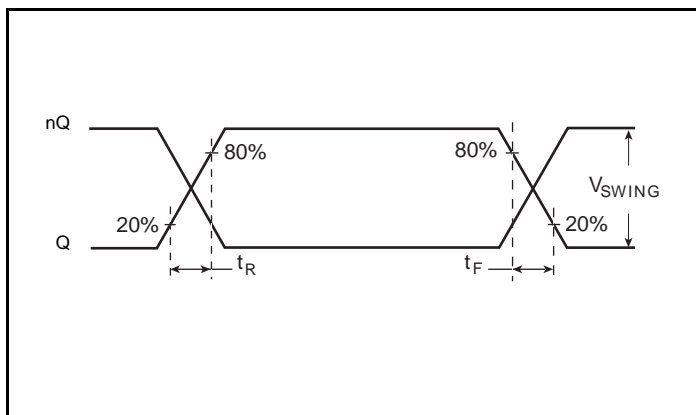
2.5V LVPECL Output Load AC Test Circuit



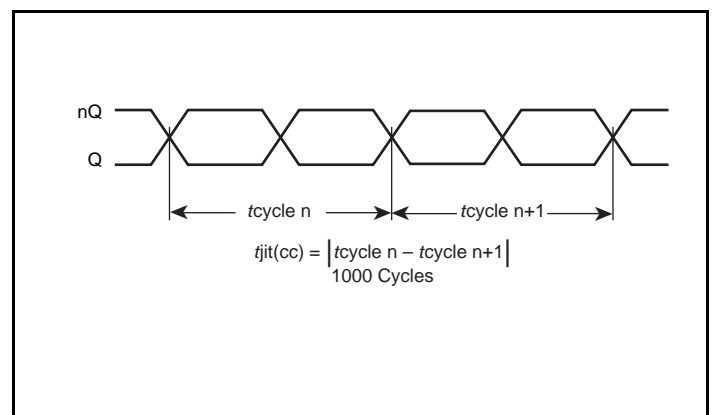
RMS Phase Jitter



Period Jitter

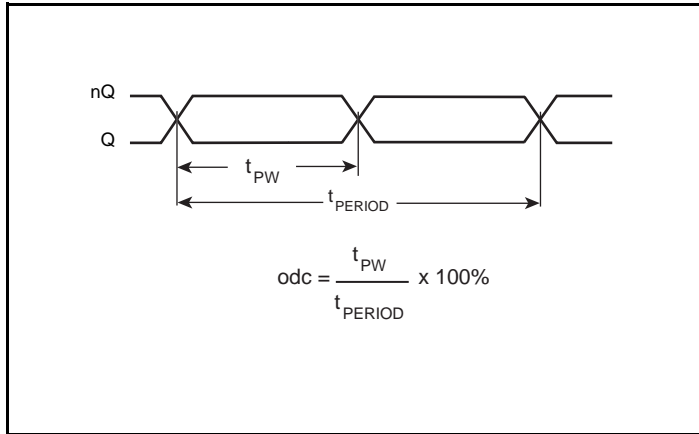


Output Rise/Fall Time



Cycle-to-Cycle Jitter

## Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period

## Applications Information

### Recommendations for Unused Input Pins

#### Inputs:

##### LVC MOS Select Pins

The FSEL[1:0] pins have internal pulldowns and OE control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used. SCLK and SDATA should be left floating if not used.

### Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 1A and 1B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

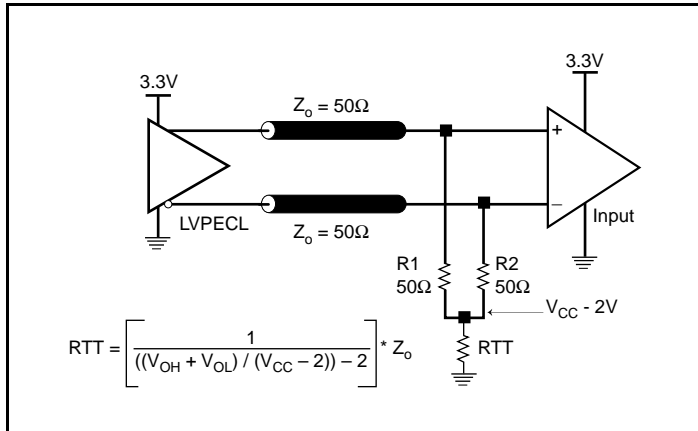


Figure 1A. 3.3V LVPECL Output Termination

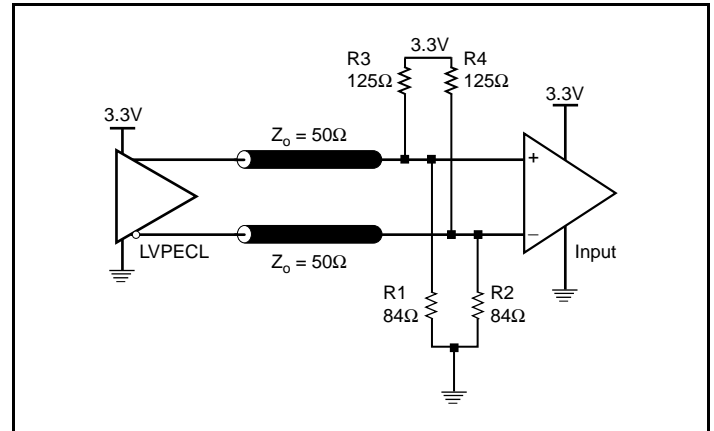


Figure 1B. 3.3V LVPECL Output Termination

### Termination for 2.5V LVPECL Outputs

Figure 2A and Figure 2B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC} - 2V$ . For  $V_{CC} = 2.5V$ , the  $V_{CC} - 2V$  is very close to ground

level. The  $R3$  in Figure 2B can be eliminated and the termination is shown in Figure 2C.

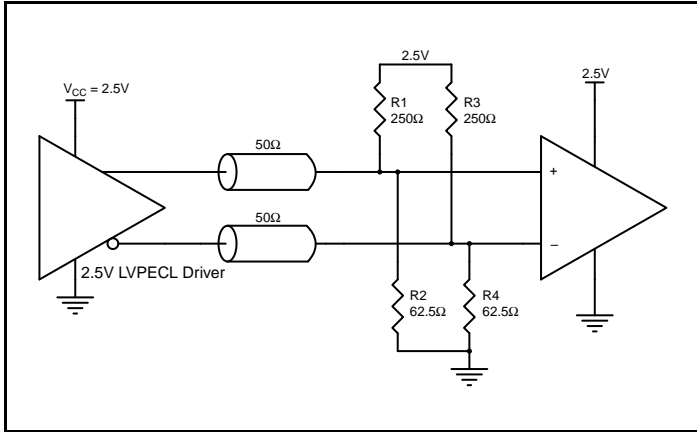


Figure 2A. 2.5V LVPECL Driver Termination Example

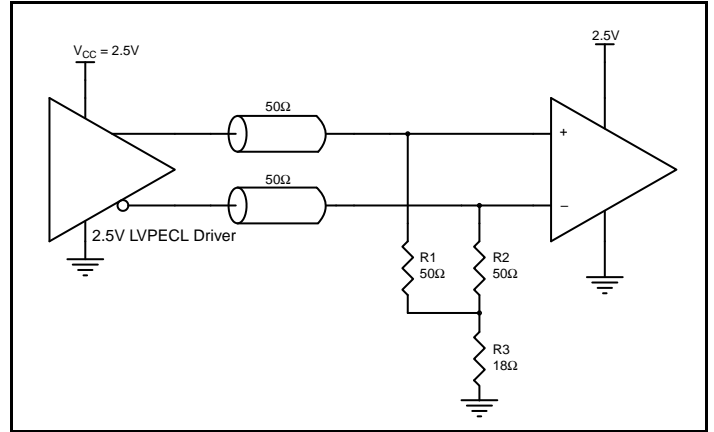


Figure 2B. 2.5V LVPECL Driver Termination Example

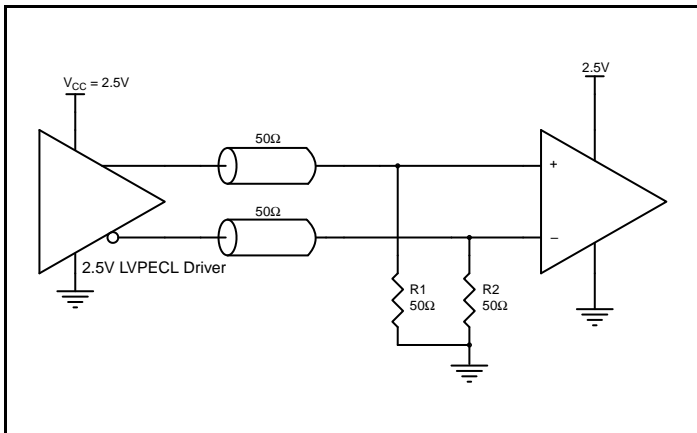


Figure 2C. 2.5V LVPECL Driver Termination Example

### Schematic Layout

Figure 3 shows an example of IDT8N3Q001 application schematic. In this example, the device is operated at  $V_{CC} = 3.3V$ . As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8N3Q001 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

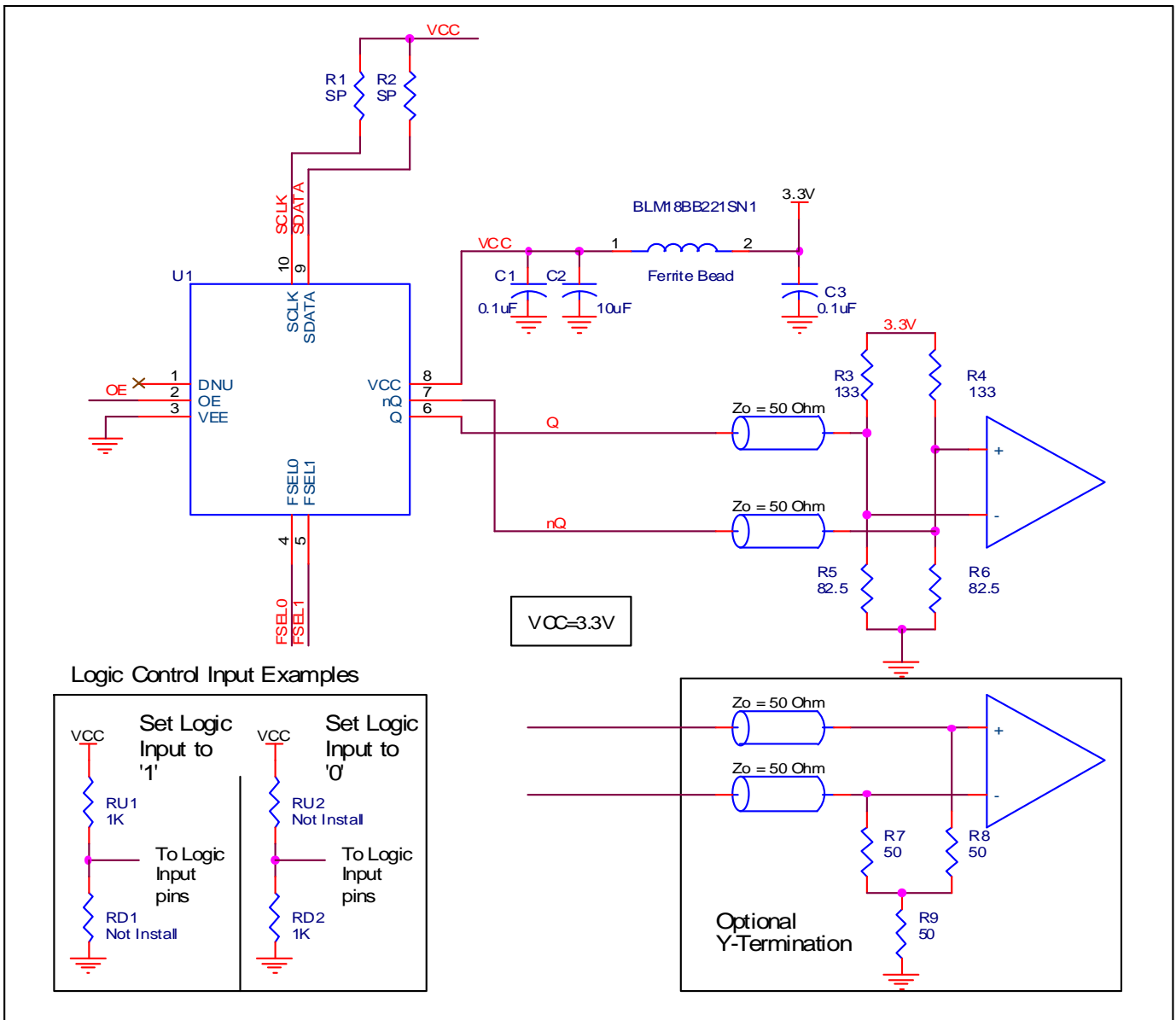


Figure 3. IDT8N3Q001 Application Schematic

## Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8N3Q001. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the IDT8N3Q001 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 140mA = 485.1mW$
- Power (outputs)<sub>MAX</sub> = **34.2mW/Loaded Output pair**

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) = 485.1mW + 34.2mW = **519.3mW**

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 49.4°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.519W * 49.4^\circ C/W = 110.7^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

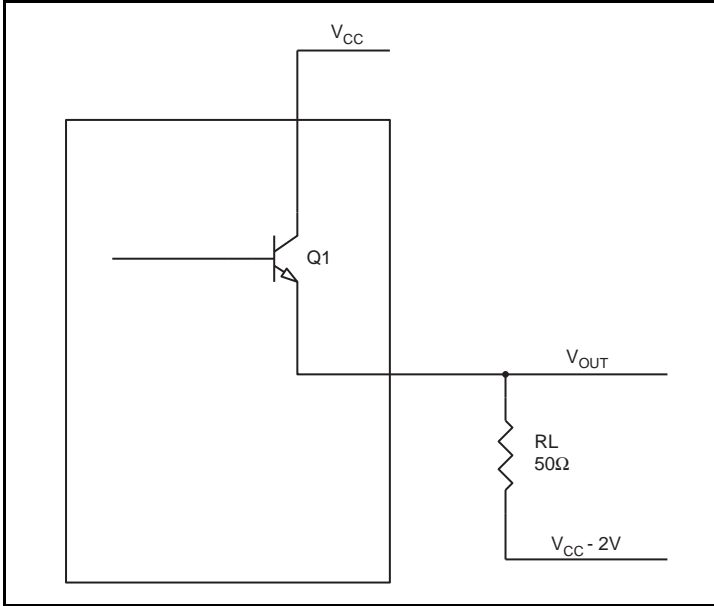
**Table 7. Thermal Resistance  $\theta_{JA}$  for 10 Lead Ceramic 5mm x 7mm Package, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	41°C/W

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 4*.



**Figure 4. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.8V$   
( $V_{CC\_MAX} - V_{OH\_MAX}$ ) = **0.8V**
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.5V$   
( $V_{CC\_MAX} - V_{OL\_MAX}$ ) = **1.5V**

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.8V)/50\Omega] * 0.8V = \mathbf{19.2mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.5V)/50\Omega] * 1.5V = \mathbf{15mW}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{34.2mW}$$

## Reliability Information

**Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 10-lead Ceramic 5mm x 7mm Package**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	<b>0</b>	<b>1</b>	<b>2.5</b>
Multi-Layer PCB, JEDEC Standard Test Boards	49.4°C/W	44.2°C/W	41°C/W

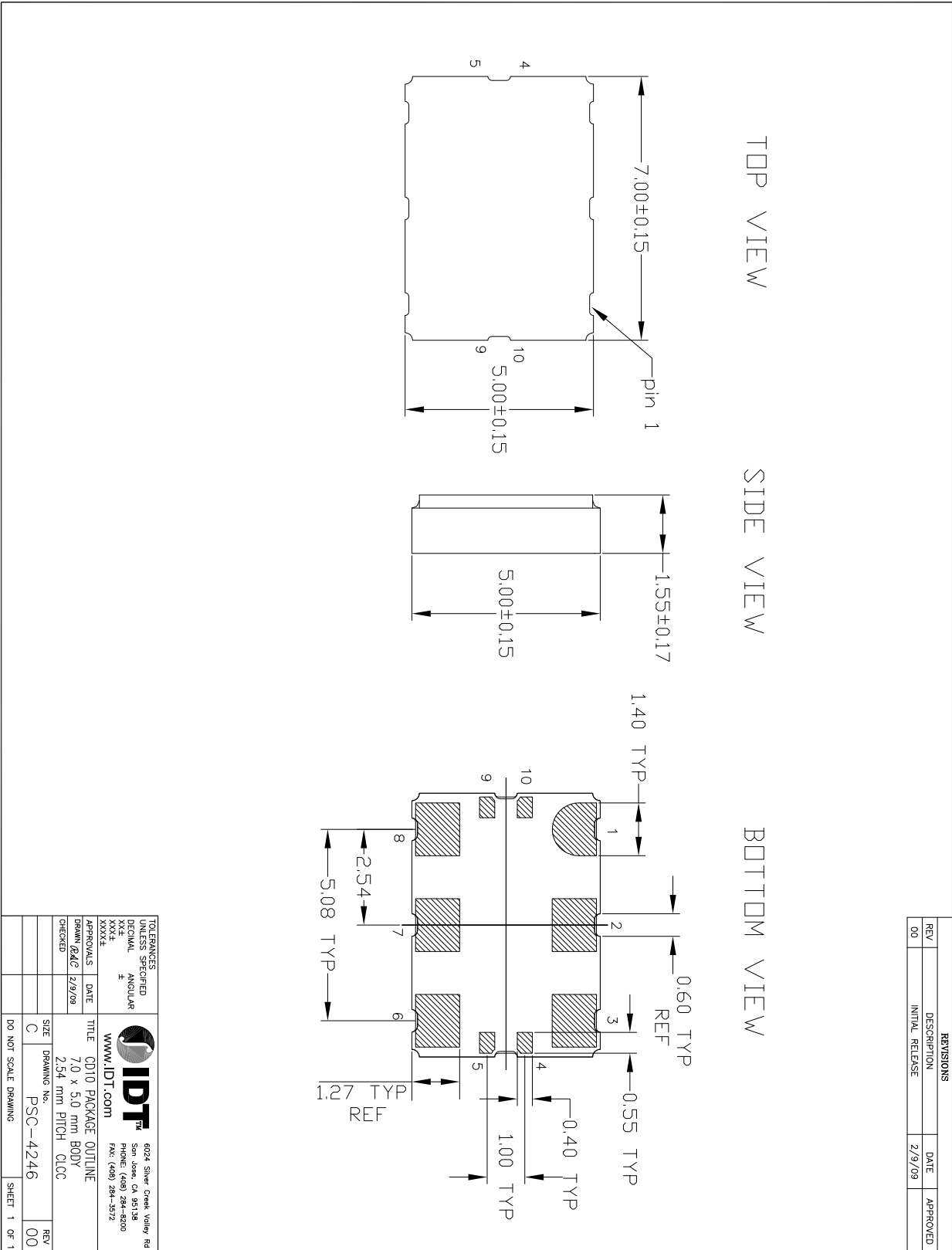
NOTE: For proper thermal dissipation, the PCB layout for the pin pad should at minimum equal the package pin dimensions.

## Transistor Count

The transistor count for IDT8N3Q001 Rev G is: 47,372



# Package Outline and Package Dimensions



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	2/9/09	

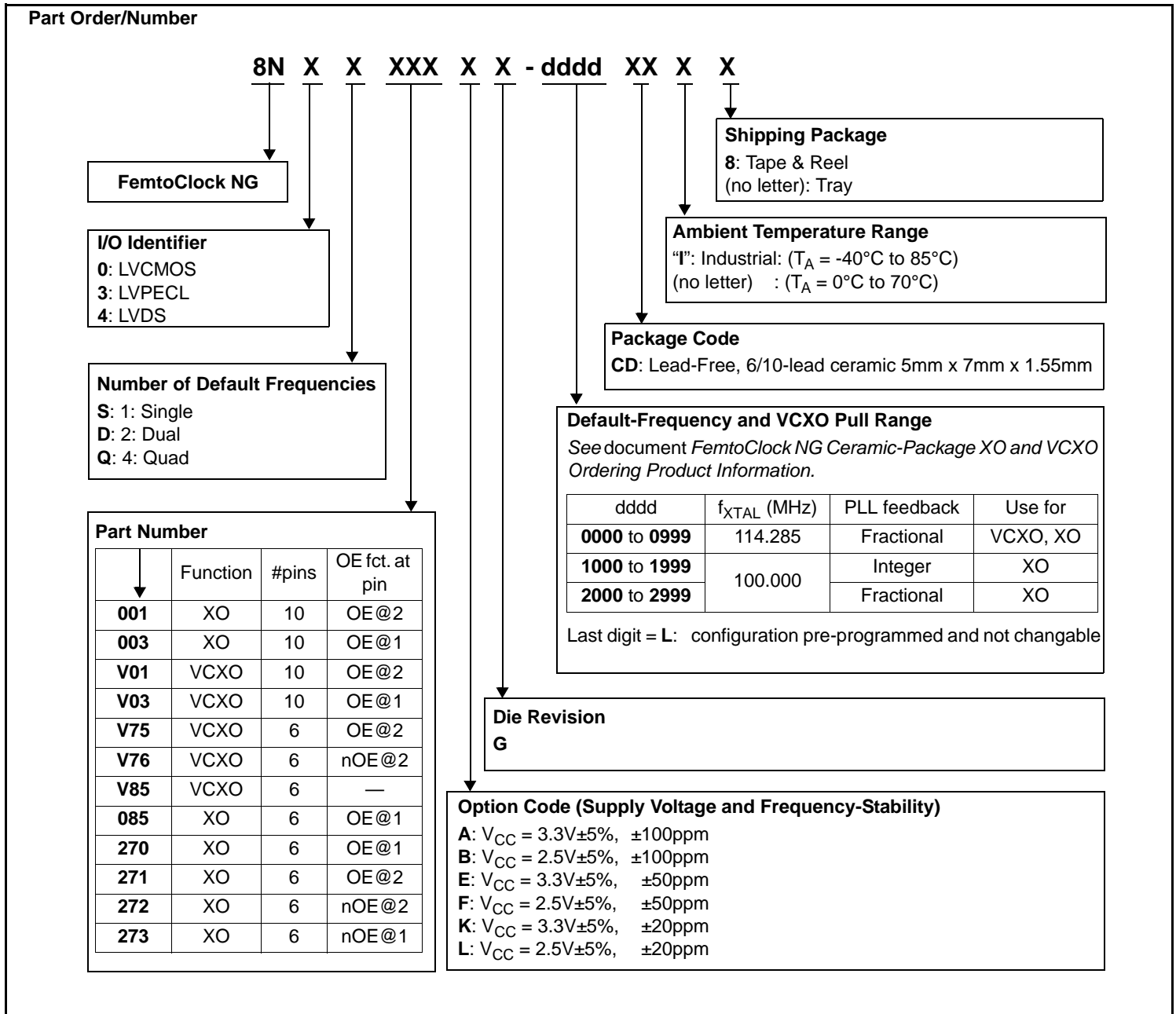
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DECIMAL	ANGULAR		
±	±	www.IDT.com	
APPROVALS		DATE	TITLE
DESIGN	CHKD	2/9/09	7.0 x 5.0 mm BODY
CHECKED			2.54 mm PITCH QJCC
SIZE	DRAWING No.	PSC-4246	
C		DO NOT SCALE DRAWING	
REV		SHEET	1 OF 1
00			

# Ordering Information for FemtoClock NG Ceramic-Package XO and VCXO Products

The programmable VCXO and XO devices support a variety of device options such as the output type, number of default frequencies, internal crystal frequency, power supply voltage, ambient temperature range and the frequency accuracy. The device options, default frequencies and default VCXO pull range must be specified at the time of order and are programmed by IDT before the shipment. Shown below are the available order codes, including the device options and default frequency configurations. Example part number: the order code 8N3QV01FG-0001CDI specifies a programmable, quad default-frequency VCXO with a voltage supply of 2.5V, a LVPECL output, a ±50 ppm crystal frequency accuracy, contains a

114.285MHz internal crystal as frequency source, industrial temperature range, a lead-free (6/6 RoHS) 10-lead Ceramic 5mm x 7mm x 1.55mm package and is factory-programmed to the default frequencies of 100MHz, 122.88MHz, 125MHz and 156.25MHz and to the VCXO pull range of minimum ±100 ppm.

Other default frequencies and order codes are available from IDT on request. For more information on available default frequencies, see the *FemtoClock NG Ceramic-Package XO and VCXO Ordering Product Information* document.



**Table 9. Device Marking**

<b>Marking</b>	Industrial Temperature Range ( $T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ )	Commercial Temperature Range ( $T_A = 0^{\circ}\text{C}$ to $70^{\circ}\text{C}$ )
	IDT8N3x001yG- <b>ddddCDI</b>	IDT8N3x001yG- <b>ddddCD</b>
	<b>x</b> = Number of Default Frequencies, <b>y</b> = Option Code, <b>dddd</b> =Default-Frequency and VCXO Pull Range	

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## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	9	19	Table 9 Device Marking, corrected marking.	3/6/12

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