## Data Sheet

## FEATURES

### 3.3 V/5.2 V single-supply operation

 150 ps propagation delay15 ps overdrive and slew rate dispersion 8 GHz equivalent input rise time bandwidth
80 ps minimum pulse width
35 ps typical output rise/fall
10 ps deterministic jitter (DJ)
200 fs random jitter (RJ)
On-chip terminations at both input pins
Robust inputs with no output phase reversal
Resistor-programmable hysteresis
Differential latch control
Extended industrial $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ temperature range

## APPLICATIONS

Clock and data signal restoration and level shifting
Automatic test equipment (ATE)
High speed instrumentation
Pulse spectroscopy
Medical imaging and diagnostics
High speed line receivers
Threshold detection
Peak and zero-crossing detectors
High speed trigger circuitry

## GENERAL DESCRIPTION

The ADCMP572 and ADCMP573 are ultrafast comparators fabricated on Analog Devices, Inc., proprietary XFCB3 Silicon Germanium (SiGe) bipolar process. The ADCMP572 features CML output drivers and latch inputs, and the ADCMP573 features reduced swing PECL (RSPECL) output drivers and latch inputs.
Both devices offer 150 ps propagation delay and 80 ps minimum pulse width for 10 Gbps operation with 200 fs rms random jitter (RJ). Overdrive and slew rate dispersion are typically less than 15 ps .

A flexible power supply scheme allows both devices to operate with a single 3.3 V positive supply and $\mathrm{a}-0.2 \mathrm{~V}$ to +1.2 V input signal range or with split input/output supplies to support a wider -0.2 V to +3.2 V input signal range and an independent range of output levels. $50 \Omega$ on-chip termination resistors are
provided at both inputs with the optional capability to be left open (on an individual pin basis) for applications requiring high impedance inputs.
The CML output stage is designed to directly drive 400 mV into $50 \Omega$ transmission lines terminated to between 3.3 V to 5.2 V . The RSPECL output stage is designed to drive 400 mV into $50 \Omega$ terminated to $\mathrm{V}_{\mathrm{CCO}}-2 \mathrm{~V}$ and is compatible with several commonly used PECL logic families. The comparator input stage offers robust protection against large input overdrive, and the outputs do not phase reverse when the valid input signal range is exceeded. High speed latch and programmable hysteresis features are also provided.

The ADCMP572 and ADCMP573 are available in a 16-lead LFCSP package and have been characterized over an extended industrial temperature range of $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$.

Rev. B

## ADCMP572/ADCMP573

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## 4/05-Revision 0: Initial Version

## ELECTRICAL CHARACTERISTICS

$\mathrm{V}_{\mathrm{CCI}}=\mathrm{V}_{\mathrm{CCO}}=3.3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, typical at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$, unless otherwise noted.
Table 1.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DC INPUT CHARACTERISTICS |  |  |  |  |  |  |
| Input Voltage Range | $\mathrm{V}_{\mathrm{P},} \mathrm{V}_{\mathrm{N}}$ | $\mathrm{V}_{\text {cıl }}=3.3 \mathrm{~V}, \mathrm{~V}_{\text {cco }}=3.3 \mathrm{~V}$ | -0.2 |  | +1.2 | V |
|  |  | $\mathrm{V}_{\text {cla }}=5.2 \mathrm{~V}, \mathrm{~V}_{\text {cco }}=3.3 \mathrm{~V}$ | -0.2 |  | +3.1 | V |
| Input Differential Voltage |  |  | -1.2 |  | +1.2 | V |
| Input Offset Voltage | Vos |  | -5.0 | $\pm 2.0$ | +5.0 | mV |
| Offset Voltage Tempco | $\Delta \mathrm{V}_{\text {os }} / \mathrm{d}_{\mathrm{T}}$ |  |  | 10.0 |  | $\mu \mathrm{V} /{ }^{\circ} \mathrm{C}$ |
| Input Bias Current | $\mathrm{I}_{\mathrm{p}} \mathrm{I}_{\mathrm{N}}$ | Open termination | -50.0 | -25.0 | 0.0 | $\mu \mathrm{A}$ |
| Input Bias Current Tempco |  |  |  | 50.0 |  | $\mathrm{nA} /{ }^{\circ} \mathrm{C}$ |
| Input Offset Current |  |  |  | $\pm 2.0$ |  | $\mu \mathrm{A}$ |
| Input Impedance |  |  |  | 50 |  | $\Omega$ |
| Input Resistance, Differential |  | Open termination |  | 50 |  | $\mathrm{k} \Omega$ |
| Input Resistance, Common-Mode |  | Open termination |  | 500 |  | $\mathrm{k} \Omega$ |
| Active Gain | $A_{v}$ |  |  | 54 |  | dB |
| Common-Mode Rejection | CMRR | $\begin{aligned} & \mathrm{V}_{\mathrm{CCI}}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{CCO}}=3.3 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{CM}}=0.0 \mathrm{~V} \text { to } 1.0 \mathrm{~V} \end{aligned}$ |  | 65 |  | dB |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CCI}}=5.2 \mathrm{~V}, \mathrm{~V}_{\text {CCO }}=3.3 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{CM}}=0.0 \mathrm{~V} \text { to } 3.0 \mathrm{~V} \end{aligned}$ |  | 65 |  | dB |
| Power Supply Rejection-V ${ }_{\text {ccI }}$ | PSRvccı | $\mathrm{V}_{\text {cl }}=3.3 \mathrm{~V} \pm 5 \%, \mathrm{~V}_{\text {cco }}=3.3 \mathrm{~V}$ |  | 74 |  | dB |
| Hysteresis |  | RHYS $=\infty$ |  | $\pm 1$ |  | mV |
| LATCH ENABLE CHARACTERISTICS |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
| Latch Enable Input Range |  |  | 2.8 |  | $\mathrm{V}_{\text {cco }}+0.2$ | V |
| Latch Enable Input Differential |  |  | 0.2 | 0.4 | 0.5 | V |
| Latch Setup Time | ts | $\mathrm{V}_{\text {OD }}=100 \mathrm{mV}$ |  | 15 |  | ps |
| Latch Hold Time | $\mathrm{t}_{\mathrm{H}}$ | $\mathrm{V}_{\text {OD }}=100 \mathrm{mV}$ |  | 5 |  | ps |
| ADCMP573 |  |  |  |  |  |  |
| Latch Enable Input Range |  |  | 1.8 |  | $V_{\text {cco }}-0.6$ | V |
| Latch Enable Input Differential |  |  | 0.2 | 0.4 | 0.5 | V |
| Latch Setup Time | $\mathrm{ts}_{5}$ | $\mathrm{V}_{\text {OD }}=100 \mathrm{mV}$ |  | 90 |  | ps |
| Latch Hold Time | $\mathrm{tH}_{\mathrm{H}}$ | $V_{\text {OD }}=100 \mathrm{mV}$ |  | 100 |  | ps |
| Latch Enable Input Impedance |  |  |  | 50.0 |  | $\Omega$ |
| Latch to Output Delay | tploh, tplol | $\mathrm{V}_{\text {OD }}=100 \mathrm{mV}$ |  | 150 |  | ps |
| Latch Minimum Pulse Width | $\mathrm{t}_{\mathrm{PL}}$ | $\mathrm{V}_{\text {OD }}=100 \mathrm{mV}$ |  | 100 |  | ps |
| DC OUTPUT CHARACTERISTICS |  |  |  |  |  |  |
| ADCMP572 (CML) |  |  |  |  |  |  |
| Output Impedance | Zout | $-8 \mathrm{~mA}<$ lout < 8 mA |  | 50.0 |  | $\Omega$ |
| Output Voltage High Level | $\mathrm{V}_{\text {OH }}$ | $50 \Omega$ terminate to $\mathrm{V}_{\text {cco }}$ | $V_{\text {ço }}-0.10$ | $V_{\text {ço }}-0.05$ | V cco | V |
| Output Voltage Low Level | Vol | $50 \Omega$ terminate to $\mathrm{V}_{\text {cco }}$ | $V_{\text {cco }}-0.60$ | $V_{\text {čo }}-0.45$ | $V_{\text {cco }}-0.30$ | V |
| Output Voltage Differential |  | $50 \Omega$ terminate to $\mathrm{V}_{\text {cco }}$ | 300 | 375 | 450 | mV |
| ADCMP573 (RSPECL) |  |  |  |  |  |  |
| Output Voltage High $-40^{\circ} \mathrm{C}$ | $\mathrm{V}_{\text {OH }}$ | $50 \Omega$ terminate to $\mathrm{V}_{\text {cco }}-2.0$ | $V_{\text {cco }}-1.14$ | $V_{\text {cco }}-1.02$ | $V_{\text {cco }}-0.90$ | V |
| Output Voltage High $+25^{\circ} \mathrm{C}$ | $\mathrm{V}_{\text {OH }}$ | $50 \Omega$ terminate to $\mathrm{V}_{\text {cco }}-2.0$ | $V_{\text {cco }}-1.10$ | $V_{\text {cco }}-0.98$ | $V_{\text {cco }}-0.86$ | V |
| Output Voltage High $+125^{\circ} \mathrm{C}$ | Vor | $50 \Omega$ terminate to $\mathrm{V}_{\text {cco }}-2.0$ | Vссо-1.04 | Vссо -0.92 | V cıo - 0.80 | V |
| Output Voltage Low $-40^{\circ} \mathrm{C}$ | Vol | $50 \Omega$ terminate to $\mathrm{V}_{\text {cco }}-2.0$ | $V_{\text {cıo }}-1.54$ | $\mathrm{V}_{\text {cıo }}-1.39$ | $V_{\text {cco }}-1.24$ | V |
| Output Voltage Low $+25^{\circ} \mathrm{C}$ | Vol | $50 \Omega$ terminate to $\mathrm{V}_{\text {cco }}-2.0$ | $V_{\text {cıo }}-1.50$ | $V_{\text {čo }}-1.35$ | $V_{\text {cco }}-1.20$ | V |
| Output Voltage Low $+125^{\circ} \mathrm{C}$ | Vol | $50 \Omega$ terminate to $\mathrm{V}_{\text {cco }}-2.0$ | V cco - $1.44^{\text {d }}$ | V cıo $^{\text {- }} 1.29$ | V cco- 1.14 | $V$ |
| Output Voltage Differential |  | $50 \Omega$ terminate to $\mathrm{V}_{\text {cco }}-2.0$ | 300 | 375 | 450 | mV |


| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| AC PERFORMANCE |  |  |  |  |  |  |
| Propagation Delay | $t_{\text {PD }}$ | $\mathrm{V}_{\text {CCI }}=3.3 \mathrm{~V}, \mathrm{~V}_{\text {OD }}=200 \mathrm{mV}$ | 150 |  |  | Ps |
|  |  | $\mathrm{V}_{\text {CII }}=3.3 \mathrm{~V}, \mathrm{~V}_{\text {OD }}=20 \mathrm{mV}$ | 165 |  |  | Ps |
|  |  | $\mathrm{V}_{\text {CCI }}=5.2 \mathrm{~V}, \mathrm{~V}_{\text {OD }}=200 \mathrm{mV}$ | 145 |  |  | Ps |
| Propagation Delay Tempco | $\Delta t_{\text {PD }} / \mathrm{d}_{T}$ |  | 0.5 |  |  | $\mathrm{ps} /{ }^{\circ} \mathrm{C}$ |
| Prop Delay Skew—Rising Transition to Falling Transition |  | $\mathrm{V}_{\text {OD }}=200 \mathrm{mV}, 5 \mathrm{~V} / \mathrm{ns}$ | 10 |  |  | Ps |
| Overdrive Dispersion |  | $50 \mathrm{mV}<\mathrm{V}_{\text {OD }}<0.2 \mathrm{~V}, 5 \mathrm{~V} / \mathrm{ns}$ | 15 |  |  | Ps |
|  |  | $10 \mathrm{mV}<\mathrm{V}_{\text {od }}<0.2 \mathrm{~V}, 5 \mathrm{~V} / \mathrm{ns}$ | 15 |  |  | Ps |
| Slew Rate Dispersion |  | $2 \mathrm{~V} / \mathrm{ns}$ to $10 \mathrm{~V} / \mathrm{ns}, 250 \mathrm{mV}$ OD | 15 |  |  | Ps |
| Pulse Width Dispersion |  | 100 ps to $5 \mathrm{~ns}, 250 \mathrm{mV}$ OD | 5 |  |  | Ps |
| 10\% - 90\% Duty Cycle Dispersion |  | $\mathrm{V}_{\text {ccl }}=3.3 \mathrm{~V}, 1 \mathrm{~V} / \mathrm{ns}, 250 \mathrm{mV}$ OD | 5 |  |  | Ps |
|  |  | $\mathrm{V}_{\text {ccl }}=5.2 \mathrm{~V}, 1 \mathrm{~V} / \mathrm{ns}, 250 \mathrm{mV}$ OD | 10 |  |  |  |
| Common-Mode Dispersion |  | $\mathrm{V}_{\text {OD }}=0.2 \mathrm{~V}, 0.0 \mathrm{~V}<\mathrm{V}_{\text {CM }}<2.9 \mathrm{~V}$ | 5 |  |  | ps/V |
| Equivalent Input Bandwidth ${ }^{1}$ | BWEq | 0.0 V to 250 mV input $\mathrm{t}_{\mathrm{R}}=\mathrm{t}_{\mathrm{F}}=17 \mathrm{ps}, 20 / 80$ | 8.0 |  |  | GHz |
| Toggle Rate |  | >50\% Output Swing | 12.5 |  |  | Gbps |
| Deterministic Jitter | DJ | $\begin{aligned} & \text { Vod }=200 \mathrm{mV}, 5 \mathrm{~V} / \mathrm{ns}, \\ & \text { PRBS }^{31}-1 \mathrm{NRZ}, 4 \mathrm{Gbps} \end{aligned}$ | 10 |  |  | Ps |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{OD}}=200 \mathrm{mV}, 5 \mathrm{~V} / \mathrm{ns}, \\ & \mathrm{PRBS}^{31}-1 \mathrm{NRZ}, 10 \mathrm{Gbps} \end{aligned}$ | 20 |  |  | Ps |
| RMS Random Jitter | RJ | Vod $=200 \mathrm{mV}, 5 \mathrm{~V} / \mathrm{ns}, 1.25 \mathrm{GHz}$ | 0.2 |  |  | Ps |
| Minimum Pulse Width | PW ${ }_{\text {MIN }}$ | $\Delta \mathrm{tpD}^{\text {/ }}$ / PW < $5 \mathrm{ps}, 200 \mathrm{mV}$ OD | 100 |  |  | Ps |
|  | PWMIN | $\Delta \mathrm{t}_{\mathrm{pD}} / \mathrm{APW}<10 \mathrm{ps}, 200 \mathrm{mV}$ OD | 80 |  |  | Ps |
| Rise Time | $\mathrm{t}_{\mathrm{R}}$ | 20/80 | 35 |  |  | Ps |
| Fall Time | $\mathrm{t}_{\mathrm{F}}$ | 20/80 | 35 |  |  | Ps |
| POWER SUPPLY |  |  |  |  |  |  |
| Input Supply Voltage Range | $\mathrm{V}_{\text {cl }}$ |  | 3.1 |  | 5.4 | V |
| Output Supply Voltage Range | Vcco |  | 3.1 |  | 5.4 | V |
| Positive Supply Differential | $V_{c \mathrm{cl}}-\mathrm{V}_{\mathrm{cco}}$ |  | -0.2 |  | +2.3 | V |
| ADCMP572 (CML) |  |  |  |  |  |  |
| Positive Supply Current | Ivccı + Ivcco | $\begin{aligned} & \mathrm{V}_{\mathrm{cc}}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{cco}}=3.3 \mathrm{~V}, \\ & \text { terminate } 50 \Omega \text { to } \mathrm{V}_{\text {cco }} \end{aligned}$ |  | 44 | 52 | mA |
|  |  | $\mathrm{V}_{\mathrm{CCI}}=5.2 \mathrm{~V}, \mathrm{~V}_{\mathrm{cco}}=5.2 \mathrm{~V},$ $\text { terminate } 50 \Omega \text { to } V_{\text {cco }}$ |  | 44 | 52 |  |
| Device Power Dissipation | PD | $\mathrm{V}_{\mathrm{CCI}}=3.3 \mathrm{~V}, \mathrm{~V}_{\mathrm{cco}}=3.3 \mathrm{~V},$ $\text { terminate } 50 \Omega \text { to } \mathrm{V}_{\text {cco }}$ |  | 140 | 165 | mW |
|  |  | $\mathrm{V}_{\mathrm{ccI}}=5.2 \mathrm{~V}, \mathrm{~V}_{\mathrm{cco}}=5.2 \mathrm{~V},$ $\text { terminate } 50 \Omega \text { to } V_{\text {cco }}$ |  | 230 | 265 |  |
| ADCMP573 (RSPECL) |  |  |  |  |  |  |
| Positive Supply Current | Ivccı + Ivcco | $\begin{aligned} & V_{\text {cll }}=3.3 \mathrm{~V}, \mathrm{~V}_{\text {coo }}=3.3 \mathrm{~V}, \\ & 50 \Omega \text { to } \mathrm{V}_{\text {cco }}-2 \mathrm{~V} \end{aligned}$ |  | 62 | 80 | mA |
|  |  | $\begin{aligned} & V_{\text {cII }}=5.2 \mathrm{~V}, \mathrm{~V}_{\text {coo }}=5.2 \mathrm{~V}, \\ & 50 \Omega \text { to } \mathrm{V}_{\text {cco }}-2 \mathrm{~V} \end{aligned}$ |  | 64 | 80 |  |
| Device Power Dissipation | PD | $\begin{aligned} & V_{\text {cll }}=3.3 \mathrm{~V}, \mathrm{~V}_{\text {cco }}=3.3 \mathrm{~V} \text {, } \\ & 50 \Omega \text { to } \mathrm{V}_{\text {cco }}-2 \mathrm{~V} \end{aligned}$ |  | 110 | 160 | mW |
|  |  | $\begin{aligned} & V_{c \mathrm{cI}}=5.2 \mathrm{~V}, \mathrm{~V}_{\text {cco }}=5.2 \mathrm{~V}, \\ & 50 \Omega \text { to } \mathrm{V}_{\text {cco }}-2 \mathrm{~V} \end{aligned}$ |  | 146 | 230 |  |

[^0]
## ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
| :---: | :---: |
| SUPPLY VOLTAGE |  |
| Input Supply Voltage (Vcı to GND) | -0.5 V to +6.0 V |
| Output Supply Voltage (Vcco to GND) | -0.5 V to +6.0 V |
| Positive Supply Differential $\left(\mathrm{V}_{\mathrm{ccI}}-\mathrm{V}_{\mathrm{cco}}\right)$ | -0.5 V to +3.5 V |
| INPUTVOLTAGE |  |
| Input Voltage | -0.5 V to $\mathrm{V}_{\text {ccl }}+0.5 \mathrm{~V}$ |
| Differential Input Voltage | $\pm\left(\mathrm{V}_{\text {cll }}+0.5 \mathrm{~V}\right)$ |
| Input Voltage, Latch Enable | -0.5 V to V cco +0.5 V |
| HYSTERESIS CONTROL PIN |  |
| Applied Voltage (HYS to GND) | -0.5 V to +1.5 V |
| Maximum Input/Output Current | $\pm 1 \mathrm{~mA}$ |
| OUTPUT CURRENT |  |
| ADCMP572 (CML) | $\pm 20 \mathrm{~mA}$ |
| ADCMP573 (RSPECL) | -35 mA |
| TEMPERATURE |  |
| Operating Temperature, Ambient | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Operating Temperature, Junction | $+150^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL CONSIDERATIONS

The ADCMP572/ADCMP573 LFCSP 16-lead package has a $\theta_{\mathrm{JA}}$ (junction-to-ambient thermal resistance) of $70^{\circ} \mathrm{C} / \mathrm{W}$ in still air.

## ESD CAUTION

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. LEAVE EPAD FLOATING UNLESS IMPROVED THERMAL OR MECHANICAL STABILITY IS DESIRED, IN WHICH CASE SOLDER IT TO THE APPLICATION BOARD.

Figure 2. ADCMP572/ADCMP573 Pin Configuration
Table 3. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
| :---: | :---: | :---: |
| 1 | $V_{\text {TP }}$ | Termination Resistor Return Pin for $\mathrm{V}_{\mathrm{P}}$ Input. |
| 2 | $V_{P}$ | Noninverting Analog Input. |
| 3 | $V_{N}$ | Inverting Analog Input. |
| 4 | $V_{\text {TN }}$ | Termination Resistor Return Pin for $\mathrm{V}_{\mathrm{N}}$ Input. |
| 5,16 | V ${ }_{\text {cI }}$ | Positive Supply Voltage for Input Stage. |
| 6 | $\overline{\mathrm{LE}}$ | Latch Enable Input Pin, Inverting Side. <br> In compare mode ( $\overline{\mathrm{LE}}=$ low), the output tracks changes at the input of the comparator. <br> In latch mode ( $\overline{\mathrm{LE}}=$ high $)$, the output reflects the input state just prior to the comparator's being placed into latch mode. $\overline{L E}$ must be driven in complement with LE. |
| 7 | LE | Latch Enable Input Pin, Noninverting Side. <br> In compare mode (LE = high), the output tracks changes at the input of the comparator. <br> In latch mode (LE = low), the output reflects the input state just prior to the comparator's being placed into latch mode. LE must be driven in complement with $\overline{\mathrm{LE}}$. |
| 8 | $\mathrm{V}_{\text {ccoo }} / \mathrm{V}_{\text {TT }}$ | Termination Return Pin for the LE/LE Input Pins. <br> For the ADCMP572 (CML output stage), this pin is internally connected to and also should be externally connected to the positive Vcco supply. <br> For the ADCMP573 (RSPECL output stage), this pin should normally be connected to the $\mathrm{V}_{\text {cco }}-2 \mathrm{~V}$ termination potential. |
| 9,12 | Vcco | Positive Supply Voltage for the CML/RSPECL Output Stage. |
| 13, 15 | GND | Ground. |
| 10 | $\overline{\mathrm{Q}}$ | Inverting Output. $\overline{\mathrm{Q}}$ is at logic low if the analog voltage at the noninverting input, $\mathrm{V}_{\mathrm{P}}$, is greater than the analog voltage at the inverting input, $\mathrm{V}_{\mathrm{N}}$, provided the comparator is in compare mode. See the $\mathrm{LE} / \overline{\mathrm{LE}}$ descriptions (Pins 6 and 7) for more information. |
| 11 | Q | Noninverting Output. Q is at logic high if the analog voltage at the noninverting input $\mathrm{V}_{\mathrm{P}}$ is greater than the analog voltage at the inverting input, $\mathrm{V}_{\mathrm{N}}$, provided the comparator is in compare mode. <br> See the LE/LE descriptions (Pins 6 and 7) for more information. |
| 14 | HYS | Hysteresis Control Pin. Leave this pin disconnected for zero hysteresis. Connect to GND with a suitably sized resistor to add the desired amount of hysteresis. Refer to Figure 7 for proper sizing of RHrs hysteresis control resistor. |
|  | Isolated Heat Sink | The metallic back surface of the package is not electrically connected to any part of the circuit, and it can be left floating for best electrical isolation between the package handle and the substrate of the die. However, it can be soldered to the application board if improved thermal and/or mechanical stability is desired. Exposed metal at package corners is connected to the heat sink paddle. |
|  | EPAD | Exposed Pad. Leave EPAD floating unless improved thermal or mechanical stability is desired, in which case solder it to the application board. |

## TYPICAL PERFORMANCE CHARACTERISTICS

$\mathrm{V}_{\mathrm{CCI}}=\mathrm{V}_{\mathrm{CCO}}=3.3 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.


Figure 3. Propagation Delay vs. Input Overdrive


Figure 4. Propagation Delay vs. Input Common-Mode


Figure 5. Propagation Delay vs. Temperature


Figure 6. Rise/Fall Time vs. Temperature


Figure 7. Hysteresis vs. RHYS Control Resistor


Figure 8. Hysteresis vs. RHYS Sink Current


Figure 9. Input Bias Current vs. Input Differential


Figure 10. Input Bias Current vs. Temperature


Figure 11. Input Offset Voltage vs. Temperature


Figure 12. Output Levels vs. Temperature


Figure 13. ADCMP572 Eye Diagram at 2.5 Gbps


Figure 14. ADCMP572 Eye Diagram at 6.5 Gbps

## APPLICATIONS INFORMATION

## POWER/GROUND LAYOUT AND BYPASSING

The ADCMP572/ADCMP573 comparators are very high speed SiGe devices. Consequently, it is essential to use proper high speed design techniques to achieve the specified performance. Of critical importance is the use of low impedance supply planes, particularly the output supply plane ( $\mathrm{V}_{\mathrm{CCO}}$ ) and the ground plane (GND). Individual supply planes are recommended as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

It is important to adequately bypass the input and output supplies. A $1 \mu \mathrm{~F}$ electrolytic bypass capacitor should be placed within several inches of each power supply pin to ground. In addition, multiple high quality $0.01 \mu \mathrm{~F}$ bypass capacitors should be placed as close as possible to each of the $V_{C C I}$ and $V_{C c o}$ supply pins and should be connected to the GND plane with redundant vias. High frequency bypass capacitors should be carefully selected for minimum inductance and ESR. Parasitic layout inductance should be avoided to maximize the effectiveness of the bypass at high frequencies.
If the input and output supplies are connected separately such that $\mathrm{V}_{\mathrm{CCI}} \neq \mathrm{V}_{\mathrm{cco}}$, care should be taken to bypass each of these supplies separately to the GND plane. A bypass capacitor should not be connected between them. It is recommended that the GND plane separate the $V_{C C I}$ and $V_{C C O}$ planes when the circuit board layout is designed to minimize coupling between the two supplies and to take advantage of the additional bypass capacitance from each respective supply to the ground plane. This enhances the performance when split input/output supplies are used. If the input and output supplies are connected together for single-supply operation such that $\mathrm{V}_{\mathrm{CCI}}=\mathrm{V}_{\text {cco }}$, coupling between the two supplies is unavoidable; however, every effort should be made to keep the supply plane adjacent to the GND plane to maximize the additional bypass capacitance this arrangement provides.

## CML/RSPECL OUTPUT STAGE

Specified propagation delay dispersion performance can be achieved only by using proper transmission line terminations. The outputs of the ADCMP572 are designed to directly drive 400 mV into $50 \Omega$ cable, microstrip, or strip line transmission lines properly terminated to the $\mathrm{V}_{\text {cco }}$ supply plane. The CML output stage is shown in the simplified schematic diagram of Figure 15. The outputs are each back terminated with $50 \Omega$ for best transmission line matching. The RSPECL outputs of the ADCMP573 are illustrated in Figure 16 and should be terminated to $\mathrm{V}_{\mathrm{Cco}}-2 \mathrm{~V}$. As an alternative, Thevenin equivalent termination networks can be used in either case if the direct termination voltage is not readily available. If high speed output signals must be routed more than a centimeter, microstrip or strip line techniques are essential to ensure proper transition times and to
prevent output ringing and pulse width dependent propagation delay dispersion. For the most timing critical applications where transmission line reflections pose the greatest risk to performance, the ADCMP572 provides the best match to $50 \Omega$ output transmission paths.


Figure 15. Simplified Schematic Diagram of the ADCMP572 CML Output Stage


Figure 16. Simplified Schematic Diagram of the ADCMP573 RSPECL Output Stage

## USING/DISABLING THE LATCH FEATURE

The latch inputs ( $\mathrm{LE} / \overline{\mathrm{LE}}$ ) are active low for latch mode and are internally terminated with $50 \Omega$ resistors to Pin 8 . This pin corresponds to and is internally connected to the Vcco supply for the CML-compatible ADCMP572. With the aid of these resistors, the ADCMP572 latch function can be disabled by connecting the $\overline{\mathrm{LE}}$ pin to GND with an external pull-down resistor and leaving the LE pin unconnected. To avoid excessive power dissipation, the resistor should be $750 \Omega$ when $\mathrm{V}_{\mathrm{CCO}}=$ 3.3 V , and $1.2 \mathrm{k} \Omega$ when $\mathrm{V}_{\mathrm{CCO}}=5.2 \mathrm{~V}$. In the PECL-compatible ADCMP573, the $\mathrm{V}_{\text {TT }}$ pin should be connected externally to the PECL termination supply at $\mathrm{V}_{\mathrm{CCO}}-2 \mathrm{~V}$. The latch can then be disabled by connecting the LE pin to $\mathrm{V}_{\text {cco }}$ with an external $500 \Omega$ resistor and leaving the $\overline{\mathrm{LE}}$ pin disconnected. In this case, the resistor value does not depend on the $\mathrm{V}_{\text {cco }}$ supply voltage.
$\mathrm{V}_{\text {cco }}$ is the signal return for the output stage and $\mathrm{V}_{\text {cco }}$ pins should of course be connected to a supply plane for maximum performance.

## OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed comparator, proper design and layout techniques are essential to obtaining the specified performance. Stray capacitance, inductance, inductive power and ground impedances, or other layout issues can severely limit performance and often cause oscillation. Discontinuities along input and output transmission lines can severely limit the specified pulse width dispersion performance.
For applications working in a $50 \Omega$ environment, input and output matching has a significant impact on data dependent (or deterministic) jitter (DJ) and on pulse width dispersion performance. The ADCMP572/ADCMP573 comparators provide internal $50 \Omega$ termination resistors for both the $V_{P}$ and $\mathrm{V}_{\mathrm{N}}$ inputs, and the ADCMP572 provides $50 \Omega$ back terminated outputs. The return side for each input termination is pinned out separately with the $\mathrm{V}_{\mathrm{TP}}$ and $\mathrm{V}_{\mathrm{TN}}$ pins, respectively. If a $50 \Omega$ termination is desired at one or both of the $\mathrm{V}_{\mathrm{P}} / \mathrm{V}_{\mathrm{N}}$ inputs, then the $V_{T P}$ and $V_{\text {TN }}$ pins can be connected (or disconnected) to (from) the desired termination potential as required. The termination potential should be carefully bypassed using high quality bypass capacitors as discussed earlier to prevent undesired aberrations on the input signal due to parasitic inductance in the circuit board layout. If a $50 \Omega$ input termination is not desired, either one or both of the $\mathrm{V}_{\mathrm{TP}} / \mathrm{V}_{\mathrm{TN}}$ termination pins can be left disconnected. In this case, the pins should be left floating with no external pull-downs or bypassing capacitors.

When leaving an input termination disconnected, the internal resistor acts as a small stub on the input transmission path and can cause problems for very high speed inputs. Reflections should then be expected from the comparator inputs because they no longer provide matched impedance to the input path leading to the device. In this case, it is important to back match the drive source impedance to the input transmission path to minimize multiple reflections. For applications in which the comparator is very close to the driving signal source, the source impedance should be minimized. High source impedance in combination with parasitic input capacitance of the comparator might cause an undesirable degradation in bandwidth at the input, therefore degrading the overall response. Although the ADCMP572/ADCMP573 comparators have been designed to minimize input capacitance, some parasitic capacitance is inevitable. It is therefore recommended that the drive source impedance be no more than $50 \Omega$ for best high speed performance.

## COMPARATOR PROPAGATION DELAY DISPERSION

The ADCMP572/ADCMP573 comparators are designed to reduce propagation delay dispersion over a wide input overdrive range of 5 mV to 500 mV . Propagation delay dispersion is variation in the propagation delay that results from a change in the degree of overdrive or slew rate (how far or how fast the input signal exceeds the switching threshold).

Propagation delay dispersion is a specification that becomes important in high speed, time-critical applications such as data communication, automatic test and measurement, instrumentation, and event driven applications such as pulse spectroscopy, nuclear instrumentation, and medical imaging. Dispersion is defined as the variation in propagation delay as the input overdrive conditions vary (Figure 17 and Figure 18). For the ADCMP572/ADCMP573, dispersion is typically $<15 \mathrm{ps}$ because the overdrive varies from 10 mV to 500 mV , and the input slew rate varies from $2 \mathrm{~V} / \mathrm{ns}$ to $10 \mathrm{~V} / \mathrm{ns}$. This specification applies for both positive and negative signals since the ADCMP572/ADCMP573 has substantially equal delays for either positive going or negative going inputs.


Figure 17. Propagation Delay—Overdrive Dispersion


Figure 18. Propagation Delay—Slew Rate Dispersion

## COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often desirable in a noisy environment or when the differential input amplitudes are relatively small or slow moving, but excessive hysteresis has a cost in degraded accuracy and slew-induced timing shifts. The transfer function for a comparator with hysteresis is shown in Figure 19. If the input voltage approaches the threshold ( 0.0 V in this example) from the negative direction, the comparator switches from low to high when the input crosses $+\mathrm{V}_{\mathrm{H}} / 2$. The new switching threshold becomes $-\mathrm{V}_{\mathrm{H}} / 2$. The comparator remains in the high state until the threshold $-\mathrm{V}_{\mathrm{H}} / 2$ is crossed from the positive direction. In this manner, noise centered on 0.0 V input does not cause the comparator to switch states unless it exceeds the region bounded by $\pm \mathrm{V}_{\mathrm{H}} / 2$.


Figure 19. Comparator Hysteresis Transfer Function
The customary technique for introducing hysteresis into a comparator uses positive feedback from the output back to the input. A limitation of this approach is that the amount of hysteresis varies with the output logic levels, resulting in hysteresis that can be load dependent and is not symmetrical about the threshold. The external feedback network can also introduce significant parasitics, which reduce high speed performance and can even induce oscillation in some cases.
The ADCMP572/ADCMP573 comparators offer a programmable hysteresis feature that can significantly improve the accuracy and stability of the desired hysteresis. By connecting an external pull-down resistor from the HYS pin to GND, a variable amount of hysteresis can be applied. Leaving the HYS pin disconnected disables the feature, and hysteresis is then less than 1 mV as specified. The maximum hysteresis that can be applied using this method is approximately $\pm 25 \mathrm{mV}$ with the
pin grounded. Figure 20 illustrates the amount of hysteresis applied as a function of external resistor value. The advantages of applying hysteresis in this manner are improved accuracy, stability, and reduced component count. An external bypass capacitor is not recommended on the HYS pin because it would likely degrade the jitter performance of the device. The hysteresis pin could also be driven by a CMOS DAC. It is biased to approximately 250 mV and has an internal series resistance of $600 \Omega$.


Figure 20. Hysteresis vs. RHYS Control Resistor

## MINIMUM INPUT SLEW RATE REQUIREMENTS

As with all high speed comparators, a minimum slew rate requirement must be met to ensure that the device does not oscillate as the input signal crosses the threshold. This oscillation is due in part to the high input bandwidth of the comparator and the feedback parasitics inherent in the package. A minimum slew rate of $50 \mathrm{~V} / \mu \mathrm{s}$ should ensure clean output transitions from the ADCMP572/ADCMP573 comparators.
The slew rate may be too slow for other reasons. The extremely high bandwidth of these devices means that broadband noise can be a significant factor when input slew rates are low. There will be at least $120 \mu \mathrm{~V}$ of thermal noise generated over the full comparator bandwidth by two $50 \Omega$ terminations at room temperature. With a slew rate of only $50 \mathrm{~V} / \mu \mathrm{s}$ the input will be inside this noise band for over 2 ps , rendering the comparator's jitter performance of 200 fs moot. Raising the slew rate of the input signal and/or reducing the bandwidth over which this resistance is seen at the input can greatly reduce jitter.

## ADCMP572/ADCMP573

## TYPICAL APPLICATION CIRCUITS



Figure 21. Zero-Crossing Detector with 3.3 V CML Outputs


Figure 22. LVDS to $50 \Omega$ Back Terminated RSPECL Receiver


Figure 23. Comparator with $\pm 1$ V Input Range and 3.3 V CML Outputs


Figure 24. Comparator with 0 V to 3 V Input Range and 3.3 V or 5.2 V Positive CML Outputs


Figure 25. Interfacing 3.3 VCML to a $50 \Omega$ Ground Terminated Instrument


Figure 26. Disabling the ADCMP572 Latch Feature


Figure 27. Disabling the ADCMP573 Latch Feature


Figure 28. Adding Hysteresis Using the HYS Control Pin

## TIMING INFORMATION

Figure 29 illustrates the ADCMP572/ADCMP573 compare and latch timing relationships. Table 4 provides definitions of the terms shown in the figure.


Figure 29. System Timing Diagram

Table 4. Timing Descriptions

| Symbol | Timing | Description |
| :---: | :---: | :---: |
| $t_{\text {PDH }}$ | Input to output high delay | Propagation delay measured from the time the input signal crosses the reference ( $\pm$ the input offset voltage) to the $50 \%$ point of an output low-to-high transition. |
| tpdL | Input to output low delay | Propagation delay measured from the time the input signal crosses the reference ( $\pm$ the input offset voltage) to the $50 \%$ point of an output high-to-low transition. |
| tpLOH | Latch enable to output high delay | Propagation delay measured from the $50 \%$ point of the latch enable signal low-to-high transition to the $50 \%$ point of an output low-to-high transition. |
| tplol | Latch enable to output low delay | Propagation delay measured from the $50 \%$ point of the latch enable signal low-to-high transition to the $50 \%$ point of an output high-to-low transition. |
| $\mathrm{tH}_{\mathrm{H}}$ | Minimum hold time | Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs. |
| $t_{\text {PL }}$ | Minimum latch enable pulse width | Minimum time that the latch enable signal must be high to acquire an input signal change. |
| ts | Minimum setup time | Minimum time before the negative transition of the latch enable signal that an input signal change must be present to be acquired and held at the outputs. |
| $\mathrm{t}_{\mathrm{R}}$ | Output rise time | Amount of time required to transition from a low to a high output as measured at the $20 \%$ and $80 \%$ points. |
| $\mathrm{t}_{\mathrm{F}}$ | Output fall time | Amount of time required to transition from a high to a low output as measured at the $20 \%$ and $80 \%$ points. |
| Vod | Voltage overdrive | Difference between the input voltages $\mathrm{V}_{\mathrm{A}}$ and $\mathrm{V}_{\mathrm{B}}$. |

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED.
$\stackrel{\widetilde{\alpha}}{\stackrel{\omega}{\omega}}$
Figure 30. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
$3 \mathrm{~mm} \times 3 \mathrm{~mm}$ Body, Very Very Thin Quad
(CP-16-21)
Dimensions shown in millimeters

## ORDERING GUIDE

| Model $^{1}$ | Temperature Range | Package Description | Package Option | Branding |
| :--- | :--- | :--- | :--- | :--- |
| ADCMP572BCPZ-WP | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-21 | G0Y |
| ADCMP572BCPZ-R2 | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-21 | G0Y |
| ADCMP572BCPZ-RL7 | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-21 | G0Y |
| EVAL-ADCMP572BCPZ |  | Evaluation Board |  |  |
| ADCMP573BCPZ-WP | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-21 | G0Z |
| ADCMP573BCPZ-R2 | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-21 | G0Z |
| ADCMP573BCPZ-RL7 | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-16-21 | G0Z |
| EVAL-ADCMP573BCPZ |  | Evaluation Board |  |  |

${ }^{1} Z=$ RoHS Compliant Part


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[^0]:    ${ }^{1}$ Equivalent input bandwidth assumes a simple first-order response and is calculated with the following formula: $B W_{E Q}=0.22 / \sqrt{ }\left(\operatorname{tr}_{C o m P}{ }^{2}-\operatorname{triN}^{2}\right)$, where $\operatorname{tr}_{1 N}$ is the $20 / 80$ transition time of a quasi-Gaussian signal applied to the comparator input, and trcomp is the effective transition time digitized by the comparator.

