PN5180

High-power NFC frontend solution

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Preliminary data sheet
COMPANY PUBLIC

1. Introduction

This document describes the functionality and electrical specification of the high-power NFC IC PN5180.

Additional documents for functional chip in description and design support are available from NXP, this information is not part of this document.

2. General description

PN5180, the best full NFC frontend of the market.

As a highly integrated high-power output NFC frontend IC for contactless communication at 13.56 MHz, this frontend IC utilizes an outstanding modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols.

The PN5180 ensures maximum interoperability for next generation of NFC enabled mobile phones. The PN5180 is optimized for point of sales terminal applications and implements a high-power NFC frontend functionality which allows to achieve EMV compliance on RF level without additional external active components.

The PN5180 frontend IC supports the following operating modes:

- Reader/Writer mode supporting ISO/IEC 14443-A up to 848 kBit/s, MIFARE
- Reader/Writer mode supporting ISO/IEC 14443-B up to 848 kBit/s
- Reader/Writer mode supporting JIS X 6319-4 (comparable with FeliCa scheme)
- Read/write mode supporting ISO/IEC 15693
- Read/write mode supporting ISO/IEC 18000-3 Mode 3
- ISO/IEC18092 (NFC-IP1)
- ISO/IEC21481 (NFC-IP-2)
- NFC-FORUM
- ISO14443-type A Card emulation up to 848 kBit/s

Enabled in Reader/Writer mode for ISO/IEC 14443-A, MIFARE the PN5180's internal transmitter part is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443A, MIFARE cards and transponders without additional active circuitry. The receiver part provides a robust and efficient implementation of a demodulation and decoding circuitry for signals from ISO/IEC 14443-A, MIFARE compatible cards and transponders. The digital part handles the complete ISO/IEC 14443-A, MIFARE framing and error detection (Parity and CRC).

The PN5180 supports all layers of the ISO/IEC 14443-B reader/writer communication scheme, given correct implementation of additional components, like oscillator, power supply, coil etc. and provided that standardized protocols, e.g. like ISO/IEC 14443-4 and/or ISO/IEC 14443-B anticollision are correctly implemented by a host microcontroller.

Enabled in Reader/Writer mode for JIS X 6319-4, the PN5180 NFC frontend IC supports the FeliCa communication scheme. The receiver part provides a robust and efficient implementation of the demodulation and decoding circuitry for JIS X 6319-4 coded signals. The digital part handles the FeliCa framing and error detection like CRC. The PN5180 supports JIS X 6319-4 contactless reader/writer communication using higher transfer speeds up to 424 kbit/s in both directions.

The PN5180 supports the vicinity protocol according to ISO/IEC 15693 and ISO/IEC 18000-3 mode 3.

The PN5180 frontend IC supports the ISO/IEC18092 modes reader, P2P (NFC-IP1 and NFC-IP2) and type A card emulation.

In Card Operation mode, the PN5180 frontend IC is able to answer to a reader/writer command according to the ISO/IEC 14443A/MIFARE card interface scheme. The Card Operation Mode allows the PN5180 to act like an NFC Forum tag if this functionality is supported by the host firmware.

One SPI-based host controller interface is implemented:

- Serial Peripheral Interface (SPI) with data rates up to 7 Mbit/s with MOSI, MISO, NSS and SCK signals
- Interrupt request line to inform host controller on events
- EEPROM configurable pull-up resistor on SPI MISO line
- Busy line to indicate to host availability of data for reading

3. Features and benefits

- Transmitter current up to 250 mA
- Dynamic Power Control controls antenna current, RF power, and the related waveforms to deliver optimized RF performance even under detuned conditions. It maximizes transmitter current during detuned conditions and thereby compensates for any negative effects generated by nearby metal, cards, or phones. The DPC ensures robust communication with smartcards and smartphones, without using any additional external components.
- Includes NXP ISO/IEC14443-A, Innovatron ISO/IEC14443-B and NXP MIFARE Crypto 1 intellectual property licensing rights
- Full compliance with all standards relevant to NFC, contactless operation and EMVCo
- Automatic EMD handling for faster design of payment terminals
- Onboard Dynamic Power Control (DPC) for optimized RF performance, even under detuned conditions
- Low-power card detection minimizes current consumption during polling
- Active load modulation supports smaller antenna with Card Emulation Mode
- Small, industry-standard packages
- NFC Cockpit GUI: software-independent register settings

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- Development kit with 32-bit NXP LPC1769 MCU and antenna
- NFC Reader Library with source code ready for EMVCo L1 and NFC Forum compliance

4. Applications

- Payment terminals
- Physical-access readers
- eGov readers
- Industrial readers
- High-performance readers

The NXP PN5180 NFC frontend, equipped with unique features that improve performance, save energy, and maximize efficiency, enables best-in-class readers that conform to the requirements for EMVCo and NFC Forum specifications, for the broadest possible interoperability.

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5. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(VBAT)}$	VBAT supply voltage	-	2.7	3.3	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage	1.8 V supply	1.65	1.8	1.95	V
		3.3 V supply	2.7	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage	-	2.7	5.0	5.5	V
I_{pd}	power-down current	VDD(TVDD) = VDD(PVDD) =VDD(VDD) 3.0 V; hard power-down; pin NRSTPD set LOW, T_{amb} = 25 °C	-	10	-	µA
I_{stb}	standby current	T_{amb} = 25 °C	-	15	-	µA
$I_{DD(TVDD)}$	TVDD supply current	-	-	180	250	mA
T_{amb}	ambient temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB	–30	+25	+85	°C
T_{stg}	storage temperature	no supply voltage applied	–55	+25	+150	°C

6. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
PN5180A0HN/C1, 551	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals + 1 central ground; body 6 x 6 x 1.0 mm; delivered in one tray, bakable, MSL=3.	SOT618-1
PN5180A0HN/C1, 518	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals + 1 central ground; body 6 x 6 x 1.0 mm; delivered on reel MSL = 3.	SOT618-1
PN5180A0ET/C1, 151	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls, delivered in one tray, MSL = 1.	SOT1336-1
PN5180A0ET/C1, 118	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls, delivered on reel, MSL = 1.	SOT1336-1

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7. Marking

Table 3. Marking codes HVQFN40

Type number	Marking code
PN5180 (first Engineering prototypes)	
Line A: These devices are intended for prototype development only,	PN51800 or PN5180A
Line B1:	“01 ... 01” or 6 characters: Diffusion Batch ID and assembly sequence ID
Line B2:	“FW 1.1” or”Z.1 01”
Line C: Engineering prototypes are marked “Product life cycle status code Before CQS”: X	8 characters: diffusion and assembly location, date code, product version (indicated by mask version), product life cycle status. This line includes the following elements at 8 positions: 1. Diffusion center code 2. Assembly center code 3. RHF-2006 indicator 4. Year code (Y) 1) 5. Week code (W) 2) 6. Week code (W) 2) 7. Mask layout version 8. (Product life cycle status code Before CQS) X
PN5180 (devices are customer qualification samples)	
Line A:	PN5180A
Line B1:	6 characters: Diffusion Batch ID and assembly sequence ID
Line B2:	blank
Line C: Customer qualification samples are marked as CQS: Y	8 characters: diffusion and assembly location, date code, product version (indicated by mask version), product life cycle status. This line includes the following elements at 8 positions: 1. Diffusion center code 2. Assembly center code 3. RHF-2006 indicator 4. Year code (Y) 1) 5. Week code (W) 2) 6. Week code (W) 2) 7. Mask layout version 8. (Product life cycle status code CQS): Y
PN5180A0HN This products are released for sale (volume production)	

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Table 3. Marking codes *...continued* **HVQFN40**

Type number	Marking code
Line A:	PN5180A
Line B:	6 characters: Diffusion Batch ID and assembly sequence ID
Line C: Release for sale products do not show any X or Y, instead position 8 is left blank	8 characters: diffusion and assembly location, date code, product version (indicated by mask version), product life cycle status. This line includes the following elements at 8 positions: 1. Diffusion center code 2. Assembly center code 3. RHF-2006 indicator 4. Year code (Y) 1) 5. Week code (W) 2) 6. Week code (W) 2) 7. Mask layout version 8. (Product life cycle status release for sale): blank

Please note that the Firmware of the product PN5180 can be updated. Please verify the Firmware version of the device in addition to the package marking to identify the implemented functionality of a device.

7.1 Package marking drawing

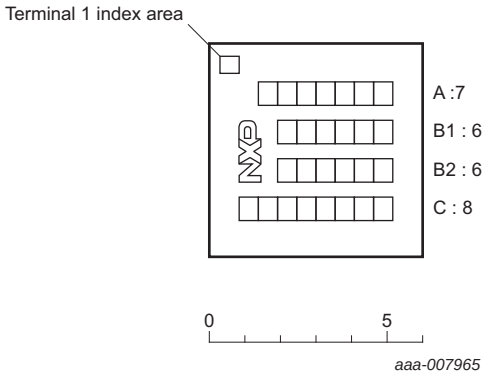

Fig 1. Marking PN5180 in HVQFN40

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8. Block diagram

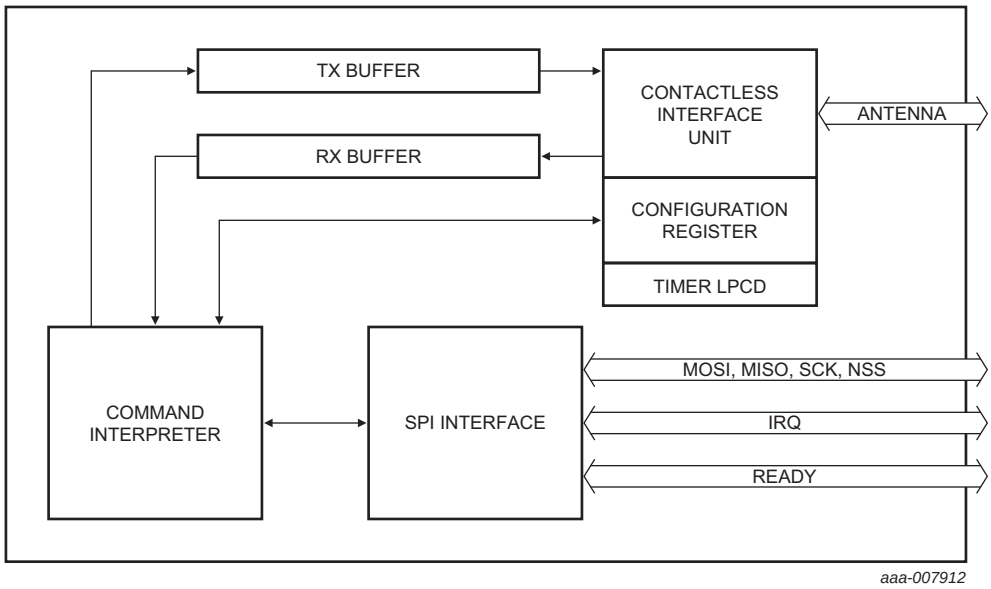

Fig 2. Block diagram

9. Pinning information

9.1 Pin description

Table 4. Pin description HVQFN40

Symbol	Pin	Type	Description
NSS	1	I	SPI NSS
AUX2 /DWL_REQ	2	I/O	Analog test bus or Download request
MOSI	3	I	SPI MOSI
PVSS	4	supply	Pad ground
MISO	5	O	SPI MISO
PVDD	6	supply	Pad supply voltage
SCK	7	I	SPI Clock
BUSY	8	O	Busy signal
VSS	9	supply	Ground
RESET_N	10	I	RESET, Low active
n.c.	11	-	leave unconnected, do not ground
VBAT	12	supply	Supply Connection, all VBAT mandatory to be connected
VBAT	13	supply	Supply Connection, all VBAT mandatory to be connected
n.c.	14	-	leave unconnected, do not ground
RXN	15	I	Receiver Input
RXP	16	I	Receiver Input

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Table 4. Pin description HVQFN40 *…continued*

Symbol	Pin	Type	Description
VMID	17	supply	Stabilizing capacitor connection output
TX2	18	O	Antenna driver output 2
TVSS	19	supply	Antenna driver ground
n.c.	20	-	leave unconnected, do not ground
TX1	21	O	Antenna driver output 1
TVDD	22	supply	Antenna driver supply
ANT1	23	O	Antenna connection 1 for load modulation in card emulation mode (only in case of PLM)
ANT2	24	O	Antenna connection 2 for load modulation in card emulation mode (only in case of PLM)
VDHF	25	supply	Stabilizing capacitor connection output
VBAT	26	supply	Supply Connection, all VBAT mandatory to be connected
VSS	27	supply	Ground
AVDD	28	supply	Analog VDD supply voltage input (1.8 V), connected to VDD
VDD	29	supply	VDD output (1.8 V)
DVDD	30	supply	Digital supply voltage input (1.8 V), connected to VDD
n.c.	31	-	leave unconnected, do not ground
n.c.	32	-	leave unconnected, do not ground
n.c.	33	-	leave unconnected, do not ground
n.c.	34	-	leave unconnected, do not ground
n.c.	35	-	leave unconnected, do not ground
CLK1	36	I	Clock input for crystal. This pin is also used as input for an external generated accurate clock (8 MHz, 12 MHz, 16 MHz, 24 MHz, other clock frequencies not supported)
CLK2	37	O	Clock output (amplifier inverted signal output) for crystal
GPO1	38	O	(double function pin) GPO1, Digital output 1
IRQ	39	O	Interrupt request output, active level configurable
AUX1	40	O	Analog/Digital Test signal

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10. Functional description

10.1 Introduction

The PN5180 is a High-Power NFC frontend. It implements the RF functionality like an antenna driving and receiver circuitry and all the low-level functionality to realize an NFC Forum-compliant reader. The PN5180 needs to be connected to a host microcontroller by means of a SPI interface for configuration, NFC data exchange and high-level NFC protocol implementation.

The PN5180 allows different supply voltages for NFC drivers, internal supply and host interface providing a maximum of flexibility.

The chip supply voltage and the NFC driver voltage can be chosen independently from each other.

The PN5180 makes use of an external 27.12 MHz crystal as clock source for generating the RF field and its internal digital logic. In addition, an internal PLL allows to use an accurate external clock source of either 8, 12, 16, 24 MHz. This allows to save the 27.12 MHz crystal in systems which implement one of the mentioned clock frequencies (e.g. for USB or system clock).

Two types of memory are implemented in the PN5180: RAM and EEPROM.

Internal registers of the PN5180 state machine store configuration data. The internal registers are reset to initial values in case of PowerON, and Hardware RESET and standby.

The RF configuration for dedicated RF protocols is defined by EEPROM data which is copied by a command issued from the host microcontroller - LOAD_RF_CONFIG- into the registers of the PN5180. The PN5180 is initialized with EEPROM data for the LOAD_RF_CONFIG command which has been tested to work well for one typical antenna. For customer-specific antenna sizes and dedicated antenna environment conditions like metal or ferrite, the pre-defined EEPROM settings can be modified by the user. This allows users to achieve the maximum RF performance from a given antenna design.

10.2 Power-up and Clock

10.2.1 Power Management Unit

10.2.1.1 Supply Connections and Power-up

The Power Management Unit of the PN5180 generates internal supplies required for operation.

The following pins are used to supply the IC:

- PVDD - supply voltage for the SPI interface and control connections
- VBAT - Supply Voltage input
- TVDD - Transmitter supply
- AVDD - Analog supply input, connected to VDD
- DVDD - Digital supply input, connected to VDD

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- VDD - 1.8 V output, to be connected to AVDD and DVDD

Blocking capacitors shall be placed as close as possible to the pins of the package. Any additional filtering/damping of the transmitter supply, e.g. by ferrite beads, might have an impact on the analog RF signal quality and needs to be monitored carefully.

Sequential order for powering up the IC

- First ramp VBAT, PVDD can immediately follow, latest 2 ms after VBAT reaches 1.8 V.
- There is no timing dependency on TVDD, only that TVDD shall rise equal or later to VBAT.
- VBAT must be equal or higher than PVDD
- TVDD has no other relationship to VBAT or PVDD

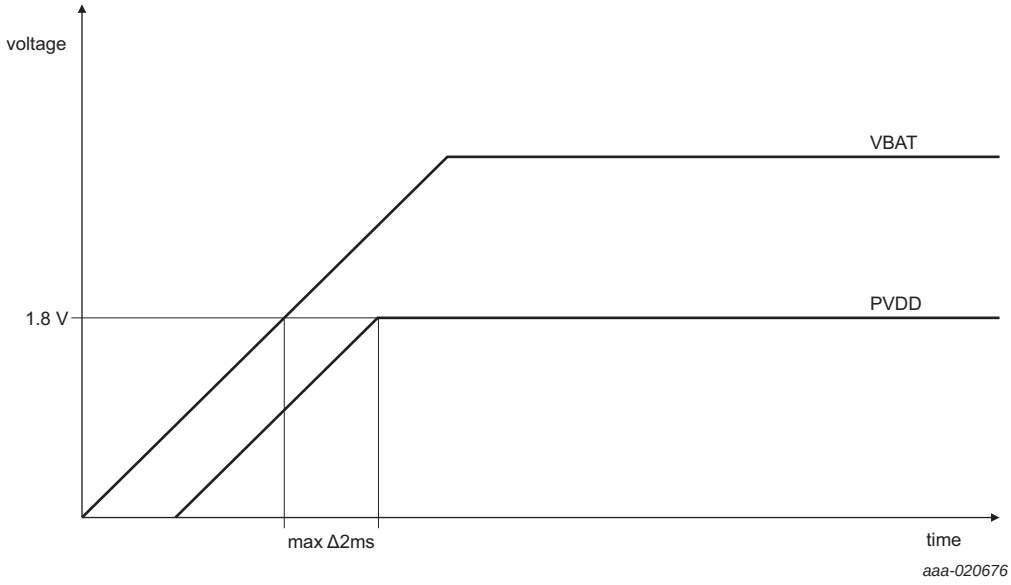

Fig 3. Power-up voltages

After power-up, the PN5180 is indicating the ability to receive command from a host microcontroller by an IDLE IRQ.

There are configurations in EEPROM, which allow to specify the behavior of the PN5180 after start-up. LPCD (Low-power card detection) and DPC (dynamic power control) are functionalities which are configurable in EEPROM.

For NFC target functionality, the configuration LOAD_RF_CONFIG General Target Mode is used.

10.2.1.2 Power-down

A hard power-down is enabled with LOW level on pin RESET_N. This puts the internal voltage regulators for the analog and digital core supply as well as the oscillator in a low-power state. All digital input buffers are separated from the input pads and clamped internally (except pin RESET_N itself). IRQ, BUSY, AUX1, AUX2 have an internal pull down resistor which is activated on RESET_N ==0. All other output pins are switched to high impedance.

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To leave the power-down mode the level at the pin RESET_N has to be set to HIGH. This starts the internal start-up sequence from Power-Down.

10.2.1.3 Standby

The standby mode is entered immediately after sending the instruction SWITCH_MODE with standby. All internal current sinks are set to low-power state.

In opposition to the power-down mode, the digital input buffers are not separated by the input pads and keep their functionality. The digital output pins do not change their state.

During standby mode, all registers values, the buffer content and the configuration itself will not be kept, exceptions are the registers with addresses 05h(PADCONFIG_REG), 07h(PADOUT_REG) 25h(TEMP_CONTROL). To leave the standby mode, various possibilities do exist. The conditions for wake-up are configured in the register STBY_CFG_REG.

- Wake-up via Timer
- Wake-up via RF level detector
- Low Level on RESET_N
- PVDD disappears

Any host communication (data is not validated) will trigger the internal start-up sequence. The reader IC is in full operation mode again when the internal start-up sequence is finalized.

10.2.1.4 Temperature Sensor

The PN5180 implements a configurable temperature sensor. The temperature sensor is configurable by the TEMP_CONTROL register (25h).

The Temperature Sensor supports temperature settings for 85 °C, 115 °C, 125 °C and 135 °C.

In case the sensed device temperature is higher than configured, a TEMPSENS_ERROR IRQ is raised. The host is able to react then in an appropriate way by e.g. switching off the RF field. There is no automatic temperature protection implemented which shuts down the device in case of overheating.

10.2.2 Reset and start-up time

A constant low level of at least 10 μs at the RESET_N pin starts the internal reset procedure.

When the PN5180 has finished the start_up, a IDLE_IRQ is raised and the IC is ready to receive commands on the host interface.

10.2.3 Clock concept

The PN5180 needs to be supplied by an 27.12 MHz crystal for operation. In addition, the internal PLL allows to use an accurate external clock source of either 8, 12, 16, 24 MHz instead of the crystal.

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The clock applied to the PN5180 provides a time basis for the synchronous system's encoder and decoder. The stability of the clock frequency, is an important factor for correct operation. To obtain optimum performance, clock jitter must be reduced as much as possible. This is best achieved using the internal oscillator buffer with the recommended circuitry.

In card mode the clock is also required.

If an external clock source of 27.12 MHz is used instead of a crystal, the clock signal must be applied to pin CLK1. In this case, special care must be taken with the clock duty cycle and clock jitter.

The crystal is a component which is impacting the overall performance of the system. A high-quality component is recommended here. The resistor RD1 allows to reduce the start-up time of the crystal. A short start-up time is especially desired in case the Low-Power card detection is used. The values of these resistors depend on the crystal which is used.

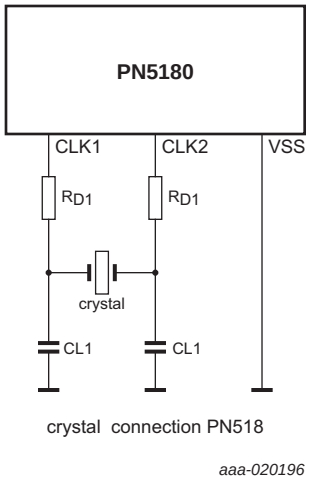

Fig 4. Connection of Crystal

10.3 Timer and Interrupt system

10.3.1 General Purpose Timer

The Timers are used to measure certain intervals between certain configurable events of the receiver, transmitter and other RF-events. The timer signals its expiration by raising a flag and the value of the timer may be accessed via the register-set.

Three general-purpose timers T0, T1, and T2 running with the PN5180 clock with several start conditions, stop conditions, time resolutions, and maximal timer periods are implemented.

For automatic time-out handling during MIFARE Authentication Timer2 is blocked during this operation.

In case EMVCo EMD is enabled, Timer1 will be automatically restarted when an EMD event occurs.

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Timers T0 to T2 have a resolution of 20 bits and may be operated at clock frequencies derived from the 13.56 MHz system clock. Several start events can be configured: start now, start on external RF-field on/off and start on Ex/Tx started/ended. The timers allow reload of the counter value. At expiration of the timers a flag is raised and an IRQ is triggered.

The clock may be divided by a prescaler for frequencies of:

- 6.78 MHz
- 3.39 MHz
- 1.70 MHz
- 848 kHz
- 424 kHz
- 212 kHz
- 106 kHz
- 53 kHz

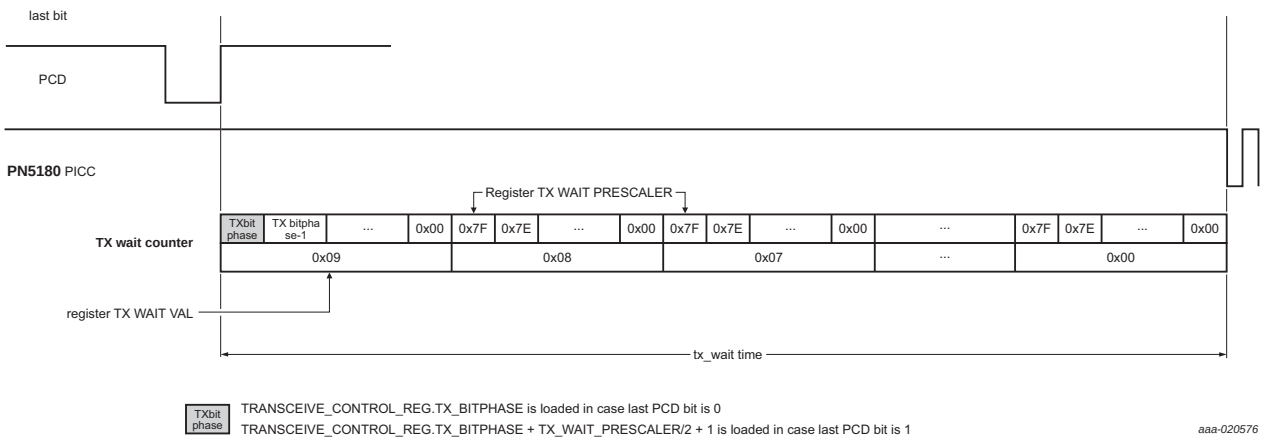

Fig 5. Target Mode case: Timer stop for started reception

10.3.2 Interrupt System

10.3.2.1 IRQ PIN

The IRQ_ENABLE_REG allows to configure, which of the interrupts are routed to the IRQ pin of the PN5180. All of the interrupts can be enabled and disabled independent from each other. The IRQ on the pin can either be cleared by writing to the IRQ_SET_CLEAR register or by reading the IRQ_STATUS register (EEPROM configuration). If not all enabled IRQ's are cleared the IRQ pin remains active.

The polarity of the external IRQ signal can be configured by EEPROM in IRQ_PIN_CONFIG (01Ah).

10.3.2.2 IRQ_STATUS Register

The IRQ_STATUS register contains the status flags. The status flags cannot be disabled. Status Flag can either be cleared by writing to the IRQ_SET_CLEAR register or when the IRQ_STATUS register is read (EEPROM configuration)

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The PN5180 indicates certain events by setting bits in the register GENERAL_IRQ_STATUS_REG and additionally, if activated, on the pin IRQ.

LPCD_IRQ, GENERAL_ERROR_IRQ and HV_ERROR_IRQ are non-maskable interrupts.

10.4 SPI Host Interface

10.4.1 Physical Host Interface

The interface of the PN5180 to a host microcontroller is based on a SPI interface, extended by signal line BUSY. The maximum SPI speed is 7 Mbps and fixed to CPOL = 0 and CPHA = 0. Only a half duplex data transfer is supported. There is no chaining allowed, meaning that the whole instruction has to be sent or the whole receive buffer has to be read out. The whole transmit buffer has to be written at once as well. No NSS assertion is allowed during data transfer.

As the MISO line is per default high-ohmic in case of NSS high, an internal pull-up resistor can be enabled via EEPROM.

The BUSY signal is used to indicate the PN5180 is not able to send or receive data over the SPI interface.

The host interface is designed to support the typical interface supply voltages of 1.8 V and 3.3 V of today's CPU's. A dedicated supply input which defines the host interface supply voltage independent from other supplies is available (PVDD). Note that only a voltage of 1.8 V or 3.3 V is supported, but no voltage in the range of 1.95 V to 2.7 V.

- Master In Slave Out (MISO)

The MISO line is configured as an output in a slave device. It is used to transfer data from the slave to the master, with the most significant bit sent first. The MISO signal is put into tri-state mode when NSS is high.

- Master Out Slave In (MOSI)

The MOSI line is configured as an input in a slave device. It is used to transfer data from the master to a slave, with the most significant bit sent first.

- Serial Clock (SCK)

The serial clock is used to synchronize data movement both in and out of the device through its MOSI and MISO lines.

- Not Slave Select (NSS)

The slave select input line is used to select a slave device. It has to be low before any data transaction and must stay low of the duration of the transaction. The NSS line on the master side must be tied high.

- Busy

During frame reception the BUSY line will go ACTIVE and will go to IDLE when PN5180 is able to receive a new frame or data is available (depending if SET or GET frame is issued). In case of a parameter error, the IRQ will be set to ACTIVE and a GENERAL_ERROR_IRQ is set.

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Both master and slave devices must operate with the same timing. The master device always places data on the MOSI line a half cycle before the clock edge SCK, in order for the slave device to latch the data.

The BUSY line is used to indicate if the system is BUSY and cannot receive any data from a host. Recommendation for the BUSY line handling by the host:

1. Assert NSS to Low
2. Perform Data Exchange
3. Wait until BUSY is high
4. Deassert NSS
5. Wait until BUSY is low

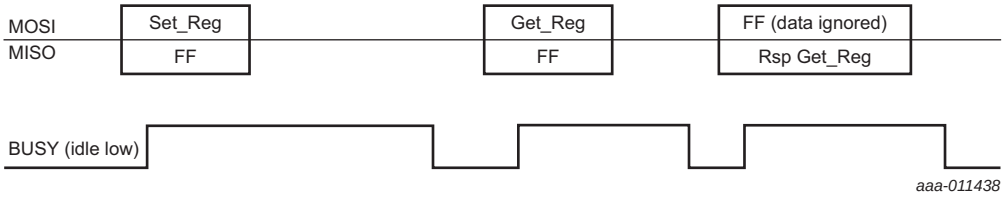

Fig 6. Read RX of SPI data using BUSY line

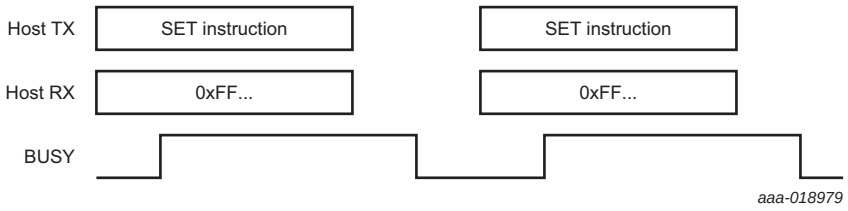

Fig 7.

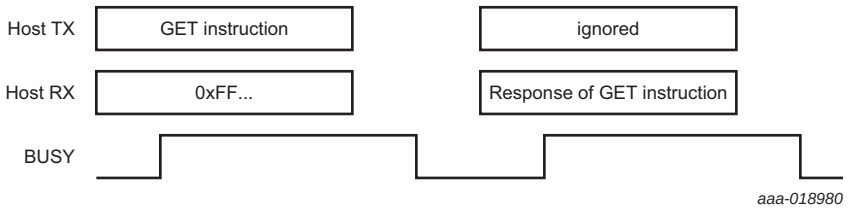

Fig 8.

10.4.2 Timing Specification SPI

The timing condition for SPI interface is as follows:

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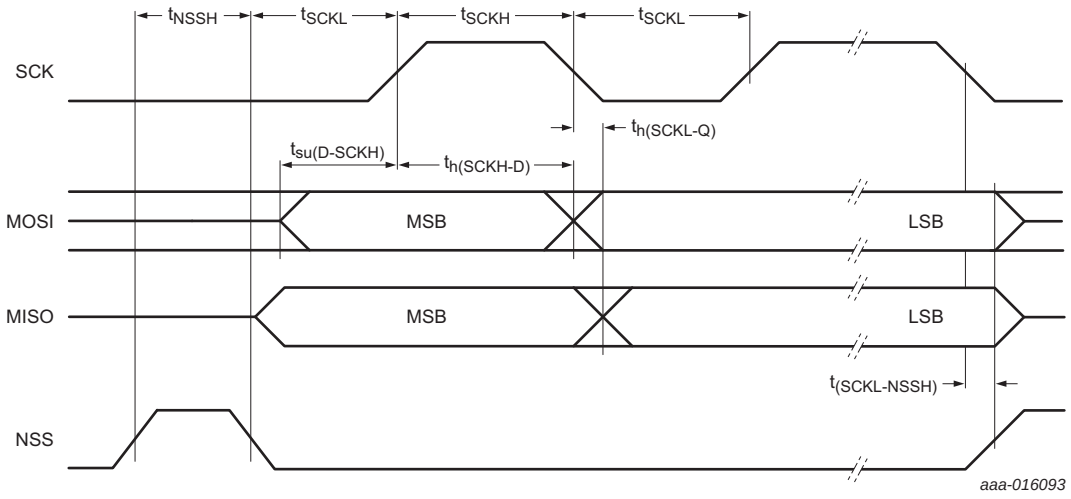

Fig 9. Connection to host with SPI

Remark: To send more bytes in one data stream the NSS signal must be LOW during the send process. To send more than one data stream the NSS signal must be HIGH between each data stream. Any data available to be read from the SPI interface is indicated by the BUSY signal de-asserted.

10.4.3 Logical Host Interface

10.4.3.1 Host Interface Command

A Host Interface Command consists of either 1 or 2 SPI frames depending if the host wants to write or read data from the PN5180. An SPI Frame consists of multiple bytes.

The protocol used between the host and the PN5180 uses 1 byte indicating the instruction code and additional bytes for the payload (instruction-specific data). The actual payload size depends on the instruction used. The minimum length of the payload is 1 byte. This provides a constant offset at which message data begins.

All commands are packed into one SPI Frame. An SPI Frame consists of multiple bytes. No NSS toggles allowed during sending of an SPI frame.

For all 4 byte command parameter transfers (e.g. register values), The payload parameters passed follow the little endian approach (Least Significant Byte first).

Direct Instructions are built of a command code (1 Byte) and the instruction parameters (max. 260 bytes). The actual payload size depends on the instruction used.

Responses to direct instructions contain only a payload field (no header). All instructions are bound to conditions. If at least one of the conditions is not fulfilled, an exception is raised.

In case of an exception, the IRQ line of PN5180 is asserted and corresponding interrupt status register contain information on the exception.

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10.4.3.2 RF Buffer

Two buffers are implemented in the PN5180. The RF transmission buffer has a buffer size of 260 bytes, the RF reception buffer has a size of 508 bytes. They buffer the input and output data streams between the host and the internal state machine / contactless UART of the PN5180. Thus, it is possible to handle data streams with lengths of up to 260 bytes for RF transmission and up to 508 bytes for RF reception without taking timing constraints into account.

10.4.3.3 Host Interface Command List

Table 5. 1-Byte Direct Commands and Direct Command Codes

Command	Command code	Description
WRITE_REGISTER	0x00	Write one 32bit register value
WRITE_REGISTER_OR_MASK	0x01	Sets one 32bit register value using a 32 bit OR mask
WRITE_REGISTER_AND_MASK	0x02	Sets one 32bit register value using a 32 bit AND mask
WRITE_REGISTER_MULTIPLE	0x03	Processes an array of register addresses in random order and performs the defined action on these addresses.
READ_REGISTER	0x04	Reads one 32bit register value
READ_REGISTER_MULTIPLE	0x05	Reads from an array of max.18 register addresses in random order
WRITE_EEPROM	0x06	Processes an array of EEPROM addresses in random order and writes the value to these addresses
READ_EEPROM	0x07	Processes an array of EEPROM addresses from a start address and reads the values from these addresses
WRITE_TX_DATA	0x08	This instruction is used to write data into the transmission buffer
SEND_DATA	0x09	This instruction is used to write data into the transmission buffer, the START_SEND bit is automatically set.
READ_DATA	0x0A	This instruction is used to read data from reception buffer, after successful reception.
SWITCH_MODE	0x0B	This instruction is used to switch the mode. It is only possible to switch from NormalMode to Standby, LPCD or Autocoll.
MIFARE_AUTHENTICATE	0x0C	This instruction is used to perform a MIFARE Classic Authentication on an activated card.
EPC_INVENTORY	0x0D	This instruction is used to perform an inventory of ISO18000-3M3 tags.
EPC_RESUME_INVENTORY	0x0E	This instruction is used to resume the inventory algorithm in case it is paused.
EPC_RETRIEVE_INVENTORY_RESULT_SIZE	0x0F	This instruction is used to retrieve the size of the inventory result.
EPC_RETRIEVE_INVENTORY_RESULT	0x10	This instruction is used to retrieve the result of a preceding EPC_INVENTORY or EPC_RESUME_INVENTORY instruction.
LOAD_RF_CONFIG	0x11	This instruction is used to load the RF configuration from EEPROM into the configuration registers.
UPDATE_RF_CONFIG	0x12	This instruction is used to update the RF configuration within EEPROM.
RETRIEVE_RF_CONFIG_SIZE	0x13	This instruction is used to retrieve the number of registers for a selected RF configuration
RETRIEVE_RF_CONFIG	0x14	This instruction is used to read out an RF configuration. The register address-value-pairs are available in the response
RF_ON	0x16	This instruction switch on the RF Field

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Table 5. 1-Byte Direct Commands and Direct Command Codes

Command	Command code	Description
RF_OFF	0x17	This instruction switch off the RF Field
ENABLE_TESTBUS_DIGITAL	0x18	Enables the Digital test bus
ENABLE_TESTBUS_ANALOG	0x19	Enables the Analog test bus

The following direct instructions are supported on the Host Interface: Detail Description of the instruction

WRITE_REGISTER

Table 6. WRITE_REGISTER

Payload	Length (byte)	Value/Description
Command code	1	0x00
Parameter	1	Register address
	4	Register content
Response	-	-

Description:

This command is used to write a 32-bit value (little endian) to a configuration register.

Condition:

The address of the register must exist.

WRITE_REGISTER_OR_MASK

Table 7. WRITE_REGISTER

Payload	Length (byte)	Value/Description
Command code	1	0x01
Parameter	1	Register address
	4	OR_MASK
Response	-	-

Description:

This command modifies the content of a register using a logical OR operation. The content of the register is read and a logical OR operation is performed with the provided mask. The modified content is written back to the register.

Condition:

The address of the register must exist.

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WRITE _REGISTER_AND_MASK

Table 8. WRITE_REGISTER_AND_MAKSK

Payload	Length (byte)	Value/Description
Command code	1	0x02
Parameter	1	Register address
	4	AND_MASK
Response	-	-

Description:

This command modifies the content of a register using a logical AND operation. The content of the register is read and a logical AND operation is performed with the provided mask. The modified content is written back to the register.

Condition:

The address of the register must exist.

WRITE_REGISTER_MULTIPLE

Table 9. WRITE_REGISTER_MULTIPLE

Payload	Length (byte)	Value/Description	
Command code	1	0x03	
Parameter		Array of up to 42 elements {address, action, content}	
		1 byte	Register address
		1 byte	Action
		4 byte	Register content
Response	-		-

Description:

This instruction allows to process actions on multiple addresses with a single command. Input parameter is an array of register addresses, actions, and values. The command processes this array, register addresses are allowed to be in random order. For each address, an individual ACTION can be defined.

Parameter value is either the REGISTER_DATA, the OR MASK or the AND_MASK.

ACTION that can be defined individually for each register address:

- 0x01 WRITE_REGISTER
- 0x02 WRITE_REGISTER_OR_MASK
- 0x03 WRITE_REGISTER_AND_MASK

Note: In case of an exception the operation is not rolled-back, i.e. registers which have been modified until exception occurs remain in modified state. Host has to take proper actions to recover to a defined state.

Condition:

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The address of the registers must exist.

READ_REGISTER

Table 10. READ_REGISTER

Payload	Length (byte)	Value/Description
Command code	1	0x04
Parameter	1	Register address
Response	4	Register content

Description:

This command is used to read the content of a configuration register. The content of the register is returned in the 4 byte response.

Condition:

The address of the register must exist.

READ_REGISTER_MULTIPLE

Table 11. READ_REGISTER_MULTIPLE

Payload	Length (byte)	Value/Description	
Command code	1	0x05	
Parameter	1..18	Array of up to 18 elements {Register address}	
		1 byte	Register address
Response	4..72	Array of up to 18 4-byte elements {Register content}	
		4..72 byte	Register content: n*32-bit register data

Description:

This command is used to read up to 18 configuration registers at once. The addresses are allowed to be in random order. The result (data of each register) is provided in the response to the command. Only the register values are included in the response. The order of the register contents within the response corresponds to the order of the register addresses within the command parameter.

Condition:

The address of the register must exist. The size of ‘Register Address’ array must be in the range from 1 – 18, inclusive.

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WRITE_EEPROM

Table 12. WRITE_EEPROM

Payload	length (byte)	Value/Description
Command code	1	0x06
Parameter	1	Address in EEPROM from which write operation starts
	1..255	Array of up to 255 elements {EEPROM content}
Response	-	-

Description:

This command is used to write up to 255 values to the EEPROM. The field ‘values’ contains the data to be written to EEPROM starting at the address given by field ‘EEPROM Address’. The data is written in sequential order.

Condition:

EEPROM Address must be in the range from 0 to 253, inclusive. The number of bytes within the array of elements must be in the range from 1 to 254, inclusive. Write operation must not go beyond EEPROM address 254.

READ_EEPROM

Table 13. READ_EEPROM

Payload	Length (byte)	Value/Description	
Command code	1	0x07	
Parameter	1	Address	Address in EEPROM from which read operation starts
	1	Length	Number of bytes to read from EEPROM
Response	1..254	Content	Array of up to 254 elements

Description:

This command is used to read data from EEPROM memory area. The field 'Address” indicates the start address of the read operation. The field Length indicates the number of bytes to read. The response contains the data read from EEPROM (content of the EEPROM); The data is read in sequentially increasing order starting with the given address.

Condition:

EEPROM Address must be in the range from 0 to 254, inclusive. Read operation must not go beyond EEPROM address 254.

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WRITE_DATA

Table 14. WRITE_DATA

Payload	Length (byte)	Value/Description	
Command code	1	0x08	
Parameter	1..260	Array of up to 260 elements {Transmit data}	
		1 byte	Transmit data: Data written into the transmit buffer
Response	-	-	

Description:

This command is used to write data into the RF transmission buffer. The size of this buffer is 260 bytes. After this instruction has been executed, an RF transmission can be started by configuring the corresponding registers.

Condition:

The number of bytes within the ‘Tx Data’ field must be in the range from 1 to 260, inclusive. The command must not be called during an ongoing RF transmission.

SEND_DATA

Table 15. SEND_DATA

Payload	Length (byte)	Value/Description
Command code	1	0x09
Parameter	1	Valid bits in last byte: Number of valid bits in last byte
	1...260	Array of up to 260 elements
Response	-	-

Description:

This command writes data to the RF transmission buffer and starts the RF transmission. The parameter ‘Number of valid bits in last Byte’ indicates the exact data length to be transmitted for the last byte (for non-byte aligned frames). For an actual transmission, it is assumed that a host has executed the transceiver command (by setting corresponding register).

Table 16. Coding of ‘valid bits in last byte’

Number/Parameter	Functionality
0	All bits of last byte are transmitted
1-7	Number of bits within last byte to be transmitted.

Note: When the instruction returns, transmission might still be ongoing, i.e. the instruction just starts the transmission but does not wait for end of transmission.

Condition:

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The size of ‘Tx Data’ field must be in the range from 0 to 260, inclusive (the 0 byte length allows a symbol only transmission when the TX_DATA_ENABLE is cleared).‘Number of valid bits in last Byte’ field must be in the range from 0 to 7. The command must not be called during an ongoing RF transmission. Transceiver must be in ‘WaitTransmit’ state with ‘Transceive’ command set.

READ_DATA

Table 17. READ_DATA

Payload	Length (byte)	Value/Description	
Command code	1	0x0A	
Parameter	1	RFU	
Response	1...508	Array of up to 508 elements {Received data}	
		1 byte	Received data: data which had been received during last successful RF reception

Description:

This command reads data from the RF reception buffer, after a successful reception. The data is available within the response of the command. The host controls the number of bytes to be read via the SPI interface.

Condition:

The RF data had been successfully received. In case the instruction is executed without preceding an RF data reception, no exception is raised but the data read back from the reception buffer is invalid.

SWITCH_MODE

Table 18. SWITCH_MODE

Payload	Length (byte)	Value/Description	
Command code	1	0x0B	
Parameter	1	Mode	
	1...n	Array of ‘n’ elements {Mode parameter}	
		1 byte	Mode parameter: Number of total bytes depends on selected mode
Return value	-	-	

Description:

This instruction is used to switch the mode. It is only possible to switch from normal mode to Standby, LPCD or Autocoll mode. Switching back to normal mode is not possible using this instruction. The modes Standby, LPCD and Autocoll terminate on specific conditions. Once a configured mode (Standby, LPCD, Autocoll) terminates, normal mode is entered again.

To force an exit from Standby, LPCD or Autocoll mode to normal mode, the host controller has to reset the PN5180.

Condition:

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Parameter ‘mode’ has to be in the range from 0 to– 2, inclusive. Dependent on the selected mode, different parameters have to be passed:

In case parameter ‘mode’ is set to 0 (Standby):

Field ‘Wake-up Control’ must contain a bit mask indicating the enabled wake-up sources and if GPO is to be used. Field ‘Wake-up Counter Value’ must contain the value used for the wake-up counter (= time PN5180 will remain in standby). The value shall be in the range from 1 – 2690, inclusive.

Table 19.

Parameter	Length (byte)	Value/Description
Wake-up Control	1	Bit mask controlling the wake-up source to be used and GPO handling.
Wake-up Counter Value	2	Used value for wake-up counter in msecs. Maximum supported value is 2690

Table 20.

b7	b6	b5	b4	b3	b2	b1	b1	
0	0	0	0	0	0			RFU
						X		Wake-up on external RF field, if bit is set to 1b.
							X	Wake-up on wake-up counter expire, if bit is set to 1b.

The field has to be present, even if wake-up counter is not defined as wake-up source. In this case the field ‘wake-up Counter value’ is ignored. No instructions must be sent while being in this mode. Termination is indicated using an interrupt.

In case field ‘Mode’ is set to 1 (LPCD):

Field ‘Wake-up Counter Value’ () defines the period between two LPCD attempts (=time PN5180 will remain in standby) as has to be in the range from 1 to 2690, inclusive. No instructions must be sent while being in this mode. Termination is indicated using an interrupt.

Table 21.

Parameter	Length (bytes)	Value/Description
Wake-up Counter Value	2	Used value for wake-up counter in msecs. Maximum supported value is 2690.

In case field ‘Mode’ is set to 2 (Autocoll):

Field ‘RF Technologies’ must contain a bit mask indicating the RF Technologies to support during Autocoll, according to Field ‘Autocoll Mode’ must be in the range from 0 to 2, inclusive. No instructions must be sent while being in this mode. Termination is indicated using an interrupt.

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Table 22.

Parameter	Length (bytes)	Value/Description
Wake-up Counter Value	2	Used value for wake-up counter in msecs. Maximum supported value is 2690.

Table 23.

Parameter	Length (bytes)	Value/Description	
RF Technologies	1	Bit mask indicating the RF technology to listen for during Autocoll	
Autocoll Mode	1	0	Autonomous mode not used, i.e. autocoll terminates when external RF field is not present.
		1	Autonomous mode used. When no RF field is present, Autocoll automatically enters standby mode. Once RF external RF field is detected, PN5180 enters again Autocoll mode.
		2	Same as 1 but without entering standby mode.

MIFARE_AUTHENTICATE

Table 24. MIFARE_AUTHENTICATE

Payload	Length (bytes)	Value/Description	
Command code	1	0x0C	
Parameter	6	Key: Authentication key to be used	
	1	Key type to be used:	
			0x60: Key type A
			0x61: key type B
	1	Blockaddress: The address of the block for which the authentication has to be performed.	
	4	UID of the card	
Return value	1	Authentication Status	

Description:

This command is used to perform a MIFARE Classic Authentication on an activated card. It takes the key, card UID and the key type to authenticate at a given block address. The response contains one byte indicating the authentication status.

Condition:

Field ‘Key’ must be 6 bytes long. Field ‘Key Type’ must contain the value 0x60 or 0x61. Block address may contain any address from 0x0 – 0xff, inclusive. Field ‘UID’ must be bytes long and should contain the 4 byte UID of the card. An ISO14443-3 MIFARE Classic card should be put into state ACTIVE or ACTIVE* prior to execution of this instruction.

In case of an error related to the authentication, the return value ‘Authentication Status’ is set accordingly.

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Timer2 is not available during the MIFARE Authentication

Table 25. Authentication status return value

Payload Field	Length (byte)	Value/Description	
Authentication Status	1	0	Authentication successful.
		1	Authentication failed (permission denied).
		2	Timeout waiting for card response (card not present).
		3..FF	RFU

EPC_INVENTORY

Table 26. EPC_INVENTORY PARAMETERS

Payload	Length (byte)	Value/Description	
Command code	1	0x0D	
Parameter	1	SelectCommandLength:	
		0	No Select command is set prior to “BeginRound” command. 'Valid Bits in last Byte' field and 'Select” Command shall not be present
		1...39	Length (n) of the 'Select” command
	0, 1	Valid Bits in last Byte	
		0	All bits of last byte of 'Select command' field are transmitted
		1..7	Number of bits to be transmitted in the last byte of 'Select command' field.
	0..39	Array of up to 39 elements {Select}	
		1 byte	Select: If present (dependent on the first parameter Select Command Length), this field contains the ‘Select’ command (according to ISO18000-3) which is sent prior to a BeginRound command. CRC-16c shall not be included.
	3	BeginRound: Contains the BeginRound command (according to ISO18000-3). CRC-5 shall not be included.	
	1	Timeslot behavior	
		0	Response contains max. Number of time slots which may fit in response buffer.
		1	Response contains only one timeslot.
		2	Response contains only one timeslot. If timeslot contains valid card response, also the card handle is included.
Response	0		-

Description:

This instruction is used to perform an inventory of ISO18000-3M3 tags. It implements an autonomous execution of several commands according to ISO18000-3M3 in order to guarantee the timings specified by this standard.

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If present in the payload of the instruction, a ‘Select' command is executed followed by a ‘BeginRound’ command. If there is a valid response in the first time slot (no time-out, no collision), the instruction sends an ACK and saves the received PC/XPC/UII. The device performs then an action according to the definitions of the field ‘Timeslot Processed Behavior’:

- If this field is set to ‘0’ a NextSlot command is issued to handle the next time slot. This is repeated until the internal buffer is full
- If this field is set to 1 the algorithm pauses
- If this field is set to 2 a Req_Rn command is issued if, and only if, there has been a valid tag response in this timeslot

Condition:

EPC_RESUME_INVENTORY

Table 27. EPC_RESUME_INVENTORY PARAMETERS

Payload	length (byte)	Value/Description
Command code	1	0x0E
Parameter	1	RFU
Response	0	-

Description:

This instruction is used to resume the inventory algorithm for the ISO18000-3M3 Inventory in case it is paused. This instruction has to be repeatedly called, as long as 'Response Size' field in EPC_RETRIEVE_INVENTORY_RESULT_SIZE is greater than 0.

A typical sequence for a complete EPC GEN2 inventory retrieval is:

1. Execute EPC_INVENTORY to start the inventory
2. Execute EPC_RETRIEVE_INVENTORY_RESULT_SIZE
3. If size is 0, inventory has finished.
4. Otherwise, execute EPC_RETRIEVE_INVENTORY_RESULT
5. Execute EPC_RESUME_INVENTORY and proceed with step 2.

Condition:

Field 'RFU' must be present and can be set to any value.

EPC_RETRIEVE_INVENTORY_RESULT_SIZE

Table 28. EPC_RETRIEVE_INVENTORY_RESULT PARAMETERS

Payload	length (byte)	Value/Description
Command code	1	0x0F
Parameter	1	RFU

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Table 28. EPC_RETRIEVE_INVENTORY_RESULT PARAMETERS

Payload	length (byte)	Value/Description	
Response	2	Response size:	
		0	Inventory has finished.
		1..512	Value indicates the length of the EPC_RETRIEVE_INVENTORY_RESULT response payload

Description:

This instruction is used to retrieve the size of the inventory result. The size is located in the response to this instruction and reflects the payload size of the response to the next execution of EPC_RETRIEVE_INVENTORY_RESULT. If the size is 0, then no more results are available which means inventory algorithm has finished.

Condition:

Field 'RFU' must be present and can be set to any value.

EPC_RETRIEVE_INVENTORY_RESULT

Table 29. EPC_RETRIEVE_INVENTORY_RESULT PARAMETERS

Payload	length (byte)	Value/Description
Command code	1	0x10
Parameter	1	RFU
Response	2	Response size
		If Response size == 0: Inventory has finished.
		If Response size == 1...512: Value indicates the length of the EPC_RETRIEVE_INVENTORY_RESULT response payload

Description:

This instruction is used to retrieve the result of a preceding or EPC_RESUME_INVENTORY instruction. The size of the payload within the response is determined by the ‘Response Size’ field of EPC_RETRIEVE_INVENTORY_RESULT_SIZE response. Depending on the ‘Timeslot Processed Behavior’ defined in that instruction, the result contains one or more time slot responses. Each timeslot response contains a status (field ‘Timeslot Status’) which indicates if there has been a valid tag reply or a collision or no tag reply at all:

0 - Tag response available, XPC/PC/UII embedded in the response within 'Tag reply' field

1- Tag response available and tag handle retrieved. XPC/PC/UII as well as tag handle available in the response within 'Tag reply' field and 'Tag Handle' field, respectively.

2- No tag replied, empty time slot

3- Collision, two or more tags replied in the same time slot

Condition:

Field 'RFU' must be present and can be set to any value.

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LOAD_RF_CONFIG

Table 30. LOAD_RF_CONFIG PARAMETERS

Payload	length (byte)	Value/Description
Command code	1	0x11
Parameter	1	Transmitter configuration byte
	1	Receiver configuration byte
Response	-	-

Description:

This instruction is used to load the RF configuration from EEPROM into the configuration registers. The configuration refers to a unique combination of mode (target/initiator) and baud rate. The configuration can be loaded separately for the receiver (Receiver configuration) and transmitter (Transmitter configuration).

The PN5180 is pre-configured by EEPROM with settings for all supported protocols. The default factory EEPROM settings are considering typical antenna. It is possible for the user to modify the EEPROM and by this adapt the default settings to individual antennas for optimum performance. The command UPDATE_RF_CONFIG needs to be used for modification of the default RF Configuration settings. There is no possibility to update the EEPROM data directly, updates need to make use of the UPDATE_RF_CONFIG command.

The parameter 0xFF has to be used if the corresponding configuration shall not be changed.

Condition:

Parameter 'Transmitter Configuration' must be in the range from 0x0 - 0x1C, inclusive. If the transmitter parameter is 0xFF, transmitter configuration is not changed.

Field 'Receiver Configuration' must be in the range from 0x80 - 0x9C, inclusive. If the receiver parameter is 0xFF, the receiver configuration is not changed.

Table 31. LOAD_RF_CONFIG: Selection of protocol register settings

Transmitter: RF configuration byte (hex)	Protocol	Speed (kbit/s)	Receiver: RF configuration byte (hex)	Protocol	Speed (kbit/s)
00	ISO 14443-A / NFC PI-106	106	80	ISO 14443-A / NFC PI-106	106
01	ISO 14443-A	212	81	ISO 14443-A	212
02	ISO 14443-A	424	82	ISO 14443-A	424
03	ISO 14443-A	848	83	ISO 14443-A	848
04	ISO 14443-B	106	84	ISO 14443-B	106
05	ISO 14443-B	212	85	ISO 14443-B	212
06	ISO 14443-B	424	86	ISO 14443-B	424
07	ISO 14443-B	848	87	ISO 14443-B	848
08	Felica / NFC PI 212	212	88	Felica / NFC PI 212	212
09	Felica / NFC PI 424	424	89	Felica / NFC PI 212	424
0A	NFC-Active Initiator	106	8A	NFC-Active Initiator	106

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Table 31. LOAD_RF_CONFIG: Selection of protocol register settings

Transmitter: RF configuration byte (hex)	Protocol	Speed (kbit/s)	Receiver: RF configuration byte (hex)	Protocol	Speed (kbit/s)
0B	NFC-Active Initiator	212	8B	NFC-Active Initiator	212
0C	NFC-Active Initiator	424	8C	NFC-Active Initiator	424
0D	ISO 15693 ASK100	26	8D	ISO 15693	26
0E	ISO 15693 ASK10	26	8E	ISO 15693	53
0F	ISO 18003M3 Manch. 424_4	Tari=18,88	8F	ISO 18003M3 Manch. 424_4	106
10	ISO 18003M3 Manch. 424_2	Tari=9,44	90	ISO 18003M3 Manch. 424_2	212
11	ISO 18003M3 Manch. 848_4	Tari=18,88	91	ISO 18003M3 Manch. 848_4	212
12	ISO 18003M3 Manch. 848_2	Tari=9,44	92	ISO 18003M3 Manch. 848_2	424
13	ISO 18003M3 Manch. 424_4	106	93	ISO 14443-A PICC	106
14	ISO 14443-A PICC	212	94	ISO 14443-A PICC	212
15	ISO 14443-A PICC	424	95	ISO 14443-A PICC	424
16	ISO 14443-A PICC	848	96	ISO 14443-A PICC	848
17	NFC Passive Target	212	97	NFC Passive Target	212
18	NFC Passive Target	424	98	NFC Passive Target	424
19	NFC Active Target 106	106	99	ISO 14443-A	106
1A	NFC Active Target 212	212	9A	ISO 14443-A	212
1B	NFC Active Target 424	424	9B	ISO 14443-A	424
1C	GTM	ALL	9C	GTM	ALL

UPDATE_RF_CONFIG:

Table 32. UPDATE_RF_CONFIG PARAMETERS

Payload	length (byte)	Value/Description
Command code	1	0x13
Parameter	1...42	Array of up to 42 elements {RF configuration byte, Register Address, Register value}
Elements	1	RF Configuration byte: RF configuration for which the register has to be changed.
	1	Register Address: Register Address within the given RF technology.
	4	Register value: Value which has to be written into the register.
Response	-	-

Description:

This instruction is used to update the RF configuration within the EEPROM. The command allows updating dedicated EEPROM addresses, if not the complete set needs to be updated.

Condition:

The size of the array of ‘Configuration data’ must be in the range from 1 – 42, inclusive. The array data elements must contain a set of ‘RF Configuration byte’, ‘Register Address’ and ‘Value’. The field ‘RF Configuration byte’ must be in the range from 0x00 – 0x1C or

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0x80-0x9C, inclusive. The address within field ‘Register Address’ must exist within the respective RF configuration. The ‘Register Value’ contains a value which will to be written into the given register and must be 4 bytes long

RETRIEVE_RF_CONFIG_SIZE

Table 33. RETRIEVE_RF_CONFIG_SIZE PARAMETERS

Payload	length (byte)	Value/Description
Command code	1	0x14
Parameter	1	RF configuration ID: RF configuration for which the number of registers has to be retrieved.
Response	1	Number of registers for the selected “RF configuration ID”

Description:

This command is used to retrieve the size (number of 32-bit registers) of a given RF configuration. The size is available in the response to this instruction.

Condition:

The field 'RF configuration ID' must be in the range from 0x00 - 0x1C or 0x80-0x9C, inclusive.

RETRIEVE_RF_CONFIG

Table 34. RETRIEVE_RF_CONFIG PARAMETERS

Payload	length (byte)	Value/Description
Command code	1	0x14
Parameter	1	RF configuration ID: RF configuration for which the number of 32-bit registers has to be retrieved.
Response	0...39	Array of up to 39 elements {RegisterAddress, RegisterContent}
	1	RegisterAddress: Address of the register to read
	4	RegisterContent: Data of register addressed by this element

Description:

This command is used to read an RF configuration. The register content available in the response. In order to know how many pairs are to be expected, the command RETRIEVE_RF_CONFIGURATION_SIZE has to be executed first.

Condition:

The field 'RF configuration ID' must be in the range from 0x00-0x1C or 0x80-0x9C, inclusive

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RF_ON

Table 35. RF_ON

Payload	length (byte)	Value/Description
Command code	1	0x16
Parameter	1	Bit0: disable collision avoidance according to ISO18092 Bit1: Use Active Communication mode according to ISO18092

Description:

This command is used to switch on the internal RF field. If enabled the TX_RFON_IRQ is set after the field is switched on.

RF_OFF

Table 36. RF_OFF

Payload	length (byte)	Value/Description
Command code	1	0x17
Parameter	1	dummy byte

Description:

This command is used to switch off the internal RF field. If enabled, the TX_RFOFF_IRQ is set after the field is switched off.

ENABLE_TESTBUS_DIGITAL

Table 37. ENABLE_TESTBUS_DIGITAL

Payload	length (byte)	Value/Description
Command code	1	0x18
Parameter	1	Signal Bank
	1*n	TB_pos: Pad Location and test bus Bit Position n can have a value between 1 and 4

Description:

This command enables the Digital test bus. There are several signal banks which can be selected. From the selected signal banks the test signals can be routed to different pads.

Attention: Test bus must be enabled before in the EEPROM settings.
Attention: Due to test bus functionality it can occur that the BUSY line is not correctly asserted during data transmission when the test bus is enabled via the EEPROM setting. It is recommended to use following sequence: First set the NSS to low, wait until BUSY is asserted and then perform the data exchange.

TB_pos byte has to be configured in the following way:

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Table 38. TB_POS

BitPos	Value	Description
0_3	0..7	Signal Selection of the Signal Bank
	8	13 MHz RF clock
	9..F	RFU
4:7	0	IRQ pad
	1	AUX1 pad
	2	AUX2 pad
	3	GPO1
	4..F	RFU

ENABLE_TESTBUS_ANALOG

Table 39. ENABLE_TESTBUS_ANALOG

Payload	length (byte)	Value/Description
Command code	1	0x19
Parameter	1	DAC output to AUX2
	1	DAC output to AUX1

Description:

This command enables the Analog test bus.

Attention: Test bus must be enabled before in the EEPROM settings.
Attention: Due to test bus functionality it can occur that the BUSY line is not correctly asserted during data transmission when the test bus is enabled via the EEPROM setting. It is recommended to use following sequence: First set the NSS to low, wait until BUSY is asserted and then perform the data exchange.

The following direct commands are supported on the Host Interface:

10.5 Memories

10.5.1 Overview

The PN5180 implements two different memories: EEPROM, RAM for buffers.

At start-up, all registers are initialized with default values. For the registers defining the RF functionality, the default values will not be useful to execute any contactless communication.

The registers defining the RF functionality can be initialized either by writing values directly to a register address using the direct instruction WRITE_REGISTER, or LOAD_RF_CONFIGURATION.

In the case of the instruction LOAD_RF_CONFIGURATION, the initialization of the registers which define the RF behavior of the IC is performed by an automatic copy of a predefined EEPROM area (read/write EEPROM section1 and section2, register reset) into the registers defining the RF behavior.

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10.5.2 EEPROM

The EEPROM memory maintains its content during Power-OFF, whereas the RAM (Buffers) will not keep any data stored in this volatile memory.

The EEPROM address range is from 0x00 to 0xFF.

The EEPROM contains information about Die Identifier, Firmware Version, System configuration and RF settings for fast configuration.

Table 40. EEPROM Addresses

EEPROM Address (HEX)	Field / Value	Access	Size (bytes)	Comments
0x00	Die identifier	R	16	Each DIE has a unique Identifier
0x10	Product Version	R	2	Product Version Indicator
0x12	Firmware Version	R	2	Firmware Version
0x14	EEPROM Version	R	2	EEPROM Version Number
0x16	IDLE_IRQ_AFTER_BOOT	RW	1	This enables the IDLE IRQ to be set after the boot has finished
0x17	TESTBUS_ENABLE	RW	1	This bit enables the test bus functionality. During this phase it can happen that the BUSY line is asserted after the frame is received. Therefore it is recommend to first set NSS to low, wait until BUSY goes high and then send the data.
0x18	XTAL_BOOT_TIME	RW	2	XTAL boot time in us
0x1A	IRQ_PIN_CONFIG	RW	1	Bit0.... 0 IRQ active low Bit0 .....1 IRQ active high Bit1.. . 0 Use IRQ_SET_CLEAR_REG to clear IRQ pin Bit1.... 1 Auto Clear on Read of IRQ_STATUS_REG
0x1B	MISO_PULLUP_ENABLE	RW	1	0/1 ... no pullup/down 2.. Pulldown 3... Pullup 4..FF... RFU
0x1C	PLL_DEFAULT_SETTING	RW	8	PLL configuration of clock input frequency in case a 13.56 MHz Crystal is not used
0x24	PLL_DEFAULT_SETTING_ALM	R/W	8	PLL configuration for the Active Load Modulation
0x2c	PLL_LOCK_SETTING	R/W	4	Lock Settings for the PLL - do not change
0x30	CLOCK_CONFIG	RW	1	bit[4 - 7]: RFU bit[0:3]: 1000: Crystal bit[0:3]: 0000: PLL all others RFU
0x31	RFU	RW	1	-
0x32	MFC_AUTH_TIMEOUT	RW	2	Timeout value used for Auth1 & Auth2 stages during MFC Authenticate
0x34	LPCD_REFERENCE_VALUE	RW	2	AGC Reference Value
0x36	LPCD_FIELD_ON_TIME	RW	1	1 byte delay * 8 in microseconds settling time for AGC measurement

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Table 40. EEPROM Addresses *…continued*

EEPROM Address (HEX)	Field / Value	Access	Size (bytes)	Comments
0x37	LPCD_THRESHOLD	RW	1	1 byte AGC threshold value which is used to compare against the (Current AGC value – Reference AGC) during the Low-Power Card Detection phase
0x38	LPCD_REFVAL_CONTROL	RW	1	Bit1:0 LPC-D mode 00 Use EEPROM value of LPCD_REFERENCE_VALUE for reference value 01 Use on begin of an LPCD a measurement cycle for generating a reference value.10...Use the Register value of CHECK_CARD_RESULT for reference value. This allows the configuration of the reference value without EEPROM programming. Bit2 GPO1 Control for external TVDD LDO 0: Disable Control of external TVDD LDO via GPO1 1: Enable Control of external TVDD LDO via GPO1
0x39	LPCD_GPO_TOGGLE_BEFORE_FIELD_ON	RW	1	1 byte value defines the time between setting GPO1 until Field is switched on. The time can be configured in 8 bits in 5us steps
0x3A	LPCD_GPO_TOGGLE_AFTER_FIELD_ON	RW	1	1 byte value defines the time between Field Off and clear GPOGPO1. The time can be configured in 8 bits in 5us steps
0x3B	NFCLD_SENSITIVITY_VAL	RW	1	NFCLD Sensitivity value to be used during the RF On Field handling Procedure.
0x3C	FIELD_ON_CP_SETTLE_TIME	RW	1	Delay in 4us steps (range: 0 - 1020us) to wait during RF on for charge pumps to be settled, to avoid initial Tx driver overcurrent
0x3D	RFU	RW	2	RFU
0x3F	RF_DEBOUNCE_TIMEOUT	RW	1	RF Debounce Timeout in step size of 10 μs
0x40	SENS_RES	RW	2	Response to ReqA / ATQA in order byte 0, byte 1
0x42	NFCID1	RW	3	in order byte 0, byte 1, byte 2; the first NFCID1 byte is fixed to 08h and the check byte is calculated automatically
0x45	SEL_RES	RW	1	Response to Select
0x46	FELICA_POLLING_RESPONSE	RW	18	FeliCa Polling response (2 bytes (shall be 01h, FEh) + 6 bytes NFCID2 + 8 bytes Pad + 2 bytes system code)
0x58	NFCID3	RW	1	NFCID3 (1 byte)
0x59	DPC_CONTROL	RW	1	bit7..4 START_GEAR; binary definition of start gear, bit4=LSB of start gear number bit3..1 GEAR_STEP_SIZE: binary definition of gear step size, bit1=LSB of gear step size bit0 DPC_ENABLE cleared: OFF; set: ENABLE
0x5A	DPC_TIME	RW	2	Sets the value for the periodic regulation. Time base is 1/20 MHz. (Example: Value of 20000 is equal to 1 ms)
0x5C	DPC_XI	RW	1	Trim Value of the AGC value

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Table 40. EEPROM Addresses *…continued*

EEPROM Address (HEX)	Field / Value	Access	Size (bytes)	Comments
0x5D	AGC_CONTROL	RW	2	Controls the AGC loop bit15..14 RFU bit13 StepSize Enable bit12..11 StepSize bit10... Duration Enable bit9..0 Duration
0x5F	DPC_THRSH_HIGH	RW	30	Defines the AGC high threshold for each gear. N defines the number of gears. N can be 1..15
0x7D	DPC_THRSH_LOW	RW	2	Defines the AGC low threshold for initial gear.
0x7F	DPC_DEBUG	RW	1	Enables the debug signals
0x80	DPC_AGC_SHIFT_VALUE	RW	1	Shift Value for the AGC dynamic low adoption to prevent oscillation
0x81	DPC_AGC_GEAR_LUT_SIZE	RW	1	Defines the number of gears for the lookup table (LUT, value can be between 1...15)
0x82	DPC_AGC_GEAR_LUT	RW	15	Defines the Gear Setting for each step size starting with Gear0 up to 15 gears. Each entry contains a definition for the DPC_CONFIG register content. Bits 8:11 are not taken into account.
0x91	DPC_GUARD_FAST_MODE	RW	2	Guard time after AGC fast mode has been triggered. This happens in the following scenarios: - End of Receive - End of Transmit - After a gear switch Time base is 1/20 MHz (Example: Value of 2000 is equal to 100us)
0x93	DPC_GUARD_SOF_DETECTED	RW	2	Guard time after SoF or SC detection. This is to avoid any DPC regulation between SoF/SC and actual begin of reception. Time base is 1/20MHz (Example: Value of 2000 is equal to 100us)
0x95	DPC_GUARD_FIELD_ON	RW	2	Guard time after Gear Switch during FieldOn instruction. Time base is 1/20MHz (Example: Value of 2000 is equal to 100us)
0x97	PCD_SHAPING_LUT_SIZE	RW	1	Number of elements for the PCD Shaping
0x98-0xD7	PCD_SHAPING_LUT	RW	64	PCD Shaping configuration lookup table: Each word contains the following information: 0..3: DPC Gear 4..7: TAU_MOD_FALLING (Sign bit + 3-bit value) 8..11: TAU_MOD_RISING (Sign bit + 3-bit value) 12..15: RESIDUAL_CARRIER (Sign bit + 3-bit value) 16..31: Bitmask identifying technology and baudrate
0xD8 - 0xFF	RFU	R/W	-	RFU

10.5.3 RAM

The RAM is used as Input/Output buffer, and implements independent buffers for input and output. The buffers are able to improve the performance of a system with limited interface speed.

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10.5.4 Register

Registers allow to configure the PN5180 for a specific RF protocol. Registers can be initialized using the host interface or by copying data from EEPROM to the register as done by the command LOAD_RF_CONFIG.

10.6 Debug Signals

10.6.1 General functionality

The debugging of the RF functionality of the PN5180 is supported by a configurable test signal output possibility. Up to 2 analog or up to 4 digital test signals can be routed to configurable output pins of the PN5180. Test signals can be either analog or digital signals. The analog test signals contain the digital data of the signal processing unit of the PN5180, converted to analog signals by a DAC to allow the inspection of these signals in real time.

Two set commands exist for configuration of the digital and analog debug signal output, SET_DIGITAL_TESTOUT and SET_ANALOG_TESTOUT.

10.6.2 Digital Debug Configuration

The digital debug output is configured by the command SET_DIGITAL_TESTOUT. Two parameters are passed within this command.

The first parameter (1 byte) defines the test signal group. Out of this test signal group, one signal can be selected for output on a pin of the PN5180 (4 bits).

The signal of the test signal group is selected by the low-nibble of parameter 2. A value of 8 on this position selects the 13.56 MHz clock to be put out on the selected pin.

The high nibble of parameter 2 (1 byte) selects the output pin for the selected test signal.

The following parameter groups are possible:

Table 41. Debug Signal Group Selection

Command parameter (hex)	Debug Signal Group
01	Clock signal group
1B	Transmitter encoder group
1D	Timer group
30	Cardmode protocol group
58	Transceive group
70	Receiver data transfer group
73	Receiver error group

The second parameter defines the pin which is used for output of the test signal in the high nibble, and the signal from one of the Debug Signal groups that will be put out in the low nibble.

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10.6.2.1 Debug signal groups

Table 42. Clock Signal Group

Value low nibble (HEX)	Debug Function
9..15	RFU
8	13.56 MHz clock is put out
7	CLIF clock reset
6	Signal indicating the PLL is locked
5	Signal indicating an external Field is present
4	20 MHz clock from the high frequency oscillator
3	27.12 MHz clock from the PLL
2	27.12 MHz clock from the RF clock recovery
1	Multiplexed 27.12 MHz clock
0	Multiplexed 13.56 MHz clock

Table 43. Transmitter Encoder Group

Value low nibble (HEX)	Debug Function
9..15	RFU
8	13.56 MHz clock is put out
7..2	RFU
1	Output TX envelope
0	Tx-IRQ

Table 44. Timer Group

Value low nibble (HEX)	Debug Function
9..15	RFU
8	13.56 MHz clock is put out
7	Running flag of timer T0
6	Expiration flag of timer T0
5	Running flag of timer T1
4	Expiration flag of timer T1
3	Running flag of timer T2
2	Expiration flag of timer T2
1..0	RFU

Table 45. Cardmode Protocol Group

Value low nibble (HEX)	Debug Function
9..15	RFU
8	13.56 MHz Clock is put out
7	Synchronized clock-fail signal
6	Flag indicating that ISO/IEC14443-Type A (Miller) was detected

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Table 45. Cardmode Protocol *...continued*Group

Value low nibble (HEX)	Debug Function
5	Flag indicating that FeliCa 212 kBd (Manchester) was detected
4	Flag indicating that FeliCa 424 kBd (Manchester) was detected
3	Flag indicating that ISO/IEC14443-Type B (NRZ) was detected
2	Flag indicating that the EOF was detected
1	CM data signal (Miller / Manchester / NRZ)
0	Signal indicating that the current data is valid

Table 46. Transceive Group

Value low nibble (HEX)	Debug Function
9..15	RFU
8	13.56 MHz clock is put out
7	Signal indicating that the tx prefetch was completed
6	Signal initiating a tx prefetch at the BufferManager
5	Start of transmission signal to TxEncoder
4	enable reception signal to RxDecoder
3	indicator that the waiting time was already expired
2	Transceive state2
1	Transceive state1
0	Transceive state0

Table 47. Receiver Data Transfer Group

Value low nibble (HEX)	Debug Function
9..15	RFU
8	13.56 MHz clock is put out
7	Signal from SigPro indicating a collision
6	Signal from SigPro indicating end of data
5	Signal from SigPro indicating that data is valid
4	Signal from SigPro indicating received data
3	Status signal set by rx_start, ends when RX is completely over
2	Status signal indicating actual reception of data
1	Reset signal for receiver chain (at start of RX)
0	Internal RxDec bitclk

Table 48. Receiver Error Group

Value low nibble (HEX)	Debug Function
9..15	RFU
8	13.56 MHz clock is put out
7	Combination of data/protocol error and collision

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Table 48. Receiver Error Group

Value low nibble (HEX)	Debug Function
6	Set if RxMultiple is set, and the LEN byte indicates more than 28 bytes
5..3	RFU
2	Set if a collision has been detected
1	Protocol error flag
0	Data integrity error flag (Parity, CRC (Collision))

10.6.2.2 Digital Debug Output Pin Configuration

Table 49. Debug Signal Output Pin Configuration

Value high nibble (HEX)	Debug Function (PIN)
0	IRQ (39)
1	GPO (38)
2	AUX2 (2)
3	AUX1 (40)
all others	RFU

10.6.3 Analog Debug Configuration

For the output of an analog debug signal, two pins are available, BUSY and AUX2.

The function of the output pins is defined by two parameters of the command

Table 50.

Parameter (hex)	Debug Function
0	Analog output of value defined in register DAC_VALUE
1	Receiver Q-channel signal; depending on SIGPRO_IN_SEL either samples signals from ADC, tx_envelope or SigIn
2	Receiver I-channel signal; depending on SIGPRO_IN_SEL either samples signals from ADC, tx_envelope or SigIn
3	Filtered Q-channel signal (rect-filter)
4	Filtered I-channel signal (rect-filter)
all others	RFU

10.7 AUX2 / DWL_REQ

10.7.1 Firmware update

The PN5180 offers the possibility to upgrade the internal Firmware.

The pin AUX2/DWL request is a double function pin. During start-up (time from power-up of the IC until IDLE IRQ is raised), the pin is used in input mode. If the polarity on this AUX2/DWL_REQ pin during start-up is high, the PN5180 enters the download mode.

If the boot process is finished (indicated by the IDLE IRQ), the pin is switched to output mode and the pin can be used for general debug purpose.

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Recommended sequence is to set the RESET_N level to 0, set AUX2 pin level to 1 and release RESET_N to 1.

Exiting the download mode is performed by setting the AUX2 pin to 0 and perform a reset of the PN5180.

10.7.2 Firmware update command set

The PN5180 uses a dedicated host interface command set for download of a new firmware. The physical SPI host interface is used for download of a new firmware image. Security features are implemented to avoid intentional or unintentional modifications of the firmware image. The access to the IC is locked based on authentication mechanism to avoid unauthorized firmware downloads. The integrity of the firmware is ensured based on a secure hash algorithm,

The Firmware image can be identified based on a version number, which contains major and minor number.

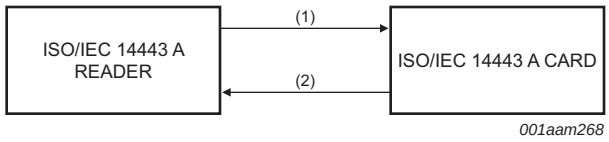
For security reasons, the download of a smaller major version number than currently installed on the PN5180 is not possible.

10.8 RF Functionality

10.8.1 Supported RF Protocols

10.8.1.1 ISO/IEC14443 A/MIFARE functionality

The physical level of the communication is shown in Figure 10.



(1) Reader to Card 100 % ASK, Modified Miller Coded, Transfer speed 106 kbit/s to 848 kbit/s

(2) Card to Reader, Subcarrier Load Modulation Manchester Coded or BPSK, transfer speed 106 kbit/s to 848 kbit/s

Fig 10. ISO/IEC 14443 A/MIFARE read/write mode communication diagram

The physical parameters are described in Table 51.

Table 51. Communication overview for ISO/IEC 14443 A/MIFARE reader/writer

Communication direction	Signal type	Transfer speed			
		106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
Reader to card (send data from the PN5180 to a card) f_c = 13.56 MHz	reader side modulation	100 % ASK	100 % ASK	100 % ASK	100 % ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit rate [kbit/s]	f_c/128	f_c/64	f_c/32	f_c/16

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Table 51. Communication overview for ISO/IEC 14443 A/MIFARE reader/writer *...continued*

Communication direction	Signal type	Transfer speed			
		106 kbit/s	**212 kbit/s**	**424 kbit/s**	**848 kbit/s**
Card to reader (PN5180 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	f_c / 16	f_c / 16	f_c / 16	f_c / 16
	bit encoding	Manchester encoding	BPSK	BPSK	BPSK

The PN5180 connection to a host is required to manage the complete ISO/IEC 14443 A/MIFARE protocol. Figure 11 shows the data coding and framing according to ISO/IEC 14443 A/MIFARE.

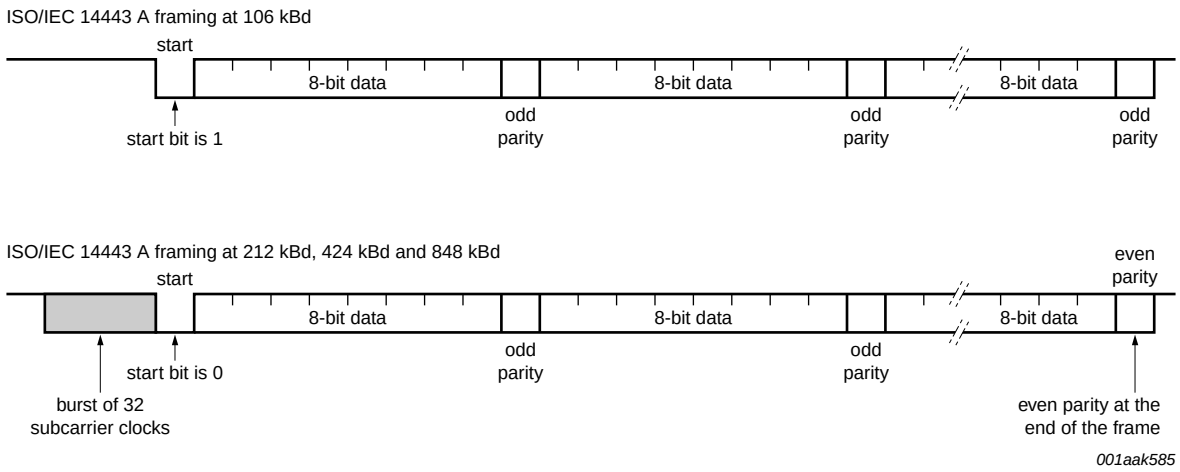

Fig 11. Data coding and framing according to ISO/IEC 14443 A card response

The internal CRC coprocessor calculates the CRC value based on the selected protocol. In card mode for higher baud rates, the parity is automatically inverted as end of communication indicator. The selected protocol needs to be implemented on a host processor.

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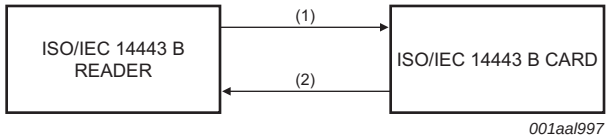
10.8.1.2 ISO/IEC14443 B functionality

The physical level of the communication is shown in Figure 12.



(1) Reader to Card NRZ, transfer speed 106 kbit/s to 848 kbit/s

(2) Card to reader, Subcarrier Load Modulation Manchester Coded or BPSK, transfer speed 106 kbit/s to 848 kbit/s

Fig 12. ISO/IEC 14443B read/write mode communication diagram

The physical parameters are described in Table 52.

Table 52. Communication overview for ISO/IEC 14443 B reader/writer

Communication direction	Signal type	Transfer speed			
		106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
Reader to card (send data from the PN5180 to a card) f_c = 13.56 MHz	reader side modulation	10 % ASK	10 % ASK	10 % ASK	10 % ASK
	bit encoding	NRZ	NRZ	NRZ	NRZ
	bit rate [kbit/s]	128 / f_c	64 / f_c	32 / f_c	16 / f_c
Card to reader (PN5180 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	f_c / 16	f_c / 16	f_c / 16	f_c / 16
	bit encoding	BPSK	BPSK	BPSK	BPSK

The PN5180 requires the host to manage the ISO/IEC 14443 B protocol.

10.8.1.3 FeliCa RF functionality

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification. The communication on a physical level is shown in Figure 13.

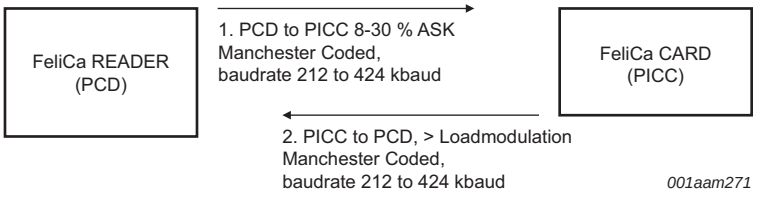


Fig 13. FeliCa read/write communication diagram

The physical parameters are described in Table 53.

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Table 53. Communication for FeliCa reader/writer

Communication direction	Signal type	Transfer speed FeliCa	FeliCa higher transfer speeds
		212 kbit/s	424 kbit/s
Reader to card (send data from the PN5180 to a card) f_c = 13.56 MHz	reader side modulation	8 % to 30 % ASK	8 % to 30 % ASK
	bit encoding	Manchester encoding	Manchester encoding
	bit rate	$f_c/64$	$f_c/32$
Card to reader (PN5180 receives data from a card)	card side modulation	Load modulation,	Load modulation,
	bit encoding	Manchester encoding	Manchester encoding

The PN5180 needs to be connected to a host which implements the FeliCa protocol.

Multiple reception cycles (RxMultiple): For FeliCa timeslot handling in PCD mode, PN5180 implements multiple reception cycles. The feature is enabled by setting the control bit RX_MULTIPLE_ENABLE in the register TRANSCEIVE_CONTROL_REG in combination with the transceive state machine.

Unlike for normal operation the receiver is enabled again after a reception is finished. As there is only one receive buffer available but several responses are expected the buffer is split into sub buffers of 32 byte length. Hence, the maximum number of responses which can be handled is limited to 8. As the maximum length defined for a FeliCa response is 20 bytes the buffer size defined does fulfill the requirements for that use-case. The first data frame received is copied onto buffer address 0. The subsequent frames will be copied to the buffer address 32 * NumberOfReceivedFrames. The maximum number of data bytes allowed per frame is limited to 28.

All bytes in the buffer between the payload and the status byte are uninitialized and therefore invalid. The firmware on the host shall not use these bytes. The last word of the sub buffer (position 28 to 31) contains a status word. The status word contains the number of received bytes (may vary from the FeliCa length in case of an error), the CLError flag indicating any error in the reception (which is a combination of 3 individual error flags DATA_INTEGRITY_ERROR || PROTOCOL_ERROR || COLLISION_DETECTED) the individual error flags and the LenError flag indicating an incorrect length byte (either length byte is greater than 28 or the number of received bytes is shorter than indicated by the length byte). All unused bits (RFU) are masked to 0.

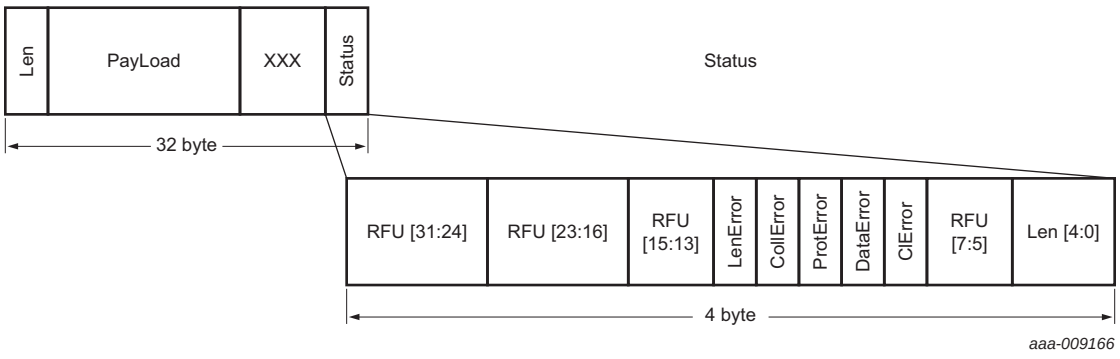

Fig 14. RxMultiple data format

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There are 4 different cases possible for a reception:

1. Correct reception - Data integrity is correct (no CRC error), and additionally the number of bytes received is equal to the length byte. Data is written to the buffer. No error set in status byte.

2. Erroneous reception - Data is incorrect (data integrity error - CRC wrong) but frame length is correct. Data is written to buffer and the bits CLError and DataError in the status byte are set.

3. Erroneous reception - the length byte received indicates a frame length greater than 28. No data is copied to buffer but status byte with LenError bit set is written.

4. Erroneous reception - the length byte is larger than the number of data bytes, which have been received. Data received is written to buffer and the ProtocolError bit in the status byte is set.

For each reception the RX_IRQ in the IRQ_STATUS_REG is set. The host firmware can disable the IRQ and use a timer for time-out after the last timeslot to avoid excessive interaction with the hardware. At the end of the reception additionally the bit field RX_NUM_FRAMES_RECEIVED in the register RX_STATUS_REG is updated to indicate the number of received frames.

After the reception of the eight frame (which is the maximum supported) a state change to next expected state is executed (WaitTransmit for transceive command). It is possible to issue the IDLE command in order to leave the RxMultiple cycle. Consequently the reception is stopped. Upon start of a new reception cycle the flag RX_NUM_FRAMES_RECEIVED is cleared.

The duration between deactivate and reactivate is at minimum 2 RF cycles and can last typically up to 2 μs.

10.8.1.4 ISO/IEC15693 functionality

The physical parameters are described below.

Table 54. Communication for ISO/IEC 15693 reader/writer “reader to card”

Communication direction	Signal type	Transfer speed
		f_c/512 kbit/s
Reader to card (send data from the PN5180 to a card)	reader side modulation	10 % to 30 % ASK 90 % to 100 % ASK
	bit encoding	1/4
	bit length	302.08 μs

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Table 55. Communication for ISO/IEC 15693 reader/writer “card to reader”

Communication direction	Signal type	Transfer speed			
		6.62 kbit/s	13.24 kbit/s	26.48 kbit/s	52.96 kbit/s[1]
Card to reader (PN5180 receives data from a card) f_c = 13.56 MHz	card side modulation	not supported	not supported	single subcarrier load modulation ASK	single subcarrier load modulation ASK
	bit length (µs)	-	-	37.76 (3.746)	18.88
	bit encoding	-	-	Manchester coding	Manchester coding
	subcarrier frequency [MHz]	-	-	$f_c/32$	$f_c/32$

[1] Fast inventory (page) read command only (ICODE proprietary command).

10.8.1.5 ISO/IEC18000-3 Mode 3 functionality

The ISO/IEC 18000-3 mode 3 is not described in this document. For a detailed explanation of the protocol, refer to the ISO/IEC 18000-3 standard.

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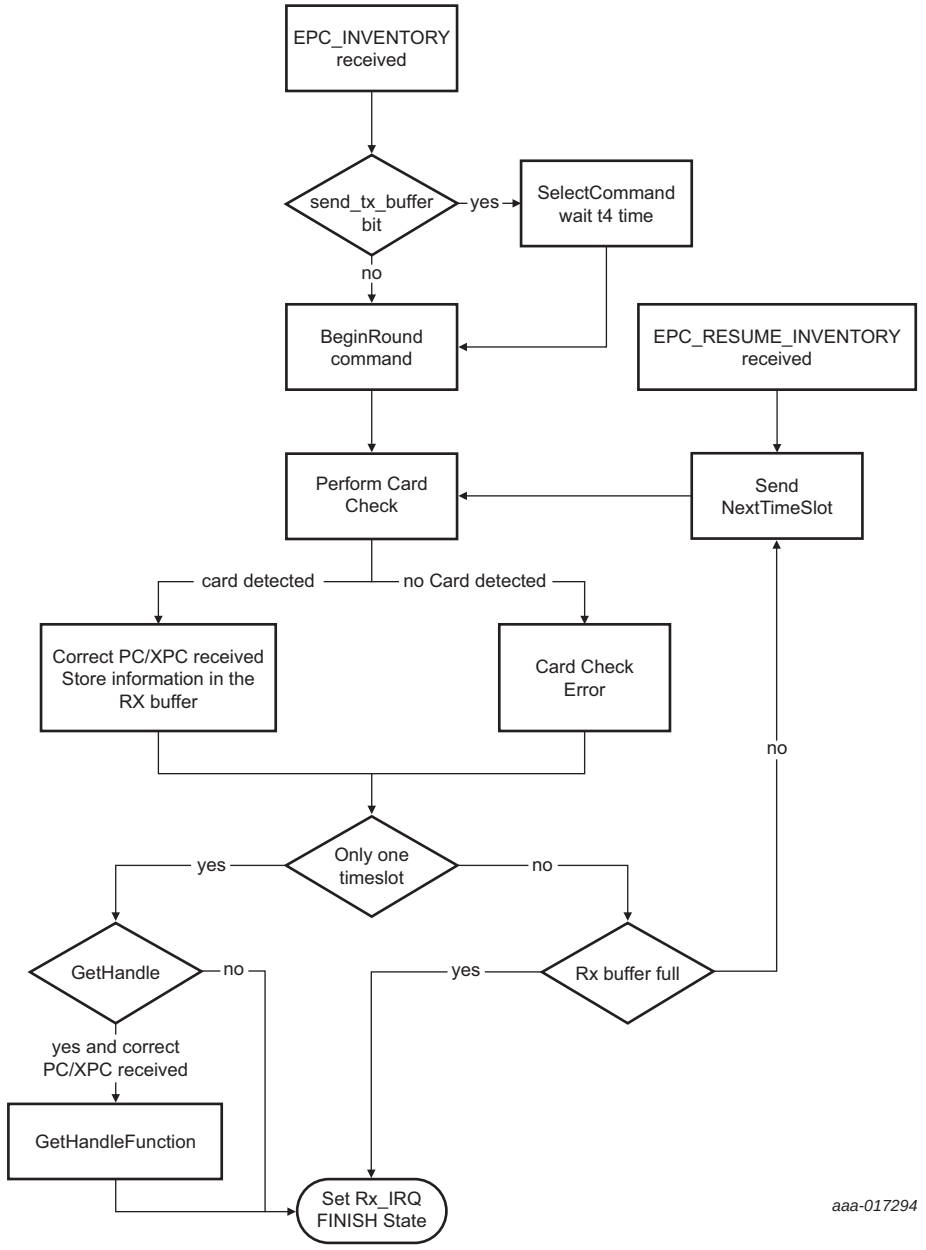

Fig 15. EPC GEN2 Inventory command

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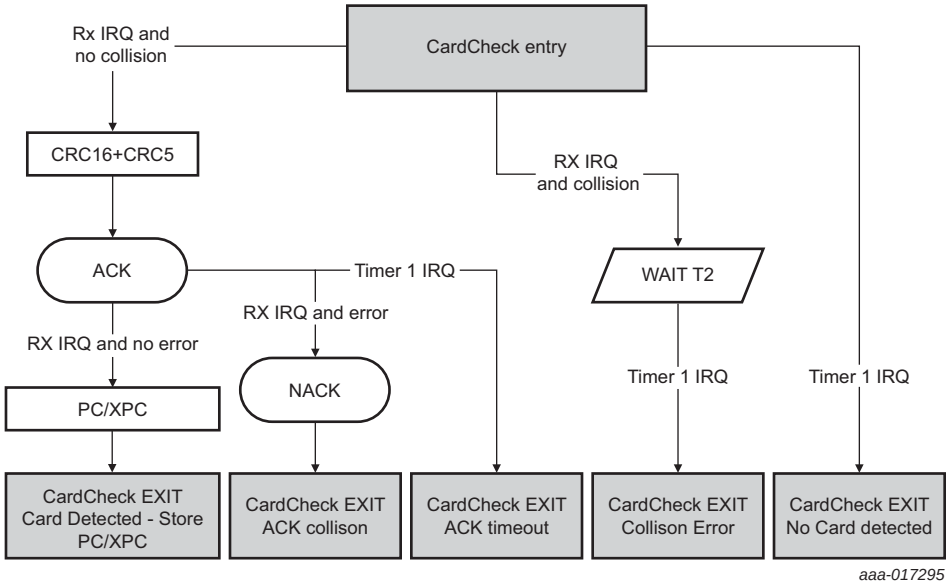

Fig 16. EPC_GEN2 Card presence check

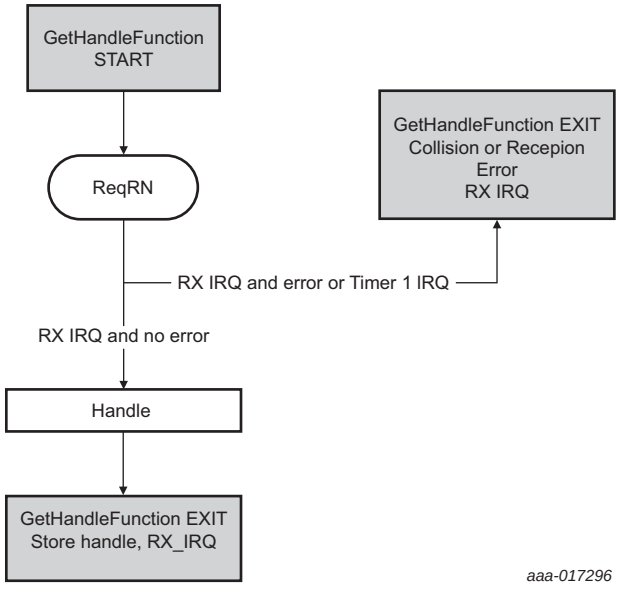

Fig 17. Get Handle

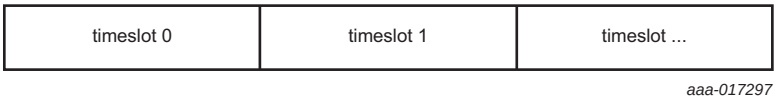

Fig 18. Timeslot order EPC Gen2

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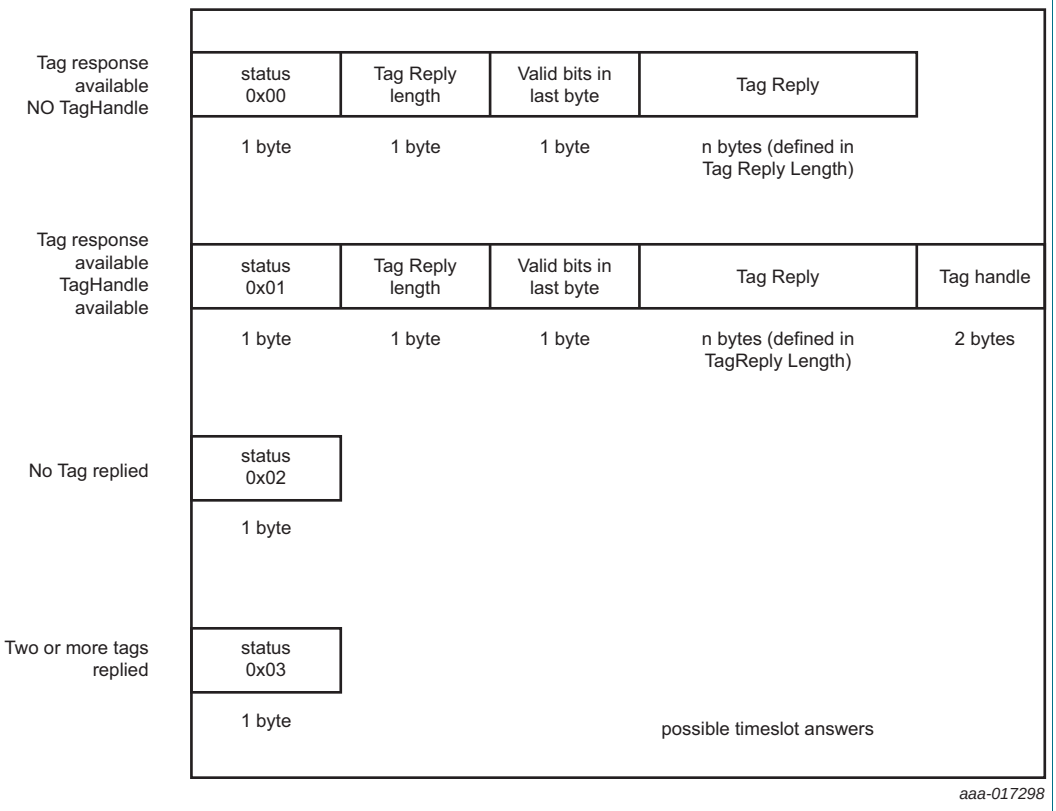

Fig 19. EPC GEN2 possible timeslot answers

10.8.1.6 NFCIP-1 modes

Overview: The NFCIP-1 communication differentiates between an Active and a Passive Communication Mode.

- Active Communication mode means both the initiator and the target are using their own RF field to transmit data.
- Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field.
- Initiator: Generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
- Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self-generated and self-modulated RF field for Active Communication mode.

In order to fully support the NFCIP-1 standard the PN5180 supports the Active and Passive Communication mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard.

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Active communication mode : Active communication mode means both the initiator and the target are using their own RF field to transmit data.

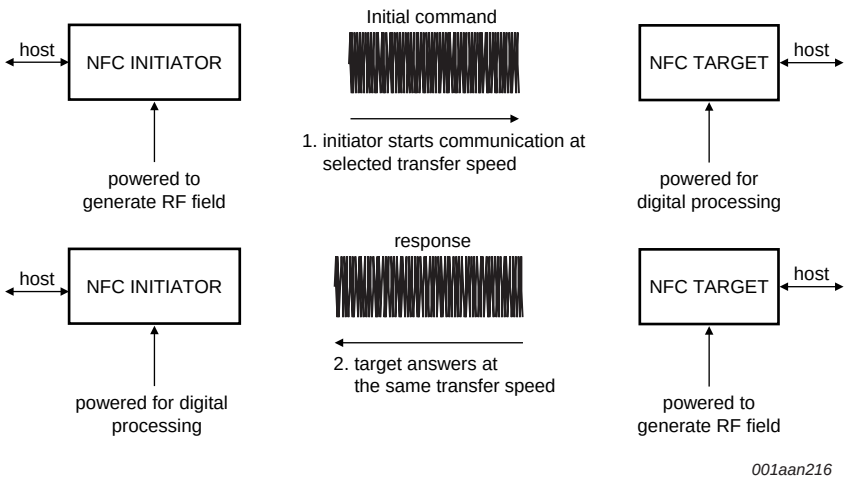

Fig 20. Active communication mode

Table 56. Communication overview for active communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s
Initiator → Target	According to ISO/IEC 14443 A 100 % ASK, modified Miller Coded	According to FeliCa, 8 % to 30 % ASK Manchester Coded	
Target → Initiator			

A dedicated host controller firmware is required to handle the NFCIP-1 protocol.

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Passive communication mode: Passive communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active (powered) to generate the RF field.

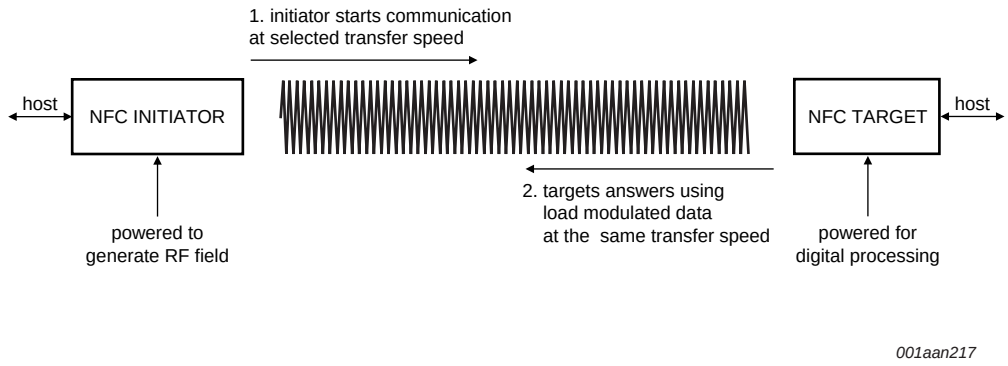

Fig 21. Passive communication mode

Table 57. Communication overview for passive communication mode

Communication direction	106 kbit/s	212 kbit/s	424 kbit/s
Initiator → Target	According to ISO/IEC 14443 A 100 % ASK, Modified Miller Coded	According to FeliCa, 8 % to 30 % ASK Manchester Coded	
Target → Initiator	According to ISO/IEC 14443 A @106 kbit modified Miller Coded	According to FeliCa, > 12 % ASK Manchester Coded	

A dedicated host controller firmware is required to handle the NFCIP-1 protocol.

Note: Transfer Speeds above 424 kbit/s are not defined in the NFCIP-1 standard.

NFCIP-1 protocol support: The NFCIP-1 protocol is not completely described in this document. The PN5180 does not implement any of the high-level protocol functions. These higher-level protocol functions need to be provided by the host. For detailed explanation of the protocol refer to the NFCIP-1 standard. However the datalink layer is according to the following policy:

- Speed shall not be changed while continuous data exchange in a transaction.
- Transaction includes initialization, anticollision methods and data exchange (in continuous way, meaning no interruption by another transaction).

In order not to disturb current infrastructure based on 13.56 MHz, the following general rules to start an NFCIP-1 communication are defined:

1. Per default an NFCIP-1 device is in Target mode - meaning its RF field is switched off.
2. The RF level detector is active.
3. Only if it is required by the application the NFCIP-1 device shall switch to Initiator mode.

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4. An initiator shall only switch on its RF field if no external RF field is detected by the RF Level detector during a time of T_{IDT}.
5. The initiator performs initialization according to the selected mode.

10.8.1.7 ISO/IEC14443 A Card operation mode

PN5180 can be configured to act as an ISO/IEC 14443 A compliant card.

This means that PN5180 can generate an answer in a load modulation scheme according to the ISO/IEC 14443 A interface description.

Note: PN5180 does not support a complete card protocol. This has to be handled by a connected host controller. Nevertheless, the layer3 type A activation is handled by the NFC frontend. The Card Activated IRQ shall be enabled and notifies if a card activation had been successfully performed.

The supports ISO/IEC14443 A card mode for data rates 106, 212, 424 and 848 kbit/s.

10.8.1.8 NFC Configuration

The NFC protocol for the 106 kbps mode defines an additional Sync-Byte (0xF0 + parity) after the normal start bit had been transmitted. As this Sync-Byte includes a parity bit, it can be handled by a host firmware as a normal data byte.

10.8.1.9 Mode Detector

The Mode Detector is a functional block of the PN5180in PICC mode which senses for an RF field generated by another device. The mode detector allows to distinguish between type A and FeliCa target mode. Dependent on the recognized protocol generated by an initiator peer device the host is able to react. Note that the PN5180 is able to emulate type A cards and peer to peer active target modes according to ISO/IEC18092.

10.8.2 RF-field handling

The NFC frontend supports generation of a RF-field dependent on external conditions like presence of another NFC device generating an RF field. A flexible mechanism to control the RF field is available.

After power-up, the RF-field is off.

The instruction RF_ON enables the generation of a RF-field. The NFC frontend can perform an initial RF collision avoidance according to ISO/IEC18092. Before enabling the RF-field, a field detection is automatically enabled for the period TIDT. In case an external field is detected, the field is not switched on and an RF_ACTIVE_ERROR_IRQ is raised. The cause for the error can be examined in the RF_STATUS_REG.

In order to switch off the RF-field generation, the RF_OFF instruction needs to be sent.

Active Mode is supported by configuring the RF_ON instruction.

10.8.3 Transmitter TX

The transmitter is able to drive an antenna circuit connected to outputs TX1 and TX2 with a 13.56 MHz carrier signal. The signal delivered on pins TX1 and pin TX2 is the 13.56 MHz carrier modulated by an envelope signal for energy and data transmission. It can be used to drive an antenna directly, using a few passive components for matching and filtering. For a differential antenna configuration either TX1 or TX2 can be configured

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to put out an inverted clock. 100 % modulation and several levels of amplitude modulation on the carrier can be performed to support 13.56 MHz carrier-based RF-reader/writer protocols as defined by standards ISO/IEC14443 A and B, FeliCa and ISO/IEC18092.

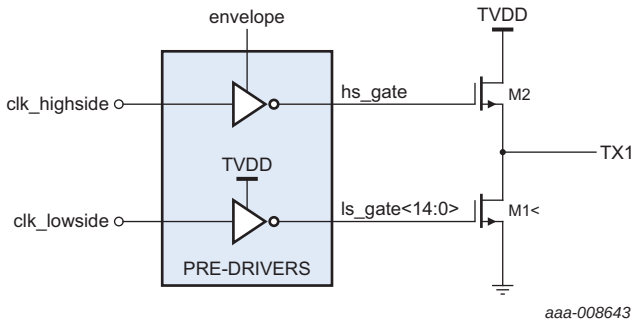

Fig 22. PN5180 Output driver

10.8.3.1 100 % Modulation

There are 5 choices for the output stage behavior during 100 % modulation, and one setting for 10 % modulation. This is controlled by TX_CLK_MODE_RM in RF_CONTROL_TX_CLK:

Table 58. Settings for TX1 and TX2

TX_CLK_MODE_RM (binary)	Tx1 and TX2 output	Remarks
000	High impedance	-
001	0	output pulled to 0 in any case
010	1	output pulled to 1 in any case
110	RF high side push	Open-drain, only high side (push) MOS supplied with clock, clock polarity defined by TX2_INV_RM; low side MOS is off
101	RF low side pull	Open-drain, only low side (pull) MOS supplied with clock, clock polarity defined by TX1_INV_RM; high side MOS is off
111	13.56 MHz clock derived from 27.12 MHz quartz divided by 2	push/pull Operation, clock polarity defined by invtx; setting for 10 % modulation

With the options “RF high side push” and “RF low side push” potentially faster fall times can be achieved for the antenna voltage amplitude at the beginning of a modulation. This basic behavior during modulation cannot be configured independently for TX1 and TX2. Only the clock polarity can be configured separately with TX1_INV_RM and TX2_INV_RM.

10.8.3.2 10 % Amplitude Modulation

For a targeted ASK 10 % amplitude modulation the bits RF_CONTROL_TX_CLK in register TX_CLK_MODE_RM need to be set to value 0b111. Then the signal envelope does not influence the clock behavior thus resulting in an ASK modulation to a modulation index as defined by RF_CONTROL_TX in the bits TX_RESIDUAL_CARRIER. The residual carrier setting is used to adjust the modulation degree at the TX output. A control loop is implemented to keep the modulation degree as constant as possible.

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The settings and resulting typical residual carrier and modulation degree is given in table below:

Table 59. Modulation degree configuration

TX_RESIDUAL_CARRIER register setting	residual carrier nominal	modulation degree nominal
0	100	0
1	98	1.01
2	96	2.04
3	94	3.09
4	91	4.71
5	89	5.82
6	87	6.95
7	86	7.53
8	85	8.11
9	84	8.7
10	83	9.29
11	82	9.89
12	81	10.5
13	80	11.11
14	79	11.73
15	78	12.36
16	77	12.99
17	76	13.64
18	75	14.29
19	74	14.94
20	72	16.28
21	70	17.65
22	68	19.05
23	65	21.21
24	60	25
25	55	29.03
26	45	37.93
27	40	42.86
28	35	48.15
29	30	53.85
30	25	60
31	0	100

10.8.3.3 TX Wait

The guard time tx_wait is started after the end of a reception, no matter if the frame is correct or erroneous. The tx_wait guard time counter is not started in case the reception is restarted because of an EMD-event or in case the RX_MULTIPLE_ENABLE bit is set to 1.

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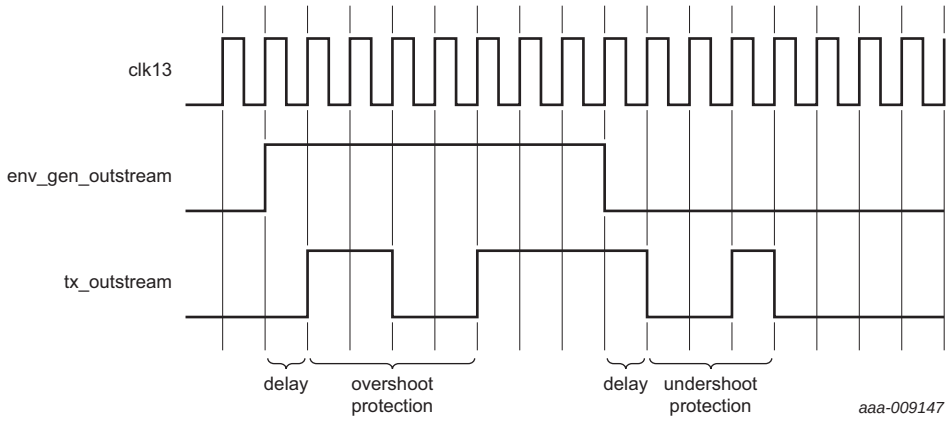
In case the register flag TX_WAIT_RFON_ENABLE is set to 1 the guard time counter is started when the devices own RF-Field is switched on.

To start a transmission, it is always necessary for the firmware to set the START_SEND bit in the SYSTEM_CONFIG register or sending the instruction SEND_DATA. Having said that it is possible to disable the guard time tx_wait by setting the register TX_WAIT_CONFIG to 00h.

Tx_wait can be used for 2 different purposes: On the one hand, it can be used to prevent start of transmission before a certain period has expired - even if FW already finished data processing and set the START_SEND bit. This behavior is mainly intended for reader mode to guaranteed PICC to PCD frame delay time (FDT).

On the other hand, the tx_wait time can be used to start the transmission at an exactly defined time. For this purpose data to be sent must be available and the START_SEND flag has to be set by FW before the period expires. In case the START_SEND bit is not set when tx_wait expires and MILLER_SYNC_ENABLE is set the transmission will be started on the bit-grid.

10.8.3.4 Over- and Undershoot prevention



Example with overshoot pattern ‘1100’ (binary) with a length of four and undershoot pattern ‘001’ (binary) with a length of three.

Fig 23. Overshoot/Undershoot prevention

The over- and undershoot protection allows to configure additional signals on the Transmitter output which allows to control the signal shaping of the antenna output.

The registers TX_OVERSHOOT_CONFIG_REG and TX_UNDERSHOOT_CONFIG_REG are used to configure the over-and undershoot protection. Additionally, in register RF_CONTROL_TX_CLK (bit TX_CLK_MODE_OVUN_PREV) it is defined which TX clock mode for the period the overshoot/undershoot prevention is active, and RF_CONTROL_TX (bit TX_RESIDUAL_CARRIER_OV_PREV) defines the value for the residual carrier for the period the overshoot prevention pattern is active.

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10.8.4 Dynamic Power Control (DPC)

The Dynamic Power Control allows to adjust the RF output current dependent on the loading condition of the antenna.

A lookup table is used to configure the output voltage and by this control the transmitter current. In addition to the control of the transmitter current, wave shaping settings can be controlled as well dependent on the selected protocol and the measured antenna load.

The PN5180 allows to measure periodically the RX voltage. The RX voltage is used as indicator for the actual antenna current. The voltage measurement is done with the help of the AGC. The time interval between two measurements can be configured with the OC_TIME byte in the EEPROM.

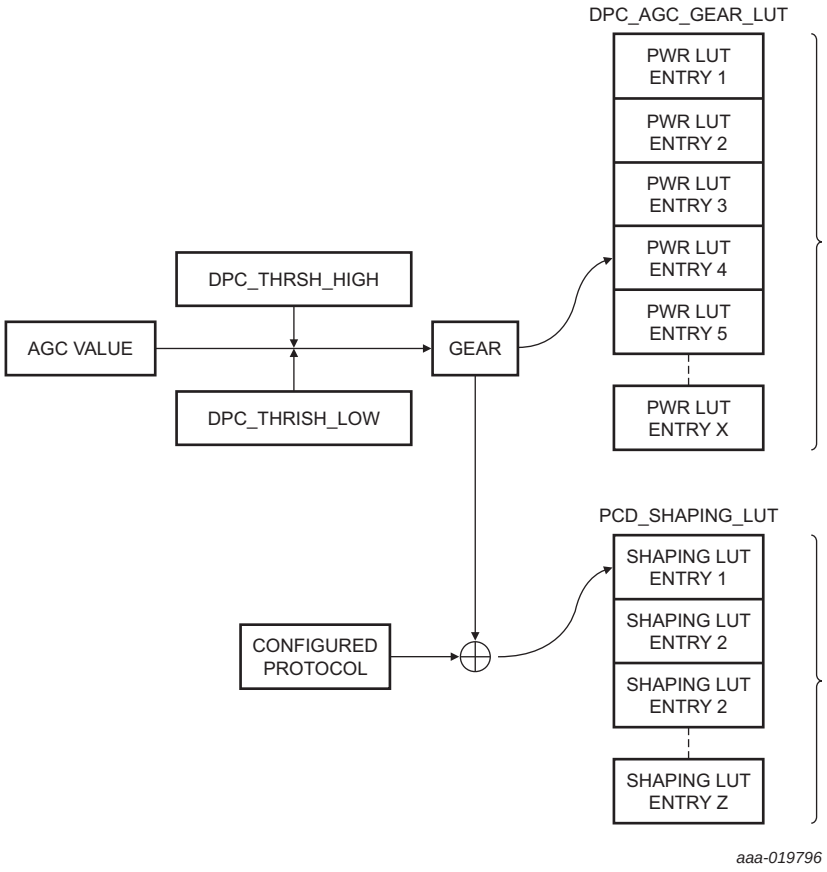

Fig 24. Lookup tables for AGC value dependent dynamic configuration

The AGC value is compared to a maximum and minimum threshold value which is stored in EEPROM.

If the AGC value is exceeding one of the thresholds, a new gear configuring another transmitter supply driver voltage will be activated. The number of gears - and by these transmitter supply voltage configurations - can be defined by the application, up to 15 gears are available.

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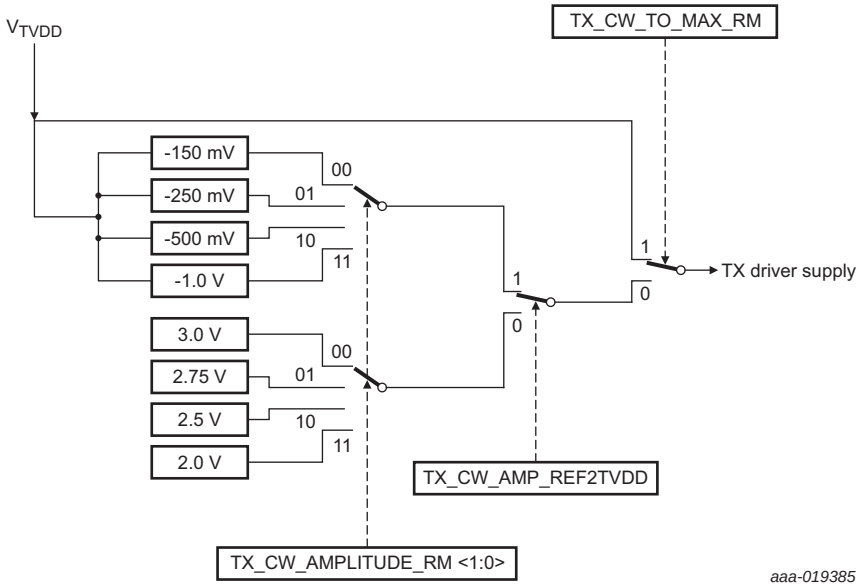

Fig 25. Transmitter supply voltage configuration, $V_{DD(TVDD)}$ > 3.5 V

10.8.5 Adaptive Waveform Control (AWC)

Depending on the level of detected detuning of the antenna, RF wave shaping related register settings can be automatically updated. The shaping related register settings are stored in a lookup table located in EEPROM, and selected dependent on the actual gear. The gear numbers need to be provided as part of the of the lookup table entries and need to be provided in ascending order in the EEPROM. Each lookup table entry allows to configure not only a dedicated wave shaping configuration for the corresponding gear, but in additionally it is possible to configure for this gear the wave shaping configuration dependent on the different protocols.

Each lookup table item contains a bitmask of technology and baudrate (in order to use an entry for multiple technologies and baudrates), the DPC Gear and a relative value (change compared to actual setting of register RF_CONTROL_TX) for TAU_MODE_FALLING, TAU_MODE_RISING and TX_RESIDUAL_CARRIER.

Table 60. Wave shaping lookup table

Bit position	Function of each DWORD
29:31	RFU
16:28	Bitmask identifying technology and baudrate

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Table 60. Wave shaping lookup table

Bit position	Function of each DWORD	
	0001h	A 106
	0002h	A 212
	0004h	A 424
	0008h	A 848
	0010h	B 106
	0020h	B 212
	0040h	B 424
	0080h	B 848
	0100h	F 212
	0200h	F424
	0400h	15693 ASK10
	0800h	15693 ASK100
	1000h	ISO 180003m3
12_15	RESIDUAL_CARRIER (Sign bit + 3-bit value) 0: Add value to current residual carrier configuration, 1; subtract value from current residual carrier configuration	
8:11	TAU_MOD_RISING (Sign bit + 3-bit value) 0: Add value to current TAU_MOD_RISING configuration, 1; subtract value from current TAU_MOD_RISING configuration	
4:7	TAU_MOD_FALLING (Sign bit + 3-bit value) 0: Add value to current TAU_MOD_FALLING configuration, 1; subtract value from current TAU_MOD_FALLING configuration	
0:3	DPC Gear	

In case of a gear switch, a EEPROM lookup is performed if the current gear (at current protocol and baudrate) has an assigned wave shaping configuration. In case of an execution of a LoadProtocol command, this lookup will be performed (example: switching from baudrate A106 to A424) as well. The change from the wave shaping configuration as configured by LOAD_RF_CONFIG is relative, which means that bits are added or subtracted from the existing configuration. For an increasing gear value, the defined change is cumulative.

10.8.6 Transceive state machine

The transceive command allows to transmit and the following expected receive data with a single command.

The transceive state machine is used to trigger the reception and transmission of the RF data dependent on the conditions of the interface.

The state machine for the command transceive is started when the SYSTEM_CONFIG command is set to transceive. The transceive command does not terminate automatically. In case of an error the host can stop the transceive state machine by setting the SYSTEM_CONFIG.command to IDLE.

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START_SEND can either be triggered by writing to the SYSTEM_CONFIG register start_send or by using the command SET_INSTR_SEND_DATA.

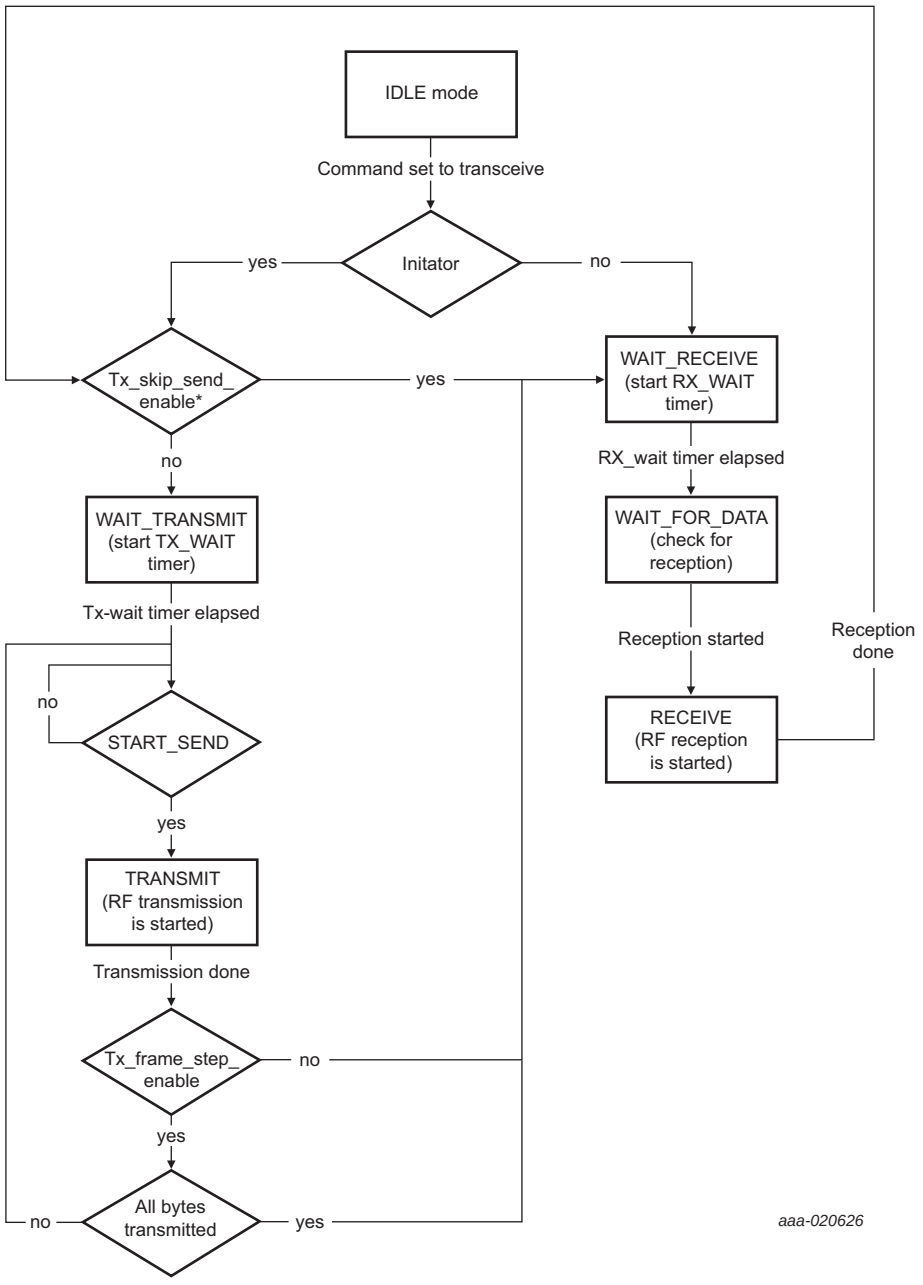

Fig 26. Transceive state machine

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10.8.7 Autocoll

The Autocoll state machine performs the time critical activation for Type-A PICC and for NFC-Forum Active and Passive Target activation.

The PICC state machine supports three configurations:

- Autocoll mode0: Autocoll mode is left when no RF field is present
- Autocoll mode1: Autocoll mode is left when one technology is activated by an external reader. During RFoff the chip enters standby mode automatically
- Autocoll mode2: Autocoll mode is left when one technology is activated by an external reader. During RFoff the chip does not enter standby mode.

At start-up the Autocoll state machine automatically performs a LOAD_RF_CONFIG with the General Target Mode Settings. When a technology is detected during activation the Autocoll state machine performs an additional LOAD_RF_CONFIG with the corresponding technology.

The card configuration for the activation is stored in EEPROM. If RandomUID is enabled, a random UID is generated after each RFoff.

For all active target modes, the own RF field is automatically switched on after the initiator has switched off its own filed.

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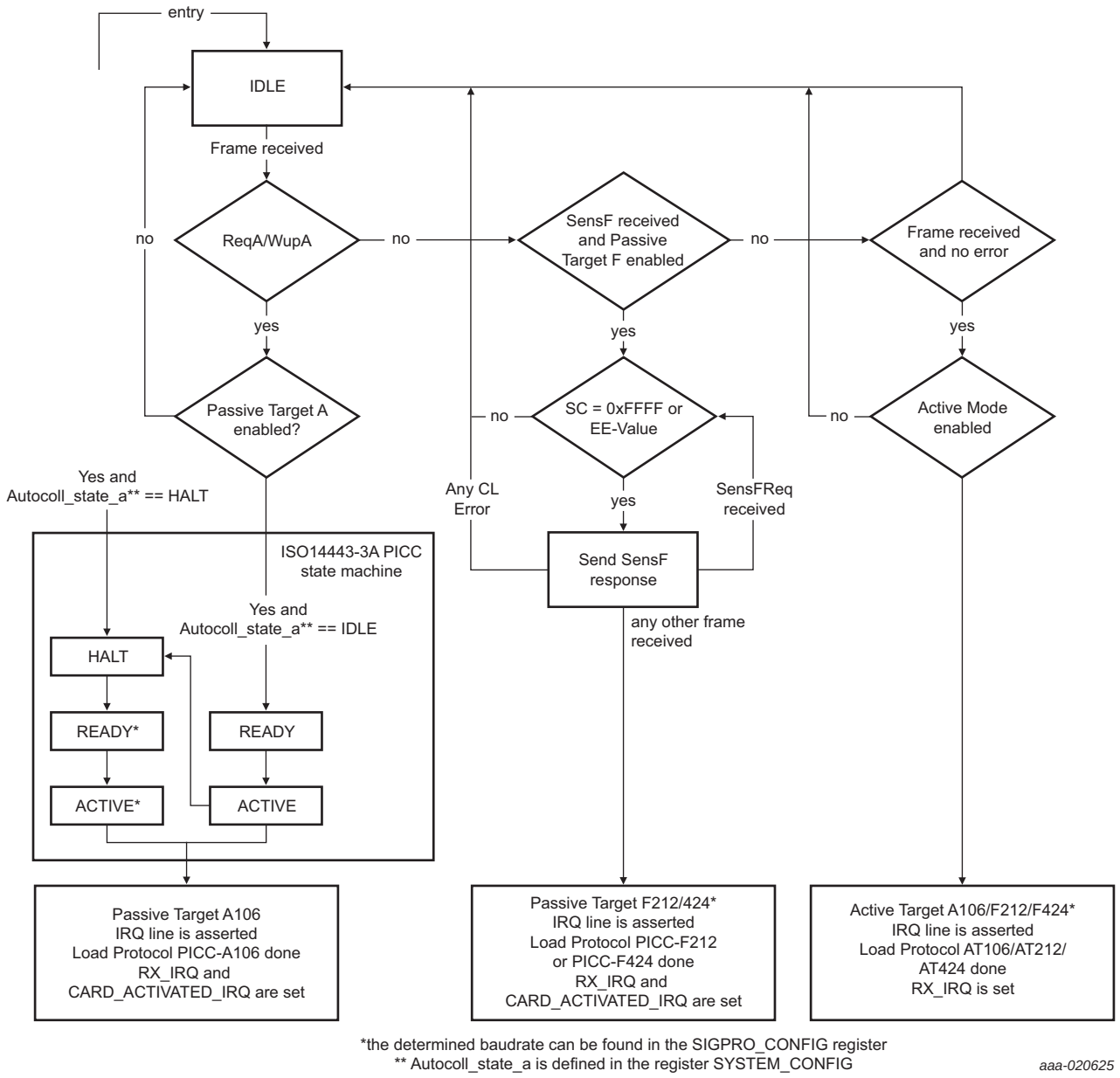

Fig 27. Autocall state machine

10.8.8 Receiver RX

10.8.8.1 Reader Mode Receiver

In Reader Mode the response of the PICC device is coupled from the PCB antenna to the differential input RXP/RXN. The Reader Mode Receiver extracts this signal by first removing the carrier in passive mixers (direct conversion for I and Q), then filtering and amplifying the baseband signal, and finally converting to digital values with 2 separate ADC's for I and Q channel. Both the I and Q channels have a differential structure which improves the signal quality.

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The I/Q-Mixer mixes the differential input RF-signal down to the baseband. The mixer has a band with of 2 MHz.

The down mixed differential RX input signals are passed to the BBA and band-pass filtered. In order to consider all the various protocols (Type A/B, FeliCa), the high-pass cut-off frequency of BBA can be configured between 45 kHz and 250 kHz in 4 different steps. The low-pass cut-off frequency is above 2 MHz.

This band-passed signal is then further amplified with a gain factor which is configurable between 30 dB and 60 dB. The baseband amplifier (BBA)/ADC I- and Q- channel can be enabled separately. This is required for ADC-based CardMode functionality as only the I-channel is used in this case.

The gain and high pass corner frequency of the BBA are not independent from each other:

Table 61.

Gain setting	hpcf setting	HPCF (kHz)	LPCF (MHz)	Gain(sB20)	Band width (MHz)
Gain3					
	0	39	3.1	60	3.1
	1	78	3.2	59	3.1
	2	144	3.5	58	3.3
	3	260	4.1	56	3.8
Gain2					
	0	42	3.1	51	3.1
	1	82	3.3	51	3.2
	2	150	3.7	49	3.5
	3	271	4.3	47	4.0
Gain1					
	0	41	3.7	43	3.7
	1	82	4.0	42	3.9
	2	151	4.5	41	4.3
	3	276	5.5	39	5.2
Gain0					
	0	42	3.8	35	3.8
	1	84	4.1	34	4.0
	2	154	4.7	33	4.5
	3	281	5.7	31	5.4

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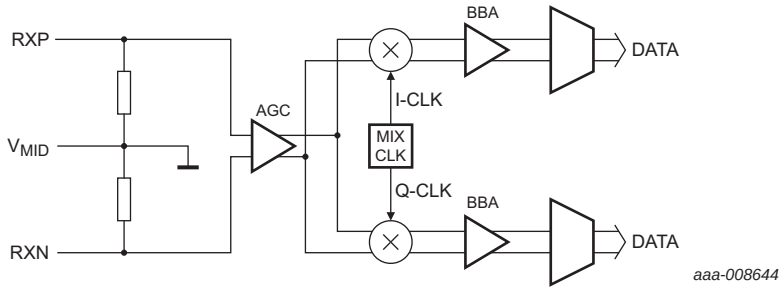

Fig 28. PN5180 Receiver Block diagram

10.8.8.2 VMID

The input voltage for PIN Vmid is generated by a resistive divider between AVDD and GND. The resistive divider is connected to the VMID pin, an external blocking capacitor shall be placed there.

10.8.8.3 Automatic Gain Control

The Automatic Gain Control (AGC) of the receiver is used to control the amplitude of the received 13.56 MHz input sine-wave signal from the antenna (input pins RXP and RXN).

It is desirable to achieve an input voltage in the range of 1.5 V to 1.65 V at the pins RXP, RXN. For symmetric antennas, the voltage levels are the same on the pins RXP, RXN. A voltage lower than 1.5 V lead to a low sensitivity of the receiver, a voltage level higher than 1.65 V could result in clipping of the received signal. Both conditions should be avoided for optimum performance of the IC. An antenna detuning of a card result in an RX input level which is outside of the desired input voltage range. Here the AGC helps to simplify the design and to keep the RX voltage as stable as possible even under dynamic changing antenna detuning conditions.

Functional description:

The peak of the input signal at RXP is regulated to be equal to a reference voltage (internally generated from the supply using a resistive divider). Two external resistors are connected to the RX inputs, the specific value of these resistors in a given design depends on the selected antenna and needs to be determined during development. This external resistor, together with an on-chip variable resistor connected to VMID, forms a resistive voltage divider for the signal processor input voltage. The resolution of the variable resistor is 10 bits.

By varying the on-chip resistor, the amplitude of the input signal can be modified. The on-chip resistor value is increased or decreased depending on the output of the sampled comparator, until the peak of the input signal matches the reference voltage. The amplitude of the RX input is thus automatically controlled by the AGC circuit.

The internal amplitude controlling resistor in the AGC has a default value of 10 kOhm typ DC coupled. (i.e. when the resistor control bits in AGC_VALUE_REG <9:0> are all 0, the resistance is 10 k). As the control bits are increased, resistors are switched in parallel to the 10k resistor thus lowering the combined resulting resistance value down to 20 OhmDC coupled (AGC_VALUE_REG <9:0>, all bits set to 1).

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10.8.8.4 RX Wait

The guard time rx_wait is started after the end of a transmission. If the register flag RX_WAIT_RFON_ENABLE is set to 1 the guard time is started when the devices did switch off its own RF-Field and an external RF-Field was detected.

The guard time rx_wait can be disabled by setting the register RX_WAIT_VALUE to 00h meaning the receiver is immediately enabled.

10.8.8.5 EMD Error handling

EMVCo

The PN5180 supports EMD handling according to the EMVCo standard. To support further extension the EMD block is configurable to allow adoption for further standard updates.

The PN5180 supports automatically restart of the receiver and CLIF timer1 is restarted in case of an EMD event. The CLIF timer is selectable in the EMD_CONTROL register.

An EMD event is generated:

- Independent of received number of bytes
- Any Residual bits and EMD_CONTROL.emd_transmission_error_above_noise = 0
- When the received number of bytes without CRC is <= EMD_CONTROL.emd_noise_bytes_threshold
- Independent of received number of bytes
- Any Residual bits and EMD_CONTROL.emd_transmission_error_above_noise = 0
- When the received number of bytes without CRC is <= EMD_CONTROL.emd_noise_bytes_threshold
- Missing CRC (1 byte frame) when EMD_CONTROL.emd_missing_crc_is_protocol_error_type_X = 0

10.8.9 Low-Power Card Detection (LPCD)

The low-power card detection is an energy saving configuration option for the PN5180.

A low frequency oscillator (LFO) is implemented to drive a wake-up counter, waking-up PN5180 from standby mode. This allows implementation of low-power card detection polling loop at application level.

The SWITCH_MODE instruction allows to enter the LPCD mode with a given standby duration value.

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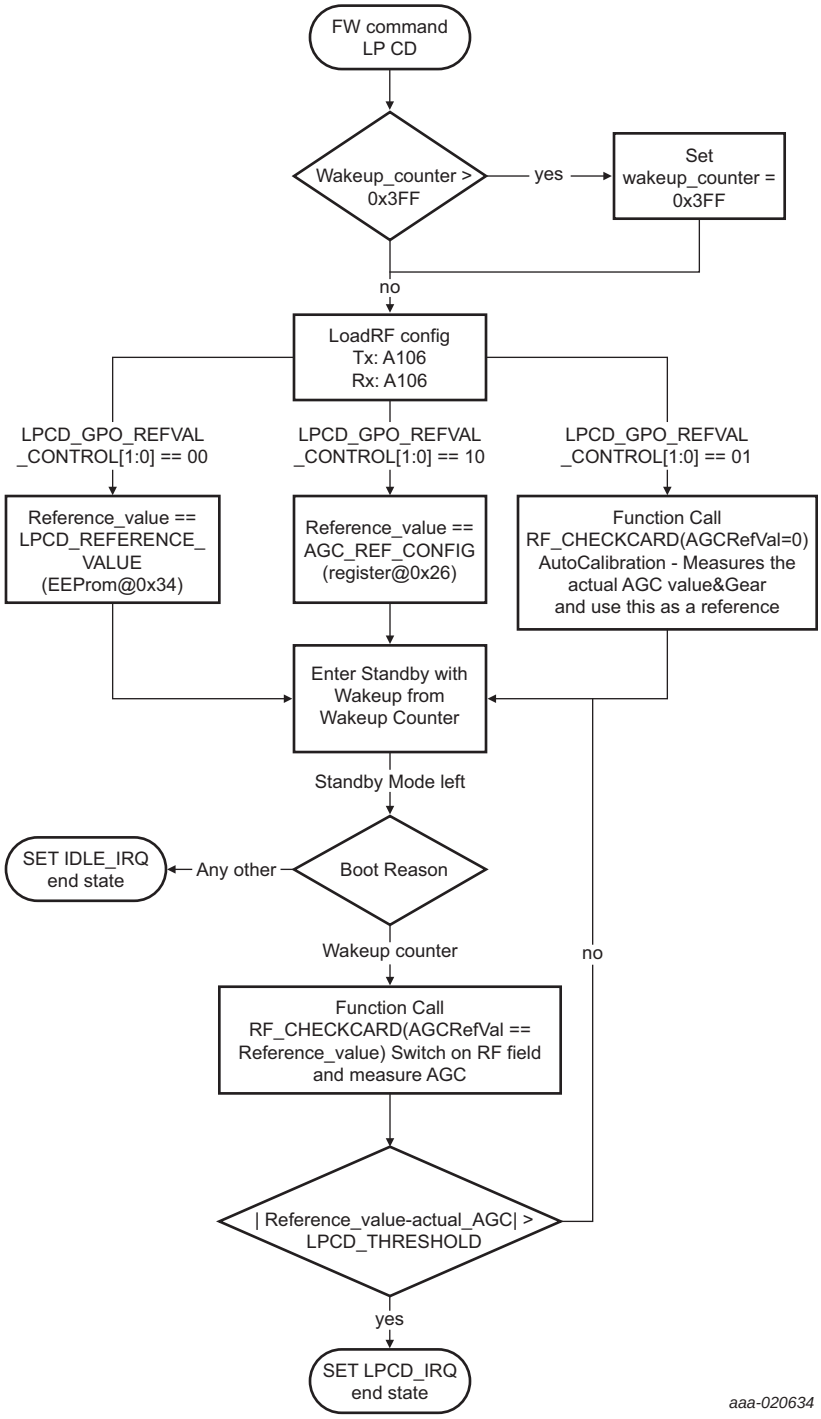

Fig 29. LPCD configuration

Before entering the LPCD mode, an LPCD reference value needs to be determined. Three options do exist for generating this reference value.

The LPCD works in two phases:

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First the standby phase is controlled by the wake-up counter (timing defined in the instruction), which defines the duration of the standby of the PN5180.

Second phase is the detection-phase. The RF field is switched on for a defined time (EEPROM configuration) and then the AGC value is compared to a reference value.

- If the AGC value exceeds the reference value, a LPCD_IRQ is raised to the host. The register configurations done by the host are not restored after wake-up. command. The host has to configure the NFC frontend for a dedicated protocol operation to allow a polling for a card.
- If the AGC value does not exceed the limit of the reference value, no LPC_IRQ is raised and the IC is set to the first phase (standby mode) again.

As an additional feature the GPO1 (general-purpose output) pin can be toggled to wake-up an external LDO from power down for the TVDD supply. The GPO1 allows to be toggled before the transmitter is switched on. This allows the wake-up of an external LDO from power down. The GPO1 can be toggled after the RF field is switched off to set an external LDO into power down. The time of toggling the GPO in relation to the RF-on and RF-off timings can be configured.

These two phases are executed in a loop until

1. Card / metal is detected (LPCD_IRQ is raised).
2. Reset occurs, which will reset all the system configurations. The LPCD is also stopped in this case.
3. NSS on Host IF
4. RF Level Detected

The behavior of the generated field is different dependent on the activation state of the DPC function:

- If the DPC feature is not active, the ISO/IEC14443 type A 106 kbit/s settings are used during the sensing time.
- If the DPC is active, the RF_ON command is executed. The RF field is switched on as soon as the timer configured by the SWITCH_MODE command elapses. The RF field is switched on for a duration as defined for an activated DPC. The timer for the LPCD_FIELD_ON_TIME starts to count as soon as the RF_ON command terminates.

Table 62. Low Power Card Detection: EEPROM configuration

EEPROM address	Name	Description
0x34	LPCD_REFERENCE_VALUE	2 byte: bit 9:0 AGC reference value; bit 13:10 AGC gear
0x36	LPCD_FIELD_ON_TIME	1 byte: Defines the RF-ON time for the AGC measurement. The minimum RF-ON time depends on the antenna configuration and the connected matching network. It needs to be chosen in such a way that a stable condition for the AGC measurement is given at the end of the time. The byte defines the delay multiplied by 8 in microseconds.
0x37	LPCD_THRESHOLD	1 byte: Defines the AGC threshold value. This value is used to compare against the current AGC value during the low-power card detection phase. if the difference between AGC reference value and current AGC value is greater than LPCD_THRESHOLD, the IC wakes up from LPCD.

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Table 62. Low Power Card Detection: EEPROM configuration

EEPROM address	Name	Description
0x38	LPCD_REFVAL_CONTROL	LPCD Reference Value Selection and GPO control BitField Description [1:0] 00 ...Use EEPROM Value for reference value 01 ...Use one AGC measurement to get reference value 10 ...Use AGC Reference value and AGC gear from the register AGC_REG_CONFIG. 11 ...RFU 2 0... Disable Control for external TVDD LDO via GPIO1 1... Enable Control for external TVDD LDO via GPIO1
0x39	LPCD_GPO_TOGGLE_BEFORE_FIELD_ON	1 byte: This value defines the time between setting GPO1 until field is switched on. The byte defines the time multiplied by 5 in microseconds.
0x3A	LPCD_GPO_TOGGLE_AFTER_FIELD_ON	1 byte: This value defines the time between field off and clearing GPO1. The byte defines the time multiplied by 5 in microseconds.

10.8.9.1 Check Card register

The Check Card register located at register 0x26 performs one LPCD cycle. This means that only the second phase - the detection phase is executed.

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10.9 Register overview

10.9.1 Register overview

Table 63. Register address overview

Address (HEX)	Address (decimal)	Name
0h	0	SYSTEM_CONFIG
1h	1	IRQ_ENABLE
2h	2	IRQ_STATUS
3h	3	IRQ_SET_CLEAR
4h	4	TRANSCEIVER_CONFIG
5h	5	PADCONFIG_REG
6h	6	RFU
7h	7	PADOUT_REG
8h	8	TIMER0_STATUS
9h	9	TIMER1_STATUS
Ah	10	TIMER2_STATUS
Bh	11	TIMER0_RELOAD
Ch	12	TIMER1_RELOAD
Dh	13	TIMER2_RELOAD
Eh	14	TIMER0_CONFIG
Fh	15	TIMER1_CONFIG
10h	16	TIMER2_CONFIG
11h	17	RX_WAIT_CONFIG
12h	18	CRC_RX_CONFIG
13h	19	RX_STATUS
14h	20	TX_UNDERSHOOT_CONFIG
15h	21	TX_OVERSHOOT_CONFIG
16h	22	TX_DATA_MOD
17h	23	TX_WAIT_CONFIG
18h	24	TX_CONFIG
19h	25	CRC_TX_CONFIG
1Ah	26	SIGPRO_CONFIG
1Bh	27	SIGPRO_CM_CONFIG
1Ch	28	SIGPRO_RM_CONFIG
1Dh	29	RF_STATUS
1Eh	30	AGC_CONFIG
1Fh	31	AGC_VALUE
20h	32	RF_CONTROL_TX
21h	33	RF_CONTROL_TX_CLK
22h	34	RF_CONTROL_RX
23h	35	LD_CONTROL
24h	36	SYSTEM_STATUS
25h	37	TEMP_CONTROL

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Table 63. Register address overview *...continued*

Address (HEX)	Address (decimal)	Name
26h	38	CHECK_CARD_RESULT
27h	39	DPC_CONFIG
28h	40	EMD_CONTROL
29h-7Ah	38-127	RFU

10.9.2 Register description

Table 64. SYSTEM_CONFIG register (address 0000h) bit description

Bit	Symbol	Access	Value	Description
31:9	RFU	R	0*,1	Reserved
9	AUTOCOLL_PICC_STATE	R/W	0*,1	Defines the entry state of the PICC TypeA state machine when Autocoll mode is entered 0.
8	SOFT_RESET	W	0*,1	performs a reset of the device by writing a “1” into this register.
7	RFU	R/W	0*,1	RFU
6	MFC_CRYPTO_ON	R/W	0*,1	If set to 1, the mfc-crypto is enabled for end-/de-cryption
5	PRBS_TYPE	R/W	0*,1	Defines the PRBS type; If set to 1, PRBS15 is selected, default value 0 selects PRBS9
4	RFU	R/W	0*,1	RFU
3	START_SEND	R/W	0*,1	If set to 1, this will trigger the data transmission according to the transceive state machine
0:2	COMMAND	R/W	001*	These bits define the command for the transceive state machine:
			000	IDLE/StopCom Command; stops all ongoing communication and set the CLIF to IDLE mode
			001	RFU
			010	RFU
			011	Transceive command; initiates a transceive cycle. Note: Depending on the value of the Initiator bit a transmission is started or the receiver is enabled Note: The transceive command does not finish automatically. It stays in the transceive cycle until stopped via the IDLE/StopCom command
			100	KeepCommand command; This command does not change the content of the command register and might be used in case other bits in the register are to be changed
			101	LoopBack command; This command is for test purposes only. It starts a transmission and at the same time enables the receiver.
			110	RFU
			111	RFU

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Table 65. IRQ_ENABLE register (address 0001h) bit description

Bit	Symbol	Access	Value	Description
17	TEMPSENS_ERROR_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the TempSensor
16	RX_SC_DET_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the RX Subcarrier Detection
15	RX_SOF_DET_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the RX SOF Detection
14	RFU	R/W	0*, 1	-
13	TIMER2_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the Timer2
12	TIMER1_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the Timer1
11	TIMER0_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the Timer0
10	RF_ACTIVE_ERROR_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the RF active error
9	TX_RFON_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the RF Field ON in PCD
8	TX_RFOFF_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the RF Field OFF in PCD
7	RFON_DET_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the RF Field ON detection
6	RFOFF_DETQ_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the RF Field OFF detection
5	STATE_CHANGE_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the State Change in the transceive state machine
4	CARD_ACTIVATED_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin when PN5180 is activated as a Card
3	MODE_DETECTED_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin when PN5180 is detecting an external modulation scheme
2	IDLE_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for the IDLE mode
1	TX_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for End of RF transmission
0	RX_IRQ_EN	R/W	0*, 1	Enable IRQ propagation to the pin for End of RF reception

Table 66. IRQ_STATUS register (address 0002h) bit description

Bit	Symbol	Access	Value	Description
20	LPCD_IRQ_STAT	R/W	0*, 1	Low-Power Card Detection IRQ
19	HV_ERROR_IRQ_STAT	R/W	0*, 1	EEPROM Failure during Programming IRQ
18	GENERAL_ERROR_IRQ_STAT	R/W	0*, 1	General Error IRQ
17	TEMPSENS_ERROR_IRQ_STAT	R/W	0*, 1	Temperature Sensor IRQ
16	RX_SC_DET_IRQ_STAT	R/W	0*, 1	RX Subcarrier Detection IRQ
15	RX_SOF_DET_IRQ_STAT	R/W	0*, 1	RX SOF Detection IRQ
14	RFU	R/W	0*, 1	-
13	TIMER2_IRQ_STAT	R/W	0*, 1	Timer2 IRQ
12	TIMER1_IRQ_STAT	R/W	0*, 1	Timer1 IRQ
11	TIMER0_IRQ_STAT	R/W	0*, 1	Timer0 IRQ

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Table 66. IRQ_STATUS register (address 0002h) bit description *…continued*

Bit	Symbol	Access	Value	Description
10	RF_ACTIVE_ERROR_IRQ_STAT	R/W	0*, 1	RF active error IRQ
9	TX_RFON_IRQ_STAT	R/W	0*, 1	RF Field ON in PCD IRQ
8	TX_RFOFF_IRQ_STAT	R/W	0*, 1	RF Field OFF in PCD IRQ
7	RFON_DET_IRQ_STAT	R/W	0*, 1	RF Field ON detection IRQ
6	RFOFF_DET_IRQ_STAT	R/W	0*, 1	RF Field OFF detection IRQ
5	STATE_CHANGE_IRQ_STAT	R/W	0*, 1	State Change in the transceive state machine IRQ
4	CARD_ACTIVATED_IRQ_STAT	R/W	0*, 1	Activated as a Card IRQ
3	MODE_DETECTED_IRQ_STAT	R/W	0*, 1	External modulation scheme detection IRQ
2	IDLE_IRQ_STAT	R/W	0*, 1	IDLE IRQ
1	TX_IRQ_STAT	R/W	0*, 1	End of RF transmission IRQ
0	RX_IRQ_STAT	R/W	0*, 1	End of RF reception IRQ

Table 67. IRQ_CLEAR register (address 0003h) bit description

Bit	Symbol	Access	Value	Description
20	LPCD_IRQ_CLR	R/W	0*, 1	Clear Low-Power Card Detection IRQ
19	HV_ERROR_IRQ_CLR	R/W	0*, 1	Clear EEPROM Failure during Programming IRQ
18	GENERAL_ERROR_IRQ_CLR	R/W	0*, 1	Clear General Error IRQ
17	TEMPSENS_ERROR_IRQ_CLR	R/W	0*, 1	Clear Temperature Sensor IRQ
16	RX_SC_DET_IRQ_STAT	R/W	0*, 1	Clear RX Subcarrier Detection IRQ
15	RX_SOF_DET_IRQ_STAT	R/W	0*, 1	Clear RX SOF Detection IRQ
14	RFU	R/W	0*, 1	-
13	TIMER2_IRQ_CLR	R/W	0*, 1	Clear Timer2 IRQ
12	TIMER1_IRQ_CLR	R/W	0*, 1	Clear Timer1 IRQ
11	TIMER0_IRQ_CLR	R/W	0*, 1	Clear Timer0 IRQ
10	RF_ACTIVE_ERROR_IRQ_CLR	R/W	0*, 1	Clear RF active error IRQ
9	TX_RFON_IRQ_CLR	R/W	0*, 1	Clear RF Field ON in PCD IRQ
8	TX_RFOFF_IRQ_CLR	R/W	0*, 1	Clear RF Field OFF in PCD IRQ
7	RFON_DET_IRQ_CLR	R/W	0*, 1	Clear RF Field ON detection IRQ
6	RFOFF_DET_IRQ_CLR	R/W	0*, 1	Clear RF Field OFF detection IRQ
5	STATE_CHANGE_IRQ_CLR	R/W	0*, 1	Clear State Change in the transceive state machine IRQ
4	CARD_ACTIVATED_IRQ_CLR	R/W	0*, 1	Clear Activated as a Card IRQ
3	MODE_DETECTED_IRQ_CLR	R/W	0*, 1	Clear External modulation scheme detection IRQ
2	IDLE_IRQ_CLR	R/W	0*, 1	Clear IDLE IRQ
1	TX_IRQ_CLR	R/W	0*, 1	Clear End of RF transmission IRQ
0	RX_IRQ_CLR	R/W	0*, 1	Clear End of RF reception IRQ

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Table 68. TRANSCEIVE_CONTROL register (address 0004h) bit description

Bit	Symbol	Access	Value	Description
4-9	STATE_TRIGGER_SELECT	R/W	000000*	Register to select the state to trigger the STATE_CHANGE_IRQ flag. Each bit of the bit field enables one state - several states are possible. Note: If all bits are 0 no IRQ is triggered.
			xxxxx1	IDLE state enabled to trigger IRQ
			xxxx1x	WaitTransmit state enabled to trigger IRQ
			xxx1xx	Transmitting state enabled to trigger IRQ
			xx1xxx	WaitReceive state enabled to trigger IRQ
			x1xxxx	WaitForData state enabled to trigger IRQ
			1xxxxx	Receiving state enabled to trigger IRQ
3	TX_SKIP_SEND_ENABLE	R/W	0*, 1	If set, not transmission is started after tx_wait is expired and START_SEND was set Note: The bit is cleared by HW when the WaitReceive state is entered.
2	TX_FRAMESTEP_ENABLE	R/W	0*, 1	If set, at every start of transmission; each byte of data is sent in a separate frame. SOF and EOF are appended to the data byte according to the framing settings. After one byte is transmitted; the TxEncoder waits for a new start trigger to continue with the next byte.
1	RX_MULTIPLE_ENABLE	R/W	0*, 1	If set, the receiver is reactivated after the end of a reception. A status byte is written to the RAM containing all relevant status information of the frame. Note: Data in RAM is word aligned therefore empty bytes of a data Word in RAM are padded with 0x00 bytes. SW has to calculate the correct address for the following frame.
0	INITIATOR	R/W	0*, 1	If set, the CLIF is configured for initiator mode. Depending on this setting the behavior of the transceive command is different

Table 69. PINCONFIG register (address 0005h) bit description

Bit	Symbol	Access	Value	Description
7	EN_SLEW_RATE_CONTROL	R/W	0*, 1	Enables slew rate control of digital pads
6	GPO7_DIR	R/W	0*, 1	Enables the output driver of GPO7. The GPO is only available for the package TFBGA64
5	GPO6_DIR	R/W	0*, 1	Enables the output driver of GPO6. The GPO is only available for the package TFBGA64
4	GPO5_DIR	R/W	0*, 1	Enables the output driver of GPO5. The GPO is only available for the package TFBGA64
3	GPO4_DIR	R/W	0*, 1	Enables the output driver of GPO4. The GPO is only available for the package TFBGA64
2	GPO3_DIR	R/W	0*, 1	Enables the output driver of GPO3. The GPO is only available for the package TFBGA64
1	GPO2_DIR	R/W	0*, 1	Enables the output driver of GPO2. The GPO is only available for the package TFBGA64
0	GPO1_DIR	R/W	0*, 1	Enables the output driver of GPO1. The GPO is only available for the package TFBGA64 and HVQFN40

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Table 70. PIN_OUT register (address 0007h) bit description

Bit	Symbol	Access	Value	Description
6	GPO7_OUT	R/W	0*, 1	Output value of GPO7. The GPO is only available for the package TFBGA64
5	GPO6_OUT	R/W	0*, 1	Output value of GPO6. The GPO is only available for the package TFBGA64
4	GPO5_OUT	R/W	0*, 1	Output value of GPO5. The GPO is only available for the package TFBGA64
3	GPO4_OUT	R/W	0*, 1	Output value of GPO4. The GPO is only available for the package TFBGA64
2	GPO3_OUT	R/W	0*, 1	Output value of GPO3. The GPO is only available for the package TFBGA64
1	GPO2_OUT	R/W	0*, 1	Output value of GPO2. The GPO is only available for the package TFBGA64
0	GPO1_OUT	R/W	0*, 1	Output value of GPO1. The GPO is only available for the package TFBGA64 and HVQFN40

Table 71. TIMER0_STATUS register (address 0008h) bit description

Bit	Symbol	Access	Value	Description
20	T0_RUNNING	R	0*, 1	Indicates that timer T0 is running (busy)
19:0	T0_VALUE	R	00000h* - FFFFFh	Value of 20bit counter in timer T0

Table 72. TIMER1_STATUS register (address 0009h) bit description

Bit	Symbol	Access	Value	Description
20	T1_RUNNING	R	0*, 1	Indicates that timer T1 is running (busy)
19:0	T1_VALUE	R	00000h* - FFFFFh	Value of 20bit counter in timer T1

Table 73. TIMER2_STATUS register (address 000Ah) bit description

Bit	Symbol	Access	Value	Description
20	T2_RUNNING	R	0*, 1	Indicates that timer T2 is running (busy)
19:0	T2_VALUE	R	00000h* - FFFFFh	Value of 20bit counter in timer T2

Table 74. TIMER0_RELOAD register (address 000Bh) bit description

Bit	Symbol	Access	Value	Description
20:32	-			RFU
19:0	T0_RELOAD_VALUE	R/W	00000h* - FFFFFh	Reload value of the timer T0.

Table 75. TIMER1_RELOAD register (address 000Ch) bit description

Bit	Symbol	Access	Value	Description
20:32	-			RFU
19:0	T1_RELOAD_VALUE	R/W	00000h* - FFFFFh	Reload value of the timer T1.

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Table 76. TIMER2_RELOAD register (address 000Dh) bit description

Bit	Symbol	Access	Value	Description
20:32	-			RFU
19:0	T2_RELOAD_VALUE	R/W	00000h* - FFFFFh	Reload value of the timer T2.

Table 77. TIMER0_CONFIG register (address 000Eh) bit description

Bit	Symbol	Access	Value	Description
20	T0_STOP_ON_RX_STARTED	R/W	0*	T0_STOP_EVENT: If set; the timer T0 is stopped when a data reception begins and the first 4 bits had been received. The additional delay of the timer is protocol dependent and listed in the appendix.
19	T0_STOP_ON_TX_STARTED	R/W	0*	T0_STOP_EVENT: If set; the timer T0 is stopped when a data transmission begins.
18	T0_STOP_ON_RF_ON_EXT	R/W	0*	T0_STOP_EVENT: If set; the timer T0 is stopped when the external RF field is detected.
17	T0_STOP_ON_RF_OFF_EXT	R/W	0*	T0_STOP_EVENT: If set; the timer T0 is stopped when the external RF field vanishes.
16	T0_STOP_ON_RF_ON_INT	R/W	0*	T0_STOP_EVENT: If set; the timer T0 is stopped when the internal RF field is turned on.
15	T0_STOP_ON_RF_OFF_INT	R/W	0*	T0_STOP_EVENT: If set; the timer T0 is stopped when the internal RF field is turned off.
14	T0_START_ON_RX_STARTED	R/W	0*	T0_START_EVENT: If set; the timer T0 is started when a data reception begins (first bit is received).
13	T0_START_ON_RX_ENDED	R/W	0*	T0_START_EVENT: If set; the timer T0 is started when a data reception ends.
12	T0_START_ON_TX_STARTED	R/W	0*	T0_START_EVENT: If set; the timer T0 is started when a data transmission begins.
11	T0_START_ON_TX_ENDED	R/W	0*	T0_START_EVENT: If set; the timer T0 is started when a data transmission ends.
10	T0_START_ON_RF_ON_EXT	R/W	0*	T0_START_EVENT: If set; the timer T0 is started when the external RF field is detected.
9	T0_START_ON_RF_OFF_EXT	R/W	0*	T0_START_EVENT: If set; the timer T0 is started when the external RF field is not detected any more.
8	T0_START_ON_RF_ON_INT	R/W	0*	T0_START_EVENT: If set; the timer T0 is started when an internal RF field is turned on.
7	T0_START_ON_RF_OFF_INT	R/W	0*	T0_START_EVENT: If set; the timer T0 is started when an internal RF field is turned off.
6	T0_START_NOW	R/W	0*	T0_START_EVENT: If set; the timer T0 is started immediately.
3:5	T0_PRESCALE_SEL	R/W	000b*	Controls frequency/period of the timer T0 when the prescaler is activated in T0_MODE_SEL:
			000b	6.78 MHz counter
			001b	3.39 MHz counter
			010b	1.70 MHz counter
			011b	848 kHz counter
			100b	424 kHz counter
			101b	212 kHz counter

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Table 77. TIMER0_CONFIG register (address 000Eh) bit description *…continued*

Bit	Symbol	Access	Value	Description
			110b	106 kHz counter
			111b	53 kHz counter
2	T0_MODE_SEL	R/W	0*	Configuration of the timer T0 clock. 0b* Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1b Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T0_PRESCALE_SEL).
1	T0_RELOAD_ENABLE	R/W	0*	If set to 0; the timer T0 will stop on expiration. 0* After expiration the timer T0 will stop counting; i.e.; remain zero; reset value. 1 After expiration the timer T0 will reload its preset value and continue counting down.
0	T0_ENABLE	R/W	0*	Enables the timer T0

Table 78. TIMER1_CONFIG register (address 000Fh) bit description

Bit	Symbol	Access	Value	Description
20	T1_STOP_ON_RX_STARTED	R/W	0*	T1_STOP_EVENT: If set; the timer T1 is stopped when a data reception begins and the first 4 bits had been received. The additional delay of the timer is protocol dependent and listed in the appendix.
19	T1_STOP_ON_TX_STARTED	R/W	0*	T1_STOP_EVENT: If set; the timer T1 is stopped when a data transmission begins.
18	T1_STOP_ON_RF_ON_EXT	R/W	0*	T1_STOP_EVENT: If set; the timer T1 is stopped when the external RF field is detected.
17	T1_STOP_ON_RF_OFF_EXT	R/W	0*	T1_STOP_EVENT: If set; the timer T1 is stopped when the external RF field vanishes.
16	T1_STOP_ON_RF_ON_INT	R/W	0*	T1_STOP_EVENT: If set; the timer T1 is stopped when the internal RF field is turned on.
15	T1_STOP_ON_RF_OFF_INT	R/W	0*	T1_STOP_EVENT: If set; the timer T1 is stopped when the internal RF field is turned off.
14	T1_START_ON_RX_STARTED	R/W	0*	T1_START_EVENT: If set; the timer T1 is started when a data reception begins (first bit is received).
13	T1_START_ON_RX_ENDED	R/W	0*	T1_START_EVENT: If set; the timer T1 is started when a data reception ends.
12	T1_START_ON_TX_STARTED	R/W	0*	T1_START_EVENT: If set; the timer T1 is started when a data transmission begins.
11	T1_START_ON_TX_ENDED	R/W	0*	T1_START_EVENT: If set; the timer T1 is started when a data transmission ends.
10	T1_START_ON_RF_ON_EXT	R/W	0*	T1_START_EVENT: If set; the timer T1 is started when the external RF field is detected.
9	T1_START_ON_RF_OFF_EXT	R/W	0*	T1_START_EVENT: If set; the timer T1 is started when the external RF field is not detected any more.
8	T1_START_ON_RF_ON_INT	R/W	0*	T1_START_EVENT: If set; the timer T1 is started when an internal RF field is turned on.
7	T1_START_ON_RF_OFF_INT	R/W	0*	T1_START_EVENT: If set; the timer T1 is started when an internal RF field is turned off.
6	T1_START_NOW	R/W	0*	T1_START_EVENT: If set; the timer T1 is started immediately.

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Table 78. TIMER1_CONFIG register (address 000Fh) bit description *…continued*

Bit	Symbol	Access	Value	Description
3:5	T1_PRESCALE_SEL	R/W	000b*	Controls frequency/period of the timer T1 when the prescaler is activated in T1_MODE_SEL:
			000b	6.78 MHz counter
			001b	3.39 MHz counter
			010b	1.70 MHz counter
			011b	848 kHz counter
			100b	424 kHz counter
			101b	212 kHz counter
			110b	106 kHz counter
			111b	53 kHz counter
2	T1_MODE_SEL	R/W	0*	Configuration of the timer T1 clock. 0b* Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1b Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T1_PRESCALE_SEL).
1	T1_RELOAD_ENABLE	R/W	0*	If set to 0; the timer T1 will stop on expiration. 0* After expiration the timer T1 will stop counting; i.e.; remain zero; reset value. 1 After expiration the timer T1 will reload its preset value and continue counting down.
0	T1_ENABLE	R/W	0*	Enables the timer T1

Table 79. TIMER2_CONFIG register (address 0010h) bit description

Bit	Symbol	Access	Value	Description
20	T2_STOP_ON_RX_STARTED	R/W	0*	T2_STOP_EVENT: If set; the timer T2 is stopped when a data reception begins and the first 4 bits had been received. The additional delay of the timer is protocol dependent and listed in the appendix.
19	T2_STOP_ON_TX_STARTED	R/W	0*	T2_STOP_EVENT: If set; the timer T2 is stopped when a data transmission begins.
18	T2_STOP_ON_RF_ON_EXT	R/W	0*	T2_STOP_EVENT: If set; the timer T2 is stopped when the external RF field is detected.
17	T2_STOP_ON_RF_OFF_EXT	R/W	0*	T2_STOP_EVENT: If set; the timer T2 is stopped when the external RF field vanishes.
16	T2_STOP_ON_RF_ON_INT	R/W	0*	T2_STOP_EVENT: If set; the timer T2 is stopped when the internal RF field is turned on.
15	T2_STOP_ON_RF_OFF_INT	R/W	0*	T2_STOP_EVENT: If set; the timer T2 is stopped when the internal RF field is turned off.
14	T2_START_ON_RX_STARTED	R/W	0*	T2_START_EVENT: If set; the timer T2 is started when a data reception begins (first bit is received).
13	T2_START_ON_RX_ENDED	R/W	0*	T2_START_EVENT: If set; the timer T2 is started when a data reception ends.
12	T2_START_ON_TX_STARTED	R/W	0*	T2_START_EVENT: If set; the timer T2 is started when a data transmission begins.
11	T2_START_ON_TX_ENDED	R/W	0*	T2_START_EVENT: If set; the timer T2 is started when a data transmission ends.
10	T2_START_ON_RF_ON_EXT	R/W	0*	T2_START_EVENT: If set; the timer T2T2 is started when the external RF field is detected.

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Table 79. TIMER2_CONFIG register (address 0010h) bit description *...continued*

Bit	Symbol	Access	Value	Description
9	T2_START_ON_RF_OFF_EXT	R/W	0*	T2_START_EVENT: If set; the timer T2 is started when the external RF field is not detected any more.
8	T2_START_ON_RF_ON_INT	R/W	0*	T2_START_EVENT: If set; the timer T2 is started when an internal RF field is turned on.
7	T2_START_ON_RF_OFF_INT	R/W	0*	T2_START_EVENT: If set; the timer T2 is started when an internal RF field is turned off.
6	T2_START_NOW	R/W	0*	T2_START_EVENT: If set; the timer T2 is started immediately.
3:5	T2_PRESCALE_SEL	R/W	000b*	Controls frequency/period of the timer T2 when the prescaler is activated in T2_MODE_SEL:
			000b	6.78 MHz counter
			001b	3.39 MHz counter
			010b	1.70 MHz counter
			011b	848 kHz counter
			100b	424 kHz counter
			101b	212 kHz counter
			110b	106 kHz counter
			111b	53 kHz counter
2	T2_MODE_SEL	R/W	0*	Configuration of the timer T2 clock. 0b* Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1b Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T2_PRESCALE_SEL).
1	T2_RELOAD_ENABLE	R/W	0*	If set to 0; the timer T2 will stop on expiration. 0* After expiration the timer T2 will stop counting; i.e.; remain zero; reset value. 1 After expiration the timer T2 will reload its preset value and continue counting down.
0	T2_ENABLE	R/W	0*	Enables the timer T2

Table 80. RX_WAIT_CONFIG (address 0011h) bit description

Bit	Symbol	Access	Value	Description
8:27	RX_WAIT_VALUE	R/W	0*	Defines the rx_wait timer reload value. Note: If set to 00000h the rx_wait guard time is disabled
0:7	RX_WAIT_PRESCALER	R/W	0*	Defines the prescaler reload value for the rx_wait timer. For correct DPC operation it is required to set the prescaler to 0x7F For type A communication, the prescaler has to be set to 0x7F as well.

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Table 81. CRC_RX_CONFIG (address 0012h) bit description

Bit	Symbol	Access	Value	Description
31:16	RX_CRC_PRESET_VALUE	R/W	0*-FFFFh	Arbitrary preset value for the Rx-Encoder CRC calculation.
15:12	RFU	R	0	Reserved
11	RX_PARITY_TYPE	R/W	0*	Defines which type of the parity-bit is used Note: This bit is set by the mod-detector if automatic mode detection is enabled and ISO14443A communication is detected. 0 Even parity calculation is used 1 Odd parity calculation is used
10	RX_PARITY_ENABLE	R/W	0*	If set to 1; a parity-bit for each byte is expected; will be extracted from data stream and checked for correctness. In case the parity-bit is incorrect; the RX_DATA_INTEGRITY_ERROR flag is set. Nevertheless the reception is continued. Note: This bit is set by the mod-detector if automatic mode detection is enabled and ISO14443A communication is detected.
9	VALUES_AFTER_COLLISION	R/W	0*	This bit defined the value of bits received after a collision occurred. 0* All received bits after a collision will be cleared. 1 All received bits after a collision keep their value.
8:6	RX_BIT_ALIGN	R/W	0*	RxAlign defines the bit position within the byte for the first bit received. Further received bits are stored at the following bit positions.
5:3	RX_CRC_PRESET_SEL	R/W	000b*	Preset value of the CRC register for the Rx-Decoder. For a CRC calculation using 5bits, only the LSByte is used.
			000b*	0000h, reset value. Note that this configuration is set by the Mode detector for FeliCa.
			001b	6363h Note that this configuration is set by the Mode detector for ISO14443 type A.
			010b	A671h
			011b	FFFFh Note that this configuration is set by the Mode detector for ISO14443 type B.
			100b	0012h
			101b	E012h
			110b	RFU
			111b	Use arbitrary preset value RX_CRC_PRESET_VALUE
2	RX_CRC_TYPE	R/W	0*	Controls the type of CRC calculation for the Rx-Decoder
			0	16bit CRC calculation, reset value
			1	5bit CRC calculation

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Table 81. CRC_RX_CONFIG (address 0012h) bit description *…continued*

Bit	Symbol	Access	Value	Description
1	RX_CRC_INV	R/W	0*	Controls the comparison of the CRC checksum for the Rx-Decoder
			0*	Not inverted CRC value. Note that this bit is cleared by the Mode detector for ISO14443 type A and FeliCa.
			1	Inverted CRC value: F0B8h Note that this bit is set by the Mode detector for ISO14443 type B.
0	RX_CRC_ENABLE	R/W	0*	If set; the Rx-Decoder will check the CRC for correctness. Note: This bit is set by the Mode Detector when ISO14443 type B or FeliCa (212 or 424kBd) is detected.

Table 82. RX_STATUS_REG register (address 0013h) bit description

Bit	Symbol	Access	Value	Description
26:31	RFU	R	0	Reserved
19:25	RX_COLL_POS	R	0*	These bits show the bit position of the first detected collision in a received frame (only databits are interpreted). Note: These bits shall only be interpreted in passive communication mode at 106 kbit/s or ISO/IEC14443 A /MIFARE reader / writer mode if bit CollPosValid is set to 1. Note: If RX_ALIGN is set to a value different to 0, this value is included in the RX_COLL_POS.
18	RX_COLLISION_DETECTED	R	0*	This flag is set to 1, when a collision has occurred. The position of the first collision is shown in the register RX_COLLPOS
17	RX_PROTOCOL_ERROR	R	0*	This flag is set to 1, when a protocol error has occurred. A protocol error can be a wrong stop bit, a missing or wrong ISO/IEC14443 B EOF or SOF or a wrong number of received data bytes. Note: When a protocol error is detected, data reception is stopped. Note: The flag is automatically cleared at start of next reception.
16	RX_DATA_INTEGRITY_ERROR	R	0*	This flag is set to 1, if a data integrity error has been detected. Possible caused can be a wrong parity or a wrong CRC. Note: On a data integrity error the reception is continued Note: The flag is automatically cleared at start of next reception. Note: If a reversed parity bit is a stop criteria, the flag is not set to 1 in case of a wrong parity.

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Table 82. RX_STATUS_REG register (address 0013h) bit description *…continued*

Bit	Symbol	Access	Value	Description
13:15	RX_NUM_LAST_BITS	R	0*	Defines the number of valid bits of the last data byte received in bit-oriented communications. If zero the whole byte is valid.
9:12	RX_NUM_FRAMES_RECEIVED	R	0*	Indicates the number of frames received. The value is updated when the RxIRQ is raised. Note: This bit field is only valid when the RxMultiple is active (bit RX_MULTIPLE_ENABLE set)
8:0	RX_NUM_BYTES_RECEIVED	R	0*	Indicates the number of bytes received. The value is valid when the RxIRQ is raised until the receiver is enabled again.

Table 83. TX_UNDERSHOOT_CONFIG register (address 0014h) bit description

Bit	Symbol	Access	Value	Description
16:31	TX_UNDERSHOOT_PATTERN			Undershoot pattern which is transmitted after each falling edge.
5:15	RESERVED			-
1:4	TX_UNDERSHOOT_PATTERN_LEN			Defines length of the undershoot prevention pattern (value +1). The pattern is applied starting from the LSB of the defined pattern; all other bits are ignored.
0	TX_UNDERSHOOT_PROT_ENABLE			If set to 1; the undershoot protection is enabled

Table 84. TX_OVERSHOOT_CONFIG register (address 0015h) bit description

Bit	Symbol	Access	Value	Description
31:16	TX_OVERSHOOT_PATTERN	R/W	0* - FFFFh	Overshoot pattern which is transmitted after each rising edge.
15:5	RFU	R	0	Reserved
4:1	TX_OVERSHOOT_PATTERN_LEN	R/W	0*-Fh	Defines length of the overshoot prevention pattern (value +1). The pattern is applied starting from the MSB of the defined pattern, all other bits are ignored.
0	TX_OVERSHOOT_PROT_ENABLE	R/W	0*, 1	If set to 1, the overshoot protection is enabled.

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Table 85. TX_DATA_MOD register (address 0016h) bit description

Bit	Symbol	Access	Value	Description
8:15	TX_DATA_MOD_WIDTH	R/W	0*-FFh	Specifies the length of a pulse for sending data with miller pulse modulation enabled. The length is given by the number of carrier clocks + 1.
0:7	TX_BITPHASE	R/W	0* - FFh	Defines the number of 13.56 MHz cycles used for adjustment of TX_WAIT to meet the FDT. This is done by using this value as first counter initialization value instead of TX_WAIT_PRESCALER. These bits of TX_BITPHASE, together with TX_WAIT_VALUE and TX_WAIT_PRESCALER are defining the number of carrier frequency clocks which are added to the waiting period before transmitting data in all communication modes. TX_BITPHASE is used to adjust the TX bit synchronization during passive NFCIP-1 communication mode at 106 kbit and in ISO/IEC 14443A and 14443A/MIFARE card mode.

Table 86. TX_WAIT_CONFIG register (address 0017h) bit description

Bit	Symbol	Access	Value	Description
27:8	TX_WAIT_VALUE	D	0* - FFFFFh	Defines the tx_wait timer value. The values TX_WAIT_VALUE and TX_WAIT_PRESCALER are the initial counter values of two independent counters. The counter linked to TX_WAIT_PRESCALER is decremented at every 13.56 MHz clock. As soon as the counter TX_WAIT_PRESCALER overflows (transition from 00h to FFh), the counter linked to TX_WAIT is decremented. At the same time, the counter linked to TX_WAIT_PRESCALER is reloaded with the TX_WAIT_PRESCALER value. The first initial TX_WAIT_PRESCALER counter value is always using the data defined in TX_BITPHASE (in case of PICC operation). All other subsequent counter reload values will be taken from TX_WAIT_PRESCALER. Note: If set to 00000h the tx_wait guard time is disabled Note: This bit is set by HW a protocol is detected in automatic mode detector.
7:0	TX_WAIT_PRESCALER	D	0* - FFh	Defines the prescaler reload value for the tx_wait timer. Note: This bit is set by HW a protocol is detected in automatic mode detector. For correct DPC operation, it is required to set the prescaler to 0x7F For type A communication, the prescaler has to be set to 0x7F as well.

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Table 87. TX_CONFIG register (address 0018h) bit description

Bit	Symbol	Access	Value	Description
14:31	RFU	R	0	Reserved
13	TX_PARITY_LAST_INV_ENABLE	R/W	0	If set to 1; the parity bit of last sent data byte is inverted
12	TX_PARITY_TYPE	R/W	0	Defines the type of the parity bit 0 Even Parity is calculated 1 Odd parity is calculated
11	TX_PARITY_ENABLE	R/W	0	If set to 1; a parity bit is calculated and appended to each byte transmitted. If the Transmission Of Data Is Enabled and TX_NUM_BYTES_2_SEND is zero; then a NO_DATA_ERROR occurs.
10	TX_DATA_ENABLE	R/W	0	If set to 1; transmission of data is enabled otherwise only symbols are transmitted.
8:9	TX_STOP_SYMBOL	R/W	0	Defines which pattern symbol is sent as frame stop-symbol 00b No symbol is sent 01b Symbol1 is sent 10b Symbol2 is sent 11b Symbol3 is sent
6:7	TX_START_SYMBOL	R/W	0	Defines which symbol pattern is sent as frame start-symbol 00b No symbol pattern is sent 01b Symbol0 is sent 10b Symbol1 is sent 11b Symbol2 is sent.
3:5	TX_LAST_BITS	R/W	0	Defines how many bits of the last data byte to be sent. If set to 000b all bits of the last data byte are sent. Note: Bits are skipped at the end of the byte
0:2	TX_FIRST_BITS	R/W	0	Defines how many bits of the first data byte to be sent. If set to 000b all bits of the last data byte are sent. Note: Bits are skipped at the beginning of the byte

Table 88. CRC_TX_CONFIG_REG (address 0019h) bit description

Bit	Symbol	Access	Value	Description
31:16	TX_CRC_PRESET_VALUE	R/W	0*-FFFFh	Arbitrary preset value for the Tx-Encoder CRC calculation.
15:7	RFU	R	0	Reserved
6	TX_CRC_BYTE2_ENABLE	R/W	0	If set; the CRC is calculated from the second byte onwards (intended for HID). Note that this option is used in the Tx-Encoder.
5:3	TX_CRC_PRESET_SEL	R/W	000-101b	Preset value of the CRC register for the Tx-Encoder. For a CRC calculation using 5 bits, only the LSByte is used.
			000b*	0000h, reset value
			001b	6363h
			010b	A671h
			011b	FFFFh
			100b	0012h
			101b	E012h
			110b	RFU
			111b	Use arbitrary preset value TX_CRC_PRESET_VALUE

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Table 88. CRC_TX_CONFIG_REG (address 0019h) bit description *…continued*

Bit	Symbol	Access	Value	Description
2	TX_CRC_TYPE	R/W	0, 1	Controls the type of CRC calculation for the Tx-Encoder
			0*	16-bit CRC calculation, reset value
			1	5-bit CRC calculation
1	TX_CRC_INV	R/W	0, 1	Controls the sending of an inverted CRC value by the Tx-Encoder
			0*	Not inverted CRC checksum, reset value
			1	Inverted CRC checksum
0	TX_CRC_ENABLE	R/W	0*, 1	If set to one, the Tx-Encoder will compute and transmit a CRC.

Table 89. SIGPRO_CONFIG register (address 001Ah) bit description

Bit	Symbol	Access	Value	Description
3:31	RFU	R	0	Reserved
2:0	BAUDRATE	D	000*-111	Defines the baudrate of the receiving signal. The MSB is only relevant for reader mode. Note: These bits are set by the mode-detector if automatic mode detector is enabled and the communication mode is detected.
			000*	Reserved
			001	Reserved
			010	Reserved
			011	Reserved
			100	106 kBd Note that this configuration is set by the Mode detector for ISO/IEC14443 type A and B.
			101	212 kBd Note that this configuration is set by the Mode detector for FeliCa 212 kBd.
			110	424 kBd Note that this configuration is set by the Mode detector for FeliCa 424 kBd.
			111	848 kBd

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Table 90. SIGPRO_CM_CONFIG_REG register (address 001Bh) bit description

Bit	Symbol	Access	Value	Description
31	RFU	R	0	Reserved
29:30	RX_FRAMING			Defines the framing in card mode. Note that these bits are set by the mod-detector if automatic mode detection is enabled and the communication mode is detected. 00* ISO14443A / MIFARE 01 ISO18092 (NFC - with Syncbyte 0xF0) 10 FeliCa 11 ISO14443B
26:28	EDGE_DETECT_TAP_SEL			Selects the number of taps of the edge-detector filter. 000* Edge detector filter with 4 taps 001 Edge detector filter with 6 taps 010 Edge detector filter with 8 taps 4 011 Edge detector filter with 12 taps 100 Edge detector filter with 16 taps 101 Edge detector filter with 18 taps 110 Edge detector filter with 24 taps 111 Edge detector filter with 32 taps
13:25	EDGE_DETECT_TH			Threshold for the edge decision block of the ADCBCM.
0:12	BIT_DETECT_TH			Threshold for the “bit” decision block of the ADCBCM.

Table 91. SIGPRO_RM_CONFIG1_REG register (address 001Ch) bit description

Bit	Symbol	Access	Value	Description
24:31	RFU	R	0	Reserved
21:23	BPSK_IQ_MODE	R/W	000*-111	Defines signal processing of I- and Q- channel
			000*	Both channels (I and Q) are used for signal processing
			001	Use only I channel
			010	Use only Q channel
			011	RFU
			100	Use the strongest channel
			101	Use the first channel
			110-111	RFU
20	BPSK_FILT6	R/W	0*-1	Reserved for test
19	RESYNC_EQ_ON	R/W	0-1*	Resynchronization during the SOF for an equal correlation value is done (default = activated).
18	CORR_RESET_ON	R/W	0	The correlator is reset at a reset (default = activated).
17	VALID_FILT_OFF	R/W	0*-1	Disables a special filter in BPSK mode. If set to 0, the correlation of 0110 is filtered with the correlation of 1110 and 0111. Otherwise the demodulation is done using the correlation with 0110
16	DATA_BEFORE_MIN	R/W	0	Data is received even before the first minimum at the SOF (default: = deactivated).
15:12	MIN_LEVEL	R/W	0*-Fh	Defines the minimum level (threshold value) for the subcarrier detector unit. Note: The MinLevel should be higher than the noise level in the system Note: Used for BPSK and Manchester with Subcarrier communication types as MinLevel!

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Table 91. SIGPRO_RM_CONFIG1_REG register (address 001Ch) bit description *...continued*

Bit	Symbol	Access	Value	Description
11:8	MIN_LEVEL_P	R/W	0*-Fh	Defines the minimum level (threshold value) for the phaseshift detector unit. Used for BPSK communication
7	USE_SMALL_EVAL	R	0	Defines the length of the eval periode for the correlator for Manchester subcarrier communication types.
6:5	COLL_LEVEL	R/W	00*-11	Defines how strong a signal must be interpreted as a collision for Manchester subcarrier communication types.
			00*	>12.5 %
			01	>25 %
			10	>50 %
			11	No Collision
4	PRE_FILTER	R/W		If set to 1 four samples are combined to one data. (average)
3	RECT_FILTER	R/W	0	If set to one; the ADC-values are changed to a more rectangular waveshape.
2	SYNC_HIGH	R/W	0*-1	Defines if the bitgrid is fixed at maximum (1) or at a minimum(0) value of the correlation.
1	FSK	R	0	If set to 1; the demodulation scheme is FSK.
0	BPSK	R/W	0*	If set to 1, the demodulation scheme is BPSK.

Table 92. RF_STATUS register (address 001Dh) bit description

Bit	Symbol	Access	Value	Description
27:31	RFU	R	0	-
26:24	TRANSCEIVE_STATE	R	0*	These registers hold the command bits 0* IDLE state 1 WaitTransmit state 2 Transmitting state 3 WaitReceive state 4 WaitForData state 5 Receiving state 6 LoopBack state 7 reserved
23:20	DPC_CURRENT_GEAR	R	0*	Current Gear of the DPC
19	DPLL_ENABLE	R	0*	This bit indicates that the DPLL Controller has enabled the DPLL (RF on, RF frequency ok, PLL locked)
18	CRC_OK	R	0	This bit indicates the status of the actual CRC calculation. If 1 the CRC is correct; meaning the CRC register has the value 0 or the residue value if inverted CRC is used. Note: This flag should only by evaluated at the end of a communication
17	TX_RF_STATUS	R	0	If set to 1 this bit indicates that the drivers are turned on; meaning an RF-Field is created by the device itself.
16	RF_DET_STATUS	R	0	If set to 1 this bit indicates that an external RF-Field is detected by the RF-level detectors (after digital filtering)

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Table 92. RF_STATUS register (address 001Dh) bit description *…continued*

Bit	Symbol	Access	Value	Description
13:15	RF_ACTIVE_ERROR_CAUSE	R	0 - 5	This status flag indicates the cause of an NFC-Active error. Note: These bits are only valid when the RF_ACTIVE_ERROR_IRQ is raised and will be cleared as soon as the bit TX_RF_ENABLE is set to 1.
			0*	No Error; reset value
			1	External field was detected on within TIDT timing
			2	External field was detected on within TADT timing
			3	No external field was detected within TADT timings
			4	Peer did switch off RF-Field but no Rx event was raised (no data received)
			5 - 7	Reserved
12	RX_ENABLE			This bit indicates if the RxDecoder is enabled. If 1 the RxDecoder was enabled by the Transceive Unit and is now ready for data reception
11	TX_ACTIVE			This bit indicates activity of the TxEncoder. If 1 a transmission is ongoing, otherwise the TxEncoder is in idle state.
10	RX_ACTIVE			This bit indicates activity of the RxDecoder. If 1 a data reception is ongoing; otherwise the RxDecoder is in idle state.
9:0	AGC_VALUE	R	0*-3FFh	Current value of the AGC
			0h*	Most sensitive: largest Rx-resistor, i.e., none of the switchable resistors is added in parallel
			3FFh	Most robust: smallest Rx-resistor, i.e., all switchable resistors are added in parallel

Table 93. AGC_CONFIG register (address 001Eh) bit description

Bit	Symbol	Access	Value	Description
16:31	RFU	R	0*	Reserved
14:15	AGC_VREF_SEL	R/W	0*	Select the comparison reference voltage.
4:13	AGC_TIME_CONSTANT	R/W	0*	Time constant for the AGC update. An AGC period is given by (AGC_TIME_CONSTANT+1) * 13.56 MHz
3	AGC_INPUT_SEL	R/W	0*	Selects the AGC value to be loaded into the AGC and the source for manual mode: 0* CLIF_AGC_INPUT_REG.AGC_CM_VALUE 1 CLIF_AGC_INPUT_REG.AGC_RM_VALUE

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Table 93. AGC_CONFIG register (address 001Eh) bit description *…continued*

Bit	Symbol	Access	Value	Description
2	AGC_LOAD	R/W	0*	If set; one AGC control value is loaded from CLIF_AGC_VALUE_REG into the internal AGC register (depending on AGC_INPUT_SEL).
1	AGC_MODE_SEL	R/W	0*	Selects the operation mode of the AGC: 0* Rx-Divider is controlled by the register CLIF_AGC_INPUT_REG.AGC_CM_VALUE or CLIF_AGC_INPUT_REG.AGC_RM_VALUE (dependent on AGC_INPUT_SEL) 1 Rx-Divider value is controlled by the AGC.
0	AGC_MODE_ENABLE	R/W	0*	If set, the AGC is enabled. If not set, the Rx-Divider is controlled by either the internal AGC register or a register value (dependent on AGC_MODE_SEL).

Table 94. AGC_VALUE_REG register (address 001Fh) bit description

Bit	Symbol	Access	Value	Description
20:31	RFU	R	0	Reserved
10:19	AGC_RM_VALUE	R/W	0	Static AGC value used for reader mode
0:9	AGC_CM_VALUE	R/W	0	Static AGC value used for card mode

Table 95. RF_CONTROL_TX register (address 0020h) bit description

Bit	Symbol	Access	Value	Description
27:31	RFU	R	0	Reserved
26	TX_ALM_TYPE_SELECT	R/W	0*	0 ... Both drivers used for ALM 1 ... Single driver used for ALM
24:25	TX_CW_AMPLITUDE_ALM_CM	R/W	0*	set amplitude of unmodulated carrier at card mode
19:23	TX_RESIDUAL_CARRIER_OV_PREV	R/W	0*	Defines the value for the residual carrier for the period the overshoot prevention pattern is active.
18	TX_CW_TO_MAX_ALM_CM	R/W	0*	TX HI output is the maximum voltage obtainable from charge pump (CM setting); if set to 1 -> TX_CW_AMPLITUDE_CM is overruled.
13:17	TX_RESIDUAL_CARRIER	R/W	0*	set residual carrier (0=100 %, 1F = 0 %)
12	TX_BYPASS_SC_SHAPING	R/W	0*	Bypasses switched capacitor shaping of the Transmitter Signal
8:11	TX_SLEW_SHUNTREG	R/W	0*	Set slew rate for shunt regulator
4:7	TX_TAU_MOD_FALLING	R/W	0*	Transmitter TAU setting for falling edge of modulation shape. In AnalogControl module the output signal is switched with the tx_envelope. Only valid is TX_SINGLE_CP_MODE is set
0:3	TX_TAU_MOD_RISING	R/W	0*	Transmitter TAU setting for rising edge of modulation shape. In Analog Control module the output signal is switched with the tx_envelope. Only valid is TX_SINGLE_CP_MODE is set

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Table 96. RF_CONTROL_TX_CLK register (address 0021h) bit description

Bit	Symbol	Access	Value	Description
19:31	RFU	R	0*	Reserved
18	TX_ALM_ENABLE	R/W	0*	If set to 1 ALM is used for transmission in card mode
14:17	RFU	R		RFU
11:13	CLOCK_CONFIG_DLL_ALM	R/W	0*	Select DLL clock phase
8:10	TX_CLK_MODE_OVUN_PREV	R/W	0*	Defines the TX clockmode for the period the overshoot/undershoot prevention is active
7	TX2_INV_RM	R/W	0*	If 1 -> TX output is inverted (clk_13m56_n is used); 0 -> clk_13m56 is used
6	TX2_INV_CM	R/W	0*	If 1 -> TX output is inverted (clk_13m56_n is used); 0 -> clk_13m56 is used
5	TX1_INV_RM	R/W	0*	If 1 -> TX output is inverted (clk_13m56_n is used); 0 -> clk_13m56 is used
4	TX1_INV_CM	R/W	0*	If 1 -> TX output is inverted (clk_13m56_n is used); 0 -> clk_13m56 is used
3:1	TX_CLK_MODE_RM	R/W	0*	TX clockmode
0	CLOCK_ENABLE_DPLL	R/W	0*	Enables the DPLL

Table 97. RF_CONTROL_RX_CLK register (address 0022h) bit description

Bit	Symbol	Access	Value	Description
8:31	RFU	R	0*	Reserved
6:7	CM_MILLER_SENS	R/W		Configuration bits for reference level of Miller demodulator
4:5	RX_ MIXER_CONTROL	R/W		Mixer Control Enable 00, 11 … power down both mixer 01… reader mode mixer 10… card mode mixer,
2:3	RX_HPCF	R/W		High Pass Corner Frequency: 00->45 kHz, 01-> 85 kHz, 10->150 kHz, 11->250 kHz
1:0	RX_GAIN	R/W	0h*-3h	Gain Adjustment BBA: 00->33 dB, 01->40 dB, 10-> 50 dB, 11->57 dB

Table 98. RF_LEVEL_DETECTOR_CONTROL register (address 0023h) bit description

Bit	Symbol	Access	Value	Description
15:31	RFU	R	0*	Reserved
14	CM_PD_NFC_DET	R/W	0*	Power Down NFC level detector
12:13	RFDET_SOURCE_SEL	R/W	0*	Select the source for RF-Field detection; 0* -> NFC-Level detector indication signal is used; 1 -> RF-Level detector indication signal is used 2; -> NFC- and RF-Level detector indication signal is used 3; -> Override - RF-Field detected is emulated
8:11	CM_RFL_NFC	R/W	0*	Programming of detection level
4:7	RFLD_REF_LO	R/W	0*	Higher Reference Value for RF Level Detector
0:3	RFLD_REF_HI	R/W	0*	Lower Reference Value for RF Level Detector

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Table 99. SYSTEM_STATUS register (address 0024h) bit description

Bit	Symbol	Access	Value	Description
9:31	RFU	R	0	Reserved
8	PARAMETER_ERROR	R	0*	Parameter Error on Host Communication
7	SYNTAX_ERROR	R	0*	Syntax Error on Host Communication
6	SEMANTIC_ERROR	R	0*	Semantic Error on Host Communication
5	STBY_PREVENT_RFLD	R	0*	Entry of STBY mode prevented due to existing RFLD
4	BOOT_TEMP	R	0*	Boot Reason Temp Sensor
3	BOOT_SOFT_RESET	R	0*	Boot Reason due to SOFT RESET
2	BOOT_WUC	R	0*	Boot Reason wake-up Counter
1	BOOT_RFLD	R	0*	Boot Reason RF Level Detector
0	BOOT_POR	R	0*	Boot Reason Power on Reset / RESET_N

Table 100. TEMP_CONTROL register (address 0025h) bit description

Bit	Symbol	Access	Value	Description
4:31	RFU	R	0	Reserved
3	TEMP_ENABLE_HYST	R/W	0*	Enable hystereses of Temperature Sensor
2	TEMP_ENABLE	R/W	0*	Enable Temp Sensor
0:1	TEMP_DELTA	R/W	0*	selects temperature value

Table 101. CHECK_CARD_RESULT register (address 0026h) bit description

Bit	Symbol	Access	Value	Description
14:31	RFU	R	0	RFU
10:13	AGC_GEAR	R/W	0	Reading from this register will start a check card routine which is an LPCD with only one measurement point without entry to standby mode. The value contains the actual gear when DPC is used and the AGC value. Writing to this register will be used as a reference value for the LPCD when LPCD mode 2 is used.
0:9	AGC_VALUE	R/W	0	

Table 102. DPC_CONFIG register (address 0027h) bit description

Bit	Symbol	Access	Value	Description
20:31		RFU	R	0
16:19	TX_GSN_CW_CM	R/W	0	GSN value for continuous wave in Card Mode
12:15	TX_GSN_MOD_CM	R/W	0	GSN value for modulation in Card Mode
8:11	TX_GSN_MOD_RM	R/W	0	GSN value for modulation in Reader Mode
4:7	TX_GSN_CW_RM	R/W	0	GSN value for continuous wave in Reader Mode
3	TX_CW_TO_MAX_RM	R/W	0	Maximum output voltage on TX driver
1:2	TX_CW_AMPLITUDE_RM	R/W	0	set amplitude of unmodulated carrier at reader mode
0	TX_CW_AMP_REF2TVDD	RW	0	If set to 1 the reference of the unmodulated carrier is defined relative to TVDD

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Table 103. EMD_CONTROL register (address 0028h) bit description

Bit	Symbol	Access	Value	Description
Recommended value for EMVCo 2.3.1 0x185 (use Timer1) Recommended value for EMVCo 2.5 0x187				
10:31	RFU	R	0	Reserved
8:9	EMD_TRANSMISSION_TIMER_USED	R/W	0	Timer used for RF communication. 00 Timer0, 01 Timer1, 10 Timer 2, 11 RFU
7	EMD_MISSING_CRC_IS_PROTOCOL_ERROR_TYPE_B	R/W	0	Missing CRC treated as protocol error in case of Type B based communication
6	EMD_MISSING_CRC_IS_PROTOCOL_ERROR_TYPE_A	R/W	0	Missing CRC treated as protocol error in case of Type A based communication
2:5	EMD_NOISE_BYTES_THRESHOLD	R/W	0	Defines the threshold under which transmission errors are treated as noise. Note: CRC bytes are NOT included/counted!
1	EMD_TRANSMISSION_ERROR_ABOVE_NOISE_THRESHOLD_IS_NO_EMD	R/W	0	Transmission errors with received byte length >= EMD_NOISE_BYTES_THRESHOLD is never treated as EMD (EMVCo 2.5 standard)
0	EMD_ENABLE	R/W	0	Enable EMD handling

Table 104. ANT_CONTROL register (address 0029h) bit description

Bit	Symbol	Access	Value	Description
8:31	RFU	R	0	Reserved
7	ANT_INVERT_ON_TXACTIVE	R/W	0	If set to 1, the ANT short interface in card mode is inverted when tx_active is asserted (i.e. while transmission). Note: this bit is only valid in card mode. Note: if it ANT_ALM_AUTO_SWITCH_ENABLE is set this setting is ignored
6	ANT_ALM_AUTO_SWITCH_ENABLE	R/W	0	If set to 1, the ANT setting for ALM is switch automatically by HW. By default for ALM the ANT_short and ANT_mod uses the same settings as for PLM.
5	ANT_ALM_FW_RESET	R/W	0	If set to 1 the ANT setting for ALM is reset to its initial receive configuration

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Table 104. ANT_CONTROL register (address 0029h) bit description *...continued*

Bit	Symbol	Access	Value	Description
4	ANT_SHORT_SELECT_RM	R/W	0	Selects the control of the ANT modulation interface in reader mode
2:3	ANT_SHORT_SELECT	R/W	0	Selects the control of the ANT short interface in cardmode for PLM; in reader mode and ALM the analog control signals are switched by digital logic. 00b Constant 0 (ANT open) 01b Constant 1 (ANT short) 10b TxEnvelope used (idle = 1, modulation = 0) 11b Inverted TxEnvelope used (idle = 0, modulation = 1)
0:1	ANT_MOD_SELECT	R/W	0	Selects the control of the ANT modulation interface in cardmode for PLM; in reader mode and ALM the analog control signals are switched by digital logic. 00b Constant 0 (No modulation on ANT mod) 01b Constant 1 (modulation on ANT mod) 10b TxEnvelope used (idle = 1, modulation = 0) 11b Inverted TxEnvelope used (idle = 0, modulation = 1)

11. Limiting values

Table 105. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(PVDD)}$	PVDD supply voltage	-	-	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage	-	-	4.6	V
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM); 1500 Ω, 100 pF; JESD22-A114-B	-	1500	V
T_{stg}	storage temperature	no supply voltage applied	-55	+150	°C
P_{tot}	total power dissipation	in still air with exposed pins soldered on a 4 layer JEDEC PCB	-	1125	mW
$T_{j(max)}$	maximum junction temperature	-	-	150	°C

12. Recommended operating conditions

Table 106. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(VBAT)}$	VBAT supply voltage	$V_{DD(VBAT)} <= V_{DD(PVDD)}$	2.7	3.3	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage	1.8 V supply	1.65	1.8	1.95	V
		3.3 V supply	2.7	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage	-	2.7	5.0	5.5	V
T_{amb}	ambient temperature	in still air with exposed pins soldered on a 4 layer JEDEC PCB	–30	+25	+85	°C

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13. Thermal characteristics

Table 107. Thermal characteristics HVQFN40 package

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB, package HVQFN40	40	K/W

Table 108. Thermal characteristics TFBGA64 package

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 4 layer JEDEC PCB, package HVQFN40	66	K/W

14. Characteristics

Table 109. Current consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(TVDD)}$	TVDD supply current	-	-	180	250	mA
$I_{DD(PVDD)}$	PVDD supply current	$V_{DD(PVDD)}$ = 3.3 V	-	20	-	mA
$I_{DD(VBAT)}$	VBAT supply current	$V_{DD(VBAT)}$ = 3.3 V max current includes current of all GPO's	-	-	20	mA
I_{pd}	power-down current	VDD(TVDD) = VDD(PVDD) =VDD(VDD) 3.0 V; hard power-down; pin RESET_N set LOW, T_{amb} = 25 °C	-	10	-	µA
I_{stb}	standby current	T_{amb} = 25 °C	-	15	-	µA
$I_{DD(idle)Idle}$	Idle mode supply current	T_{amb} = 25 °C	-	7	-	mA

Table 110. Reset pin RESET_N

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(RESET_N)}$	RESET_N pulse width		10	-	-	µs
V_{IH}	HIGH-level input voltage	PVDD<= VBAT	1.1	-	PVDD	V
V_{IL}	LOW-level input voltage		0	-	0.4	V
I_{IH}	HIGH-level input current	V_I = VBAT	-	-	1	mA
I_{IL}	LOW-level input current	V_I = 0 V	-1	-	-	mA
C_i	input capacitance		-	5	-	pF

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Table 111. Input Pin REQ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	PVDD<= VBAT	0.65 x P_{VDD}	-	PVDD	V
V_{IL}	LOW-level input voltage	-	0	-	0.4	V
I_{IH}	HIGH-level input current	V_I = VBAT	-	-	1	mA
I_{IL}	LOW-level input current	V_I = 0 V	-1	-	-	mA
C_i	input capacitance	-	-	5	-	pF
$t_{(REQ)}$	time from RESET_N high to REQ high	-	0	-	50	µs

Table 112. GPO pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(p-p)}$	peak-to-peak input voltage	-	-	-	$V_{DD(PVDD)}$	V
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3.3 V	-	-	3	mA
I_{IL}	LOW-level input current	$V_{DD(PVDD)}$ = 3.3 V	-	-	3	mA

Table 113. CLK1, CLK2 pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(p-p)}$	peak-to-peak input voltage	-	0.2	-	1.65	V
I_{IH}	HIGH-level input current	V_I= 1.65 V	-	-	1	µA
I_{IL}	LOW-level input current	V_I = 0 V	1	-	-	µA
δ	duty cycle	-	35		65	%
$C_{i(CLK1)}$	input capacitance on pin CLK1	VDD = 1.8 V, VDC = 0.65 V, VAC = 0.9 Vpp	-	2	-	pF
$C_{i(CLK2)}$	input capacitance on pin CLK2	VDD = 1.8 V, VDC = 0.65 V, VAC = 0.9 Vpp	-	2	-	pF

Table 114. Output pin characteristics IRQ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 3 mA	P_{VDD} -0.4	-	P_{VDD}	V
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
C_L	load capacitance		-	-	20	pF
t_f	fall time	C_L = 12 pF max	1	-	3	ns
t_r	rise time	C_L = 12 pF max	1	-	3	ns
R_{pd}	pull-down resistance		0.4	-	0.7	MΩ

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Table 115. Input pins SCLK, MOSI, NSS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		0.65 x P_{VDD}	-	P_{VDD}	V
V_{IL}	LOW-level input voltage		0	-	0.35 x P_{VDD}	V
C_i	input capacitance		-	5	-	pF
I_{IH}	HIGH-level input current	$V_I = P_{VDD}$	-	-	1	mA
I_{IL}	LOW-level input current	V_I = 0 V	-	-	1	mA

Table 116. Output pin MISO

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} < 3 mA	P_{VDD} -0.4	-	P_{VDD}	V
V_{OL}	LOW-level output voltage	I_{OL} < 3 mA	0	-	0.4	V
C_L	load capacitance		-	-	20	pF
t_f	fall time	C_L = 12 pF max	1	-	3	ns
t_r	rise time	C_L = 12 pF max	1	-	3	ns

Table 117. Timing conditions SPI

Symbol	Parameter	Min	Typ	Max	Unit
t_{SCKL}	SCK LOW time	72	-	-	ns
t_{SCKH}	SCK HIGH time	72	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	25	-	-	ns
$t_{su(D-SCKH)}$	data input to SCK HIGH set-up time	25	-	-	ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time	0	-	-	ns
t_{NSSH}	NSS HIGH time	72	-	-	ns

Table 118. Output pins ANT1 and ANT2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Z_{(ANT1-ANT2)}$	impedance from ANT1 to ANT2	Low impedance	-	10	17	Ohm
$V_{i(start)(lim)(ANT1)}$	limiter start input voltage on ANT1	I=10 mA	-	3.3	-	V
$V_{i(start)(lim)(ANT2)}$	limiter start input voltage on ANT2	I=10 mA	-	3.3	-	V

Table 119. Input pins RXp and RXn

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(dyn)}$	dynamic input voltage		-	-	V_{DD}	V
C_i	input capacitance		-	12	-	pF
$Z_{(RX-VMID)}$	impedance from RX to VMID	Reader, Card and P2P modes	0	-	15	kΩ

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Table 120. Output pins TX1 and TX2

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	T_{VDD}=5 V	-	T_{VDD}-150	T_{VDD}	mV
V_{OL}	LOW-level output voltage	T_{VDD}=5 V	0	200	-	mV

Table 121. Start-up time

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{boot}	boot time[1]	RESET_N = High	2.3	2.5	dependent on configuration of XTAL_BOOT_TIME in EEPROM	ms

[1] (PN5180 ready to receive commands on the host interface). The PN5180 indicates the ability to receive commands from a host by raising an IDLE IRQ.

Table 122. Crystal requirements for ISO/IEC14443 compliant operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	ISO/IEC 14443 and ISO/IEC 18092 compliancy	27.12 - 14 kHz	27.12	27.12 + 14 kHz	MHz
f_{xtal}	crystal frequency	Full operating range	-100	±50	+100	ppm
ESR	equivalent series resistance	-		50	100	Ω
C_L	load capacitance	-	-	10	-	pF
P_{drive}	drive power	-	-	-	100	µW

Table 123. Reference input frequency requirements for 8 MHz, 12 MHz, 16 MHz and 24 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
φ_n	phase noise	Input noise floor at 50 kHz	-	-	-140	db/Hz
$V_{i(p-p)}$	peak-to-peak input voltage	sinus signal	0.2	-	1.8	V
$V_{i(p-p)}$	peak-to-peak input voltage	square signal	0	-	1.98	V
$f_{i(ref)acc}$	reference input frequency accuracy	-	-100	±50	+100	ppm

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15. Application information

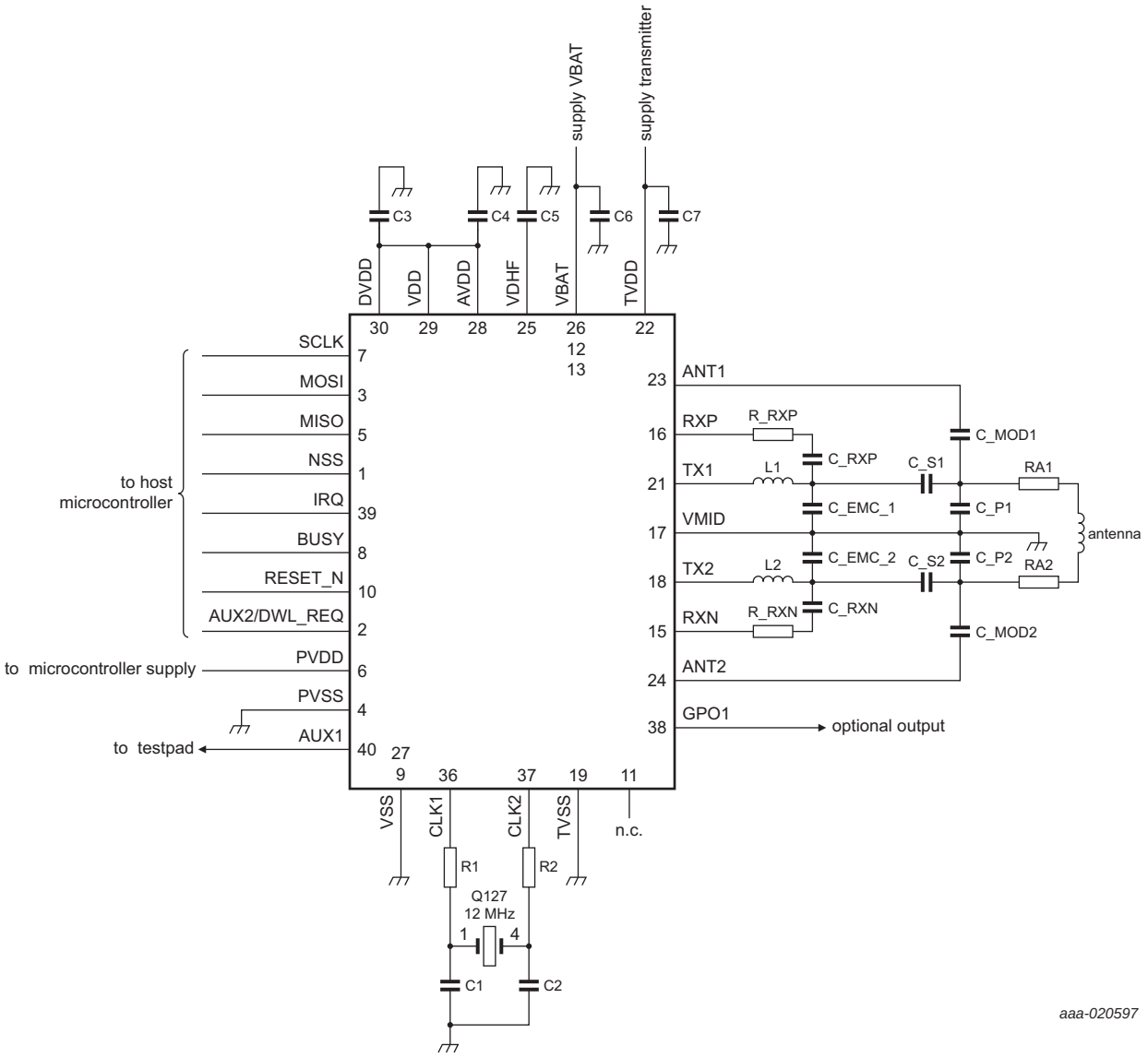

Fig 30. Application diagram with minimum components

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16. Packaging information

Moisture Sensitivity Level (MSL) evaluation has been performed according to SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C). MSL for theHVQFN40 package is level 3 which means 260 °C convection reflow temperature.

- 1 weekout-of-pack floor life at maximum ambient temperature 30°C/ 60 % RH (Relative Humidity) to limit possible moisture intrusion.
- When used in production, stored under nitrogen conditions for not more than 8 days

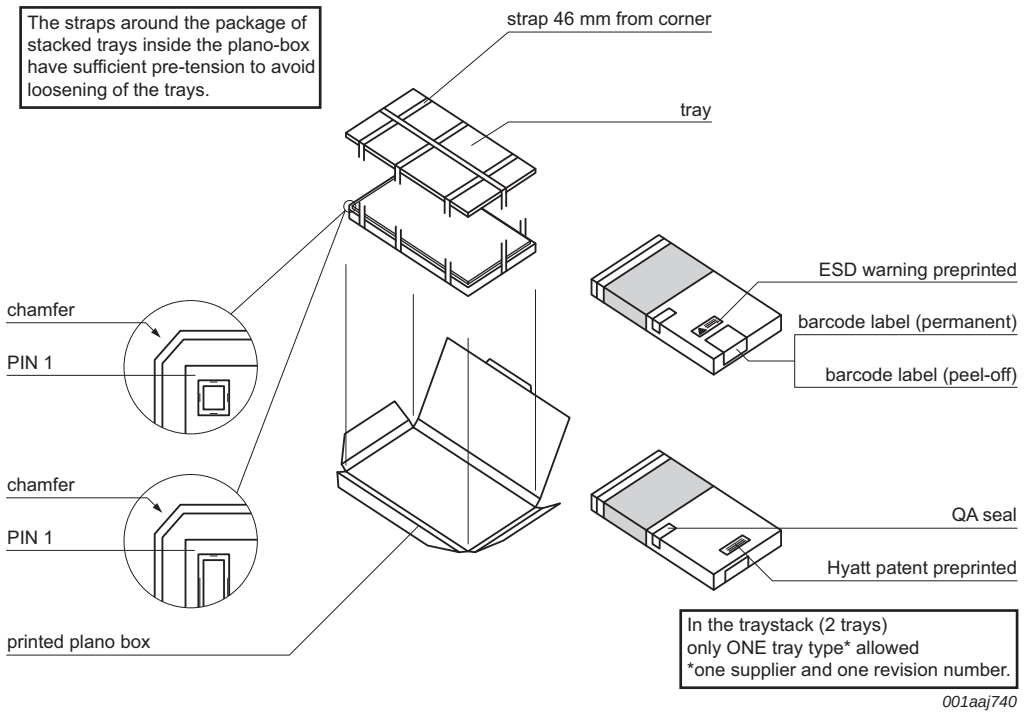

Fig 31. Packaging information 1 tray

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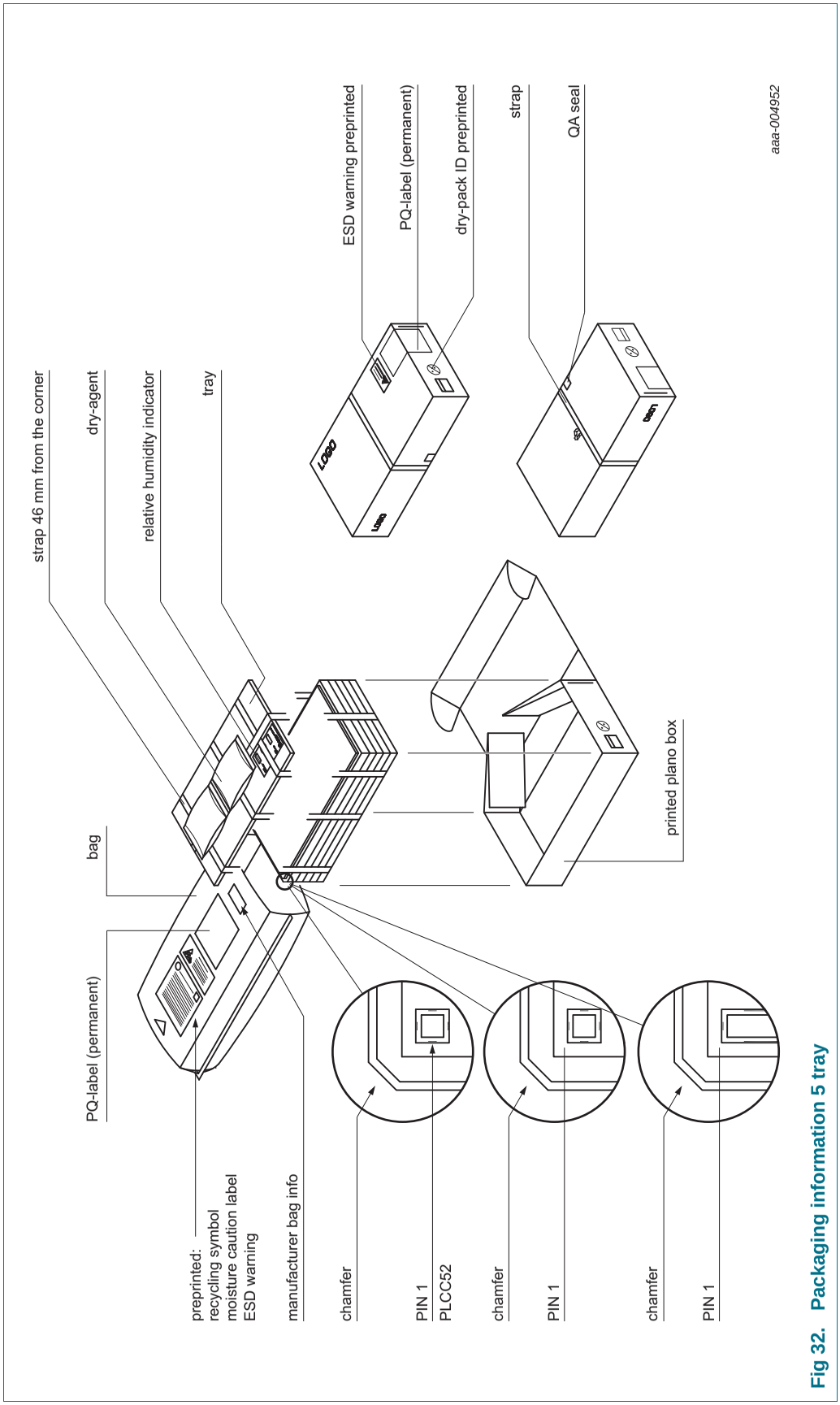

Fig 32. Packaging information 5 tray

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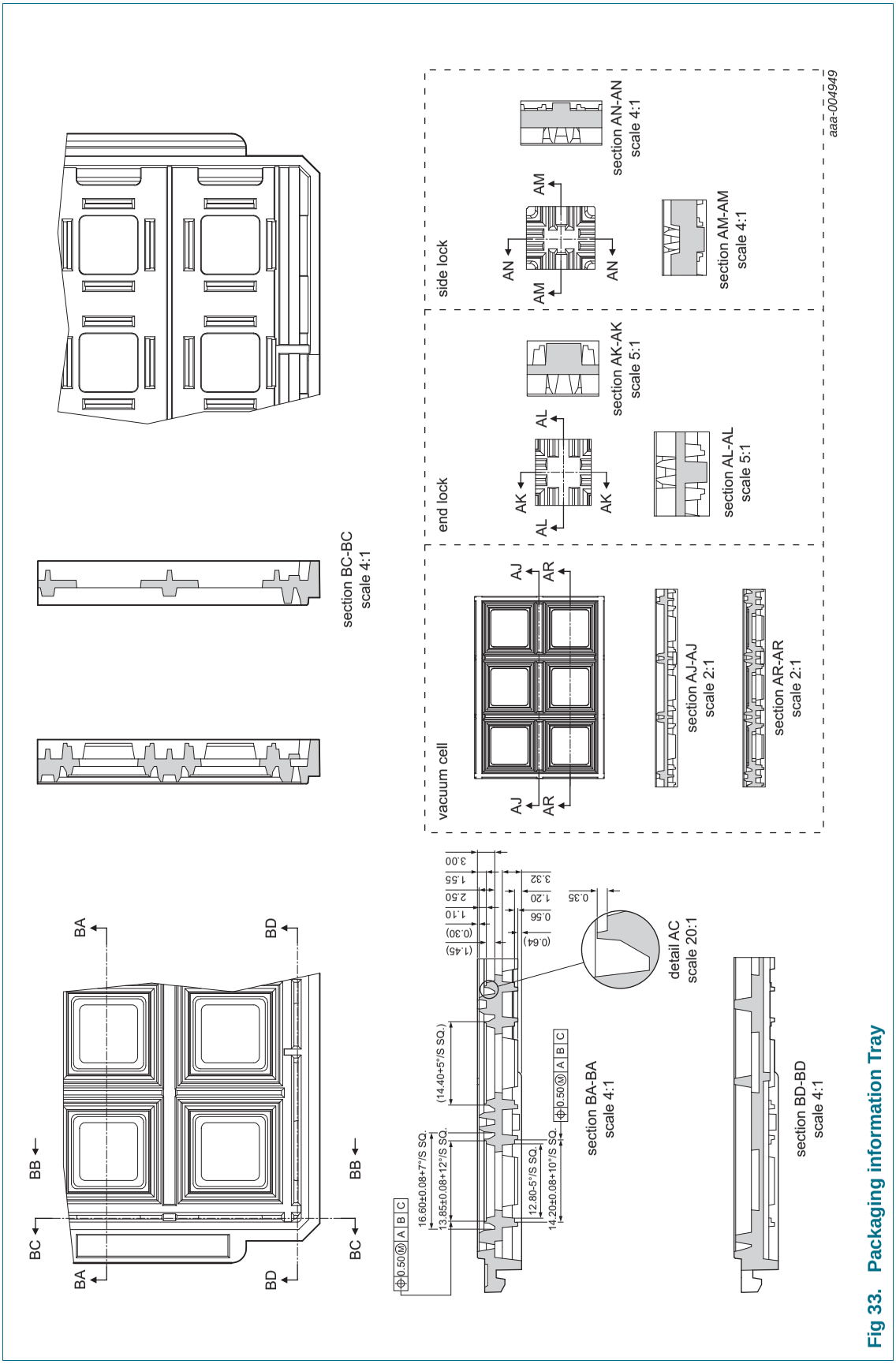

Fig 33. Packaging information Tray

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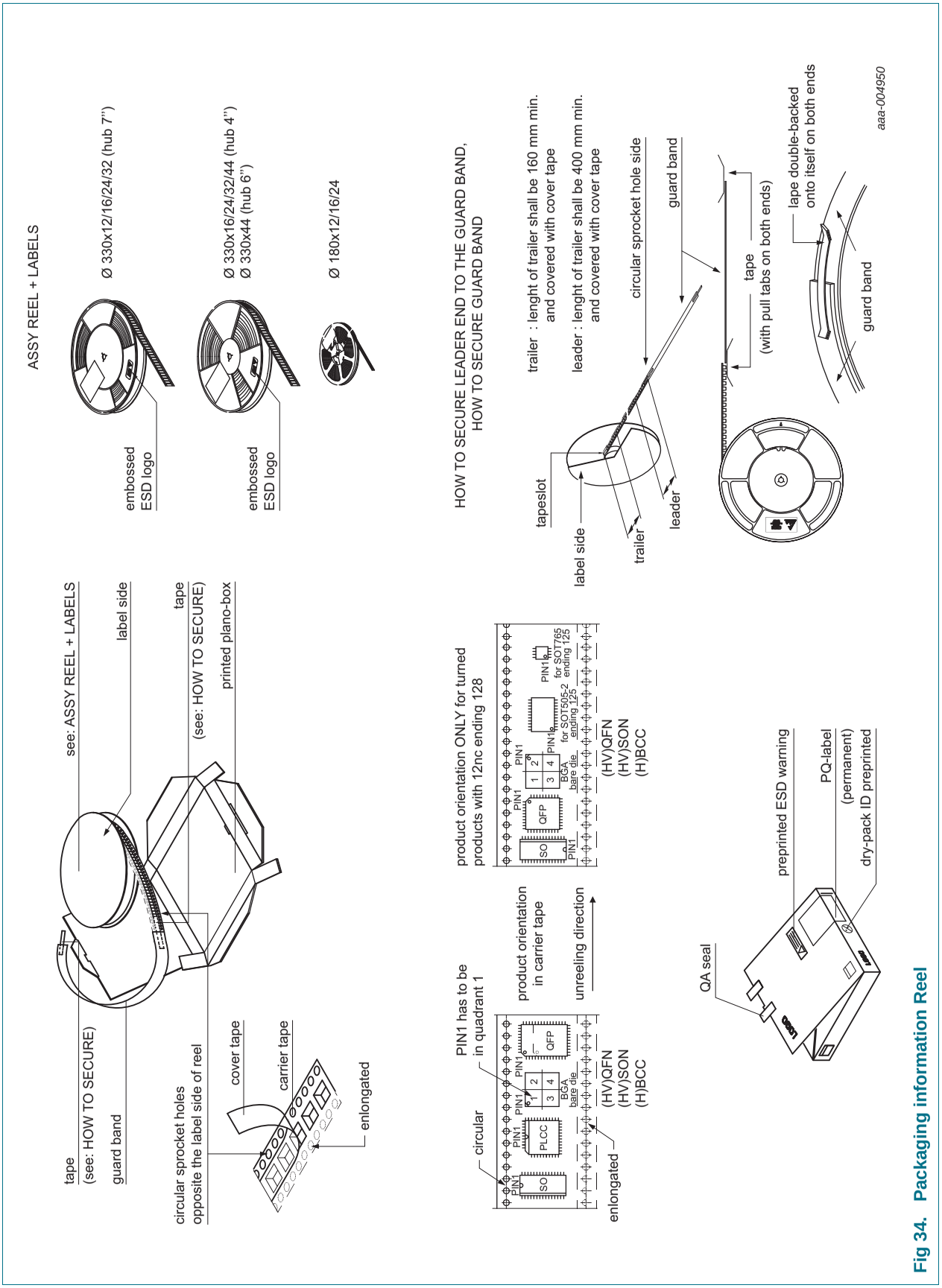

Fig 34. Packaging information Reel

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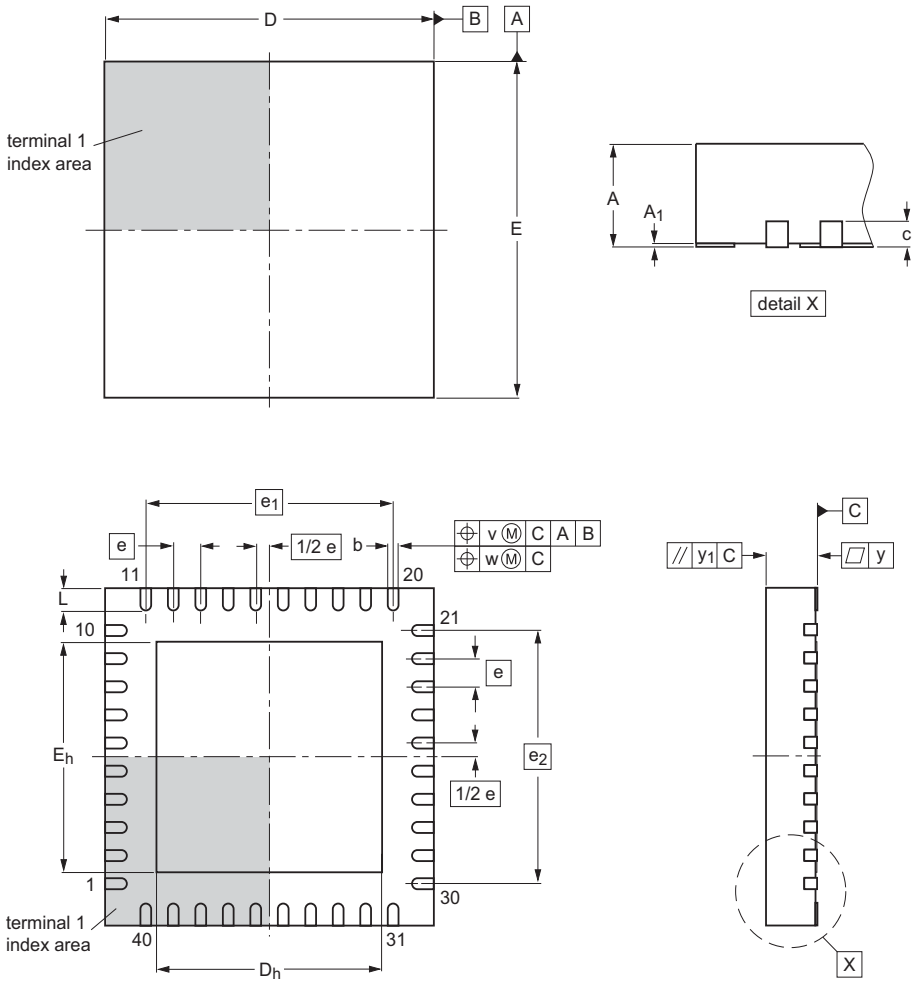
17. Package outline

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.30	0.2	6.1	4.25	6.1	4.25	0.5	4.5	4.5	0.5	0.1	0.05	0.05	0.1
mm	nom	0.85	0.02	0.21		6.0	4.10	6.0	4.10				0.4				
	min	0.80	0.00	0.18		5.9	3.95	5.9	3.95				0.3				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot618-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT618-1		MO-220				~~02-10-22~~ 13-11-05

Fig 35. Package outline SOT618-1

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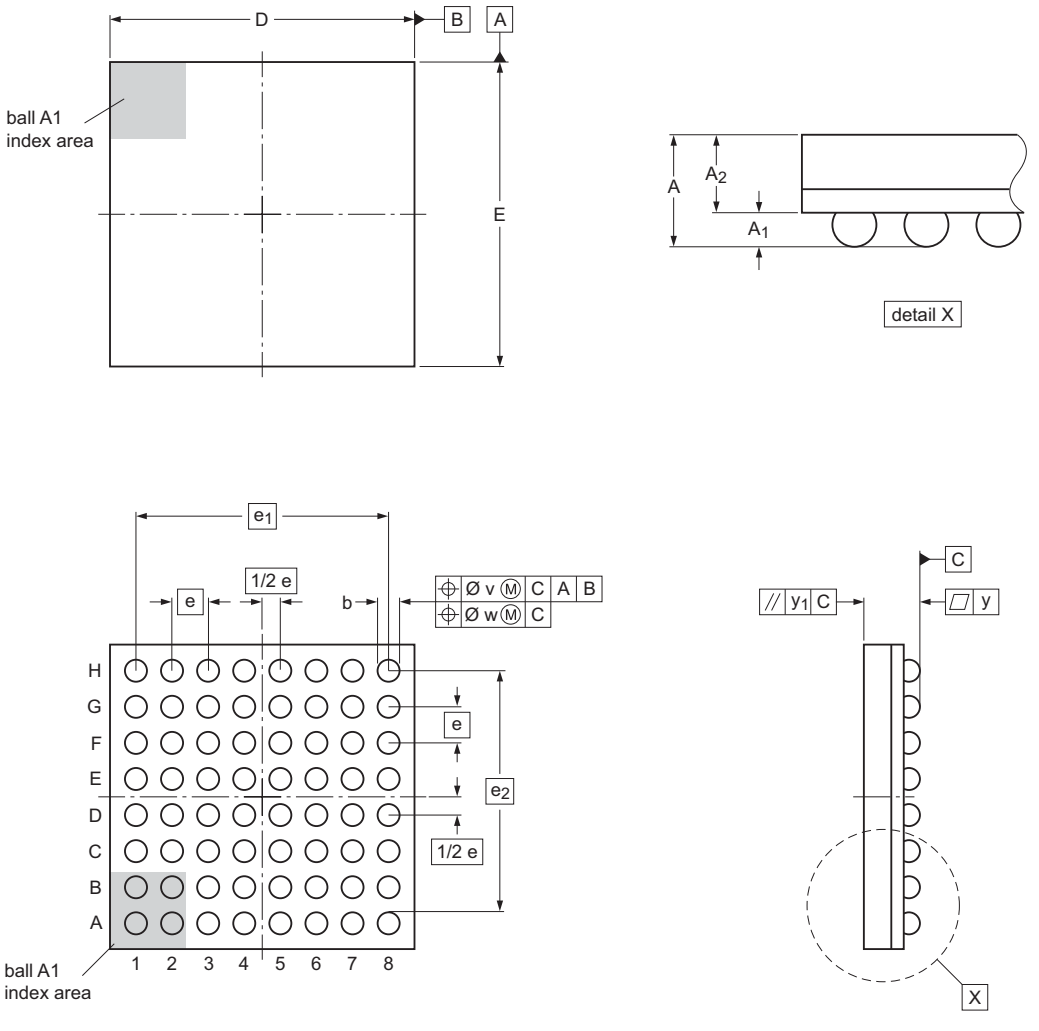
TFBGA64: plastic thin fine-pitch ball grid array package; 64 balls **SOT1336-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
	max	1.15	0.35	0.80	0.45	5.6	5.6							
mm	nom	1.00	0.30	0.70	0.40	5.5	5.5	0.65	4.55	4.55	0.15	0.08	0.1	0.1
	min	0.90	0.25	0.65	0.35	5.4	5.4							

sot1336-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1336-1		- - -				~~12-06-19~~ 12-08-28

Fig 36. Package outline package version (TFBGA64)

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18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 37) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 124 and 125

Table 124. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 125. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 37.

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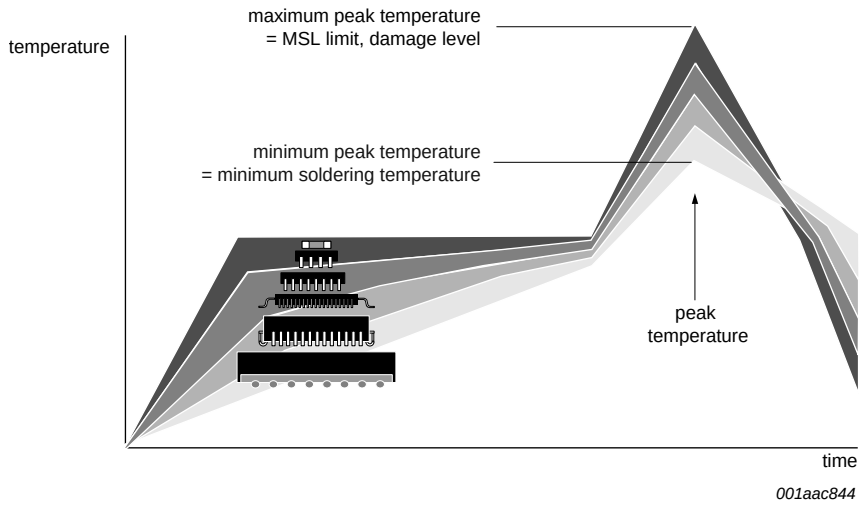

MSL: Moisture Sensitivity Level

Fig 37. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

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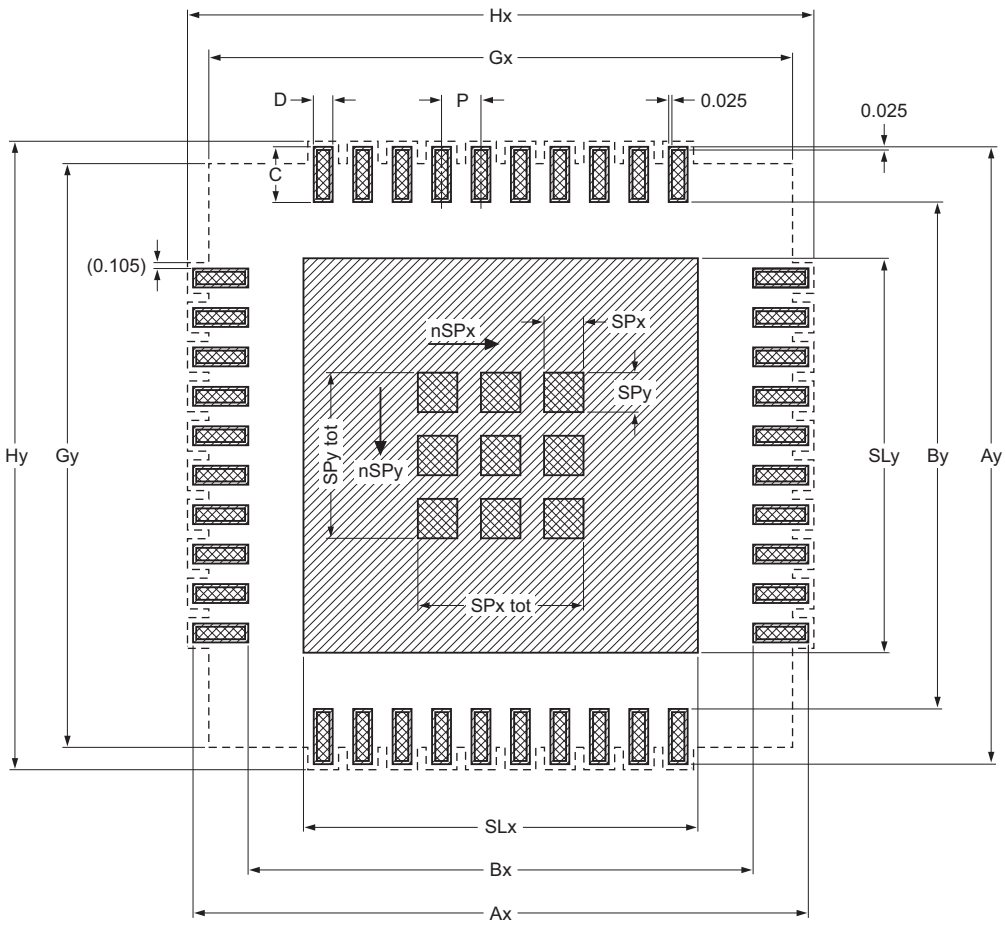
19. Soldering

Footprint information for reflow soldering of HVQFN40 package **SOT618-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

occupied area
solder resist
solder lands
solder paste

nSPx	nSPy
3	3

Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.500	7.000	7.000	5.200	5.200	0.900	0.290	4.100	4.100	2.400	2.400	0.600	0.600	6.300	6.300	7.250	7.250

Issue date ~~09-06-11~~ 14-08-13 *sot618-1_fr*

Fig 38. Soldering HVQFN40 package

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20. Appendix

20.1 Timer Delay for start of reception measurement

Table 126. Timer delay for STOP_ON_RX_STARTED configuration

Setting	Protocol	Speed (kbit/s)	Modulation	delay (us)
0x80	ISO 14443-A	106	Manch. SubC	48
0x81	ISO 14443-A	212	BPSK	24
0x82	ISO 14443-A	424	BPSK	12
0x83	ISO 14443-A	848	BPSK	6
0x84	ISO 14443-B	106	BPSK	182
0x85	ISO 14443-B	212	BPSK	91
0x86	ISO 14443-B	424	BPSK	46
0x87	ISO 14443-B	848	BPSK	23
0x88	Felica	212	-	95
0x89	Felica	424	-	48
0x8A	NFC-Active Initiator	106	-	-
0x8B	NFC-Active Initiator	212	-	-
0x8C	NFC-Active Initiator	424	-	-
0x8D	ISO 15693	26	1 out 4 / SC	321
0x8E	ISO 15693	53	1 out 4 / SC	161
0x8F	ISO 18003M3 Manch. 424_4	106	manch. 424 / 4 period	121
0x90	ISO 18003M3 Manch. 424_2	212	manch. 424 / 2 period	75
0x91	ISO 18003M3 Manch. 848_4	212	manch. 848 / 4 period	47
0x92	ISO 18003M3 Manch. 848_2	424	manch. 848 / 2 period	11
0x93	ISO 14443-A PICC	106	Miller	48
0x94	ISO 14443-A PICC	212	Miller	24
0x95	ISO 14443-A PICC	424	Miller	12
0x96	ISO 14443-A PICC	848	Miller	6
0x97	NFC Passive Target 212	212	-	95
0x98	NFC Passive Target 424	424	-	48

20.2 Default protocol settings for LOAD_RF_CONFIG, Transmitter

20.2.1 ISO/IEC 14443 A-106

Table 127. ISO/IEC 14443 A-106

Register name	Initialization value
RF_CONTROL_TX_CLK	0x74
TX_DATA_MOD	0x2350
TX_UNDERSHOOT_CONFIG	0x17
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0xDBCF43
ANT_CONTROL	0x10

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20.2.2 ISO/IEC 14443 A-212

Table 128. ISO/IEC 14443 A-212

Register name	Initialization value
RF_CONTROL_TX_CLK	0x82
TX_DATA_MOD	0x2350
TX_UNDERSHOOT_CONFIG	0x17
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0xDBCF043
ANT_CONTROL	0x10

20.2.3 ISO/IEC 14443 A-424

Table 129. ISO/IEC 14443 A-424

Register name	Initialization value
RF_CONTROL_TX_CLK	0x82
TX_DATA_MOD	0x650
TX_UNDERSHOOT_CONFIG	0x5
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0xDBCF43
ANT_CONTROL	0x10

20.2.4 ISO/IEC 14443 A-848

Table 130. ISO/IEC 14443 A-848

Register name	Initialization value
RF_CONTROL_TX_CLK	0x82
TX_DATA_MOD	0x150
TX_UNDERSHOOT_CONFIG	0x1
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0xF9EF45
ANT_CONTROL	0x10

20.2.5 ISO/IEC 14443 B-106

Table 131. ISO/IEC 14443 B-106

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0x0
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x3A4756
ANT_CONTROL	0x10

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20.2.6 ISO/IEC 14443 B-212

Table 132. ISO/IEC 14443 B-212

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0x0
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x39C746
ANT_CONTROL	0x10

20.2.7 ISO/IEC 14443 B-424

Table 133. ISO/IEC 14443 B-424

Register name	Initialization value
RF_CONTROL_TX_CLK	0x78E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0x0
TX_OVERSHOOT_CONFIG	0x1FE0013
RF_CONTROL_TX	0x71CF54
ANT_CONTROL	0x10

20.2.8 ISO/IEC 14443 B-848

Table 134. ISO/IEC 14443 B-848

Register name	Initialization value
RF_CONTROL_TX_CLK	0x78E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0x0
TX_OVERSHOOT_CONFIG	0x7E000D
RF_CONTROL_TX	0x69AF32
ANT_CONTROL	0x10

20.2.9 Felica-212

Table 135. Felica-212

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0x0
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x39E744
ANT_CONTROL	0x10

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20.2.10 Felica-424

Table 136. Felica-424

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0x0
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x39EF33
ANT_CONTROL	0x10

20.2.11 NFC active initiator A-106

Table 137. NFC active initiator A-106

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8782
TX_DATA_MOD	0x2350
TX_UNDERSHOOT_CONFIG	0x17
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0xDBCF43
ANT_CONTROL	0x10

20.2.12 NFC active initiator A-212

Table 138. NFC active initiator A-212

Register name	Initialization value
RF_CONTROL_TX_CLK	0x808E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0x0
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x39E744
ANT_CONTROL	0x10

20.2.13 NFC active initiator A-424

Table 139. NFC active initiator A-424

Register name	Initialization value
RF_CONTROL_TX_CLK	0x808E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0x0
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x39EF33
ANT_CONTROL	0x10

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20.2.14 ISO/IEC15693-26

Table 140. ISO/IEC15693-26

Register name	Initialization value
RF_CONTROL_TX_CLK	0x782
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0xF000001F
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0xDBC745
ANT_CONTROL	0x10

20.2.15 ISO/IEC15693-53

Table 141. ISO/IEC15693-53

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0xFF000F
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x3A4F44
ANT_CONTROL	0x10

20.2.16 ISO/IEC18003M3 - TARI=18.88us

Table 142. ISO/IEC18003M3 - TARI=18.88us

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0xFF000F
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x3A2734
ANT_CONTROL	0x10

20.2.17 ISO/IEC18003M3 - TARI=9.44us

Table 143. ISO/IEC18003M3 - TARI=9.44us

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0xFF000F
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x3A4734
ANT_CONTROL	0x10

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20.2.18 PICC ISO/IEC14443-A 106

Table 144. PICC ISO/IEC14443-A 106

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8000
TX_DATA_MOD	0x72
RF_CONTROL_TX	0x0
ANT_CONTROL	0xC

20.2.19 PICC ISO/IEC14443-A 212

Table 145. PICC ISO/IEC14443-A 212

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8000
TX_DATA_MOD	0x72
RF_CONTROL_TX	0x0
ANT_CONTROL	0xC

20.2.20 PICC ISO/IEC14443-A 424

Table 146. PICC ISO/IEC14443-A 424

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8000
TX_DATA_MOD	0x72
RF_CONTROL_TX	0x0
ANT_CONTROL	0xC

20.2.21 PICC ISO/IEC14443-A 848

Table 147. PICC ISO/IEC14443-A 848

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8000
TX_DATA_MOD	0x72
RF_CONTROL_TX	0x0
ANT_CONTROL	0xC

20.2.22 NFC passive target 212

Table 148. NFC passive target 212

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8000
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0x0
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x0
ANT_CONTROL	0xC

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20.2.23 NFC passive target 424

Table 149. NFC passive target 424

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8000
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0x0
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x0
ANT_CONTROL	0xC

20.2.24 NFC active target 106

Table 150. NFC active target 106

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8782
TX_DATA_MOD	0x2350
TX_UNDERSHOOT_CONFIG	0x17
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0xDBCF43
ANT_CONTROL	0x10

20.2.25 NFC active target 212

Table 151. NFC active target 212

Register name	Initialization value
RF_CONTROL_TX_CLK	0x0808E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0x0
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x39E744
ANT_CONTROL	0x10

20.2.26 NFC active target 424

Table 152. NFC active target 424

Register name	Initialization value
RF_CONTROL_TX_CLK	0x808E
TX_DATA_MOD	0x0
TX_UNDERSHOOT_CONFIG	0x0
TX_OVERSHOOT_CONFIG	0x0
RF_CONTROL_TX	0x39EF33
ANT_CONTROL	0x10

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20.2.27 NFC general target mode - all data rates

Table 153. NFC general target mode - all data rates

Register name	Initialization value
RF_CONTROL_TX_CLK	0x8000
TX_DATA_MOD	0x72

20.3 Default protocol settings for LOAD_RF_CONFIG, Receiver

20.3.1 ISO/IEC 14443 A-106

Table 154. ISO/IEC 14443 A-106

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x804B
ANA_RX_POWER_CONTROL_RFU	0x200
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0x430DC
RF_CONTROL_RX	0x1E

20.3.2 ISO/IEC 14443 A-212

Table 155. ISO/IEC 14443 A-212

Register name	Initialization value
AGC_VALUE	0x0x801F0801F0
AGC_CONFIG	0x860B
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0x430DC
RF_CONTROL_RX	0x1E

20.3.3 ISO/IEC 14443 A-424

Table 156. ISO/IEC 14443 A-424

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x860B
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0x192905
RF_CONTROL_RX	0x16

20.3.4 ISO/IEC 14443 A-848

Table 157. ISO/IEC 14443 A-848

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x860B

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Table 157. ISO/IEC 14443 A-848

Register name	Initialization value
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0xF2505
RF_CONTROL_RX	0x11

20.3.5 ISO/IEC 14443 B-106

Table 158. ISO/IEC 14443 B-106

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x860B
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0x1F2415
RF_CONTROL_RX	0x16

20.3.6 ISO/IEC 14443 B-212

Table 159. ISO/IEC 14443 B-212

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x860B
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0x192805
RF_CONTROL_RX	0x16

20.3.7 ISO/IEC 14443 B-424

Table 160. ISO/IEC 14443 B-424

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x860B
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0x192A05
RF_CONTROL_RX	0x16

20.3.8 ISO/IEC 14443 B-848

Table 161. ISO/IEC 14443 B-848

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x860B
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0xF2505
RF_CONTROL_RX	0x1A

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20.3.9 Felica 212

Table 162. Felica 212

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x860B
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0xF2605
RF_CONTROL_RX	0x11

20.3.10 Felica 424

Table 163. Felica 424

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x860B
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0x2605
RF_CONTROL_RX	0x15

20.3.11 NFC Active Initiator 106

Table 164. NFC Active Initiator 106

Register name	Initialization value
AGC_VALUE	0xC0150
AGC_CONFIG	0xA00B
RX_RFU	0x1
SIGPRO_CM_CONFIG	0x0
RF_CONTROL_RX	0x23

20.3.12 NFC Active Initiator 212

Table 165. NFC Active Initiator 212

Register name	Initialization value
AGC_VALUE	0xC0150
AGC_CONFIG	0xA00B
SIGPRO_CM_CONFIG	0x50010060
RF_CONTROL_RX	0x23

20.3.13 NFC Active Initiator 424

Table 166. NFC Active Initiator 424

Register name	Initialization value
AGC_VALUE	0xC0150
AGC_CONFIG	0xA00B
SIGPRO_CM_CONFIG	0x50010060
RF_CONTROL_RX	0x23

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20.3.14 ISO/IEC 15693-26

Table 167. ISO/IEC 15693-26

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x804B
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0x4010
RF_CONTROL_RX	0x1A

20.3.15 ISO/IEC 15693-53

Table 168. ISO/IEC 15693-53

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x804B
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0xC4010
RF_CONTROL_RX	0x1A

20.3.16 ISO 18003M3- Tari 18.88

Table 169. ISO 18003M3- Tari 18.88

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x860B
SIGPRO_CM_CONFIG	0x0
SIGPRO_CM_CONFIG_RFU	0x0
SIGPRO_RM_CONFIG	0x8014
RF_CONTROL_RX	0x1A

20.3.17 ISO 18003M3- Tari 9.44 848_2

Table 170. ISO 18003M3- Tari 9.44 848_2

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x860B
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0xC6014
SIGPRO_CM_CONFIG2_RFU	0x1

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20.3.18 ISO 18003M3- Tari 9.44 -848_4

Table 171. ISO18003M3- Tari 9.44 -848_4

Register name	Initialization value
AGC_VALUE	0x801F0
AGC_CONFIG	0x860B
SIGPRO_CM_CONFIG	0x0
SIGPRO_RM_CONFIG	0xC8094
RF_CONTROL_RX	0x1F

20.3.19 ISO 14443A-PICC 106

Table 172. ISO 14443A-PICC 106

Register name	Initialization value
AGC_CONFIG	0xA003
RX_RFU	0x1
SIGPRO_CM_CONFIG	0x1000801C
RF_CONTROL_RX	0x23

20.3.20 ISO 14443A-PICC 212

Table 173. ISO 14443A-PICC 212

Register name	Initialization value
AGC_CONFIG	0xA003
SIGPRO_CM_CONFIG	0x1C0600E0
RF_CONTROL_RX	0xE3

20.3.21 ISO 14443A-PICC 424

Table 174. ISO 14443A-PICC 424

Register name	Initialization value
AGC_CONFIG	0xA003
SIGPRO_CM_CONFIG	0x14040040
RF_CONTROL_RX	0x23

20.3.22 ISO 14443A-PICC 848

Table 175. ISO 14443A-PICC 848

Register name	Initialization value
AGC_CONFIG	0xA003
SIGPRO_CM_CONFIG	0x8030040
RF_CONTROL_RX	0x2F

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20.3.23 NFC-Passive target -212

Table 176. NFC-Passive target -212

Register name	Initialization value
AGC_CONFIG	0xA003
SIGPRO_CM_CONFIG	0x50010060
RF_CONTROL_RX	0x23

20.3.24 NFC-Passive target -424

Table 177. NFC-Passive target -424

Register name	Initialization value
AGC_CONFIG	0xA003
SIGPRO_CM_CONFIG	0x50010060
RF_CONTROL_RX	0x23

20.3.25 NFC-active target - 106

Table 178. NFC-active target - 106

Register name	Initialization value
AGC_VALUE	0xC0150
AGC_CONFIG	0xA00B
SIGPRO_CM_CONFIG	0x0
RF_CONTROL_RX	0x23

20.3.26 NFC-active target - 212

Table 179. NFC-active target - 212

Register name	Initialization value
AGC_VALUE	0xC0150
AGC_CONFIG	0xA00B
SIGPRO_CM_CONFIG	0x50010060
RF_CONTROL_RX	0x23

20.3.27 NFC-active target - 424

Table 180. NFC-active target - 424

Register name	Initialization value
AGC_VALUE	0xC0150
AGC_CONFIG	0xA00B
SIGPRO_CM_CONFIG	0x50010060
RF_CONTROL_RX	0x23

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20.3.28 NFC-General target mode - all data rates

Table 181. NFC-General target mode - all data rates

Register name	Initialization value
AGC_VALUE	0xC0150
AGC_CONFIG	0xA003
SIGPRO_CM_CONFIG	0x10010060
RF_CONTROL_RX	0x23

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21. Abbreviations

Table 182. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AWC	Adaptive Waveform Control
BPSK	Binary Phase Shift Keying
BBA	Base Band Amplifier
CRC	Cyclic Redundancy Check
DPC	Dynamic Power Control
EGT	Extra Guard Time
EMC	ElectroMagnetic Compatibility
EMD	ElectroMagnetic Disturbance
EOF	End Of Frame
ETU	Elementary Time Unit
HBM	Human Body Model
LFO	Low Frequency Oscillator
LPCD	Low-Power Card Detection
LSB	Least Significant Bit
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
NRZ	Not Return to Zero
NSS	Not Slave Select
PCD	Proximity Coupling Device
PLL	Phase-Locked Loop
RZ	Return To Zero
RX	Receiver
SOF	Start Of Frame
SPI	Serial Peripheral Interface
SW	Software
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter
UID	Unique Identification

22. References

[1] **ISO/IEC 14443 —** parts 2: 2001 COR 1 2007 (01/11/2007), part 3: 2001 COR 1 2006 (01/09/2006) and part 4: 2nd edition 2008 (15/07/2008)

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23. Revision history

Table 183. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PN5180 v. 2.2	20151217	Preliminary data sheet	-	PN5180 v. 2.1
Modifications:	• Section 10.4.3.2 “RF Buffer”: Size of RX buffer corrected to 508 bytes • Waveform control description added • Figure 30 “Application diagram with minimum components”: updated			
PN5180 v. 2.1	20151126	Preliminary data sheet	-	PN5180 v. 2.0
Modifications:	• Minor updates			
PN5180 v. 2.0	20151124	Preliminary data sheet	-	-

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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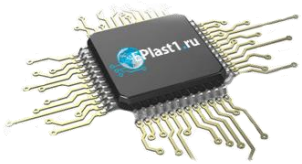

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