

## LOW VOLTAGE VIDEO AMPLIFIER WITH LPF

### ■GENERAL DESCRIPTION

The **NJM2563** is a Low Voltage Video Amplifier contained LPF circuit. Internal 75Ω driver is easy to connect TV monitor directly.

The **NJM2563** features low power and small package, and is suitable for low power design on downsizing of DSC and DVC.

### ■PACKAGE OUTLINE

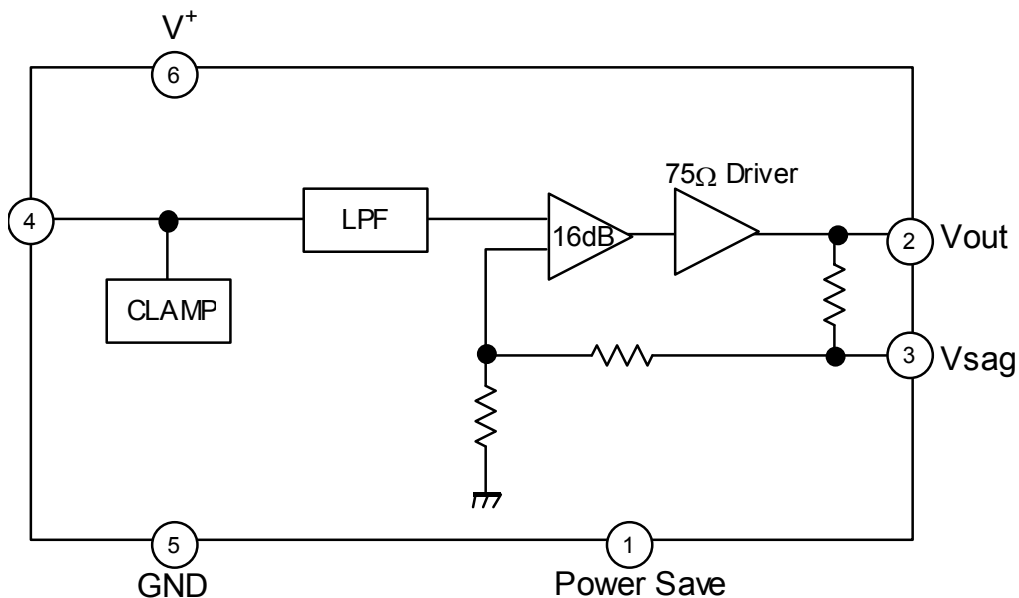
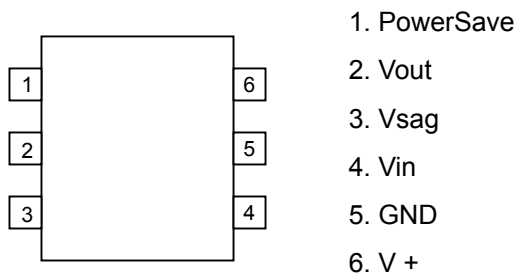


**NJM2563F1**

### ■FEATURES

- Operating Voltage                    2.8 to 5.5V
- 16dB amplifier
- Internal LPF                            -31dB at 19MHz typ.
- Internal 75Ω Driver Circuit (2-system drive)
- Power Save Circuit
- Bipolar Technology
- Package Outline                        MTP6

### ■BLOCK DIAGRAM



# NJM2563

## ■ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V <sup>+</sup>	7.0	V
Power Dissipation	P <sub>D</sub>	200	mW
Operating Temperature Range	T <sub>opr</sub>	-40 to +85	°C
Storage Temperature Range	T <sub>stg</sub>	-40 to +125	°C

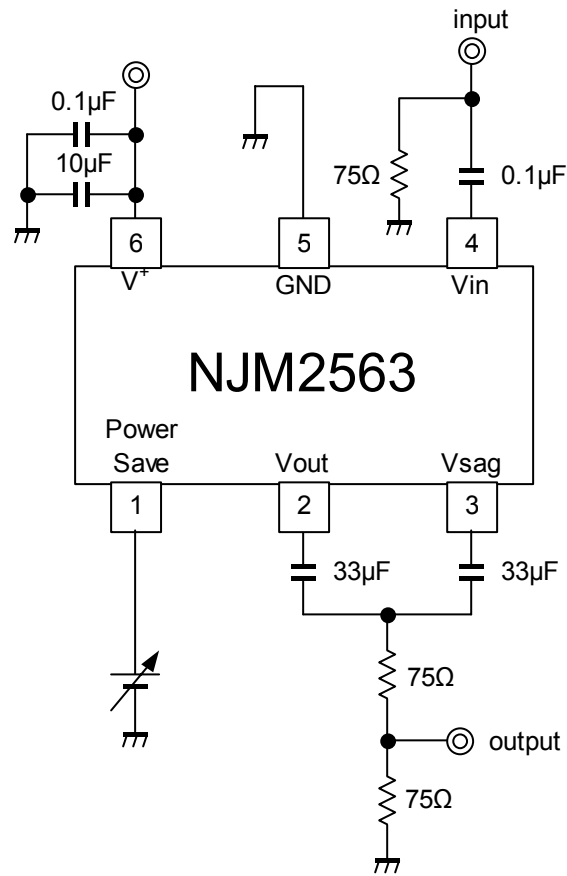
## ■ELECTRICAL CHARACTERISTICS (V<sup>+</sup>=3.0V, R<sub>L</sub>=150Ω, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I <sub>CC</sub>	No Signal	-	8.0	12.0	mA
Operating Current at Power Save	I <sub>save</sub>	Power Save Mode	-	30	50	μA
Maximum Output Voltage Swing	V <sub>omv</sub>	f=100kHz, THD=1%	2.2	2.5	-	Vp-p
Voltage Gain	G <sub>v</sub>	V <sub>in</sub> =100kHz, 0.3Vp-p, Input Sine Signal	16.1	16.5	16.9	dB
Low Pass Filter Characteristic	G <sub>fy</sub> 4.5M	V <sub>in</sub> =4.5MHz/100kHz, 0.3Vp-p	-0.6	-0.1	0.4	dB
	G <sub>fy</sub> 19M	V <sub>in</sub> =19MHz/100kHz, 0.3Vp-p	-	-31	-21	
Differential Gain	DG	V <sub>in</sub> =0.3Vp-p, 10step Video Signal	-	0.5	-	%
Differential Phase	DP	V <sub>in</sub> =0.3Vp-p, 10step Video Signal	-	0.5	-	deg
S/N Ratio	SN <sub>v</sub>	V <sub>in</sub> =0.3Vp-p, R <sub>L</sub> =75Ω 100% White Video Signal, 100KHz to 6MHz	-	+60	-	dB
2nd. Distortion	H <sub>v</sub>	V <sub>in</sub> =0.3Vp-p, 3.58MHz, Sine Signal, R <sub>L</sub> =75Ω	-	-50	-	dB
SW Change Voltage High Level	V <sub>thPH</sub>	Active	1.8	-	V <sup>+</sup>	V
SW Change Voltage Low Level	V <sub>thPL</sub>	Non-active	0	-	0.3	

## ■CONTROL TERMINAL

PARAMETER	STATUS	NOTE
Power Save	H	Power Save: OFF
	L	Power Save: ON
	OPEN	Power Save: ON

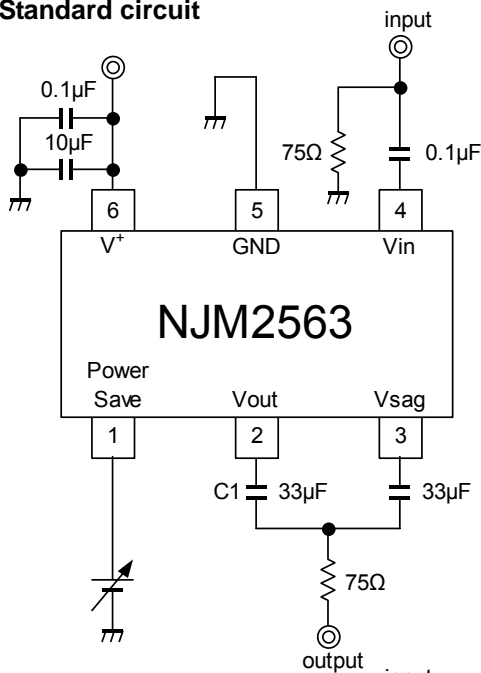
## TEST CIRCUIT



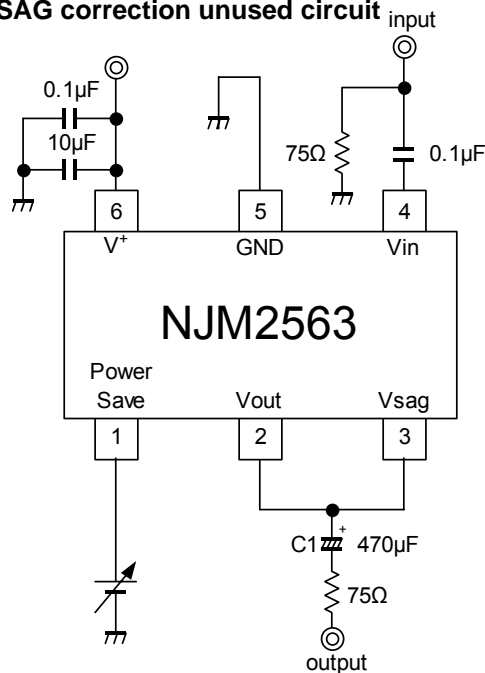
# NJM2563

## APPLICATION CIRCUIT

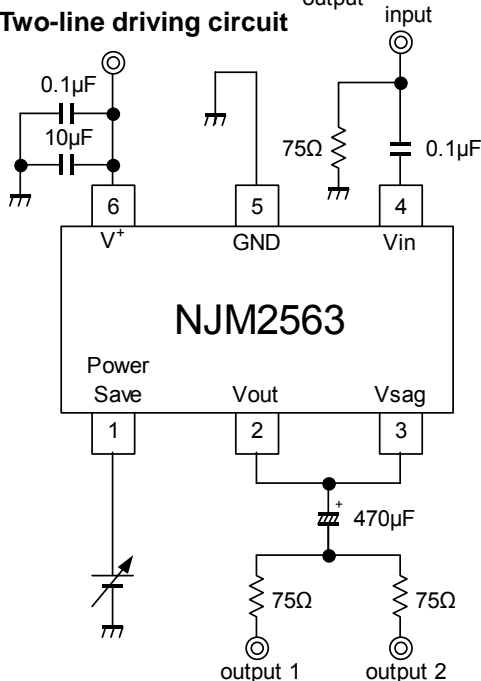
### (1) Standard circuit



### (2) SAG correction unused circuit



### (3) Two-line driving circuit



### (1) Standard circuit

The SAG correction reduces output coupling capacitor values. The capacitor of C1 (33µF) is recommended for the portable application. However, the 33µF capacitor may deteriorate SAG, and lose synchronization by luminance fluctuation. Adjust the C1 value, checking the waveform containing a lot of low frequency components like a bounce waveform (In case of worst condition). Change the capacitor of C1 into a large value to improve SAG.

### (2) SAG correction unused circuit

Cancel the SAG correction to improve lost synchronization. Connect the coupling capacitor after connecting the Vout pin and Vsag pin. The recommended value is 470µF or more.

### (3) Two-line driving circuit

The NJM2563 drives two-line load of 150Ω. The capacitance value of C1 should be 100µF or more, because SAG is deteriorated than a standard circuit.

## ■ TERMINAL DESCRIPTION

No.	SYMBOL	VOLTAGE	EQUIVALENT CIRCUIT
1	Power Save	-	
2	Vout	0.33V	
3	Vsag	-	
4	Vin	1.10V	
5	GND	-	
6	V+	3V	

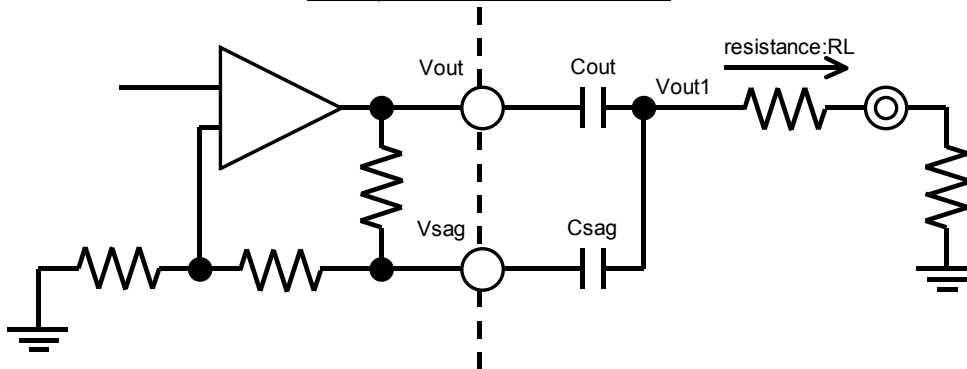
## APPLICATION

### ◆ SAG correction circuit

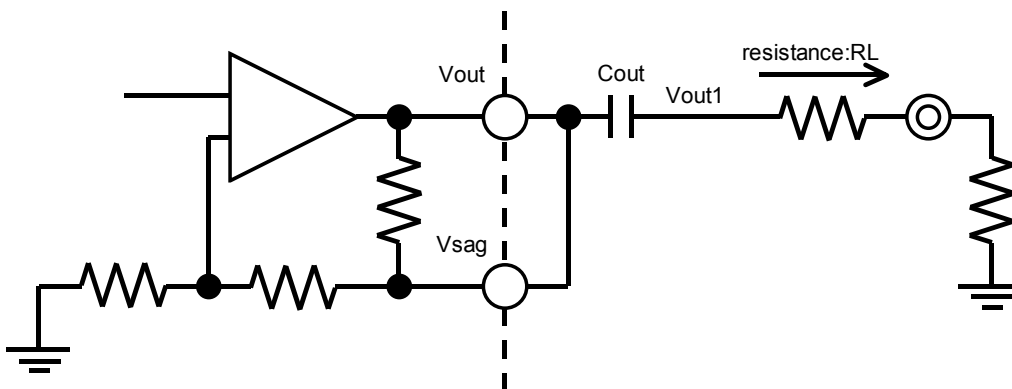
SAG correction circuit is a circuit to correct for low-frequency attenuation by high-pass filter consisting of the output coupling capacitance and load resistance. Low-frequency attenuation raises the sag in the vertical period of the video signal.

Capacitor for  $V_{sag}$  ( $C_{sag}$ ) is connected to the negative feedback of the amplifier. This  $C_{sag}$  increase the low frequency gain to correct for the attenuation of low frequency gain.

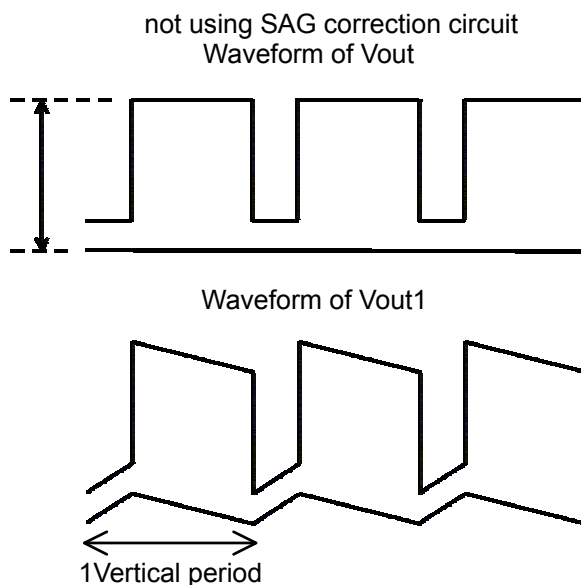
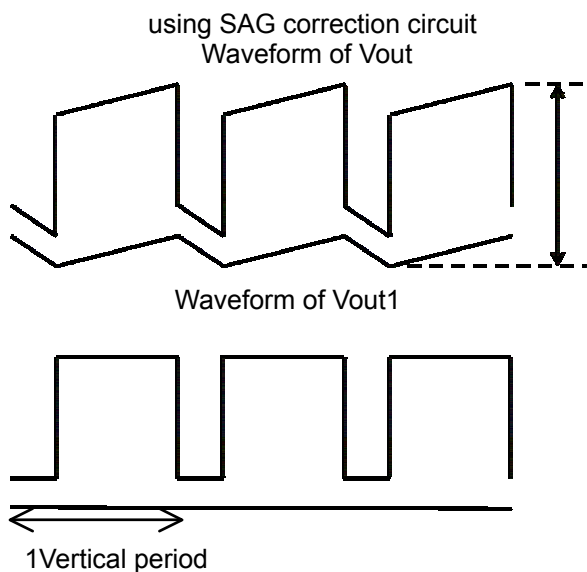
Example SAG collection circuit



Example of not using sag compensation circuit

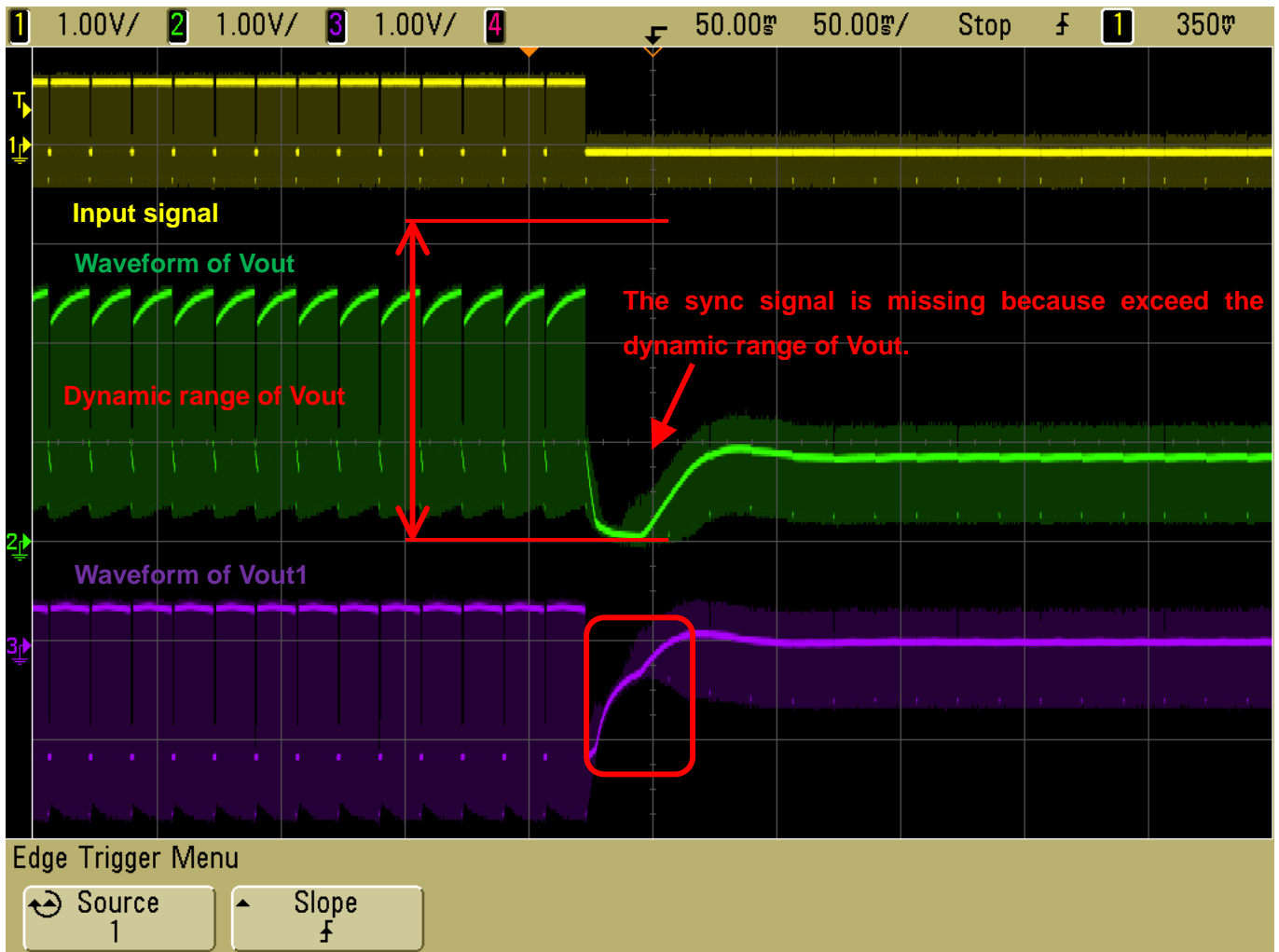


Waveform of Vout terminal and Vout1 terminal



SAG correction circuit generates a low frequency component signal amplified to Vout terminal. Changes of the luminance signal will be low-frequency components, if you want to output a large signal luminance changes. Therefore, generate correction signal of change of a luminance signal to Vout pin. At this time, signal is over the dynamic range of Vout pin. This may cause a lack of sync signal, and waveform distortion.

Please see diagram below (green waveform), if you want to output large changes of a signal luminance, such as 100% white video signal and black signal. Thus, output signal exceed dynamic range of Vout pin and may be the signal lack.



## < Countermeasure for waveform distortion >

1. Please using small value the Sag compensation capacitor (VSAG).

It can ensure the dynamic range by using small value the capacitor (VSAG). It because of low-frequency variation of Vout pin is smaller. However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

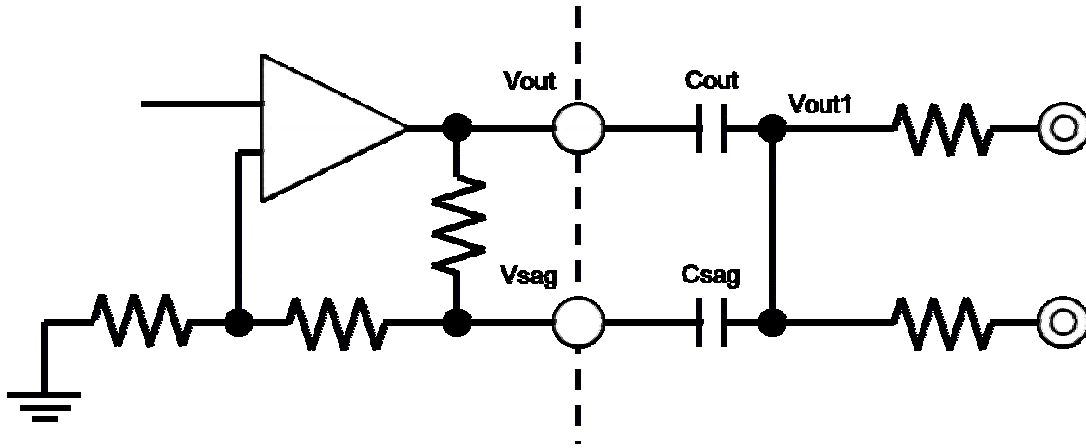
2. Please do not use the sag correction circuit.

Signal can output within dynamic range for reason it does not change the DC level of the output terminal. However, the output (VOUT) must be use large capacitor for this reason sag characteristics become exacerbated.

< Dual drive at using SAG correction circuit >

Using sag correction circuit at dual drive circuit is below. Dual drives are less load resistance. Thus, the cut-off frequency of HPF that is composed of the output capacitor and load resistance will be small. Therefore, the sag characteristics deteriorate.

Please size up to the output capacitor (Vout) for not to deteriorate the sag characteristics.



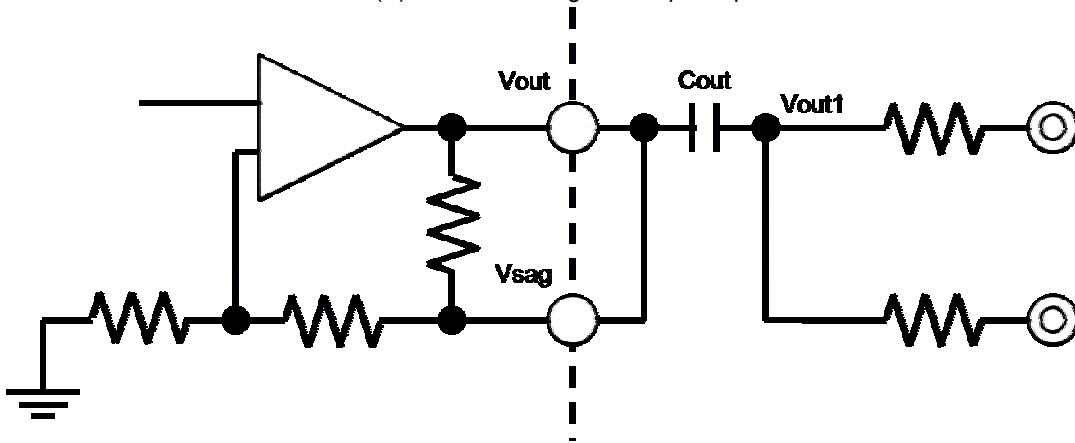
< Dual drive at not using SAG correction circuit >

We recommended two-example dual drive circuit with not use sag correction circuit. Please change the configuration to be used according to the situation. Please configure to meet the following conditions. Then you can adjust the characteristics of each configuration.

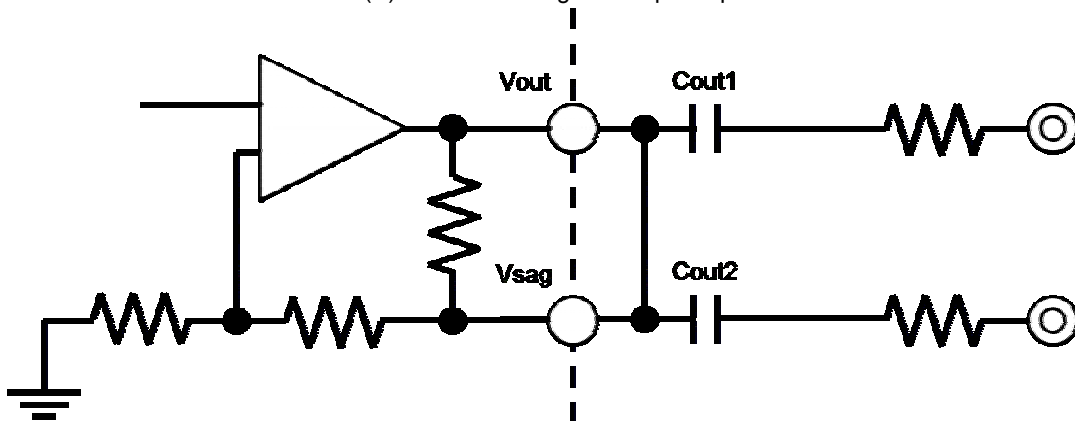
$$C_{out} = C_{out1} + C_{out2}$$

$$C_{out1} = C_{out2}$$

(A) In case of using one output capacitor



(B) In case of using two output capacitors

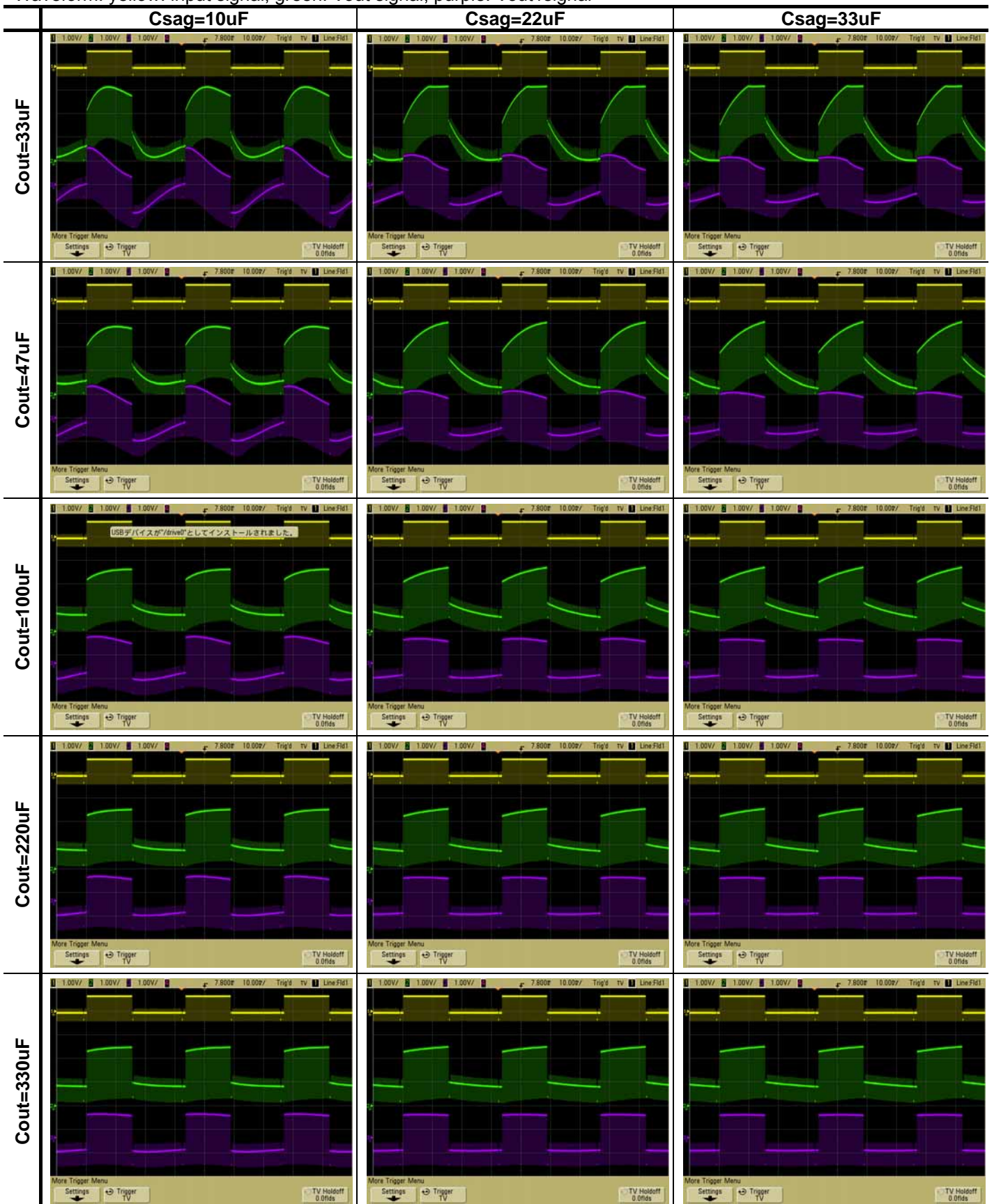




< Using SAG correction circuit >

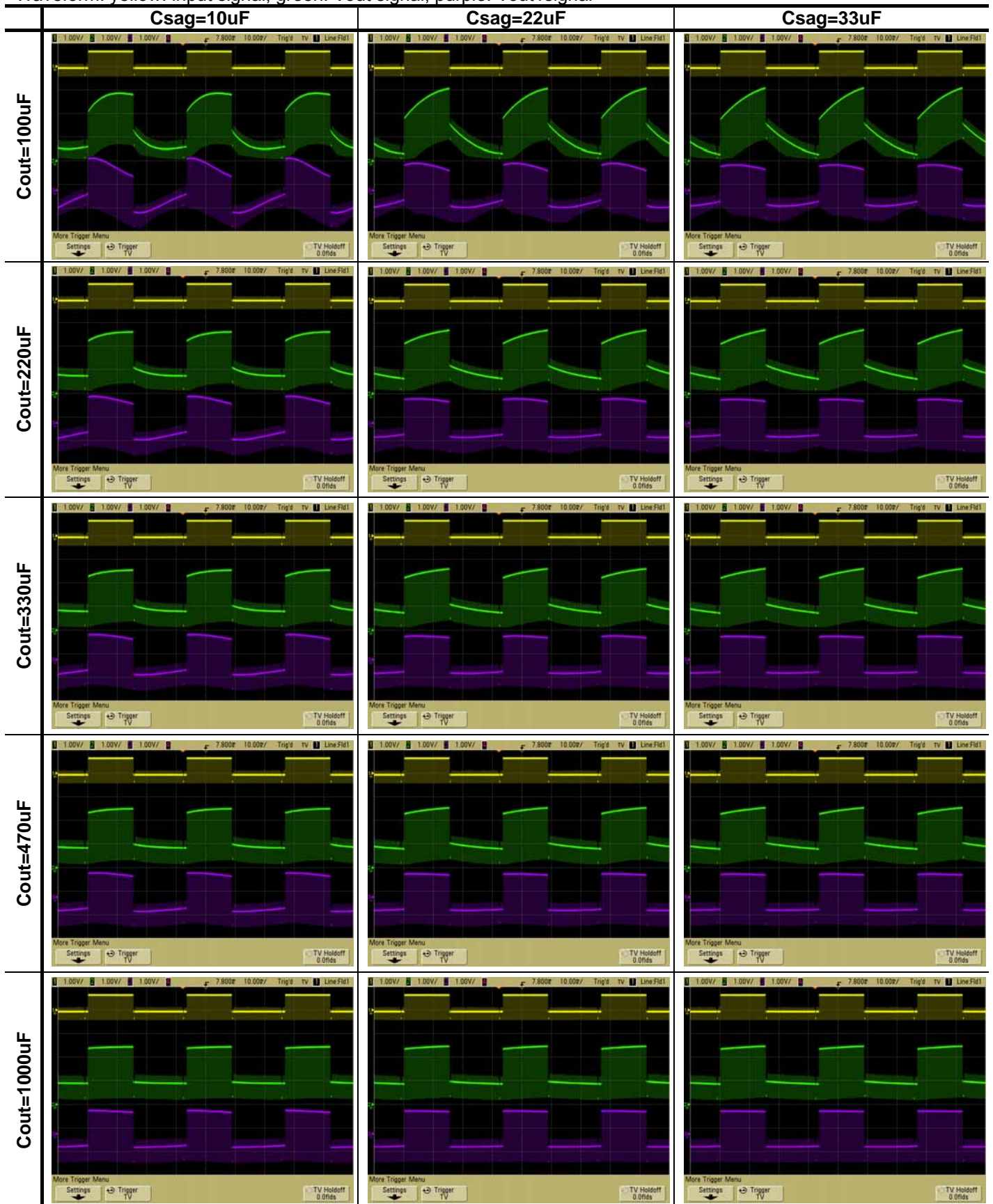
Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal



# NJM2563

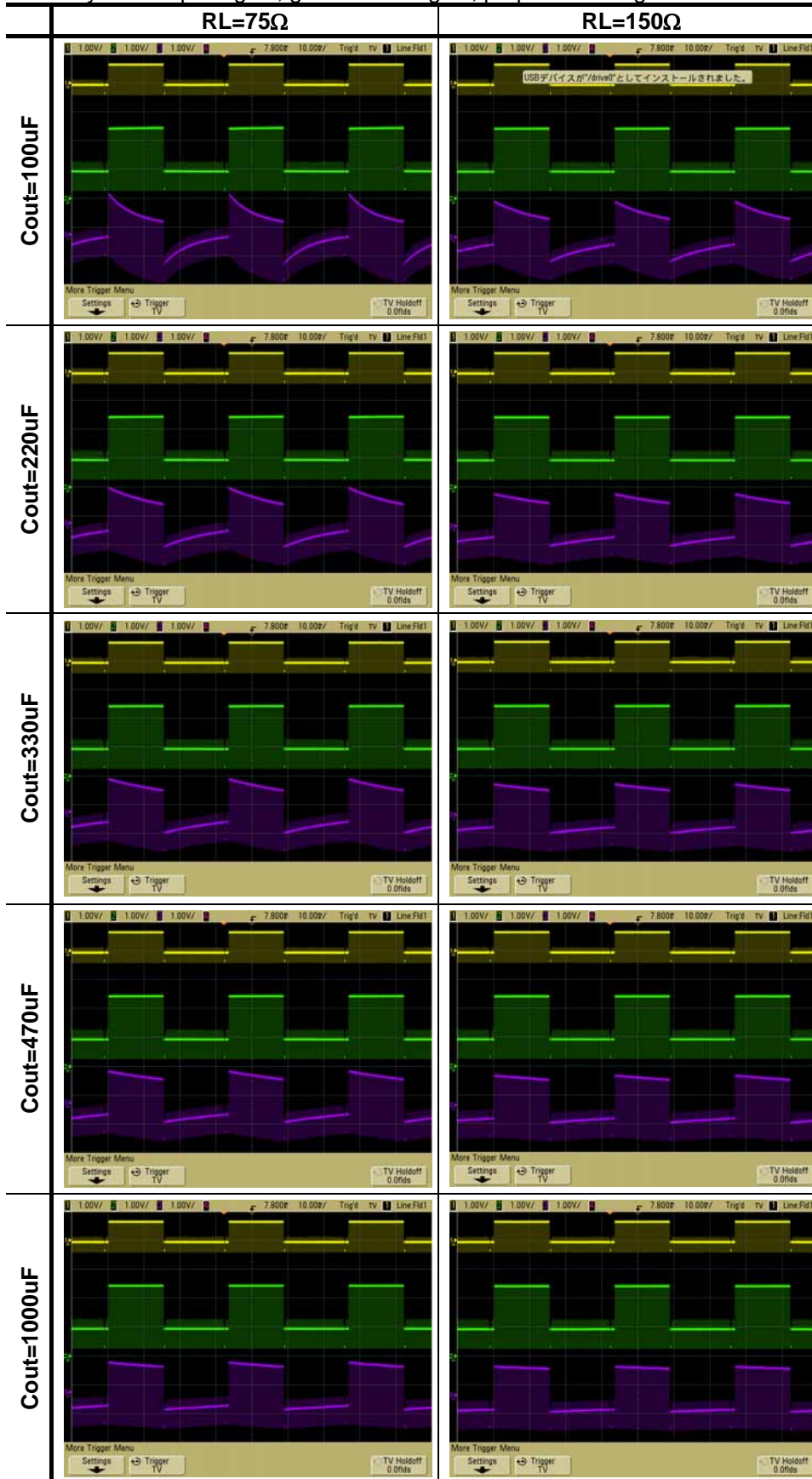
Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω  
 Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal



< Not using SAG correction circuit >

Input signal: bounce signal (IRE0%, IRE100%, 30Hz), resistance=150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1 signal

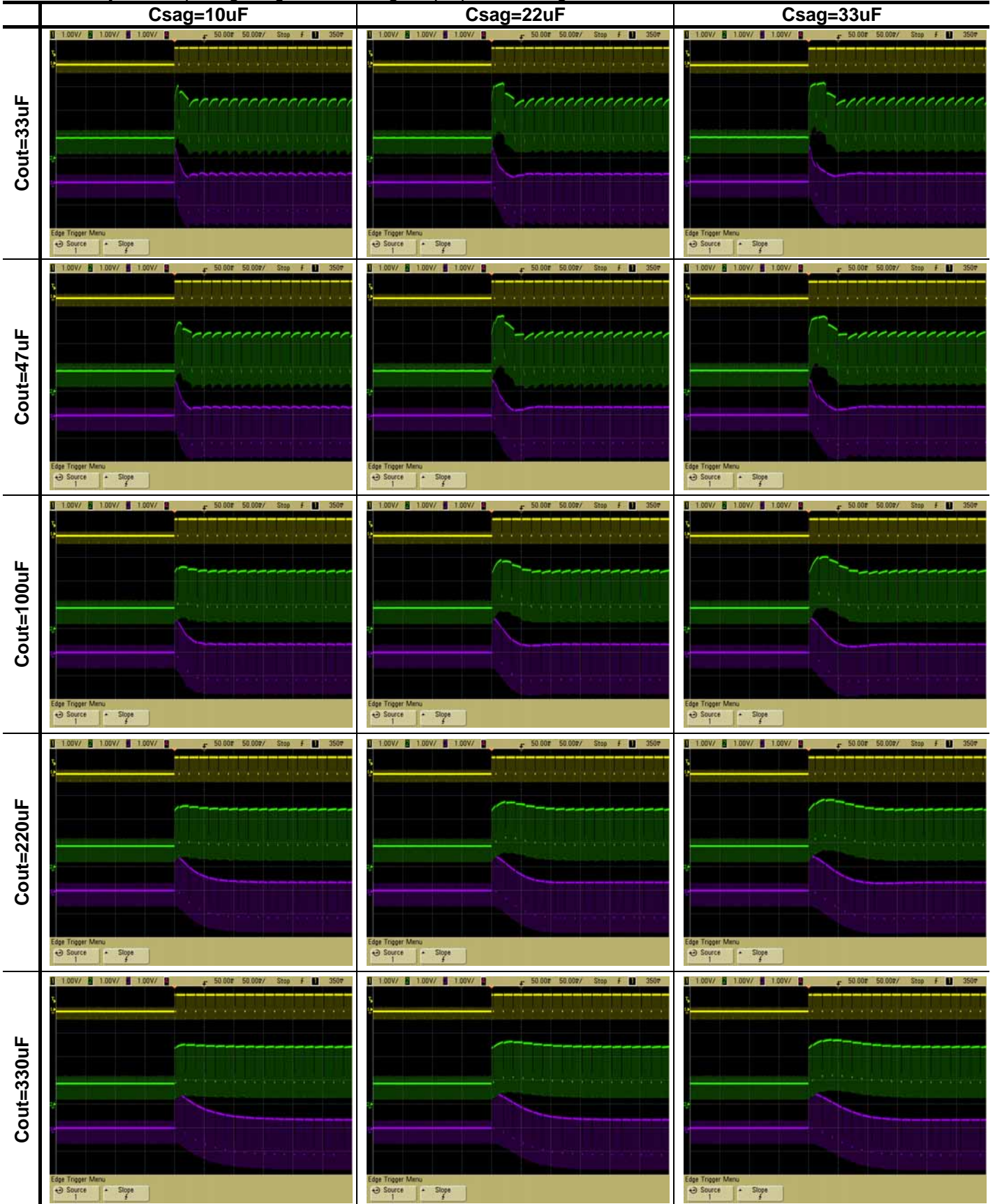


# NJM2563

< Using SAG correction circuit >

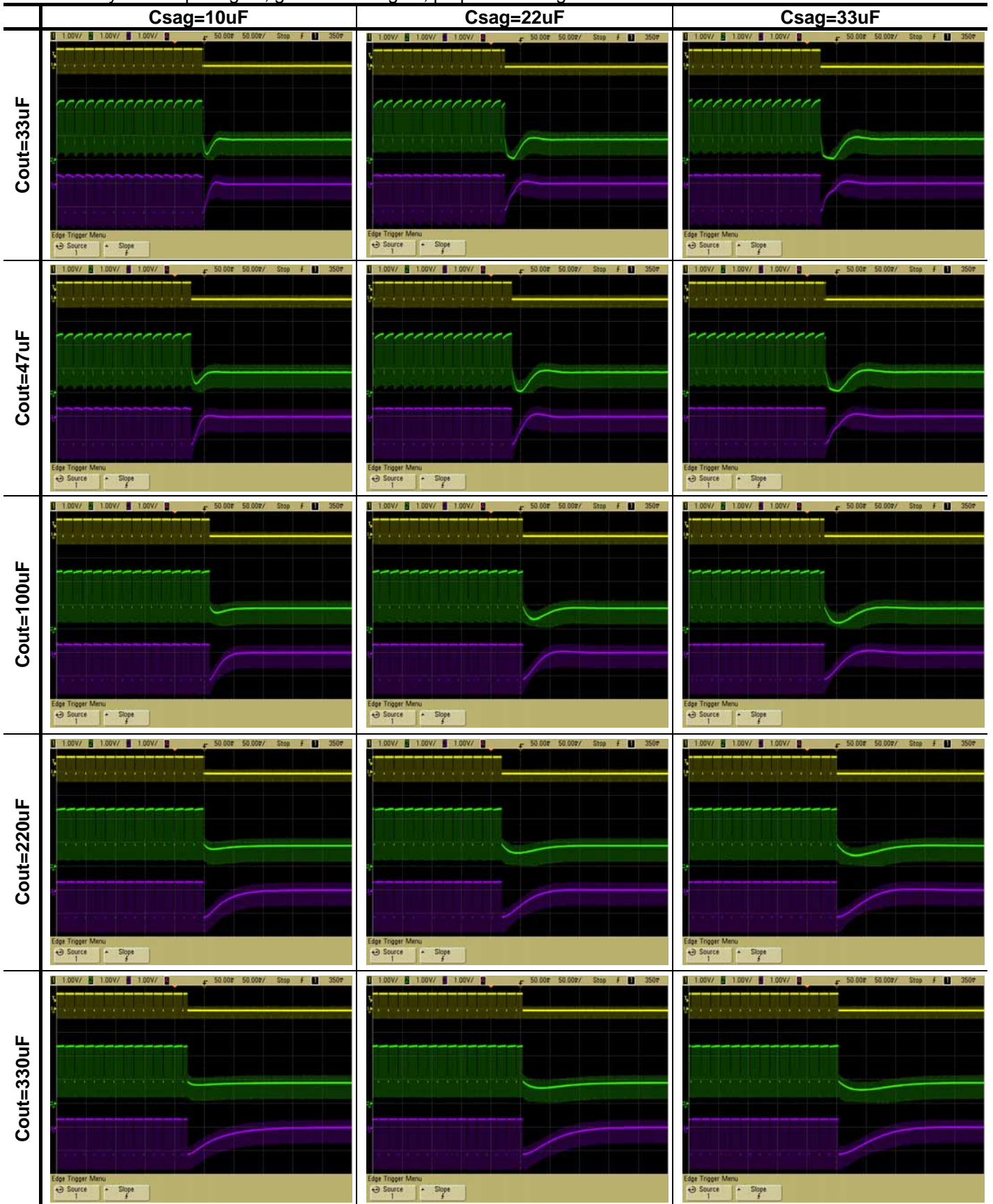
Input signal: Black to White 100%, resistance 150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal



Input signal: White100% to Black, resistance150Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal

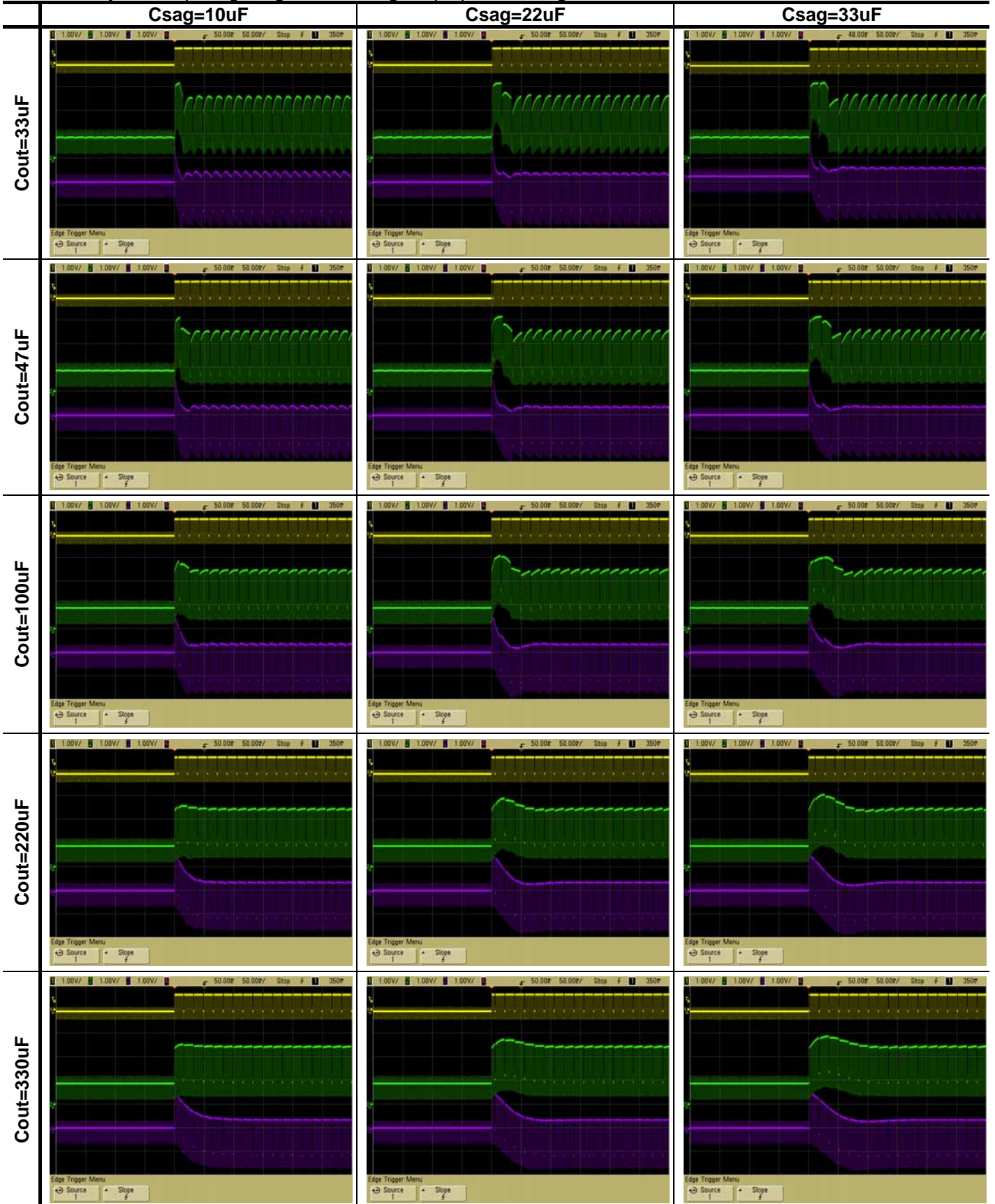


# NJM2563

< Using SAG correction circuit >

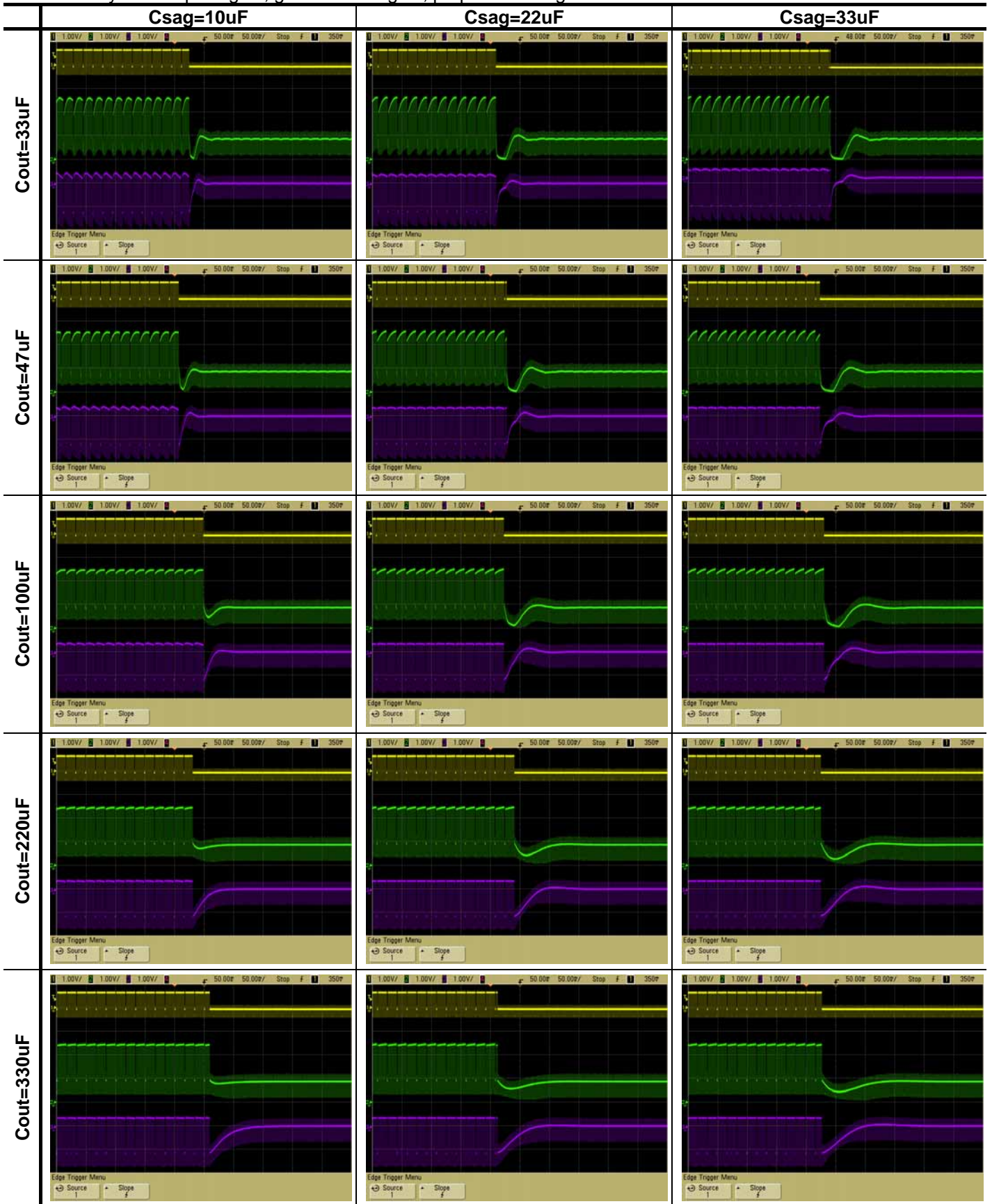
Input signal: Black to White 100%, resistance=75Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal



Input signal: White100% to Black, resistance=75Ω

Waveform: yellow: input signal, green: Vout signal, purple: Vout1signal



## ◆ Clamp circuit

### 1. Operation of Sync-tip-clamp

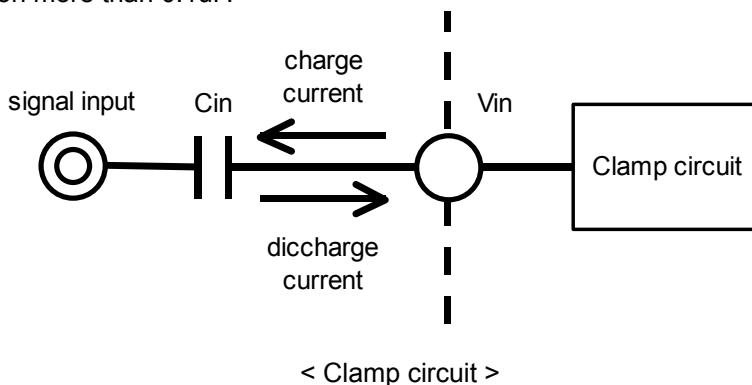
Input circuit will be explained. Sync-tip clamp circuit (below the clamp circuit) operates to keep a sync tip of the minimum potential of the video signal. Clamp circuit is a circuit of the capacitor charging and discharging of the external input  $C_{in}$ . It is charged to the capacitor to the external input  $C_{in}$  at sync tip of the video signal. Therefore, the potential of the sync tip is fixed.

And it is discharged charge by capacitor  $C_{in}$  at period other than the video signal sync tip. This is due to a small discharge current to the IC.

In this way, this clamp circuit is fixed sync tip of video signal to a constant potential from charging of  $C_{in}$  and discharging of  $C_{in}$  at every one horizontal period of the video signal.

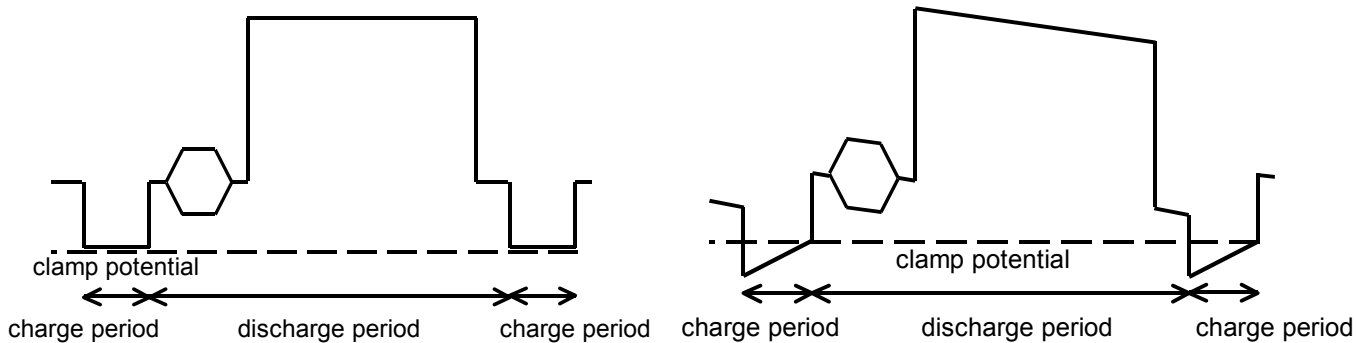
The minute current be discharged an electrical charge from the input capacitor at the period other than the sync tip of video signals. Decrease of voltage on discharge is dependent on the size of the input capacitor  $C_{in}$ .

If you decrease the value of the input capacitor, will cause distortion, called the H sag. Therefore, the input capacitor recommend on more than 0.1 $\mu$ F.



A.  $C_{in}$  is large

B.  $C_{in}$  is small (H sag experience)



< Waveform of input terminal >

### 2. Input impedance

The input impedance of the clamp circuit is different at the capacitor discharge period and the charge period.

The input impedance of the charging period is a few  $k\Omega$ . On the other hand, the input impedance of the discharge period is several  $M\Omega$ . Because is a small discharge-current through to the IC.

Thus the input impedance will vary depending on the operating state of the clamp circuit.

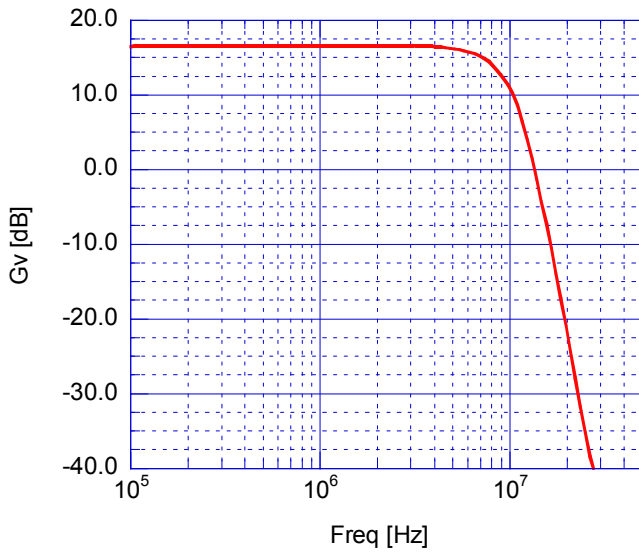
### 3. Impedance of signal source

Source impedance to the input terminal, please lower than 200 $\Omega$ . A high source impedance, the signal may be distorted. If so, please to connect a buffer for impedance conversion.

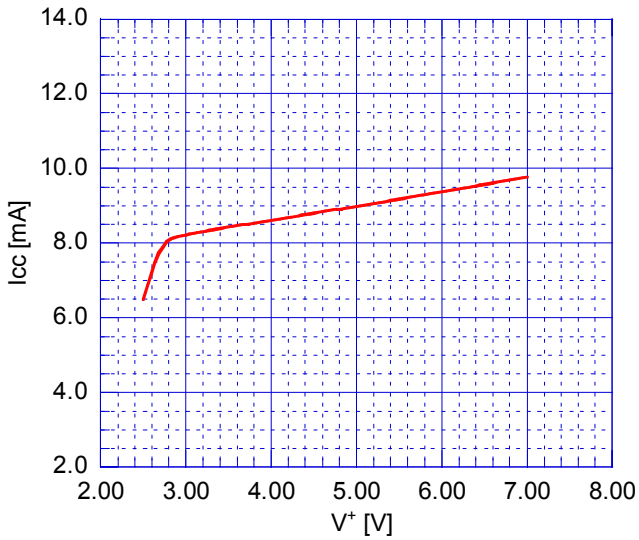


## TYPICAL CHARACTERISTICS

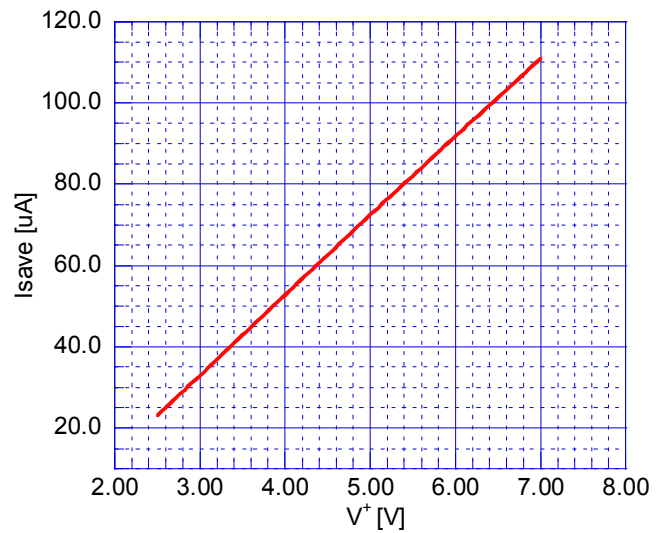
### Voltage Gain vs. Frequency



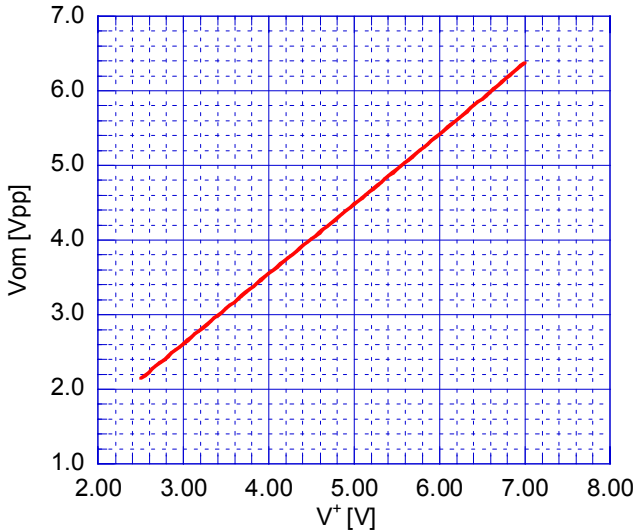
### I<sub>cc</sub> vs V<sup>+</sup>



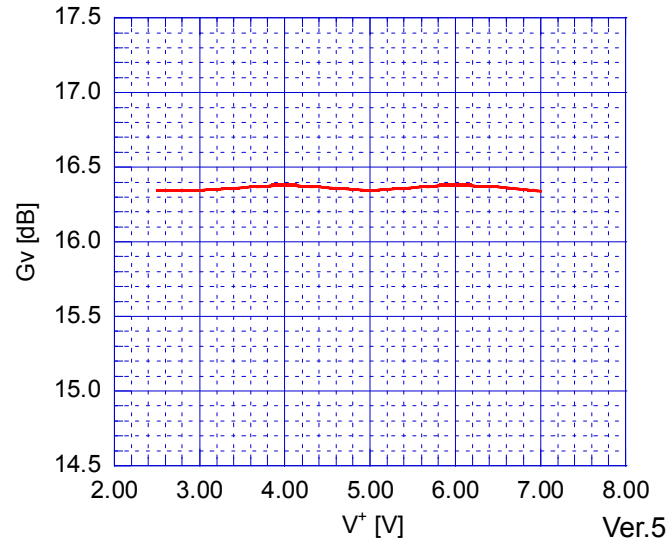
### I<sub>save</sub> vs V<sup>+</sup>



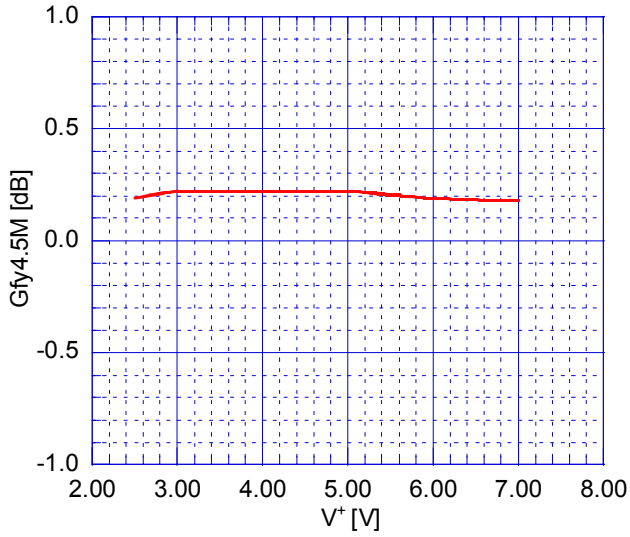
### V<sub>om</sub> vs V<sup>+</sup>



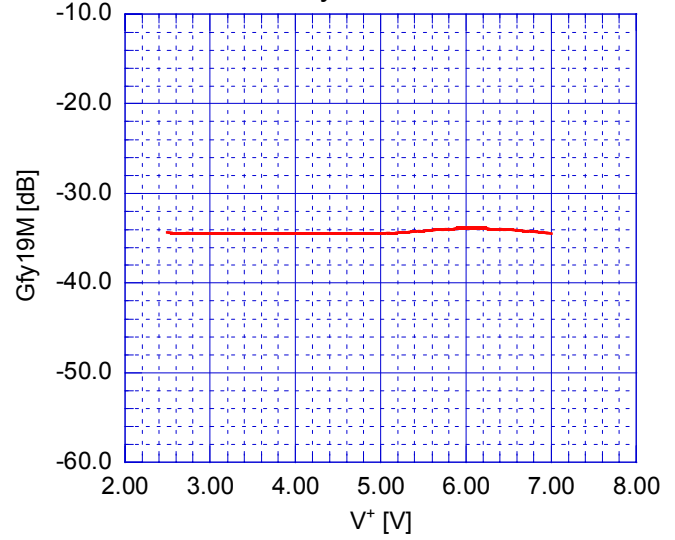
### Gv vs V<sup>+</sup>



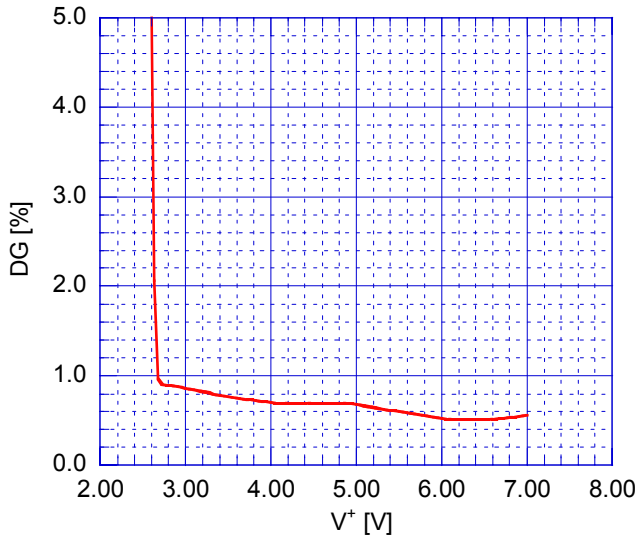
Gfy4.5M vs V<sup>+</sup>



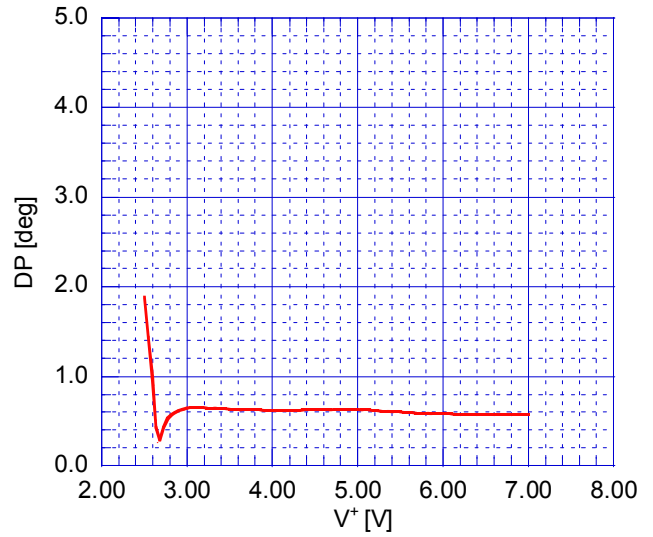
Gfy19M vs V<sup>+</sup>



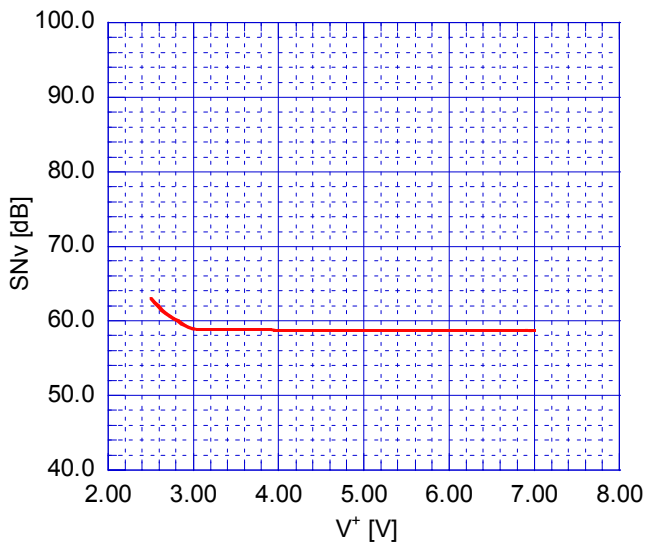
DG vs V<sup>+</sup>



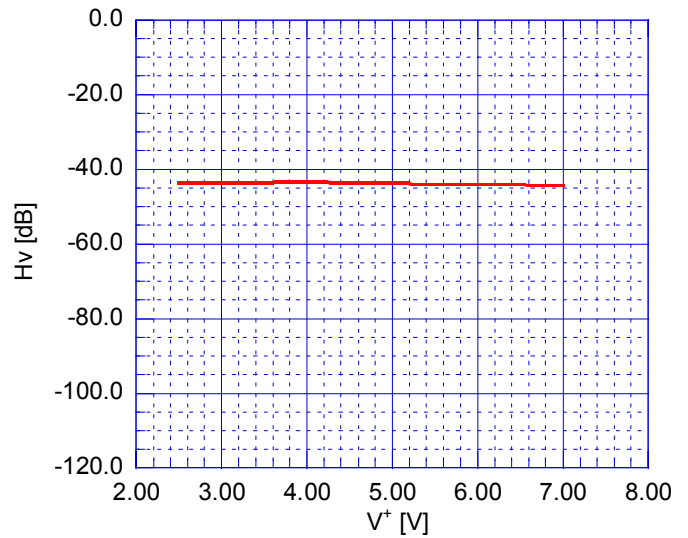
DP vs V<sup>+</sup>

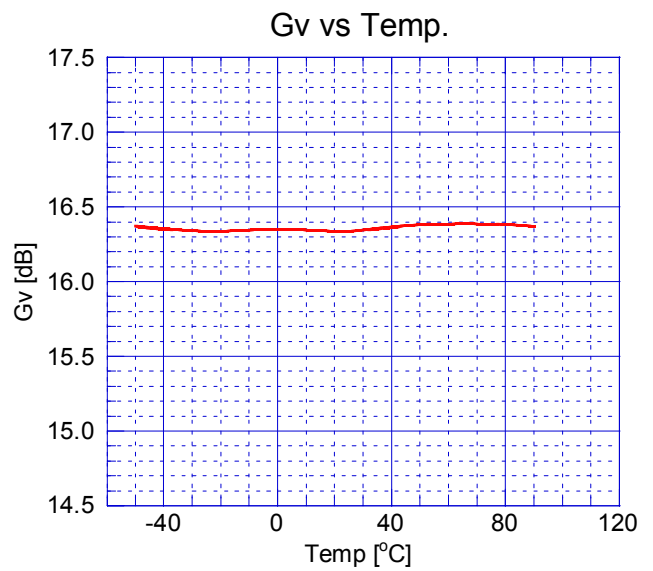
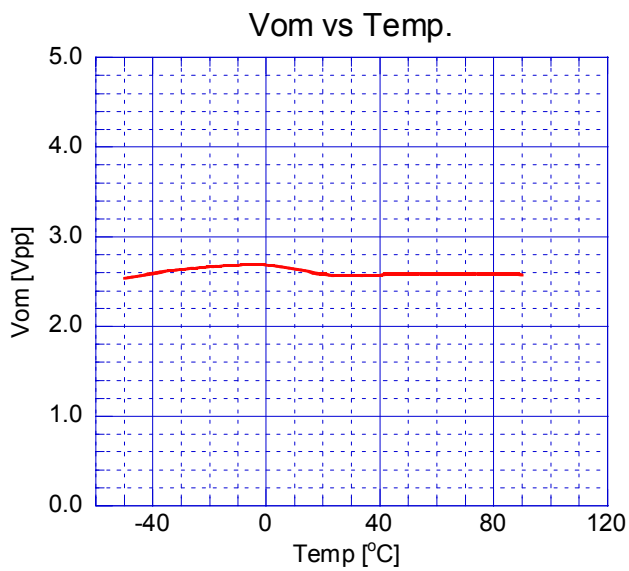
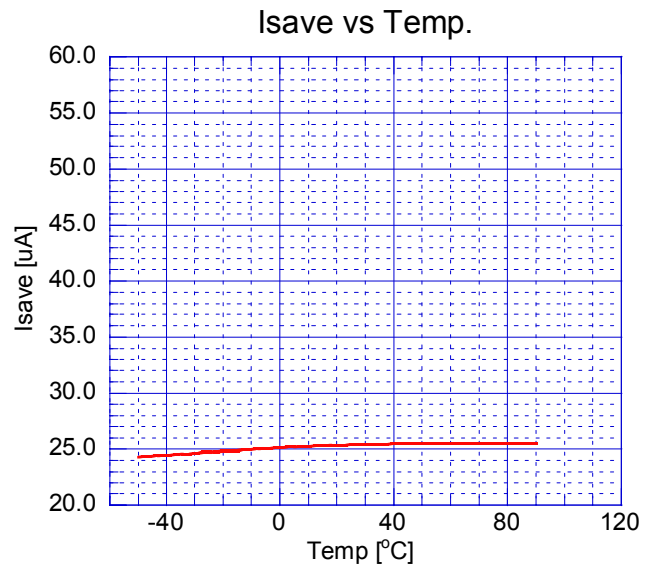
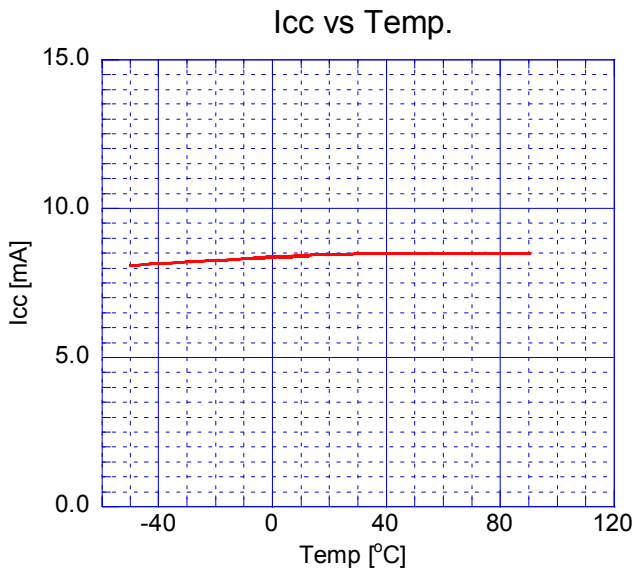
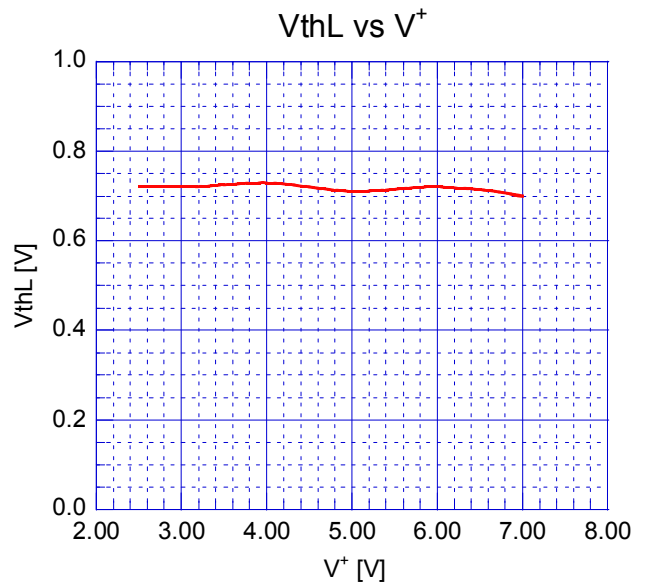
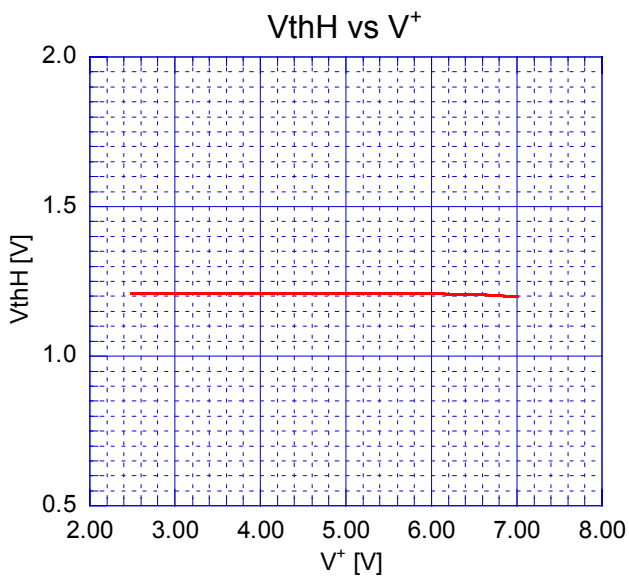


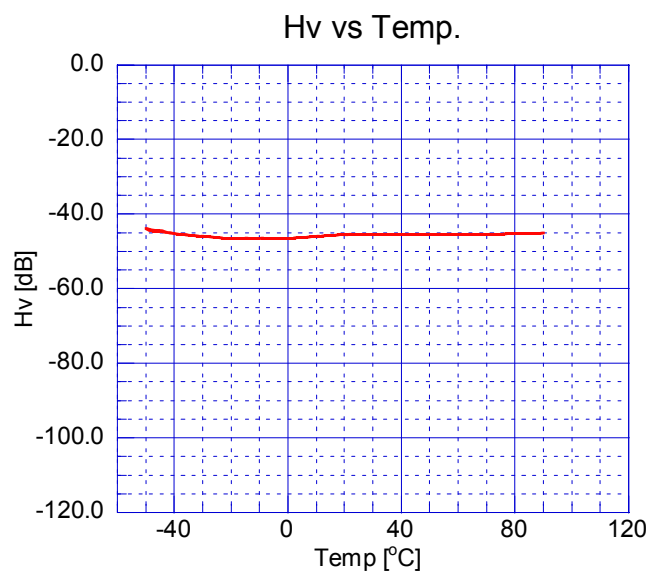
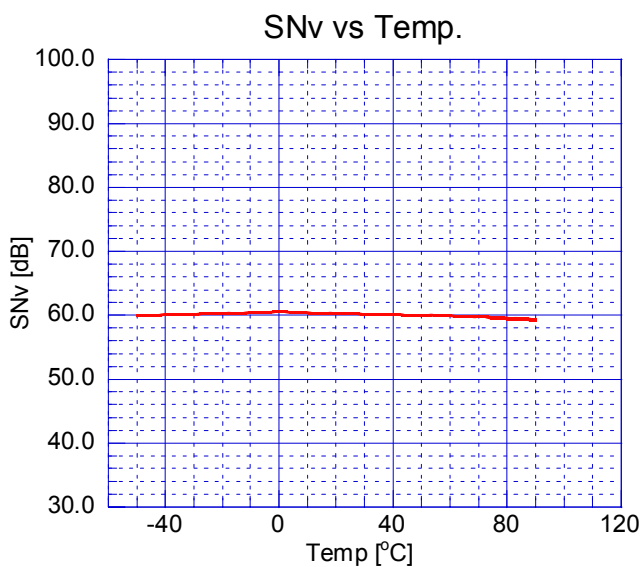
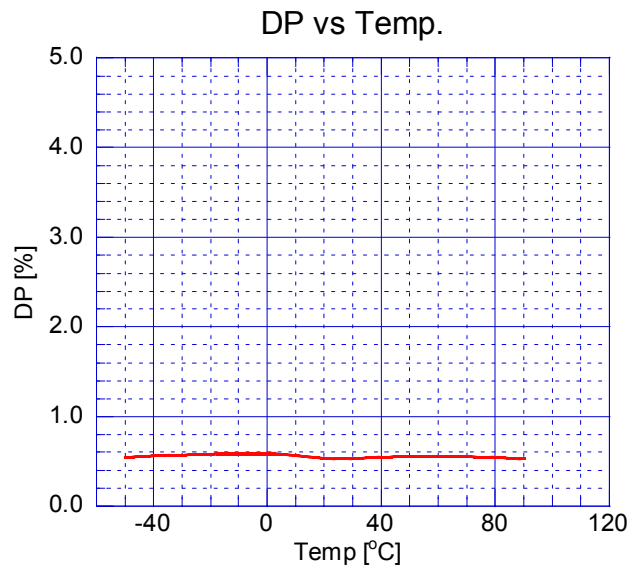
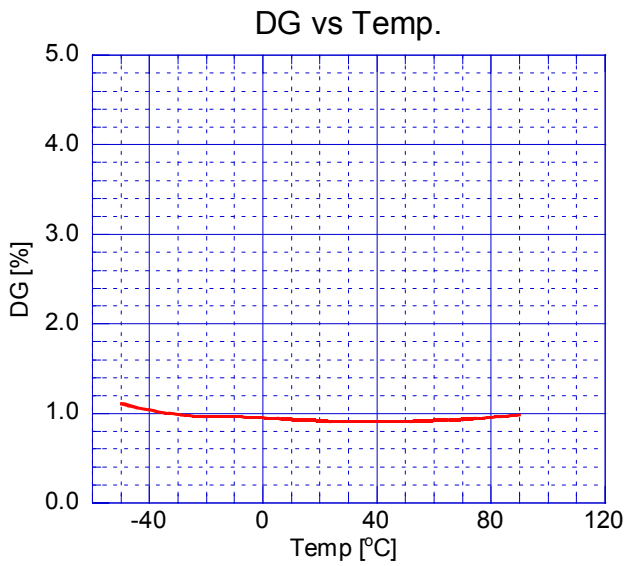
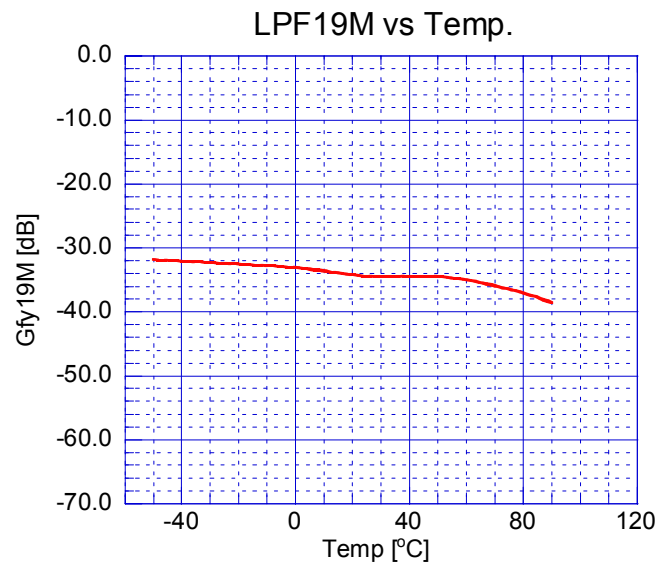
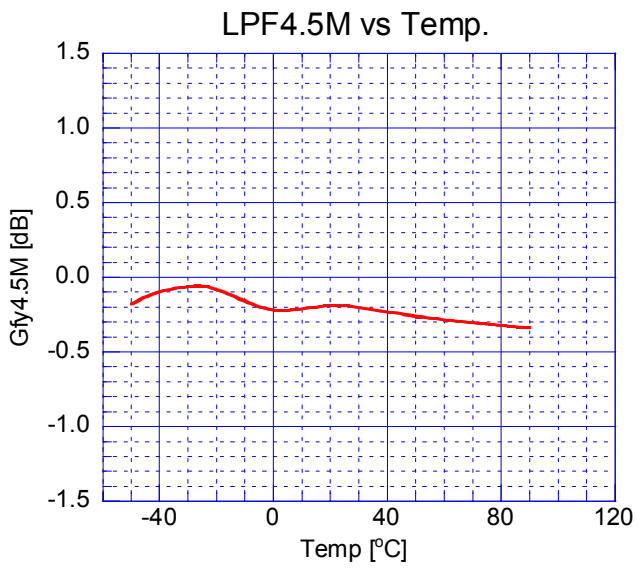
SNv vs V<sup>+</sup>



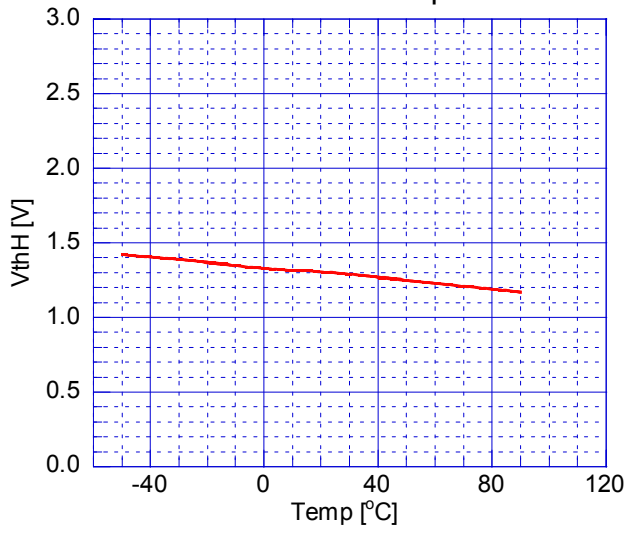
Hv vs V<sup>+</sup>



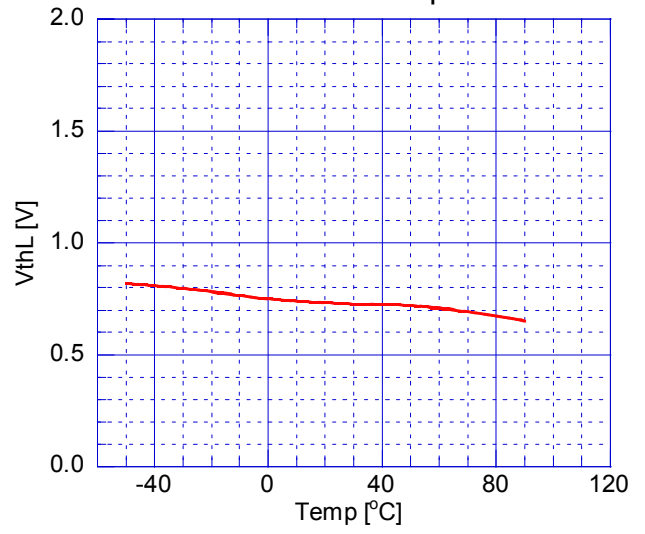




VthH vs Temp.



VthL vs Temp.



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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
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**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.