FAIRCHILD SEMICONDUCTOR®

December 2006

FDS6982AS

Dual Notebook Power Supply N-Channel PowerTrench® SyncFET™

General Description

The FDS6982AS is designed to replace two single SO-8 MOSFETs and Schottky diode in synchronous DC:DC power supplies that provide various peripheral voltages for notebook computers and other battery powered electronic devices. FDS6982AS contains two unique 30V, N-channel, logic level, PowerTrench MOSFETs designed to maximize power conversion efficiency. The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized to reduce conduction losses. Q2 also includes an integrated Schottky diode using Fairchild's monolithic SyncFET technology.

Applications

- Notebook

Features

- **Q2**: Optimized to minimize conduction losses Includes SyncFET Schottky body diode

  8.6A, 30V $R_{DS(on)}$ max= 13.5mΩ @ V_{GS} = 10V

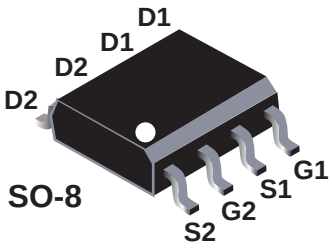
  $R_{DS(on)}$ max= 16.5mΩ @ V_{GS} = 4.5V

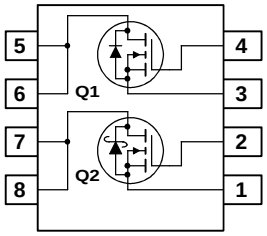
- Low gate charge (21nC typical)
- **Q1**: Optimized for low switching losses

  6.3A, 30V $R_{DS(on)}$ max= 28.0mΩ @ V_{GS} = 10V

  $R_{DS(on)}$ max= 35.0mΩ @ V_{GS} = 4.5V

- Low gate charge (11nC typical)





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q2	Q1	Units
V_{DSS}	Drain-Source Voltage		30	30	V
V_{GSS}	Gate-Source Voltage		±20	±20	V
I_D	Drain Current - Continuous	(Note 1a)	8.6	6.3	A
	- Pulsed		30	20	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6982AS	FDS6982AS	13"	12mm	2500 units
FDS6982AS	FDS6982AS_NL (Note 4)	13"	12mm	2500 units
FDS6982AS	FDS6982AS_NF40 (Note 5)	13"	12mm	2500 units

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Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA V_{GS} = 0 V, I_D = 250 uA	Q2 Q1	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C I_D = 250 µA, Referenced to 25°C	Q2 Q1		28 24		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q2 Q1			500 1	µA
I_{GSS}	Gate-Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V	Q2 Q1			±100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA V_{DS} = V_{GS}, I_D = 250 µA	Q2 Q1	1 1	1.4 1.9	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C I_D = 250 uA, Referenced to 25°C	Q2 Q1		–3.1 –4.3		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 8.6 A V_{GS} = 10 V, I_D = 8.6 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 7.5 A	Q2		11 16 13	13.5 20.0 16.5	mΩ
		V_{GS} = 10 V, I_D = 6.3 A V_{GS} = 10 V, I_D = 6.3 A, T_J = 125°C V_{GS} = 4.5 V, I_D = 5.6 A	Q1		20 26 25	28 33 35	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	Q2 Q1	30 20			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 8.6 A V_{DS} = 5 V, I_D = 6.3 A	Q2 Q1		32 19		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	Q2 Q1		1250 610		pF
C_{oss}	Output Capacitance		Q2 Q1		410 180		pF
C_{rss}	Reverse Transfer Capacitance		Q2 Q1		130 85		pF
R_G	Gate Resistance	V_{GS} = 15mV, f = 1.0 MHz	Q2 Q1		1.4 2.2		Ω
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10V, R_{GEN} = 6 Ω	Q2 Q1		9 10	18 20	ns
t_r	Turn-On Rise Time		Q2 Q1		6 7	12 14	ns
$t_{d(off)}$	Turn-Off Delay Time		Q2 Q1		27 24	44 39	ns
t_f	Turn-Off Fall Time		Q2 Q1		11 3	20 6	ns
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 4.5V, R_{GEN} = 6 Ω	Q2 Q1		12 12	22 22	ns
t_r	Turn-On Rise Time		Q2 Q1		13 14	23 25	ns
$t_{d(off)}$	Turn-Off Delay Time		Q2 Q1		19 15	34 27	ns
t_f	Turn-Off Fall Time		Q2 Q1		10 5	20 10	ns

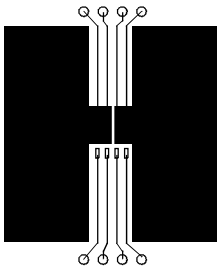
Electrical Characteristics (continued)

T_A = 25°C unless otherwise noted

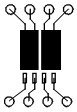
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$Q_{g(TOT)}$	Total Gate Charge at Vgs=10V	Q2: V_{DS} = 15 V, I_D = 11.5A	Q2 Q1		21 11	30 15	nC
Q_g	Total Gate Charge at Vgs=5V	Q1: V_{DS} = 15 V, I_D = 6.3A	Q2 Q1		12 6	16 9	nC
Q_{gs}	Gate–Source Charge		Q2 Q1		3.1 1.8		nC
Q_{gd}	Gate–Drain Charge		Q2 Q1		3.6 2.4		nC
Drain–Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q2 Q1			3.0 1.3	A
T_{rr}	Reverse Recovery Time	I_F = 11.5 A, d_{iF}/d_t = 300 A/µs (Note 3)	Q2		19		ns
Q_{rr}	Reverse Recovery Charge				12		nC
T_{rr}	Reverse Recovery Time	I_F = 6.3 A, d_{iF}/d_t = 100 A/µs (Note 3)	Q1		20		ns
Q_{rr}	Reverse Recovery Charge				9		nC
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3 A (Note 2) V_{GS} = 0 V, I_S = 6 A (Note 2) V_{GS} = 0 V, I_S = 1.3 A (Note 2)	Q2 Q2 Q1		0.5 0.6 0.8	0.7 1.0 1.2	V

Notes:

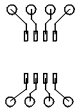
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in^2 pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in^2 pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. See "SyncFET Schottky body diode characteristics" below.

4. FDS6982AS_NL is a lead free product. The FDS6982AS_NL marking will appear on the reel label.

5. FDS6982AS_NF40 is a lead free product. The FDS6982AS_NF40 marking will appear on the reel label.

Typical Characteristics: Q2

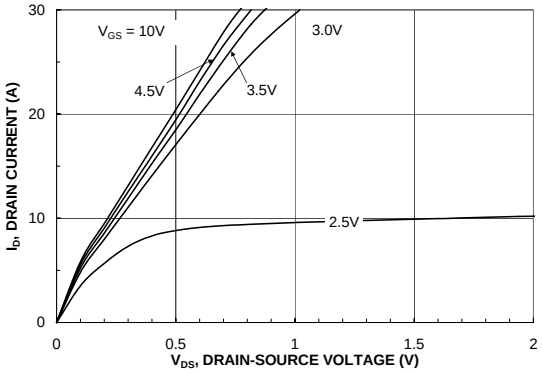


Figure 1. On-Region Characteristics.

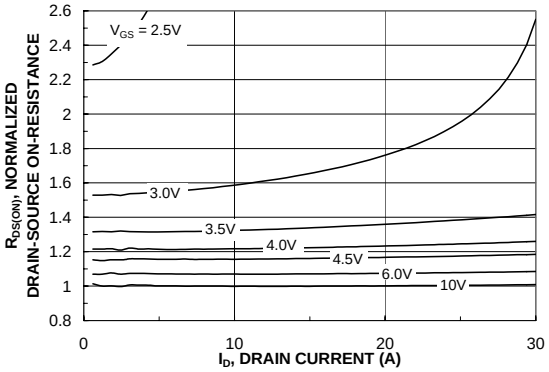


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

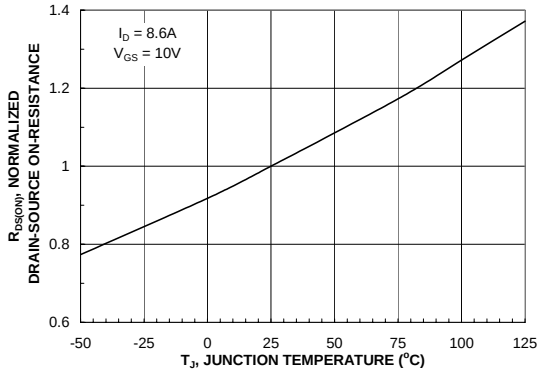


Figure 3. On-Resistance Variation with Temperature.

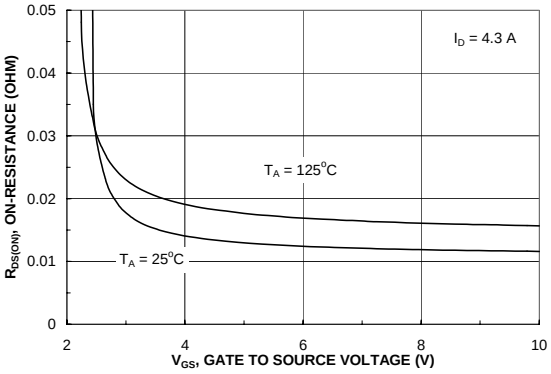


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

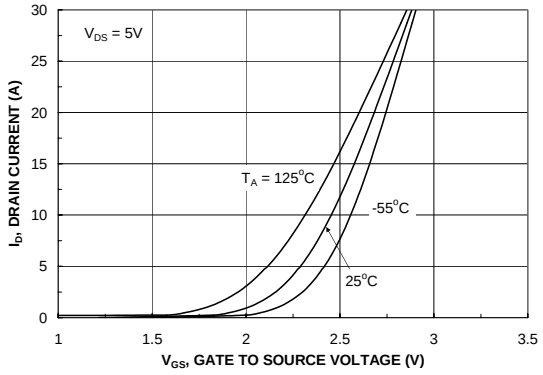


Figure 5. Transfer Characteristics.

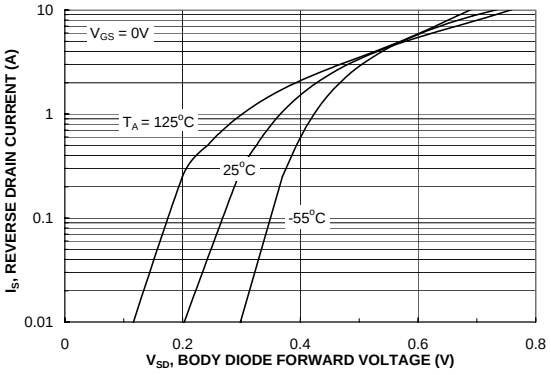


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2

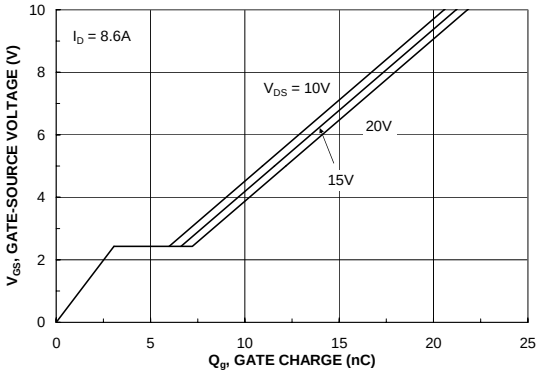


Figure 7. Gate Charge Characteristics.

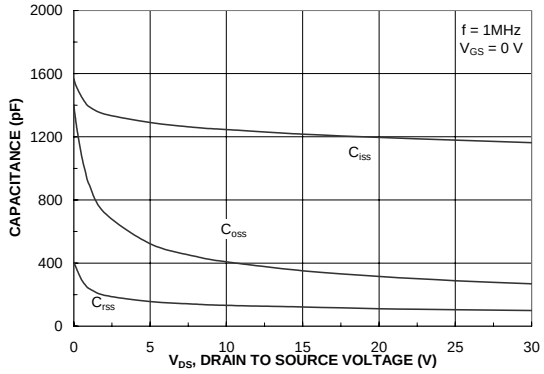


Figure 8. Capacitance Characteristics.

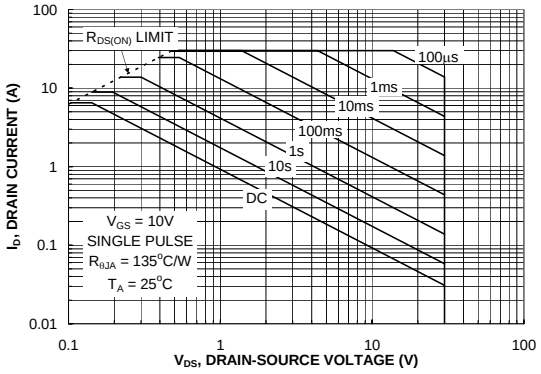


Figure 9. Maximum Safe Operating Area.

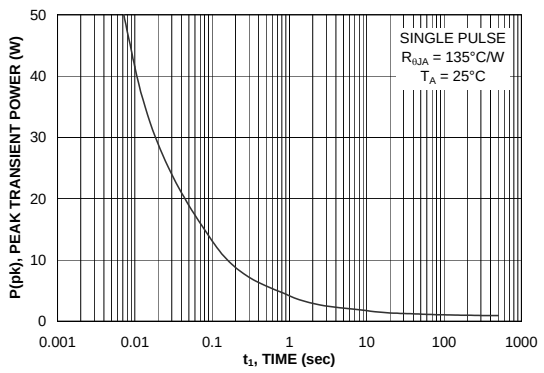


Figure 10. Single Pulse Maximum Power Dissipation.

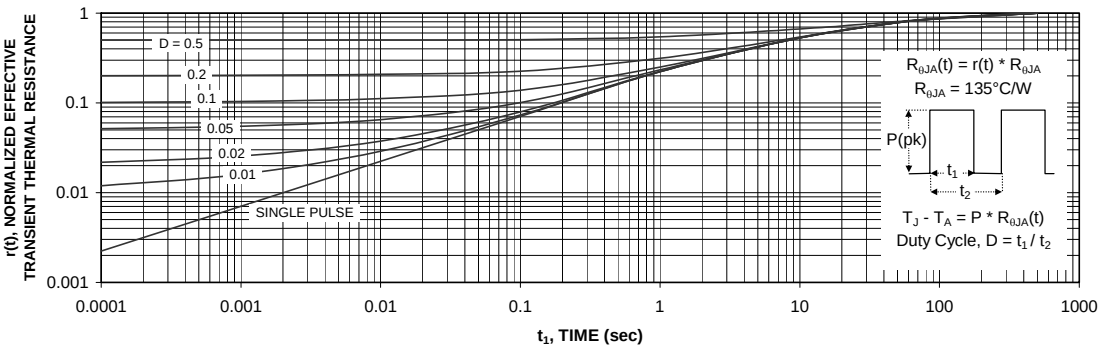


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics Q1

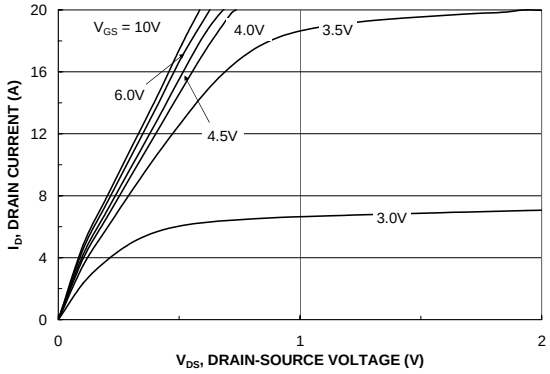


Figure 12. On-Region Characteristics.

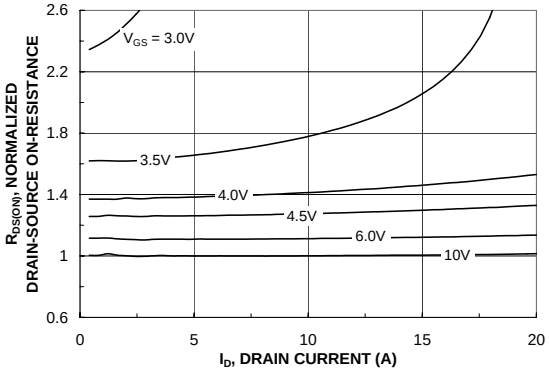


Figure 13. On-Resistance Variation with Drain Current and Gate Voltage.

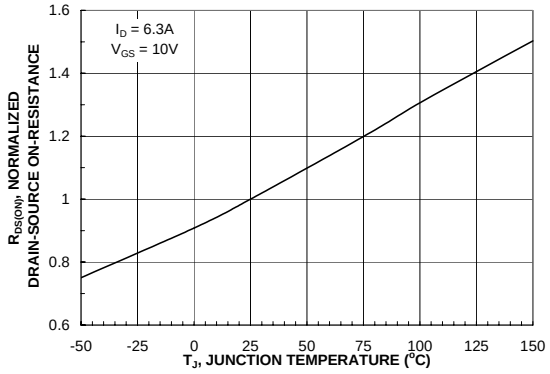


Figure 14. On-Resistance Variation with Temperature.

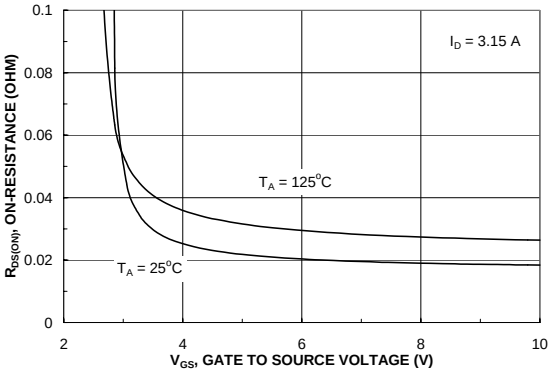


Figure 15. On-Resistance Variation with Gate-to-Source Voltage.

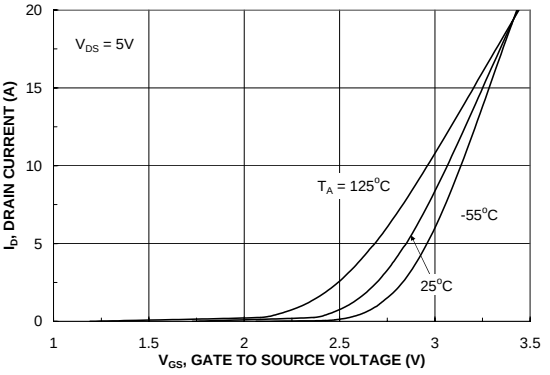


Figure 16. Transfer Characteristics.

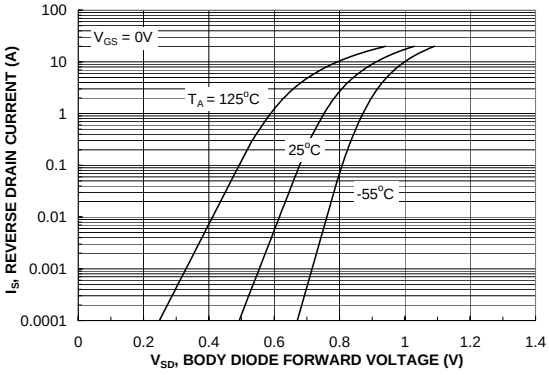


Figure 17. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics Q1

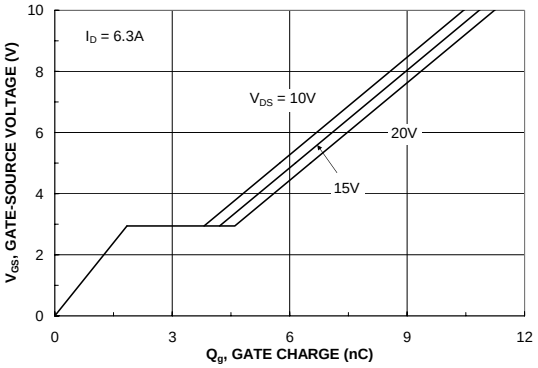


Figure 18. Gate Charge Characteristics.

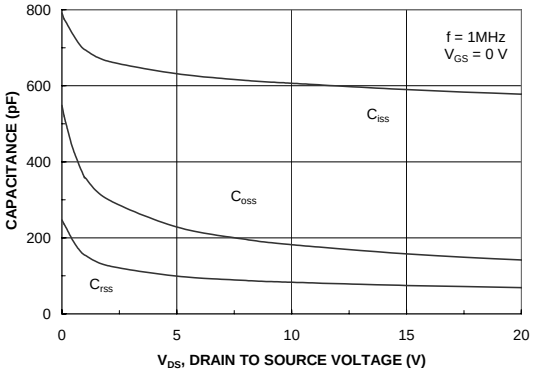


Figure 19. Capacitance Characteristics.

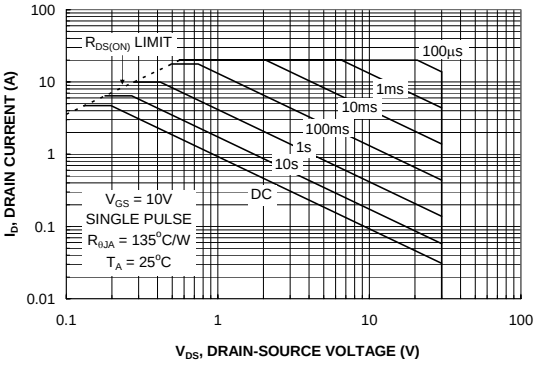


Figure 20. Maximum Safe Operating Area.

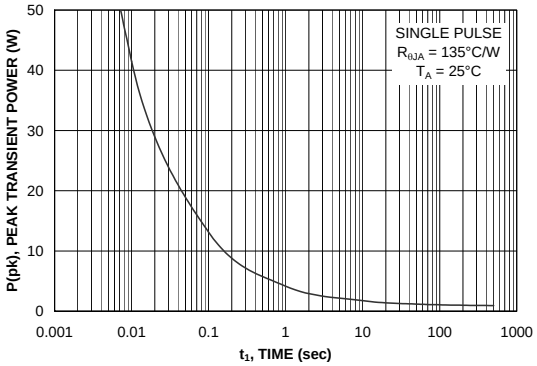


Figure 21. Single Pulse Maximum Power Dissipation.

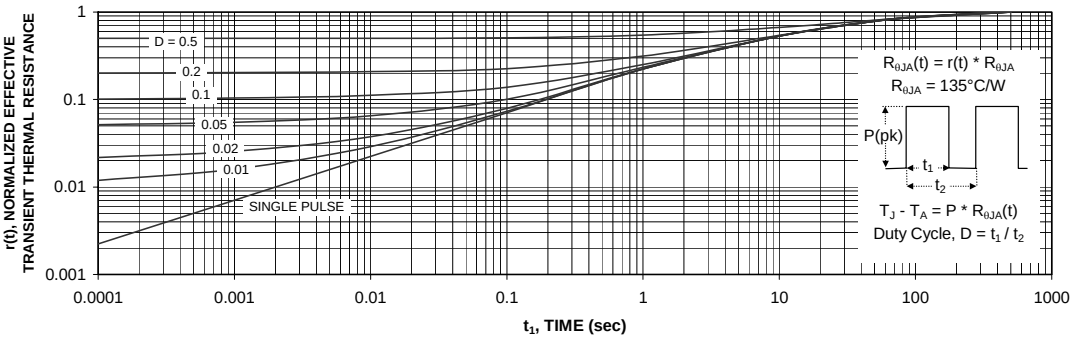


Figure 22. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics (continued)

SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. **Figure 23** shows the reverse recovery characteristic of the FDS6982AS.

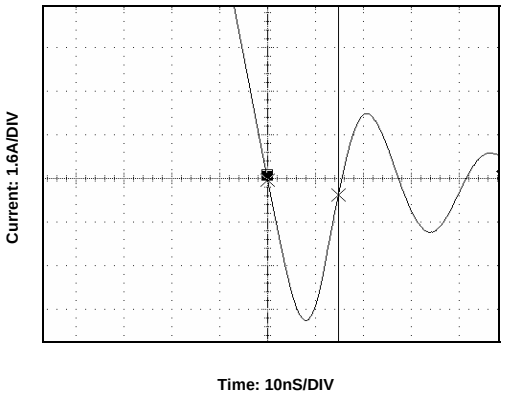


Figure 23. FDS6982AS SyncFET body diode reverse recovery characteristic.

For comparison purposes, **Figure 24** shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDS6982).

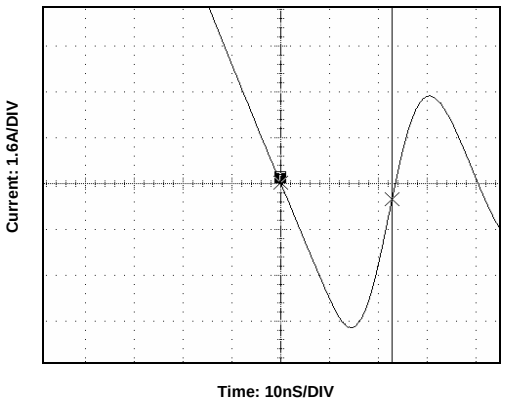


Figure 24. Non-SyncFET (FDS6982) body diode reverse recovery characteristic.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

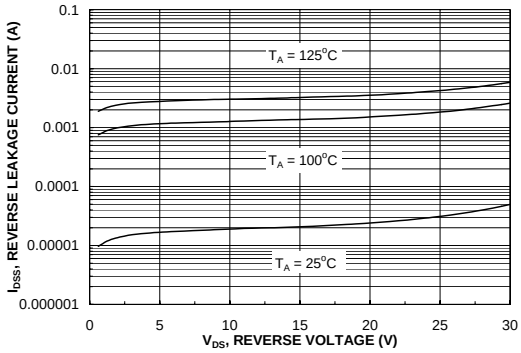


Figure 25. SyncFET body diode reverse leakage versus drain-source voltage and temperature

Typical Characteristics

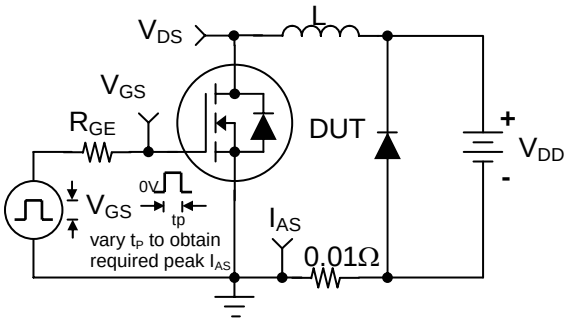


Figure 26. Unclamped Inductive Load Test Circuit

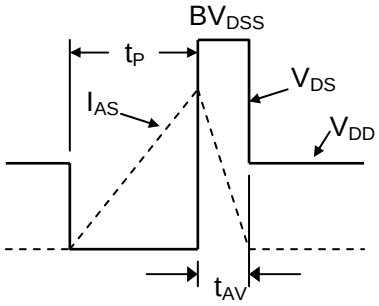


Figure 27. Unclamped Inductive Waveforms

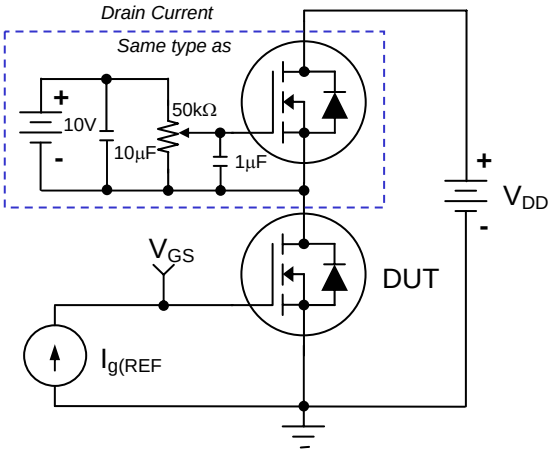


Figure 28. Gate Charge Test Circuit

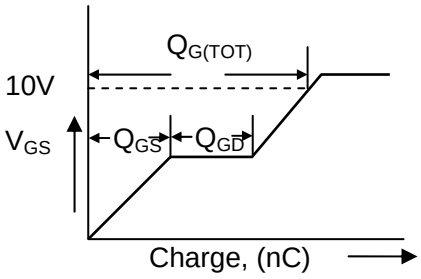


Figure 29. Gate Charge Waveform

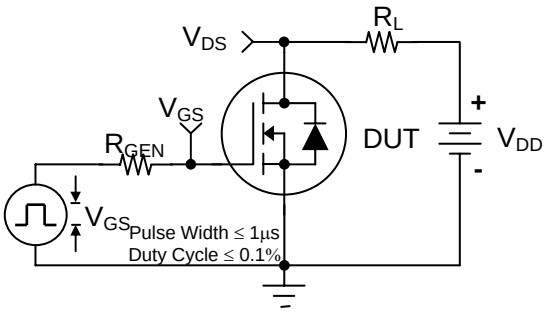


Figure 30. Switching Time Test Circuit

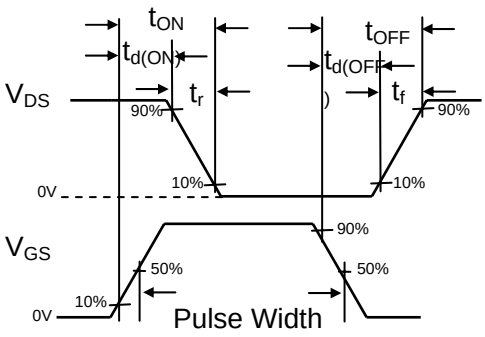


Figure 31. Switching Time Waveforms

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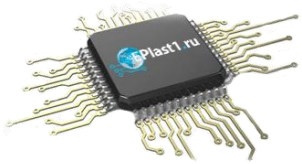
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