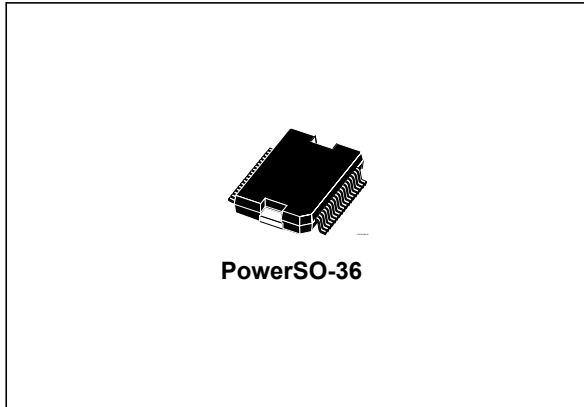


## Four channel valve driver

Datasheet - production data



- 16 bit serial peripheral interface, up to 5 MHz with diagnosis
- Battery compatible supply voltage
- Detailed load diagnosis
  - Over load protection
  - Open load (off-state)
  - Undercurrent
  - Undervoltage
  - Temperature warning and shutdown
  - Power or signal GND loss
  - Freewheeling diode loss
  - Silent valve driver test

### Features

- Four protected low-side drivers with diagnostics
  - Two 140 mΩ PWM controlled outputs (Q1 & Q2)
  - Two 250 mΩ current controlled outputs with 6 % accuracy (Q3 & Q4)
- All outputs with 35 V Zener Clamp
- Programmable output timer
- Clock monitor
- Integrated recirculation diodes

### Description

The L9374LF is a SPI (serial peripheral interface) controlled four channel low side driver with integrated recirculation diodes.

The output duty cycle (all channels) / current regulation level (Q3 & Q4 only) can be programmed individually. It is possible to program two consecutive output duty cycles or target currents per channel as well as an individual duration time for each channel actuation.

Table 1. Device summary

Order code	Package	Packing
L9374LF	PowerSO-36	Tube
L9374TRLF	PowerSO-36	Tape and reel

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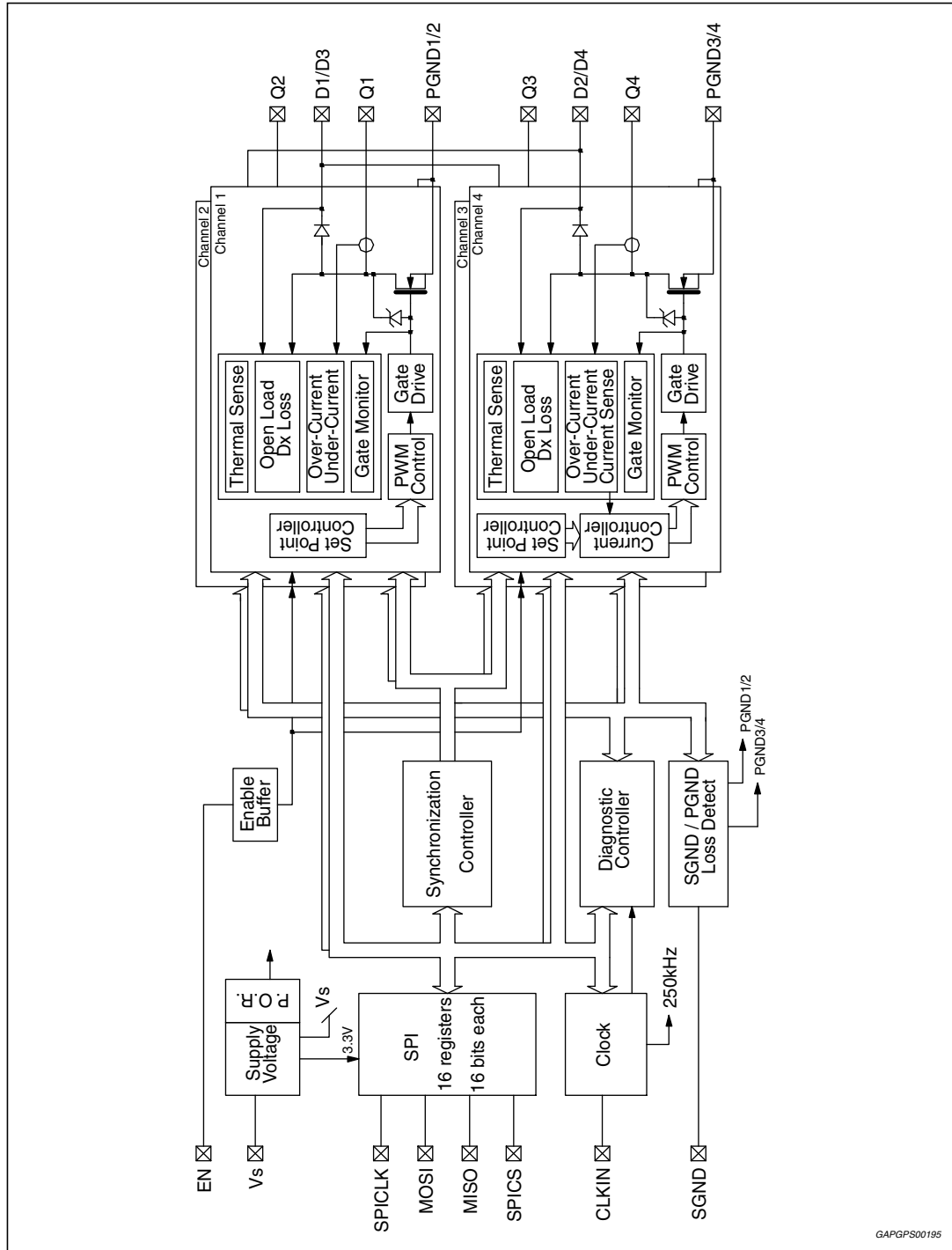
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# 1 Block diagram

Figure 1. Block diagram



GAPGPS00195



## 2 Pins description

Figure 2. PowerSO-36 pins connection (top view)

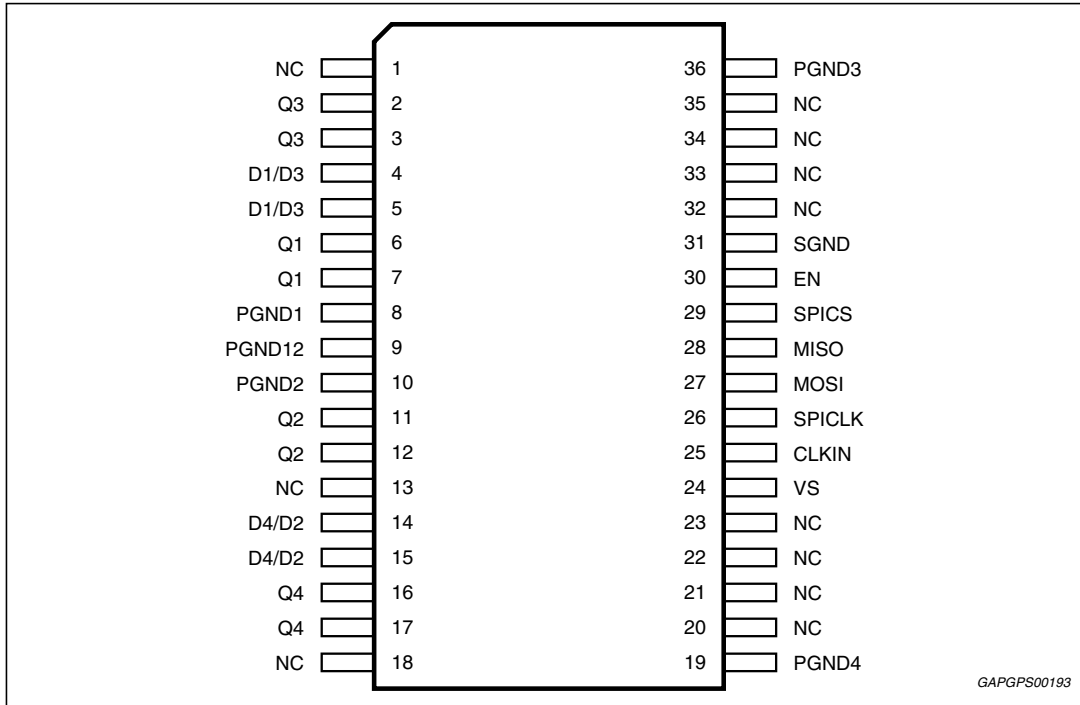


Table 2. Pins description

Pin #	Pin name	Description
1	PGND	Not connected/Power ground.
2	Q3	Output.
3	Q3	Output.
4	D1/D3	Free wheeling diode.
5	D1/D3	Free wheeling diode.
6	Q1	Output.
7	Q1	Output.
8	PGND1	Power ground of the output driver 1 & 2.
9	PGND12	Power ground of the output driver 1 & 2.
10	PGND2	Power ground of the output driver 1 & 2.
11	Q2	Output.
12	Q2	Output.
13	N.C.	Not connected.
14	D4/D2	Free wheeling diode.
15	D4/D2	Free wheeling diode.
16	Q4	Output.

Table 2. Pins description (continued)

Pin #	Pin name	Description
17	Q4	Output.
18	PGND	Not connected/Power ground.
19	PGND4	Power ground of the output driver 4.
20	N.C.	Not connected.
21	N.C.	Not connected.
22	N.C.	Not connected.
23	N.C.	Not connected.
24	VS	Supply pin.
25	CLKIN	Input for precise clock.
26	SPICLK	SPI communication clock.
27	MOSI	Master Out Slave In for SPI communication.
28	MISO	Master In Slave Out for SPI communication.
29	SPICS	SPI chip select.
30	EN	Enable.
31	SGND	Signal ground.
32	N.C.	Not connected.
33	N.C.	Not connected.
34	N.C.	Not connected.
35	N.C.	Not connected.
36	PGND3	Power ground of the output driver 3.

### 3 Electrical specifications

#### 3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
$V_s$	Supply voltage	-0.3	38	V
$V_{Dx}$	Freewheeling diode voltage	-0.3	35	V
$V_{Qx}$	Output voltage	-0.3	Internally Clamped	V
$V_{EN}$ $V_{SPICLK}$ $V_{SPICS}$ $V_{MOSI}$ $V_{MISO}$ $V_{CLKIN}$	Enable voltage SPI clock voltage SPI chip select voltage SPI MOSI voltage SPI MISO voltage SPI clock input voltage	-0.3	6	V
$I_{Q1; 2}$	Output current at reversal voltage	-	-4	A
$I_{Q3; 4}$		-	-2	A
$I_{EN\_CL}$ $I_{SPICLK\_CL}$ $I_{SPICS\_CL}$ $I_{MOSI\_CL}$ $I_{CLKIN\_CL}$	Input clamping currents (static) Input clamping currents (dynamic)	-3 -10	+3 +10	mA
$T_{amb}$	Ambient operating temperature	-40	+125	°C

Definition: Current flowing into the L9374LF are considered positive -> "+"  
Current flowing out of the L9374LF are considered negative -> "-"

**Warning:** Transients beyond this limit will cause currents into ESD structures which must be limited externally to  $\pm 10$  mA (maximum energy to be dissipated: 2 mJ).

### 3.2 ESD susceptibility

#### 3.2.1 HBM

ESD susceptibility HBM according to EIA/JESD 22-A 114B

**Table 4. HBM**

Pin	Condition	Min.	Max.	Unit
All pins	-	± 2	-	kV
Output pins D <sub>X</sub> ; Q <sub>X</sub> ;	PGND12, PGND3, PGND4, LGND and GND are connected together.	± 4	-	kV

#### 3.2.2 MM

ESD susceptibility according to EIA/JESD22-A115-A

**Table 5. MM**

Parameter	Condition	Min.	Max.	Unit
Machine model (MM)	All pins	± 250	-	V

### 3.3 Electrical characteristics

V<sub>S</sub> = 5.2 to 20 V; -40 °C ≤ T<sub>j</sub> ≤ 175 °C, unless otherwise specified.

Function is guaranteed until thermal shutdown threshold, T<sub>SD</sub>;

#### 3.3.1 Supply current

**Table 6. Supply current**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I <sub>VS</sub>	Supply current	V <sub>s</sub> = 13.5 V @+175 °C @+25 °C @-40 °C	2.0 - -	- 7.5 -	- - 9.0	mA
V <sub>s</sub>	Supply voltage operating range	-	5.2	-	20	V

#### 3.3.2 Output power stages

The output power stages consist of an MOSFET and a freewheeling diode. Each output contains diagnostic and protection circuitry. Additional current sensing is present in the current regulated outputs (for more details see [Section 4.7: Output driver](#)).

Figure 3. Output power stages Q1/Q2

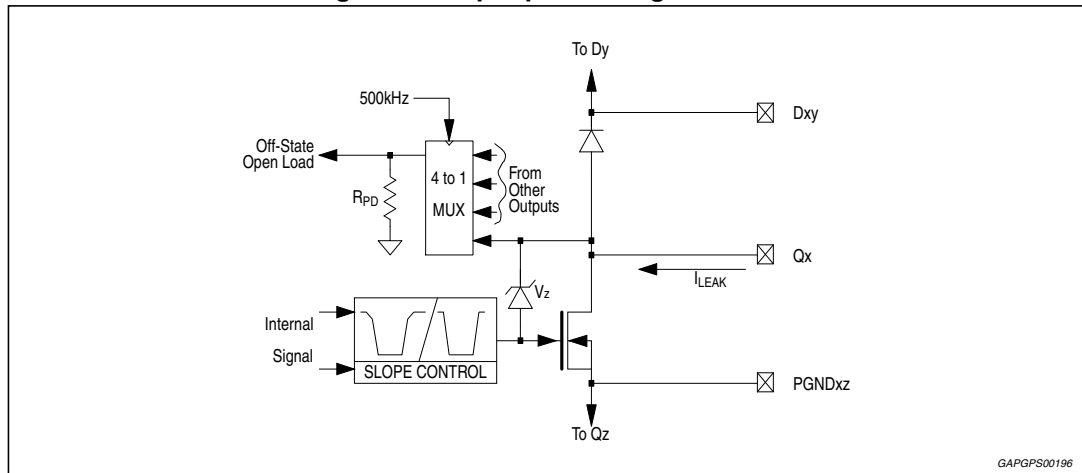
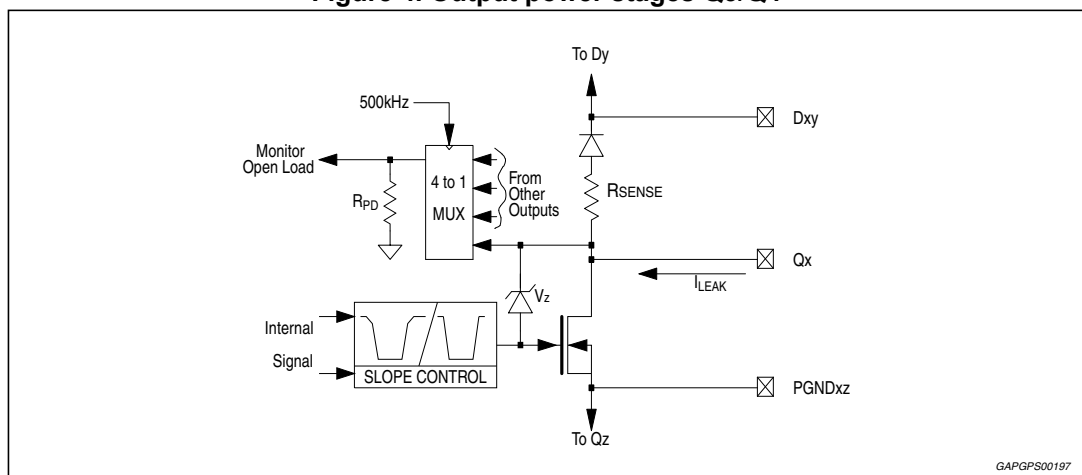


Table 7. Output power stages

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$R_{ON}(Q_1/Q_2)$	Static drain-source on-resistance $Q_1 / Q_2$	$I_Q = 1 \text{ A}$ (TK: 0.58 % / K; Typ @ RT)	60	140	390	mΩ
$R_{ON}(Q_3/Q_4)$	Static drain-source on-resistance $Q_3 / Q_4$	$I_Q = 1 \text{ A}$ (TK: 0.58 % / K; Typ @ RT)	80	250	520	mΩ
$V_Z$	Z-diode clamping voltage	$I_Q = \text{current limitation}$	35	-	40	V
$R_{PD}$	Output pull down resistor (multiplexed to the 4 outputs sequentially) <sup>(1)</sup>	EN = 1	20	40	100	kΩ
$I_{LEAK}$	Output leakage current	$V_Q = 20 \text{ V}; \text{EN} = 0 \text{ V}$ $T_j = 130 \text{ }^\circ\text{C}$ $T_j = 25 \text{ }^\circ\text{C}$	-	-	5 1	μA μA

1.  $R_{PD}$  is sequentially connected to each output for 2 μs (8 μs period) for the purpose of detecting off-state open load.

Figure 4. Output power stages Q3/Q4



### 3.3.3 Freewheeling diode

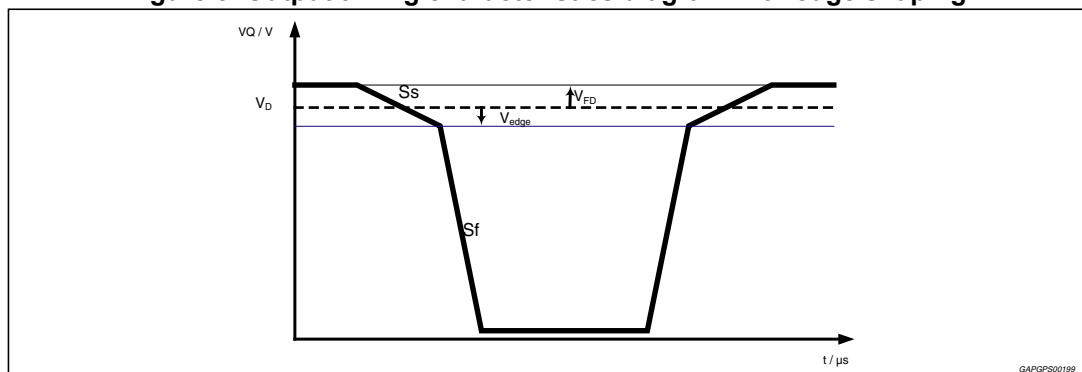
Table 8. Freewheeling diode electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{FD1/2}$	Forward voltage of free wheeling diodes $D_1 / D_2$	$I_{FD} = -1.5 A$	0.5	0.75	1.75	V
$V_{FD3/4}$	Forward voltage of free wheeling path	D3, D4 @-250 mA	0.5	1.0	1.5	V
		D3, D4 @-1.8 A	1.6		3.6	V
$R_{sense}$	$Q_3/Q_4$ Sense resistor	Calculated: $(V_{FD\_1.8A} - V_{FD\_250mA}) / 1.55 A$	-	1	-	$\Omega$
$R_{D1/3}$	Resistor $D_{13}$ -Pin	$V_Q < V_D < 18 V$ (Typ @ $T_j = 25^\circ C$ )	100	240	700	k $\Omega$
$I_{leak\_Dx\_0}$	Leakage current into Dx-Pin $D_{13}$	EN = 0	5	-	160	$\mu A$
$I_{leak\_Dx\_1/0}$	Leakage current into Dx-Pin $D_{13} D_{24}$	EN = 1 $I_{DAC} = 0A$	90	70	400	$\mu A$
$I_{leak\_Dx\_1/1.8}$	Leakage current into Dx-Pin $D_{13} D_{24}$	EN = 1 $I_{DAC} = 1.8A$	90	-	2400	$\mu A$

### 3.3.4 Output timing characteristics

The DMOS outputs have controlled slopes to minimize EME. The Edge Shaping option is programmed via SPI (See [Edge shaping \(EDGE\\_SH\)](#)); without edge shaping, the slope is fixed to 10V/ $\mu s$  in both directions.

Figure 5. Output timing characteristics diagram with edge shaping



Where:

- $V_D$ : Valve supply voltage
- $V_{FD}$ : Forward voltage drop across the recirculation diode
- $V_{EDGE}$ : Voltage Sf to Ss slope transition
- Ss: Slow slope
- Sf: Fast slope

Table 9. Output timing electrical characteristics<sup>(1)</sup>

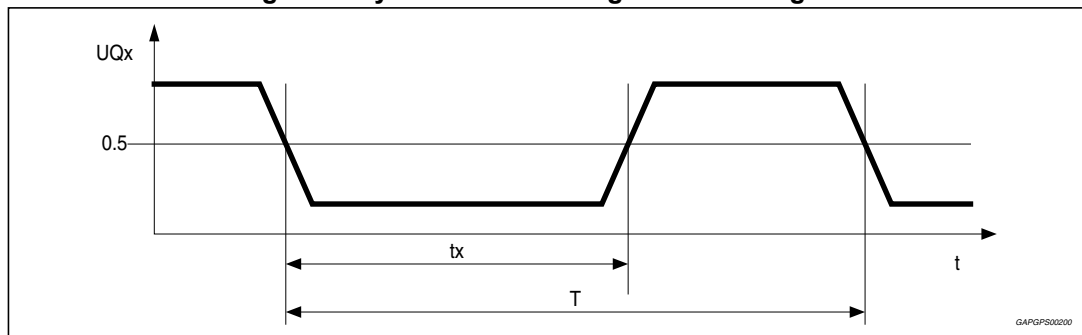
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{edge}$	Edge shaping threshold	measured from $V_D$	-2.2	-	-1	V
$Sf_{Q_1/Q_2}$	Sf output on/off slope fast $Q_1/Q_2$	$V_D = 20\text{ V}$ $I_{load} = 1.5\text{ A}$ resistive load	3	10	17	V/ $\mu\text{s}$
$Ss_{Q_1/Q_2}$	Ss output on/off slope slow $Q_1/Q_2$		2	4	6	V/ $\mu\text{s}$
$Sf_{Q_3/Q_4}$	Sf output on/off slope fast $Q_3/Q_4$		6	13	20	V/ $\mu\text{s}$
$Ss_{Q_3/Q_4}$	Ss output on/off slope slow $Q_3/Q_4$		2.5	5	7.5	V/ $\mu\text{s}$

1. See [Figure 5](#) for waveform.

The slope is defined between 20 % and 80 % of the edge.

### Symmetric switching of DMOS

Figure 6. Symmetric switching of DMOS diagram



A Symmetric switching is present to ensure a reliable PWM at the output.

Table 10. Symmetric switching of DMOS electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_{sym1}$	Symmetry II with edge shaping	$t_{x-dc} \cdot T < 1.5\ \mu\text{s}$ $dc = 50\%$	-1.0	-	2.0	$\mu\text{s}$
$t_{sym2}$	Symmetry II without edge shaping	$V_Q = 10\text{ V}$	0	-	3.0	$\mu\text{s}$

### 3.3.5 PWM output behavior

(refer to [Section 4.4: Set-point controller](#) for details)

Table 11. PWM output behavior characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$f_{Q_x}$	Output frequency	-	-2 %	4	+2 %	kHz
DC	Duty range	-	0	-	100	%
$DC_{RES}$	Duty resolution of $f_A$	-	-	0.2	-	%
$N_{RES}$	Number of bits for duty resolution/target current value	-	-	9	-	-

Table 11. PWM output behavior characteristics (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t(n)_{RES}$	Resolution of duration	$1/f_A$	-	250 500	-	$\mu s$ $\mu s$
	Add. 0 bit D9 = 0					
$t(n)_{MAX}$	Max. Duration	$(2^5-1) \times 250 \mu s$ $(2^5-1) \times 500 \mu s$	-	-	7.75 15.5	ms ms
	Add. 0 bit D9 = 0					
$N_{Bit}$	Number of bits for duration	-	-	5	-	-

3.3.6 Q3 / Q4 (current controller)

(refer to Section 4.5: Current controller for details)

Table 12. Q3 / Q4 (current controller) electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$I_{Q3/Q4}$	Current range	-	0		1.8	A
$I_{Q3/Q4\_res}$	Current resolution	-	-	3.5	-	mA
$I_{Q3/Q4\_acc}$	Current accuracy	$I_{load} = 0 \text{ mA to } 400 \text{ mA}$	-	-	$\pm 24$	mA
		$I_{load} > 400 \text{ mA}$			$\pm 6$	%

3.3.7 Logic inputs / outputs

Figure 7. Logic inputs

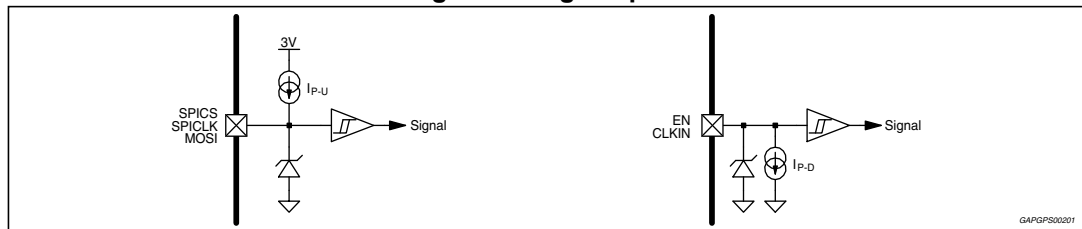


Table 13. Logic inputs electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{In\_low}$	Input threshold	-	-0.3	-	1.0	V
$V_{In\_high}$	Input threshold	-	2.0	-	3.5	V
$V_{In\_hys}$	Input threshold hysteresis	-	50	100	350	mV
$I_{P-U}$	Internal pull-up current source for SPICS, SPICLK, MOSI	$0 \text{ V} \leq V_{In-xy} \leq 2 \text{ V}$	-12	-30	-60	$\mu A$
$I_{P-D}$	Internal pull-down current source for EN, CLKIN	$1 \text{ V} \leq V_{In-xy} \leq 3.45 \text{ V}$	+12	+30	+60	$\mu A$
$C_{in}$	Input capacitance	Designed but not tested	3.5	-	7.5	pF



### 3.3.8 Logic outputs (MISO)

Figure 8. Logic outputs (MISO) circuit

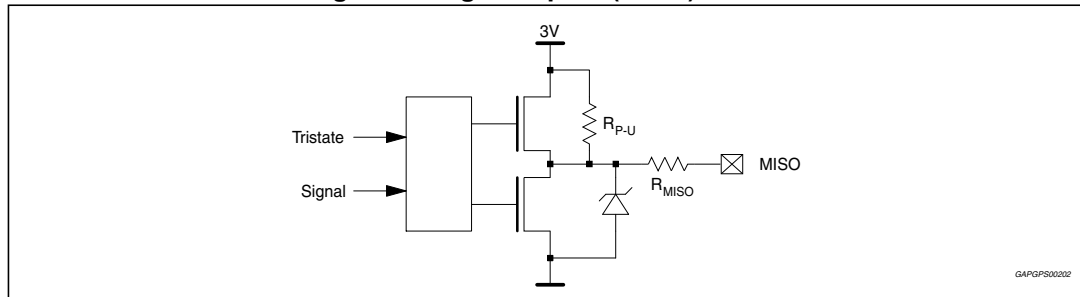


Table 14. Logic outputs (MISO) electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{MISO\_L}$	MISO low voltage	$I_{Out-xy} \leq 25 \mu A$ ; $C_L \leq 30 \text{ pF}$	0	-	0.4	V
$V_{MISO\_H}$	MISO high voltage	$I_{Out-xy} \leq -25 \mu A$ ;	2.5	3.3	3.45	V
$R_{MISO-ON}$	MISO ON resistance	$R_{ON} + R_{MISO}$	40	100	400	$\Omega$
$R_{P-U}$	MISO pull up resistor	SPICS = high → MISO in tristate mode	50	120	300	k $\Omega$
$C_{in}$	Input capacitance	designed but not tested	3.5	-	7.5	pF

### 3.3.9 Diagnostic functions at output stage

(refer to [Section 4.8: Diagnostics](#) for details)

Table 15. Diagnostic functions at output stage electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{OL}$	Open load threshold	output off	0.3	0.33	0.39	x VS
$I_{UC}$	Undercurrent threshold	output on	50	100	140	mA
$T_{SD}$	Temperature shut down threshold <sup>(1)</sup>	-	180	200	220	$^{\circ}\text{C}$
$T_W$	Temperature warning	-	160	180	200	$^{\circ}\text{C}$
$\Delta T_{WSD}$	Difference between $T_W$ and $T_{SD}$	$T_{SD} - T_W$	10	-	40	$^{\circ}\text{C}$
$D_{x \text{ loss}}$	Supply loss threshold	-	32	-	39	V
$I_{OC1(1/2)}$	Overcurrent threshold 1 $Q_1/Q_2$	OC_TH_Qx = '01'	5	7.5	9	A
$I_{OC2(1/2)}$	Overcurrent threshold 2 $Q_1/Q_2$	OC_TH_Qx = '10'	7	8.5	10	A
$I_{OC(3/4)}$	Overcurrent threshold $Q_3/Q_4$	-	3	5	8	A
$V_{G\_ON}$	Gate monitoring threshold	Internal node	2.5	-	-	V
$V_{G\_OFF}$	Gate monitoring threshold	$I_Q > 15 \text{ mA}$ , Internal node	-	-	1	V

1. Monitoring is only active if the output is on.

### 3.3.10 General diagnostic functions

(refer to [Section 4.8: Diagnostics](#) for details)

**Table 16. General diagnostic functions electrical characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V <sub>UV</sub>	Under voltage threshold	(VS-pin)	3.0	-	5.2	V
V <sub>SG_L</sub>	Signal GND loss threshold	-	0.2	0.4	0.6	V
V <sub>PG_L</sub>	Power GND loss threshold	-	0.5	-	2.5	V
V <sub>PG_Lh</sub>	Power GND loss hysteresis	-	-	1.0	-	V

**Table 17. CLKIN-monitoring characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f <sub>CLKIN_H250</sub>	CLKIN monitoring @ 250 kHz-mode set SPI bit	frequency too high	300	-	760	kHz
f <sub>CLKIN_L250</sub>	CLKIN monitoring @ 250 kHz-mode set SPI bit	frequency too low	90	-	190	kHz
f <sub>CLKIN_H1M</sub>	CLKIN monitoring @ 1 MHz-mode set SPI bit	frequency too high	1.20	-	3.04	MHz
f <sub>CLKIN_L1M</sub>	CLKIN monitoring @ 1 MHz-mode set SPI bit	frequency too low	0.36	-	0.76	MHz
f <sub>CLKIN_OK</sub>	CLKIN monitoring clear SPI bit	CLKIN frequency ok	-	250 1	-	kHz MHz

### 3.3.11 Filtering times

**Table 18. Failure filtering times characteristics**

Symbol	Parameter <sup>(1)</sup>	Condition	Min.	Typ.	Max.	Unit
t <sub>OL</sub>	Openload filtering time	outputs off	20	44	70	µs
t <sub>UC</sub>	Under current filtering time	-	10	20	40	µs
t <sub>OVL</sub>	Overload switch-off delay time	-	10	20	40	µs
t <sub>SD</sub>	Thermal shutdown delay time	-	10	40	80	µs
t <sub>TW</sub>	Thermal warning filtering time	-	10	20	40	µs
t <sub>DX_L</sub>	Dx loss filtering time	-	1	2	5	µs
t <sub>PGND_L</sub>	Power GND loss filtering time	-	10	20	40	µs
t <sub>SGND_L</sub>	Signal GND loss filtering time	-	10	20	40	µs
t <sub>EN_F</sub>	EN filtering time <sup>(2)</sup>	-	1.5	2	2.5	µs
t <sub>CLK_F</sub>	CLKIN-failure detection time	-	140	200	310	µs
t <sub>CURR_F</sub>	Current not reachable failure filtering time	-	7.75	8	8.25	ms

1. All parameters based on valid CLKIN (250 kHz / 1 MHz) signal.

2. Digital filter only for falling edges and analog filter for both edges.

Table 19. SVDT test timing

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$t_x$	Minimum passing test time	SVDT Enabled $I_{Qx} < I_{UC}$	90	100	110	$\mu s$
$t_y$	Maximum failing test time	SVDT Enabled $I_{Qx} < I_{UC}$	450	500	550	$\mu s$

Refer to [Section 4.8.13: Silent valve driver test \(SVDT\)](#).

### 3.3.12 $V_D$ measurement

(refer to [Section 4.5.2  \$V\_D\$](#)  for details)

Table 20.  $V_D$  measurement electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{Dtol}$	$V_D$ measurement accuracy	$V_D = 10 V$	-	-	10	%
$V_{res}$	Voltage resolution	-	-	0.1	-	V
$t_{int}$	Integration Time	$V_D = 13.5 V$		0.71	-	ms

$V_D$ -Integration time increases linearly with  $V_D$ .

Table 21.  $V_D$  measurement bit values

SPI - bit	D8	D7	D6	D5	D4	D3	D2	D1	D0
$V_D$ -value	16 V	8 V	4 V	2 V	1 V	1/2 V	1/4 V	1/8 V	1/16 V

### 3.3.13 $R_S$ measurement

(refer to [Section 4.5.2 :  \$R\_S\$](#)  for details)

Table 22.  $R_S$  measurement electrical characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$R_{S\_M\_ACC}$	$R_S$ -measurement accuracy	-	-	-	10	%
$R_{S\_M\_RES}$	$R_S$ -measurement resolution	-	-	8.6	-	m $\Omega$

Table 23.  $R_S$  SPI bit values

SPI - Bit	D8	D7	D6	D5	D4	D3	D2	D1	D0
$R_S$ -value	4 $\Omega$	2 $\Omega$	1 $\Omega$	1/2 $\Omega$	1/4 $\Omega$	1/8 $\Omega$	1/16 $\Omega$	1/32 $\Omega$	1/64 $\Omega$

Note:  $R_S$ -measurement time increases linearly with  $R_S$ .

### 3.3.14 V\_FWD measurement

(refer to [Section 4.5.2 : V\\_FWD](#) for details)

**Table 24. V\_FWD measurement electrical characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_FWD_ACC	V_FWD measurement accuracy	-	-	-	10	%
V_FWD_RES	V_FWD measurement resolution	-	-	7.8	-	mV
V_FWD_MEAS	Expected measured voltage range	-	0.5	0.7	1.3	V

V\_FWD-measurement time increases linearly with V\_FWD.

**Table 25. V\_FWD SPI bit Values**

SPI - Bit	D8	D7	D6	D5	D4	D3	D2	D1	D0
V_FWD	2 V	1 V	1/2 V	1/4 V	1/8 V	1/16 V	1/32 V	1/64 V	1/128 V

### 3.3.15 Internal oscillator

**Table 26. Internal oscillator electrical characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f <sub>osc</sub>	Oscillator frequency	-	1.4	2.0	2.6	MHz

### 3.3.16 SPI timing characteristics SPICLK, MISO, MOSI, SPICS

**Figure 9. SPI timing characteristics SPICLK, MISO, MOSI, SPICS**

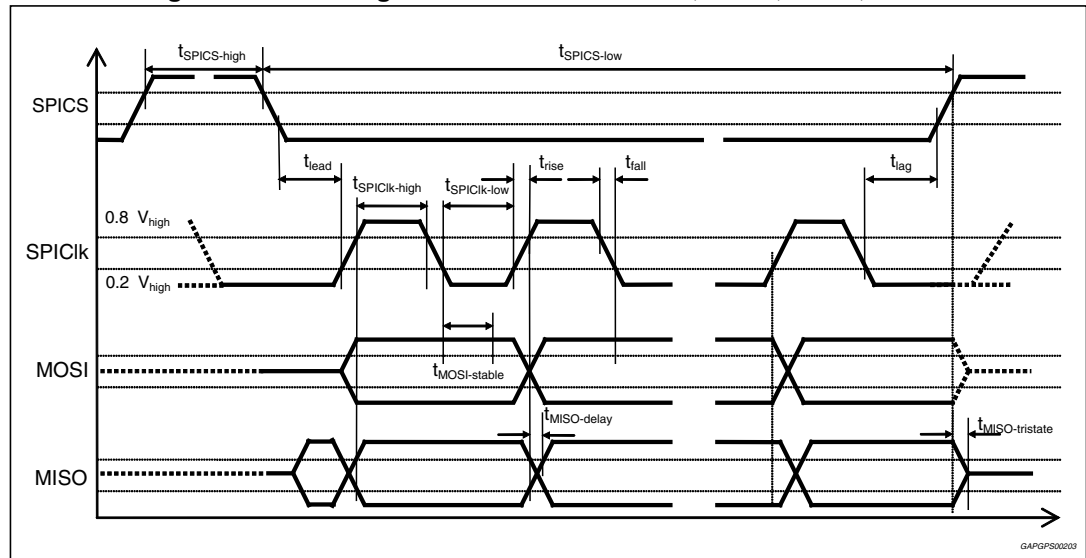


Table 27. SPI timing characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$f_{\text{SPICLK}}$	SPICLK frequency	$C_{\text{load}} \leq 30 \text{ pF}$	0	-	5	MHz
$t_{\text{SPICLK-high}}$ , $t_{\text{SPICLK-low}}$	SPICLK high time / low time	-	68	-	-	ns
$t_{\text{lead}}$	SPICS -> SPICLK delay	-	80	-	-	ns
$t_{\text{lag}}$	SPICLK -> SPICS delay	-	60	-	-	ns
$t_{\text{MOSI-stable}}$	MOSI stable	-	68	-	-	ns
$t_{\text{rise}}/t_{\text{fall}}$	SPICLK, MOSI rise time / fall time	$C_{\text{load}} \leq 150 \text{ pF}$	0	-	100	ns
$t_{\text{MISO-delay}}$	SPICLK -> MISO delay	$C_{\text{load}} \leq 150 \text{ pF}$	-	-	80	ns
$t_{\text{MISO-rise}}$ , $t_{\text{MISO-fall}}$	MISO rise time / fall time <sup>(1)</sup>	$C_{\text{load}} \leq 15 \text{ pF}$ $C_{\text{load}} \leq 50 \text{ pF}$ $C_{\text{load}} \leq 65 \text{ pF}$	0.8 2.5 3.5	2 7 9	7 21 28	ns ns ns
$t_{\text{SPICS-high}}$	SPICS high time / low time	$C_{\text{load}} \leq 150 \text{ pF}$	150	-	-	ns
$t_{\text{MISO-tri}}$	MISO tri-state	$C_{\text{load}} \leq 150 \text{ pF}$	-	-	100	ns

1. guaranteed by design

**Note:** The MISO pin is tri-stated with a weak pull-up when SPICS is high.

## 4 Circuit description

The L9374LF is a four channel low side driver with integrated recirculation diodes intended for ABS applications. The device communicates entirely by 16 individual SPI commands. All outputs can be switched or PWMed. Two outputs have the additional capability of providing current regulation

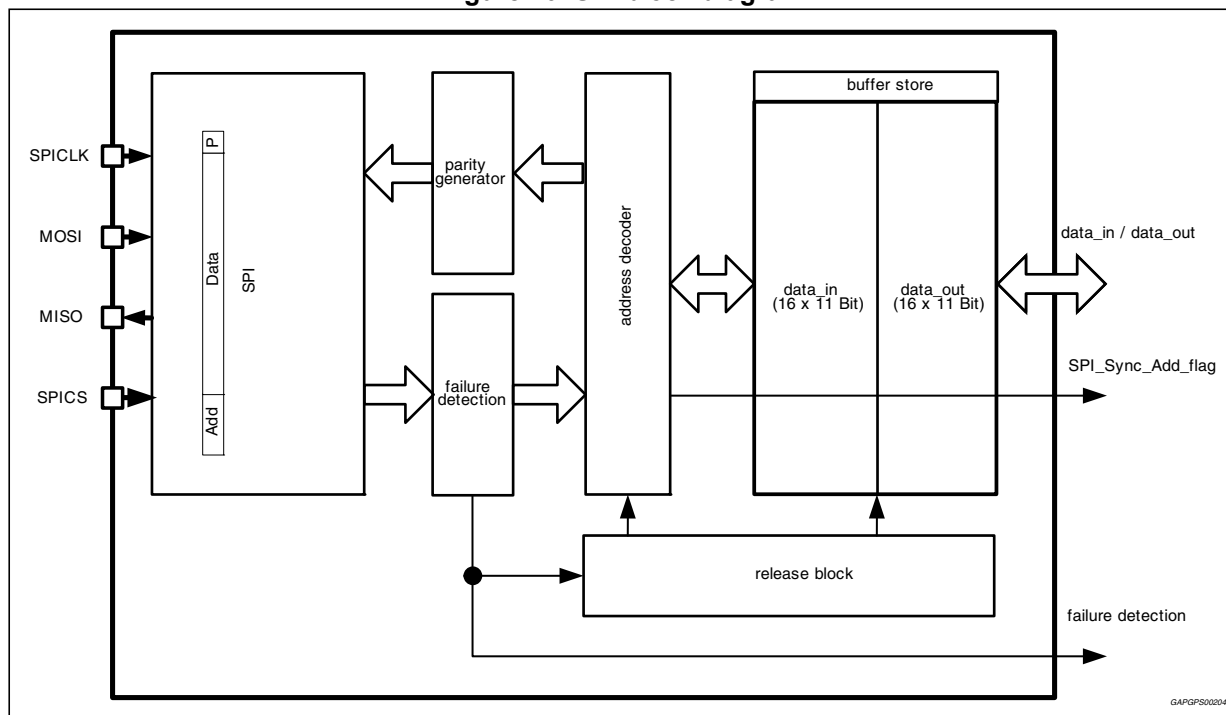
It is possible to program two consecutive PWM duty cycles / Current levels at one time. Individual switched on-times can also be generated.

All outputs have high level diagnostic capabilities. These include off state open load, under current, shorted load, gate voltage monitoring, thermal warning and shutdown flags. Higher level diagnostics include a Silent-Valve-Detection-test (SVDT) to verify load and driver integrity as well as a Built-in-Self-test (BIST) to verify the internal logic integrity. The L9374LF can detect and report a missing recirculation diode, Ground loss, Clock failure, and synchronization failure.

### 4.1 SPI serial peripheral interface

The L9374LF SPI is a fully bidirectional serial interface configured as a SLAVE for communication between a  $\mu$ C (the MASTER) and the L9374LF. All data management is handled in 16 sets of SPI registers of 16 bits each. There are 16 input or command registers and 16 status registers. All output control including current control and PWM / switching timing is realized internally. The control parameters (Duty Cycle, Duration, and Current regulation) are programmed via serial communication. The 16 status registers provide a high level of diagnostic capability from output status to internal control parameter confirmation.

Figure 10. SPI block diagram



Messages from the master ( $\mu\text{C}$ ) to the L9374LF is sent over the MOSI (Master out Slave In) pin. Messages from the L9374LF to the master will be sent over the MISO (Master in Slave Out) pin.

The master starts the communication with a '1'  $\rightarrow$  '0' transition on the SPICS pin. After  $t_{\text{LEAD}}$ , (Table 27.) the master sends a clock signal to the SPICLK and data to the MOSI pin. The SPICLK pin must be low at the falling edge of SPICS and remain low for  $t_{\text{LEAD}}$  for correct communication to occur. The SPICS pin must rise after every 16 bits sent.

The MISO pin is tri-stated with an high ohmic pull-up resistor when the SPI chip select (SPICS) pin is held high.

The SPI has the following features:

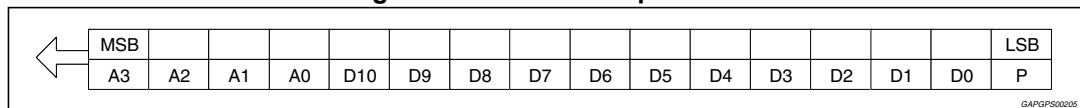
- 4 wire SPI (SPICS, SPICLK, MOSI, MISO)
- Word length of 16-Bits (0..15)
- 4 address and 11 data bits and one parity bit
- 16 receive-buffers (11 bit wide)
- 16 send-buffers (11 bit wide)

#### 4.1.1 General protocol

The protocol has the following structure:

- A parity-bit at the LSB and eleven data bits (bits 1 to 11).
- The four address bits are at the highest position at the transfer (bits 12 - 15).
- SPI communication begins with the MSB.
- High level = '1'
- Low level = '0'

Figure 11. General SPI protocol



- Ax: address bits
- Dx: data bits
- P: parity bit

A message from the L9374LF to the master  $\mu\text{C}$  (MISO) contains 4 address bits. These bits are not a copy of the received address from the previous transmission, but are addresses that were decoded from the address decoder. This is done so that the master ( $\mu\text{C}$ ) has the ability to discern the integrity of the L9374LF address decoder.

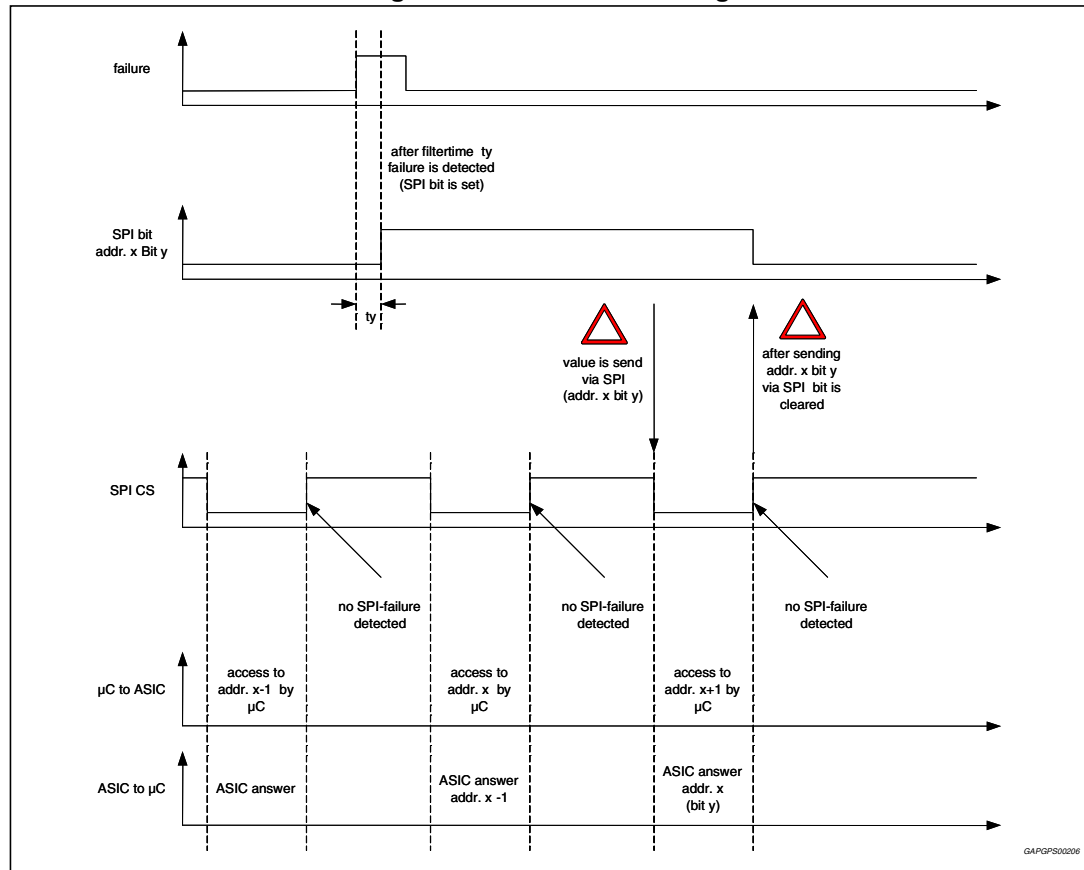
Every time an error bit in one of the SPI registers is set by the L9374LF it will remain set until the corresponding register has been read out via SPI. Once a status register has been read the corresponding register will be reset upon the rising edge of SPICS.

Every SPI communication writes data into a register (read only not possible). Every SPI response is associated with the address of the message sent one communication before.

### 4.1.2 SPI failure detection

SPI communications sent to the L9374LF that contain errors are ignored. This inaction includes both the commands given and the data retrieved. That is, commands are ignored and the initial state of the output is not changed. Also data registers referenced by the erroneous SPI communication will not be reset.

Figure 12. SPI error handling



Three functions are monitored to discern a correct SPI communication from the master:

1. Correct number of Clock pulses in SPICLK per transfer.  
During each SPICS-low-phase the L9374LF counts the number of positive edges of SPICLK. If this number is unequal to 16 a SPICLK-error is detected.
2. Parity check (odd)  
The L9374LF detects a parity error if the number of '1's within a transfer is even.
3. Data-failure monitoring:  
This bit is set if the master writes inappropriate data to any of the configuration registers (2/14/15).

### 4.1.3 Data transfer

Upon the completion of each 16 bit SPI command (rising edge of SPICS), data is transferred from the SPI block to the appropriate internal registers. Some internal SPI registers are reset (such as fault bits) once they are accessed.



#### 4.1.4 Address decoder

The address decoder routes incoming data into the appropriate receive buffer and sets up the appropriate send buffer register to transmit information back to the master (MISO) for the subsequent SPI communication.

#### 4.1.5 Parity generator

The parity generator completes the output messages with a parity bit. The number of '1's within an output-transfer has to be odd. Parity is verified prior to the SPICS going high.

#### 4.1.6 Initial MISO information

After initial power on, the first SPI-answer from the L9374LF reflects the Chip-ID information. Typically, the information will appear as follows:

A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P
1	0	1	0	0	0	1	1	1	0	0	0	0	1	1	0

This information is unique to this device and reflects specific device information relevant only to ST.

#### 4.1.7 Register map

This is a brief reference to the register locations within the L9374LF. Refer to [Section 5: Programmers guide](#) for a more detailed description of each register.

### Command buffer (data in)

**Table 28. Command buffer (data\_in)**

Address(HEX)	Content	Buffer name
0	Sync-trigger, Reset, and Sync values	SYNC_REG
1	STW min and max values	STW_V
2	Configuration register	CONFIG 1
3	Fast Switch ON gate commands	FSON
4	Duration Registers doe Q1 /Q2	Duration Q1/Q2
5	Duration of current 1 Q3 + duration of current 1 Q4	Duration Q3/Q4
6	Duty cycle 1 Q1	DUTY1_Q1
7	Duty cycle 2 Q1	DUTY2_Q1
8	Duty cycle 1 Q2	DUTY1_Q2
9	Duty cycle 2 Q2	DUTY2_Q2
10	Current/duty cycle1 Q3	CUR/DTY1_Q3
11	Current/duty cycle 2 Q3	CUR/DTY2_Q3
12	Current/duty cycle 1 Q4	CUR/DTY1_Q4
13	Current/duty cycle 2 Q4	CUR/DTY2_Q4
14	Current / PWM controller configuration register 2	CONFIG 2
15	Current / PWM controller configuration register 3	CONFIG 3

### Status buffer (data out)

**Table 29. Status buffer (data\_out)**

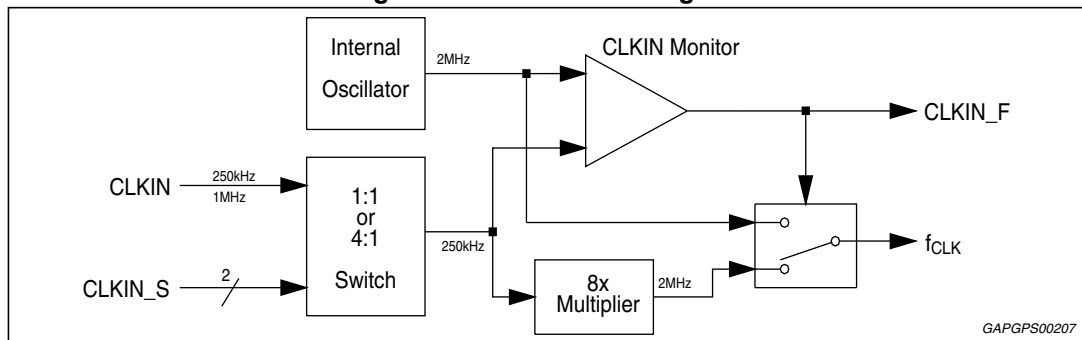
Address(HEX)	Content	Buffer name
0	General status	G_STATUS
1	Q1 output status register	STATUS_Q1
2	Q2 output status register	STATUS_Q2
3	Q3 output status register	STATUS_Q3
4	Q4 output status register	STATUS_Q4
5	Voltage of Dx	VD
6	Output-duty Q3	OUT_DUTY_Q3
7	Output-duty Q4	OUT_DUTY_Q4
8	ISAT value for Q3	ISAT_Q3
9	ISAT value for Q4	ISAT_Q4
10	Internal diode Voltage measurement	V_FWD
11	Measurement resistor	RS
12	Current controller status	CC-STATUS
13	Error average Q3	ERRORAVG_Q3
14	Error average Q4	ERRORAVG_Q4
15	Reserved → data ,000 0000 0000'	RESERVED

A more detailed explanation about the register settings can be found in section [Section 5: Programmers guide](#).

## 4.2 Clock

The clock controller contains a CLKIN-monitoring function to validate the CLKIN frequency, a clock multiplier to produce an internal 2 MHz clock, and an internal oscillator for monitoring purposes and backup.

**Figure 13. Clock block diagram**



### 4.2.1 Clock multiplier

The Clock Multiplier provides a steady 2MHz signal ( $f_{CLK}$ ) for the internal logic based on the CLKIN signal. The multiplier factor is determined by setting the CLKIN\_S bits in the SPI Command register [Configuration register 1 \(address 2\)](#). It is possible to have the wrong CLKIN\_S bits set for a specific CLKIN frequency. When this occurs a CLKIN failure (CLKIN\_F) is registered.

### 4.2.2 Internal oscillator

The 2MHz internal oscillator ( $f_{osc}$ , [Table 26.](#)) provides a comparison signal used to validate the incoming CLKIN signal. If the CLKIN signal is determined to be out of range then the internal oscillator is used to provide clock signals internal to the L9374LF. The internal oscillator does not have the accuracy of a proper CLKIN signal. Therefore the diagnostic filter times will reflect the accuracy of this clock for that case.

### 4.2.3 CLKIN signal monitoring

The CLKIN signal is an external 250 kHz or 1MHz signal from the  $\mu C$  to the L9374LF. This signal is monitored to be within a specified range ( $f_{CLKIN\_L} < f_{CLKIN} < f_{CLKIN\_H}$ , [Table 17.](#)). If the value is out of range, then the CLKIN\_F (CLKIN failure) bit is set to '1'. If a CLKIN failure ( $f_{CLK}$  out of range) is detected, the outputs are disabled and the internal 2MHz oscillator is used as the clock for the internal logic.

**Table 30. Clock validation**

CLKIN	CLKIN_S 250 kHz / 1 MHz	$f_{CLK}$	CLKIN_F
250 kHz	250 kHz	2 MHz	0 (no failure)
1 MHz	1 MHz	2 MHz	0 (no failure)
250 kHz	1 MHz	1 MHz	1 (failure)
1 MHz	250 kHz	8 MHz	1 (failure)

## 4.3 Synchronization controller

Due to the natural SPI communication task time jitter, proper actuation of the outputs requires some level of synchronization. The Synchronization Controller provides synchronized output actuation eliminating SPI task time jitter issues.

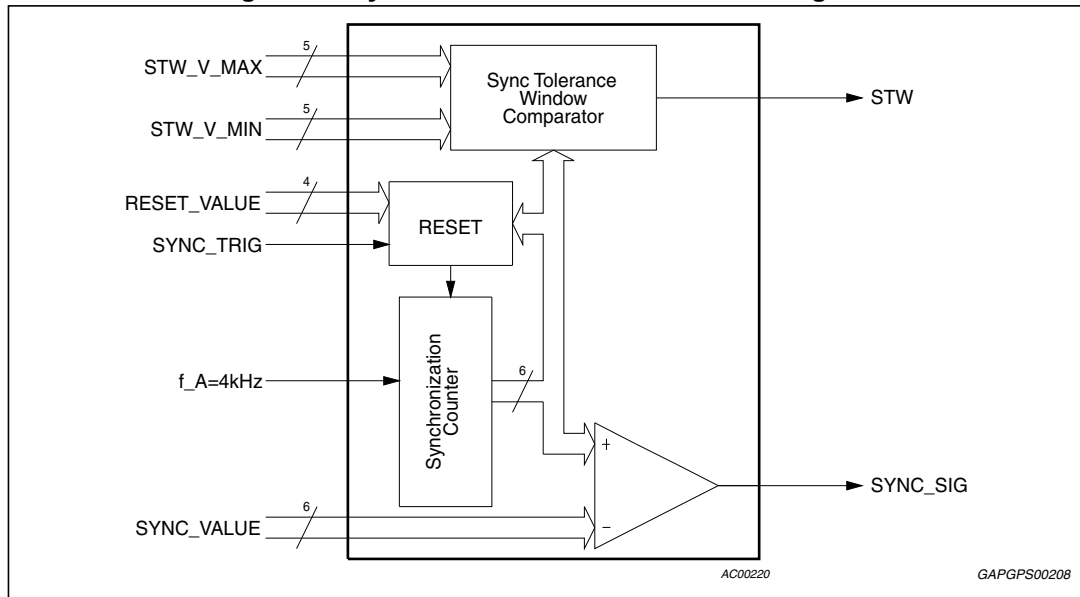
This function forces the outputs to change their commanded state at a specified point in time outside the SPI communication window. This also ensures a more stable SPI communication by minimizing ground fluctuation due to output switching during periods of SPI communications. This delay between the SPI commands and the output actuation is programmed by setting the RESET\_VALUE and SYNC\_VALUE parameters located in register 0.

### 4.3.1 Output synchronization

The RESET\_VALUE time value is determined by using the typical time between SPI cycles. When programmed properly, the SPI communications occur at or around the RESET\_VALUE timing. The Sync Tolerance Window (STW) is an interval of time between RESET\_VALUE times where accessing the Sync [Section 5.1.1: Sync + Sync-trigger register \(address 0\)](#) during this interval generates a sync failure (SYNC\_F). This window is defined by the parameters STW\_V\_MIN and STW\_V\_MAX.

The SYNC\_VALUE is a programmed delay after the RESET\_VALUE when the output transitions occur. This delay is typically set as half of the RESET\_VALUE. This sets the output transitions furthest from each SPI cycle and during the STW.

Figure 14. Synchronization controller block diagram



### Inputs

The synchronization controller receives the following input signals:

- $f_A = 4$  kHz for internal clocking.
- $\text{SYNC\_TRIG} = "1"$  initiates the synchronization timing with that SPI event.
- SPI synchronization values ( $\text{SYNC\_VALUE}$ ,  $\text{RESET\_VALUE}$ ,  $\text{STW\_V\_MIN}$ ;  $\text{STW\_V\_MAX}$ ) provide the parameters that allow for output synchronization.

### Outputs

The synchronization controller provides the following output signals:

- The STW signal is used in conjunction with accessing address 0 to notify the master that the SPI cycles are within the programmed exclusionary window ( $\text{SYNC\_F}=1$ ).
- The SYNC\_SIG initiates the actuation of the new output commands.

The synchronization counter increases its value with every period of  $f_A$ . When the value of the counter equals the SYNC\_VALUE a synchronization signal (SYNC\_SIG) is generated ( $\text{SYNC\_SIG}='1'$ ).

The synchronization counter continually counts to the RESET\_VALUE and resets unless a SYNC\_TRIG command is sent. If a SYNC\_TRIG command is sent then the counter resets immediately. Upon resetting the SYNC\_TRIG and STW signals are reset ( $\text{SYNC\_SIG} = \text{STW} = '0'$ ).

### Normal sequence

When stepping through a normal sequence of events the following occurs:

- At a SYNC\_TRIG (SYNC\_TRIG='1') command the synchronization counter, STW and SYNC\_SIG flags are reset (STW='0', SYNC\_SIG='0')
- The counter counts up at a rate defined by  $f_A = 4 \text{ kHz}$ .
- When the counter value reaches STW\_V\_MIN the STW flag is set (STW='1')
- When the counter value reaches SYNC\_VALUE the SYNC\_TRIG flag is set (SYNC\_TRIG='1') which activates the most recent output commands.
- When the counter value reaches the STW\_V\_MAX value the STW flag is reset (STW='0')
- When the counter value is equal to the RESET\_VALUE the counter is reset and the output signal sync\_signal is reset (SYNC\_SIG='0')

### Disallowed programming states

Erroneous programming results in the STW flag being set '1'

- If the STW\_V\_MIN value is higher than or equal to STW\_V\_MAX value the STW flag is set (STW = 1)
- If the STW\_V\_MAX value is higher or equal to the RESET\_VALUE value the STW flag is set (STW = 1)

### Synchronization failure

Sync failure detects a timing error in the output command synchronization. The master  $\mu\text{C}$  programs a timing window (STW) where accessing to the Status Register address 0 is not allowed. If there is an access to the Status Register address 0 when the STW flag is set then a sync-failure is generated (SYNC\_F = 1). Also, a SYNC\_F will be detected if there is no SPI traffic at all between two SYNC\_SIG events. This status will be read out on the subsequent SPI transfer.

Without a SYNC\_SIG or at sync-failure there is no effect for the actuation and setpoints

### Synchronization controller programming

It is necessary to write into two registers (Command Register addresses 0 and 1, sections 5.1.1 and 5.1.2) to program the Synchronization Controller. The SYNC\_VALUE, the RESET\_VALUE and the SYNC\_TRIG values are programmed through address 0. The SYNC\_TRIG is written to once to initialize the counter. Once initialized the SYNC\_TRIG bit is reset by the controller. Subsequent SPI transfers the SYNC\_TRIG bit should not be set to avoid re-initializing the sync counter. There is no influence on the sync counter if the SYNC\_TRIG is not set. Occasionally, the sync counter may need re-initializing depending on the timing between the RESET\_VALUE and the  $\mu\text{C}$  loop time. The RESET\_VALUE is incremented by 1ms intervals. The SYNC\_VALUE is incremented by 250 $\mu\text{s}$  intervals.

The STW\_V\_MIN and STW\_V\_MAX values are programmed via register 1 (Section 5.1.2). Their interval length is dependant on the RESET\_VALUE MSB (address '0', bit D9)

**Table 31. Sync. tolerance window interval length**

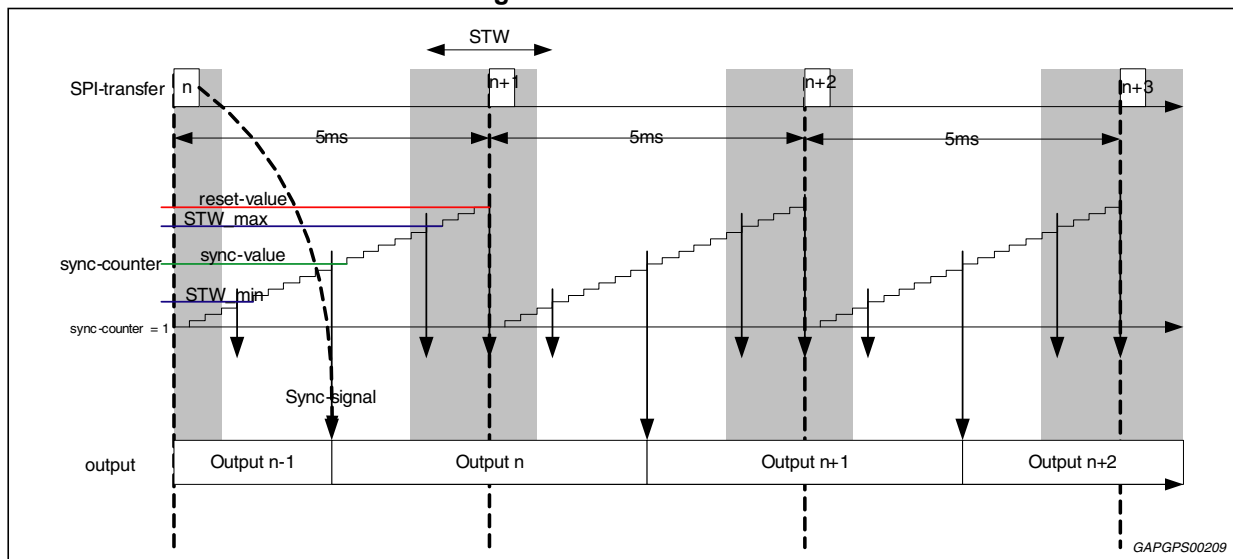
RESET_VALUE (add.0, bit D9)	RESET_VALUE Duration	Sync tolerance window interval
0	<8ms	250 $\mu\text{s/bit}$
1	$\geq 8\text{ms}$	500 $\mu\text{s/bit}$

**Example**

Example for a 5 ms cycle time, 2.5 ms SYNC\_VALUE-, STW of +1.75 ms/-1.25 ms:

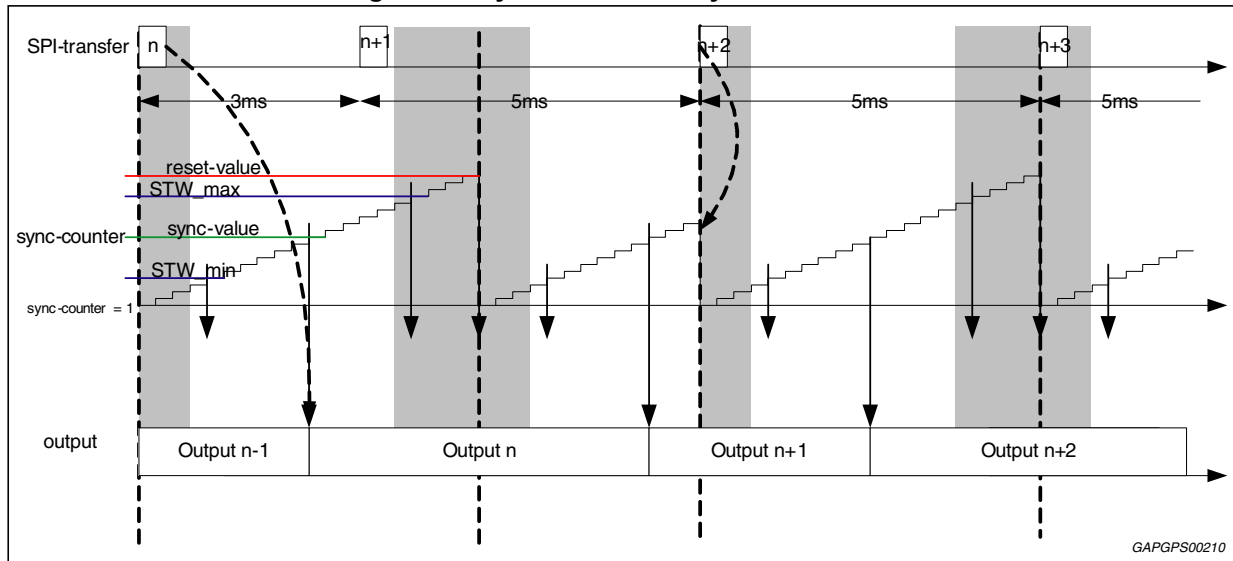
- Cycle time:
  - For programming the cycle time the master has to write the RESET\_VALUE (4 bit) via SPI. One bit has the resolution of  $4/f_A = 1 \text{ ms}$ .
  - RESET\_VALUE:  $5 \text{ ms} / 1 \text{ ms} = 5 \rightarrow 0101_{(2)}$
- SYNC\_VALUE:
  - For programming the sync-signal the master has to write the SYNC\_VALUE (6 bit). The LSB has the resolution of  $250 \mu\text{s}$ .
  - SYNC\_VALUE:  $2.5 \text{ ms} / 250 \mu\text{s} = 10 \rightarrow 00 1010_{(2)}$
- Sync tolerance window:
  - For programming the STW the master must write min and max values (2 x 5 bit):  
 STW\_V\_MIN: 0.75 ms  
 STW\_V\_MAX: 3.75 ms  
 STW\_V\_MIN:  $0.75 \text{ ms} / 250 \mu\text{s} + 1 = 4 \rightarrow 0 0100_{(2)}$   
 STW\_V\_MAX:  $3.75 \text{ ms} / 250 \mu\text{s} + 1 = 16 \rightarrow 1 0000_{(2)}$

**Figure 15. Normal mode**



SPI transfer means transfer of all send and receive registers (0 through 15).

Figure 16. Sync-failure + re-synchronization

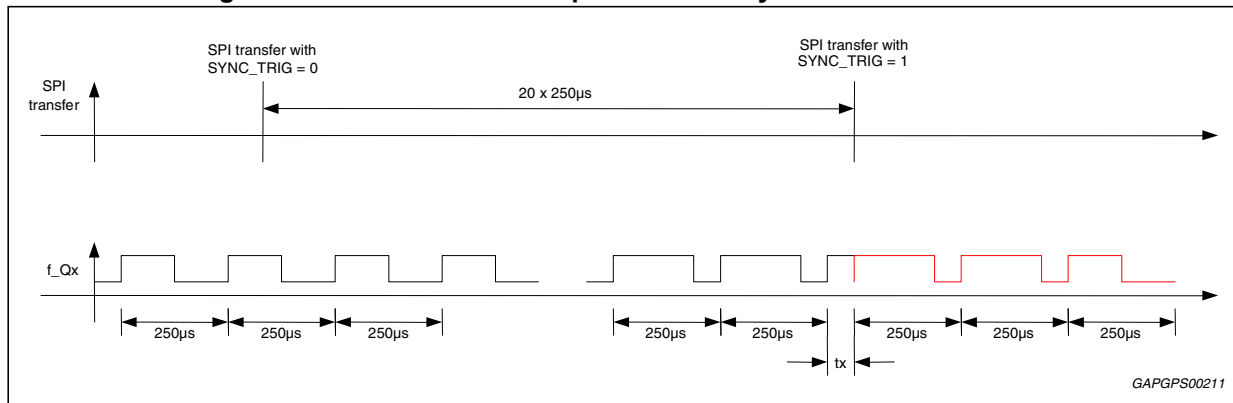


### Re-synchronizing

The master sets the SYNC\_TRIG bit to '1' (section 5.1.1) to re-initialize the sync counter. This re-synchronizes the L9374LF synchronization controller to the master. When this bit is set three counters are reset: the PWM counter (output frequency and duty cycle), synchronization counter and the duration counter. The SYNC\_TRIG bit is reset (set to '0') by the L9374LF upon re-synchronization.

The picture below shows the behavior of the output when the synchronization is done. The time tx is anything lower than 250 μs.

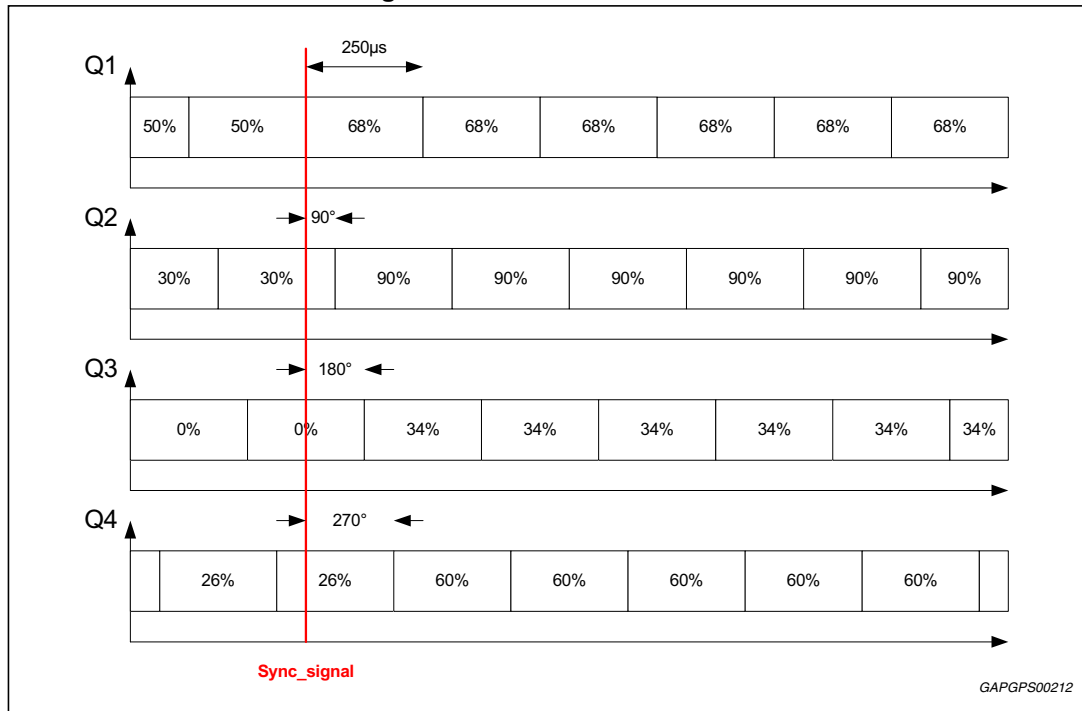
Figure 17. Behavior of the output when the synchronization is done



### 4.3.2 Time shift between output actuation

The actuations of the outputs are time shifted by 90° (typ. 62.5 μs) to offset their effect on the supply during switching. This balances the incremental switching current and reduces the EME generated by the switching of these channels. The new duty cycle or target current also becomes valid with this 90 degree time shift after the SYNC\_SIG.

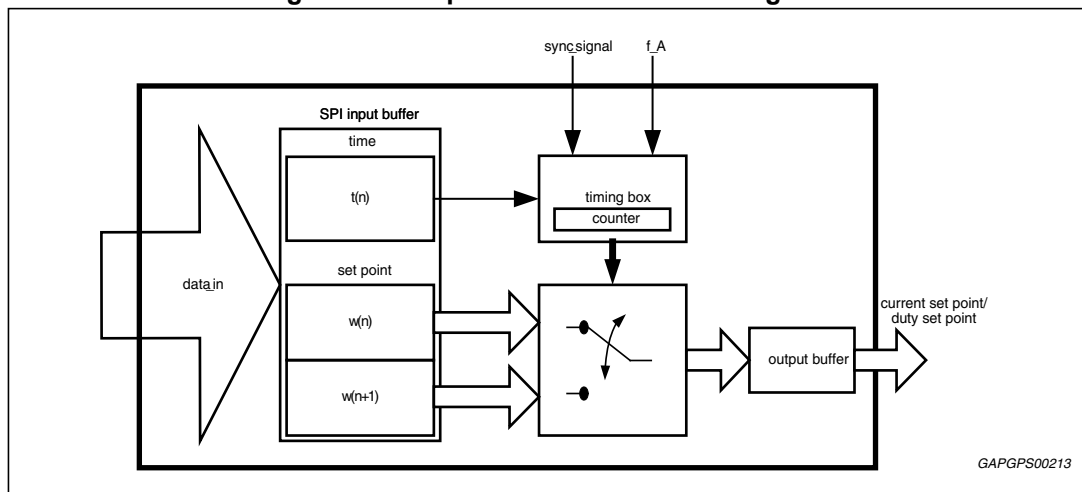
Figure 18. Channels time shift



### 4.4 Set-point controller

The set point controller generates a PWM duty cycle based on a duty cycle value or a regulated current value from the SPI command registers for each output. This circuit is designed to generate two different PWM duty cycle / current regulation values for each output per SPI cycle. This translates to a duty cycle/current level  $w(n)$  for a duration  $t(n)$  and then a second duty cycle/current level  $w(n+1)$  until otherwise commanded for each output per SPI cycle. Depending on what is driving this controller (Direct SPI command (in the form of a duty cycle value) or Current Controller) the end result is either a fixed commanded PWM duty cycle or a regulated current.

Figure 19. Set-point controller block diagram





The set point controller receives the following input information:

- Synchronization-signal (SYNC\_SIG)
- Frequency of the PWM-generator ( $f_A$ ; duty 50 %)
- Set Point 1 (Duty cycle/current 1) =  $w(n)$ (9 bits)
- Set Point 2 (Duty cycle/current 2) =  $w(n+1)$ (9 bits)
- Duration (duration of Duty cycle/current 1) =  $t(n)$ (5 bits)

The Duty cycle/current set point value is the only output signal.

The timer commands the change between  $w(n)$  and  $w(n+1)$  to the Duty cycle/current set point according to the programmed timing value  $t(n)$ . The counter in the timing box is controlled by  $f_A$  and bit D9 of address 0 (see [Table 33](#)). If the value of the counter is lower than  $t(n)$  the Duty Cycle/current set point is set to  $w(n)$ . If the value is equal or higher the Duty Cycle/current set point is set to  $w(n+1)$ .

**Table 32. Example of PWM duration timing,  $t(n)$**

Duration value (5 Bit)	Add. 0, bit D9	on-time (ms)
00000 <sub>(2)</sub>	X	0 ms (off)
11111 <sub>(2)</sub>	0	7.75 ms
01101 <sub>(2)</sub>	0	3.25 ms
11111 <sub>(2)</sub>	1	15.5 ms
01101 <sub>(2)</sub>	1	6.5 ms

Note that the RESET\_VALUE MSB (bit 9 of address 0) affects the timer duration. With the MSB set the timer values double. This means if the SPI cycle time is equal or higher than 8 ms ( $>100_{(H)}$ ) the resolution of the duration  $t(n)$  is 500  $\mu$ s per LSB instead of 250  $\mu$ s.

**Table 33. Timer  $t(n)$  resolution versus RESET\_VALUE MSB**

RESET_VALUE (add.0, bit D9)	RESET_VALUE duration	Resolution of timer duration
0	<8ms	250 $\mu$ s
1	$\geq$ 8ms	500 $\mu$ s

The timer counter is reset by the SYNC\_SIG.

All buffers and the timer counter are reset by:

- A CLKIN failure detection (CLKIN\_F = '1')
- A re-synchronization command (SYNC\_TRIG = '1')

The value range (externally programmed):

- $w(n)$ : 9 Bit
- $w(n+1)$ : 9 Bit
- $t(n)$ : 5 Bit

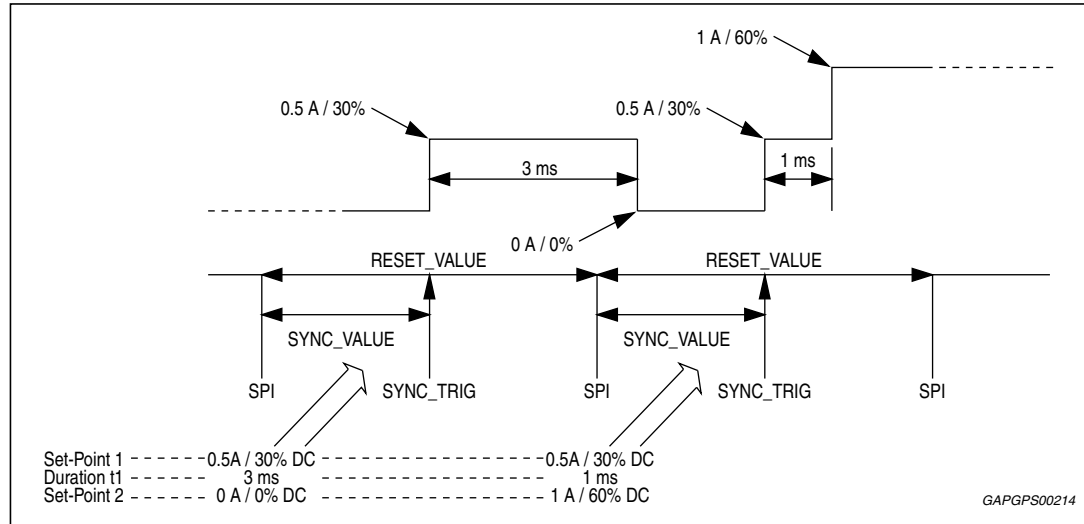
### Example of set-point control

Below is an example of programming two sets of Set-Points sequentially. After programming the parameters that govern the synchronization (RESET\_VALUE, SYNC\_VALUE and the

SWT values) the parameters Set-Point 1 (DUTY1 or CUR/DTY1), Set-Point 2 (DUTY2 or CUR/DTY2) and duration t1 (D\_Qx) are programmed (for programming instructions see section 5.1.5: *Duration registers (address 4 and 5)*).

Generically, after the SYNC\_TRIG the Set-Point 1 is valid for t1 ms. After t1 ms the set-point controller switches to Set-Point 2 until the next SYNC\_TRIG event.

**Figure 20. Set-point control example**



In this example the RESET\_VALUE (and therefore the SPI transfer loop time) is set to 5ms and the SYNC\_VALUE is set to 2.5 ms. This sets the SYNC\_TRIG at 2.5 ms after each SPI transfer. At SYNC\_TRIG, the new information received at the previous SPI transfer is incorporated into the Set-Point Controller.

## 4.5 Current controller

Two outputs (Q3 & Q4) are equipped with a current controller. The current controller converts the Set-Point controller output (Current Set Point) into a current level regulated duty cycle command using a sophisticated algorithm incorporating Load resistance supply voltage, and recirculation path variances.

The current controller output duty cycle information is calculated using a dedicated load model in standard Arithmetic Logic Unit (ALU). This model includes the supply voltage, the recirculation path as well as the load resistance. The load resistance value is programmable via SPI while the recirculation path and the load supply voltage parameters are measured by the L9374LF. These measured values are readable via SPI as well.

### 4.5.1 Load resistance error integration phase

The value of the programmed Load is corrected during the valve actuation. This correction is called the Error Integration Phase and the resulting value (ISAT\_Qx,) is accessible via SPI (Status registers 8 and 9, Section 5.2.5). ISAT\_Qx is an internal value of the current controller. In an ideal system (without any system tolerances) the first approximation is determined by the equation:

$$ISAT \approx \frac{RL\_real}{RL\_SPI} - 1$$

$$RL_{real} \approx RL_{SPI} \cdot (1 + ISAT)$$

ISAT is the relative error of the SPI-Value  $RL_{SPI}$  to the real load  $RL_{real}$  (within an ideal system).

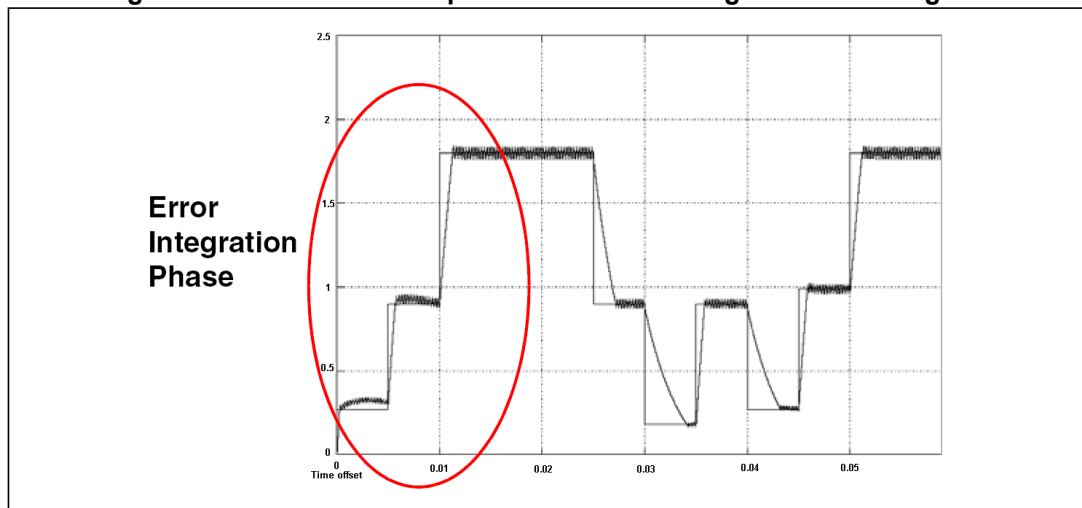
ISAT is a twos complement. The range value is  $\{-1 \dots +(1-LSB)\}$  and

$$|LSB_{(ISAT)}| = \frac{1}{512}$$

With this algorithm a fast controller dynamic can be achieved. *Figure 21* shows the load current response for different target currents. The ISAT\_Qx value integration is disabled for commanded target current values less than  $29_{(DEC)}$ . This corresponds to a target current of:

$$1.8A \times \frac{29}{512} = 102mA$$

**Figure 21. Load current response for different target currents diagram**



Starting at time zero a load error is corrected by modifying the programmed load resistor value with an integral correction factor  $I_{SAT}$ . This integration function is valid for target currents higher than 110mA. If the ISAT value is once corrected in the system the load model will respect the required precision immediately if the target current is reached in the load. To avoid a long error integration phase during actuation of the ABS system it is recommended that the current controlled outputs (Q3 & Q4) be activated periodically. This will allow the L9374LF to adjust the  $I_{SAT}$  parameter for any possible load resistance changes due to temperature.

The integral correction factor (ISAT) is remembered and potentially modified at every load actuation. It can be reset by changing RL or resetting the Current controller (see [Section 5.1.9](#)). If reset, the load resistance error correction will be recalculated upon the next output actuation.

## 4.5.2 Analog signal measure blocks

All internal analog measurements are converted into digital values for use internal to the L9374LF. These values are accessible via SPI. The supply of the load, an equivalent measured resistor, as well as an equivalent recirculation diode forward voltage are measured with the same analog to digital converter sequentially.

- VD, Register 5, bits D0-D8
- RS, Register 11, bits D0-D8
- V\_FWD, Register 10, bits D0-D8

### VD

The VD is measured by the L9374LF as the voltage present at pin D13. The value for VD can be read in the SPI register 5 (refer to [3.3.12: VD measurement](#) and [5.2.3: VD \(address 5\)](#)).

### RS

An equivalent sense resistor is measured internal to the L9374LF. The digital value is stored in SPI-register 11. The value is corresponding to the measurement resistor which is used for the current controller. The digital value is multiplied with the factor of 1.8 (refer to [3.3.13: Rs measurement](#) and [5.2.7: Sense resistor measurement \(Rs\) \(address 11\)](#)).

This means:

$$RS_{(SPI)} = 1.8 \cdot RS_{measured}$$

To get the right value of Rs it is necessary to divide the SPI-value by 1.8.

The resolution of the LSB is 8.7mΩ (typ.) and the parameter range is:

Condition	Rs-value (Ω) (after division by 1.8)
Min	0.62
Typ	1.00 (TK = 1.57 mV/K)
Max	1.58

### V\_FWD

An internal reference diode forward voltage is measured using a fixed bias current. This corresponds to the forward voltage drop across one of the current controller freewheeling diodes. The digital value is stored in SPI Status register 10 (refer to [3.3.14: V\\_FWD measurement](#) and [5.2.6: Reference diode voltage measurement \(V\\_FWD\) \(address 10\)](#)).

### Load current measurements

The load current is measured in both the on and the off state of the output. This measured current is subtracted from the target current which is set by a digital to analog converter. The load current difference is converted into a digital signal for each output. This digital signal is called error average. The error average is an internal value of the current controller. The error average is the integral of the difference between the target current and real current within a PWM period (250 μs).

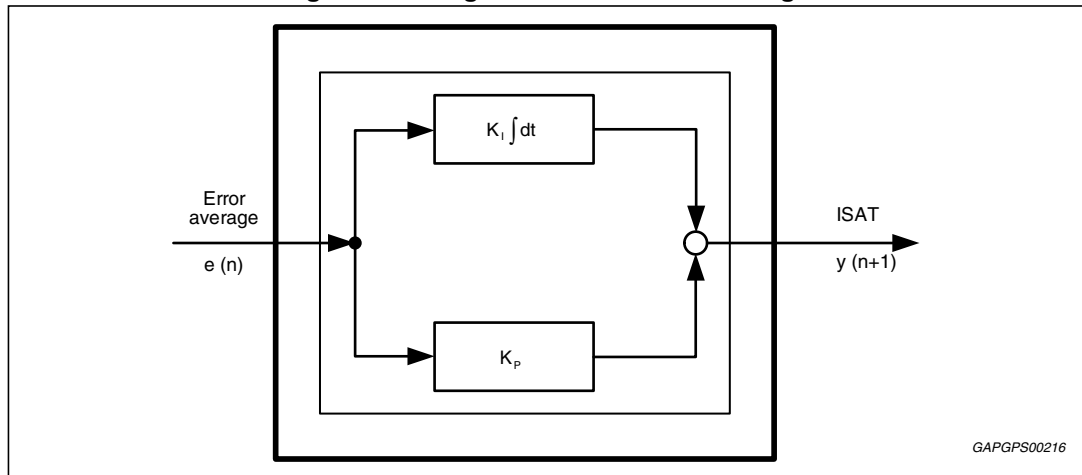
$$ERRORAVG\_Qx = \frac{1}{T} \int_T (I_{target} - I_{real}) dt$$

The error average is a two's complement number. The range value is  $\{-[\text{value}] \dots +([\text{value}] - \text{LSB})\}$  and

$$|\text{LSB}_{(\text{erroraverage})}| = 3.6\text{mA}$$

This value is available in the SPI Status registers 13 and 14 (refer to [5.2.9: Error average \(address 13 + 14\)](#)).

**Figure 22. Integration of the error average**



The current controller calculates the correction factor ISAT out of the error average within an output period ( $1/f_A$ ). During a period ( $n$ ) it calculates the control variable  $y(n)$  with the current deviation  $e(n)$ . At the next period  $n+1$  the control variable  $y(n)$  is used. The value ISAT is always stable if the load resistor value is stable. More details about the usage of ISAT you will find in the following chapters.

### 4.5.3 Duty cycle calculation in the ALU

The ALU is shared between outputs 3 and 4 in the L9374LF. The following equation is used by the ALU to provide the output PWM duty cycle information to the Duty cycle Generator.

$$j_c = \frac{V_{DR} + I_{TARGET} \cdot R_s}{V_{DR} + V_{BAT} + I_{TARGET} \cdot (R_s - R_{DS(on)})} + \frac{I_{TARGET} \cdot R_{LSPI}}{V_{DR} + V_{BAT} + I_{TARGET} \cdot (R_s - R_{DS(on)})} \cdot (I_{SAT} + 1)$$

Where:

$V_{DR}$ : Forward voltage of the recirculation diode (measured value stored in register  $V\_FWD\_Qx$ )

$I_{TARGET}$ : Value programmed by the SPI and provided by the Set Point Unit

$R_s$ : Sense resistor value (measured value stored in register RS)

$R_{LSPI}$ : Value given by the SPI

$V_{BAT}$ : Supply voltage of the load (measured on pin D1/3 stored in register VD)

$R_{DS(on)}$ : fixed value of 500mOhm temperature coefficient is not respected

$I_{SAT}$ : Current Controller correction factor

### 4.5.4 Current controller diagnostic performance

The maximum output value from the current controller is 1FF. This value is only reached if the measured current does not reach the commanded current. If this maximum value extends for more than  $t_{CNR}$  (8ms typ, [Table 18.](#)) the Current Not Reachable flag (CNRx, [5.2.4](#)) is set. The PWM controller contains the check for this condition (for details see [section 4.6.1: Current not reachable detection\(Q3 and Q4 only\):](#)).

A set CNRx flag indicates that the load regulation is out of control and resets the ISAT value. This forces the ALU to re-learn a new ISAT value returning the system to a stable dynamic performance.

The ISAT register can be monitored by the master  $\mu$ C to determine if it is on the positive or negative limit. This will indicate if the current controller is out of range and that the current precision can not be assured.

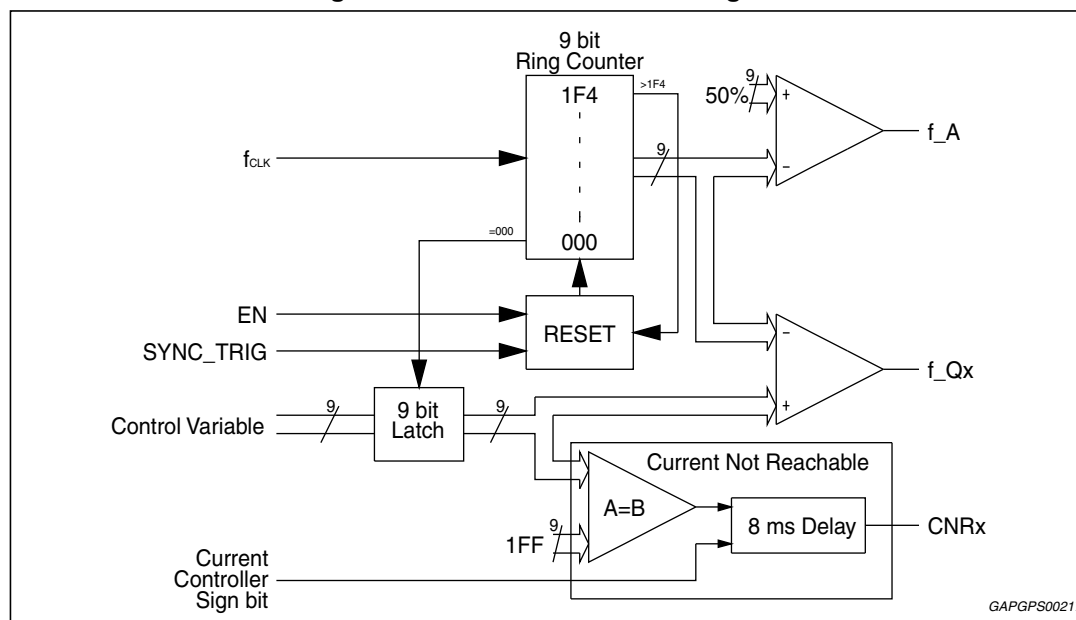
## 4.6 PWM generator

The PWM Generator converts a Duty Cycle Set Point value into a PWM signal for each Output Driver. The duty cycle setpoint can be derived from either a direct SPI command (through the Set-Point Controller directly) or through the Current Controller.

The PWM-generator ([Figure 23](#)) provides a 4 kHz PWM duty cycle ( $f_{Qx}$ ) depending on the value of the 9 bit control variable. A 9-Bit ring counter counts with a frequency of  $f_{CLK}$  (2 MHz). The ring counter output is compared to the control variable. If the value of the counter is lower than the control variable the output  $f_{Qx}$  is high turning on the output Qx. If the value of the counter is equal or higher to the output  $f_{Qx}$  is low turning off the output Qx.

The counter can be reset by either a counter overflow at '1F4<sub>(Hex)</sub>' ( $\rightarrow 500_{(10)}$ ), or by a SYNC\_TRIG command. The control variable value is changed only when the counter passes through zero.

Figure 23. PWM control block diagram



#### 4.6.1 Current not reachable detection(Q3 and Q4 only):

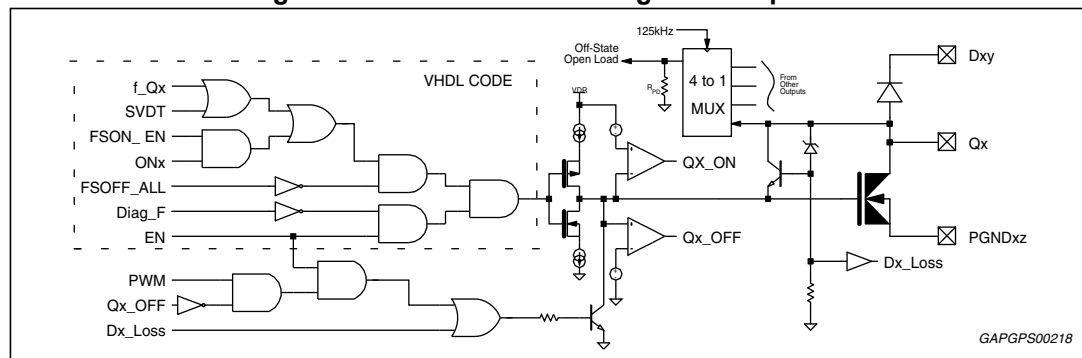
The current not reachable bit is set (CNRx = 1, see section 5.2.4) when the current controller control variable is set to 1FF<sub>(Hex)</sub> for more than t<sub>CURR\_F</sub> (8ms typ, Table 18). This indicates that the current requested has not been attained for that duration. The CNRx bit is also set when the current measurement sign bit is set to 1 for more than t<sub>CURR\_F</sub> (8ms typ, Table 18).

In both cases a failure is indicated via SPI (and the ISAT parameter is reset).

### 4.7 Output driver

The output driver controls the gate of the low side power DMOS as well as provides specific diagnostic information to the SPI diagnostic registers. There are several signals that control the actuation of the output power DMOS. In normal operation the typical input is the f<sub>Qx</sub> from the PWM generator. Other inputs that can turn on the output are the silent valve driver test (SVDT) and the Fast Switch on circuitry. Inputs that can disable the outputs are the fast switch off command, device enable, and certain failure detections that can potentially cause catastrophic damage if the output is left on.

Figure 24. Gate drive block diagram with power



#### 4.7.1 Input controls

The output driver control circuit includes the logical combination of the following signals:

- PWM Generator output signal: (f<sub>Qx</sub>)
- Silent Valve Driver Test signal (SVDT)
- Device Enable (EN)
- Specific Diagnostic failure indications such as PGND loss, overload, over temperature (Diag\_F).
- Fast Switch off for all outputs: (FSOFF\_ALL)
- Fast Switch on Enable: (FSON\_EN)
- Direct SPI driven output switching through the Fast Switch On command (ON<sub>x</sub>)

In normal operation, the signals EN = '1', FSOFF\_ALL = '0', Diag\_F = '0', allow the gate to be driven by the PWM Generator signal (f<sub>Qx</sub>). PWM Generator signal can override the SVDT input if actuation is commanded during an SVDT.

The signals Diag\_F='0', EN='0' and FSOFF\_ALL='1' by-pass all other inputs and turn off the output immediately. The Diag\_F flag is set to '1' at the detection of PGND loss, overload and

over-temperature disabling the affected output. Hardware Enable (EN) is an external pin and is controlled by the  $\mu$ C directly. FSOFF\_ALL is a SPI command that provides a method to shut down all outputs in one SPI command.

### 4.7.2 Diagnostics

Output stage diagnostics provide fault feedback information for the SPI status registers.

#### Gate monitoring

Qx\_ON and Qx\_OFF provide Gate voltage status history information. If the output DMOS Gate voltage is above the Qx\_ON threshold at any point between two SPI cycles the Qx\_ON output will latch on ('1') the SPI bit associated with that signal (bit 6 of status registers 1 - 4). If the output DMOS Gate is below the Qx\_OFF threshold at any point between two SPI cycles the Qx\_OFF output will latch on ('1') the appropriate SPI bit associated with that signal (bit 7 of status of status registers 1 - 4). If an output is PWMmed both Qx\_ON and Qx\_OFF will return a '1' when read by the SPI. Upon reading status registers 1 through 4 the Qx\_ON and Qx\_OFF bits are reset to '0'.

Conversely if the Gate voltage remains above or below the thresholds mentioned the status bits Qx\_ON or Qx\_OFF will indicate only one state was present. At no time will both bit not be set.

**Table 34. Qx\_ON and Qx\_OFF provide gate voltage status history information**

Condition	QX_ON	QX_OFF
duty: 100%	1	0
duty: 0%	0	1
duty: 0% < dc <100%	1	1
defect	0	0

#### Freewheeling diode loss detection

Dx\_Loss transmits to the SPI register latch a '1' whenever the output protection clamping structure is used. This notifies the SPI that the freewheeling diode, Dx, was not in the circuit.

According [Figure 23](#) the Device Enable has a direct link to a separate discharge path on the power gate. Only the high voltage clamp (Dx\_loss) gets a higher priority, to protect the DMOS from high voltage damage if the freewheeling diode is "lost".

**Table 35. Output driver possible input configuration**

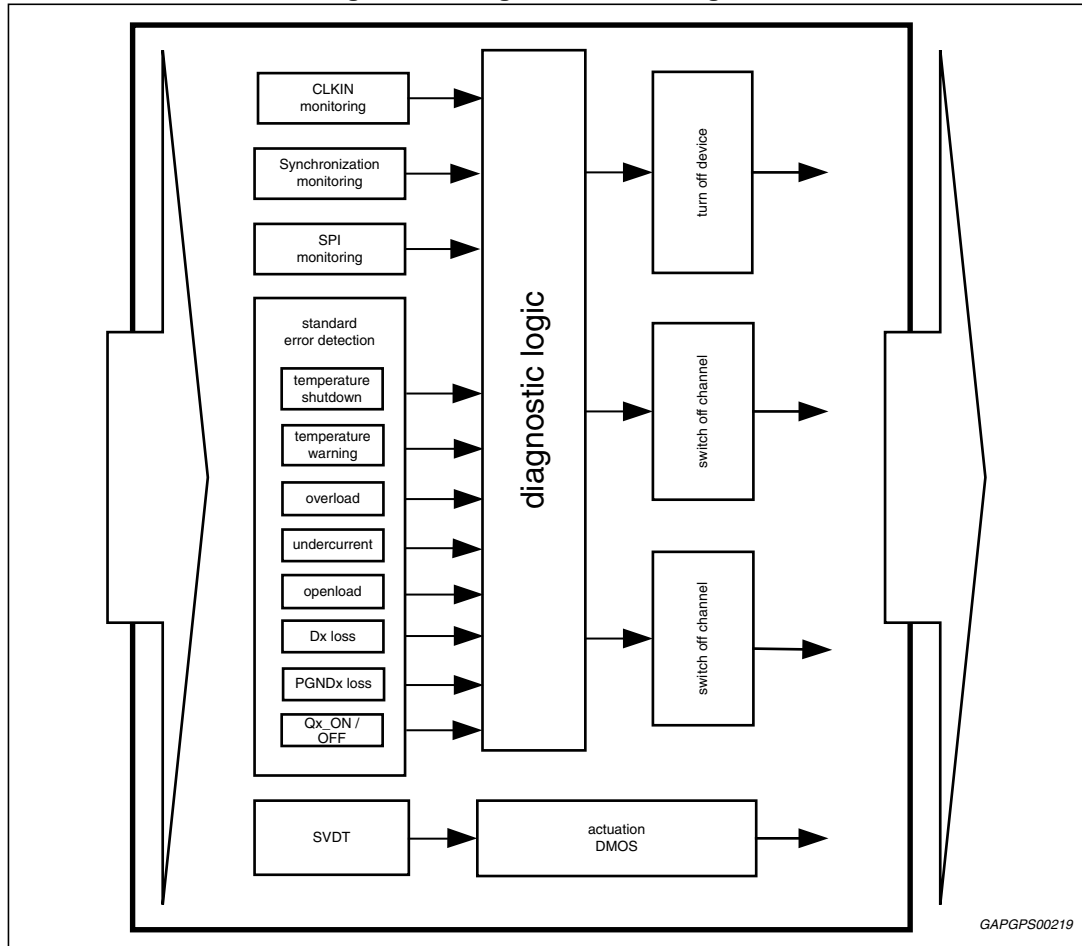
FSOFF_ALL	FSON_EN	ON <sub>x</sub>	Setpoints	Output Qx (0=off, 1=on)	Remark
10	x	x	Q = on / PWM	0	like EN pin
10	x	x	Q = off	0	like EN pin
01	0	x	Q = on / PWM	1 or PWM	-
01	0	x	Q = off	0	-
01	x	0	Q = on / PWM	1 or PWM	-
01	x	0	Q = off	0	-
01	1	1	Q = on / PWM	1	Channel switched on without a sync-signal
01	1	1	Q = off	1	Channel switched on without a sync-signal



## 4.8 Diagnostics

There is a large amount of diagnostic functions in the L9374LF. These functions are designed to verify internal as well as external conditions to the L9374LF. In so doing virtually every function is checked for proper operation. All of the diagnostic results are read by the master  $\mu\text{C}$  via SPI commands.

Figure 25. Diagnosis block diagram



### 4.8.1 Undercurrent / openload

Undercurrent can be detected if the current through the load in on-state is below the undercurrent threshold ( $I_{UC}$ , [Table 15](#)) for longer than the filter time ( $t_{UC}$ , [Table 18](#)). The filter is active in that a counter counts up when the undercurrent is detected (the device is on AND load current below  $I_{UC}$ ) and counts down when undercurrent is not detected (either the device is off OR the current is above  $I_{UC}$ ). Once undercurrent is detected the SPI fault bit is reset when the counter reaches 0.

This bit is not latched unless undercurrent is detected during the SVDT test.

Figure 26. Diagram under current

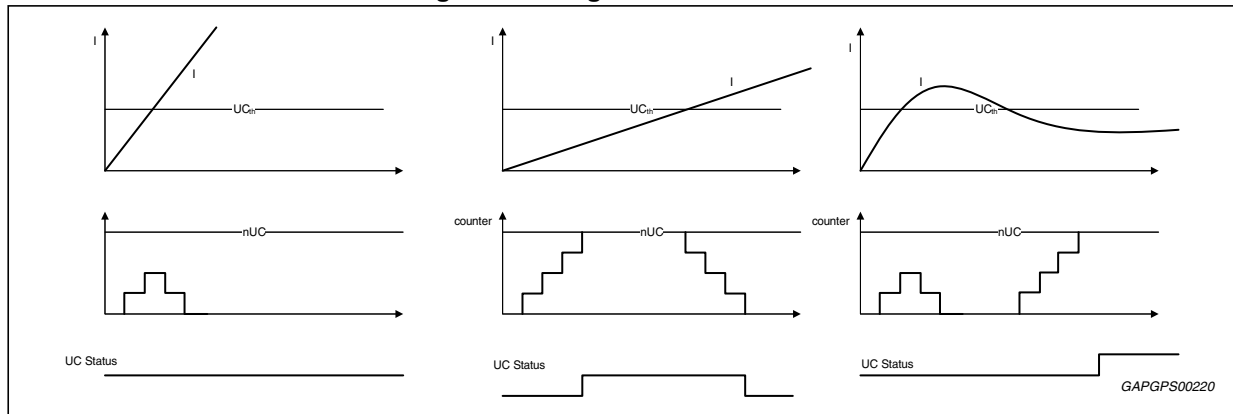
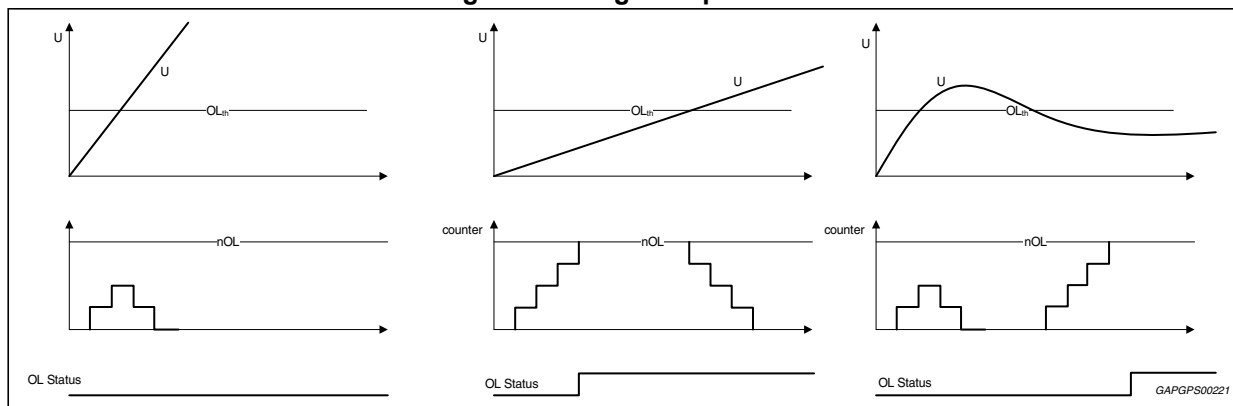


Figure 27. Diagram openload



### 4.8.2 Openload

Openload detection is done in the off-state through a multiplexed pull-down resistor,  $R_{PD}$  (see [Figure 4](#)).  $R_{PD}$  is multiplexed onto each output node sequentially at a fixed 125kHz rate. The output voltage is measured while  $R_{PD}$  is connected to the output. Voltages below  $V_{OL}$  ([Table 15](#)) indicate an off-state Open load condition. Multiplexing  $R_{PD}$  reduces the overall “leakage” current while providing a substantial pull-down current to verify open load status. There is a counter that “debounces” the open load detection similar to the undercurrent filter counter. Open load is reported in the SPI status registers (bit D0 of registers 1 - 4, [5.2.2: Output status Q1... Q4 \(address 1 to 4\)](#)) and is cleared once read.

### 4.8.3 Overload

If the measured load current is higher than the overcurrent threshold ( $I_{OCx}$ , [Table 15](#)) a failure is detected. The overcurrent detection is measured in on state only. This failure is filtered for  $t_{OL}$  (20 $\mu$ s typ., [Table 18](#)). After  $t_{OL}$  the output is shut down immediately and all of the set point and control variables are set to zero. This disables the output from further actuation until the appropriate status registers are read and cleared (refer to [5.2.2](#)). Once the appropriate SPI status registers are read the offending output(s) are released to be driven again. This failure detection is used for all outputs.

The overcurrent bit is latched upon an overcurrent detection and reset after reading the corresponding SPI register.

Outputs Q1 and Q2 have a selectable overcurrent threshold. These currents are individually selectable as well. (see [Table 15](#) also [5.1.8: Configuration register 2 - current control / over-voltage threshold \(address 14\)](#))

This failure detection is also used during SVDT (see [4.8.13: Silent valve driver test \(SVDT\)](#)).

#### 4.8.4 Thermal warning and thermal shutdown

The L9374LF is equipped with a two stage thermal protection system. This system provides for an early thermal warning and a thermal overload shutdown protection. With thermal warning some countermeasures can be realized by the Master  $\mu\text{C}$  to potentially prevent thermal shutdown. The temperature for each output is only measured when the output is on.

Temperature warning has the same functionality as over-temperature. The only differences are:

- The threshold is 20°C below over-temperature.
- The Output is not shut down.
- The SPI-Bit shows the actual status at the time it is accessed.

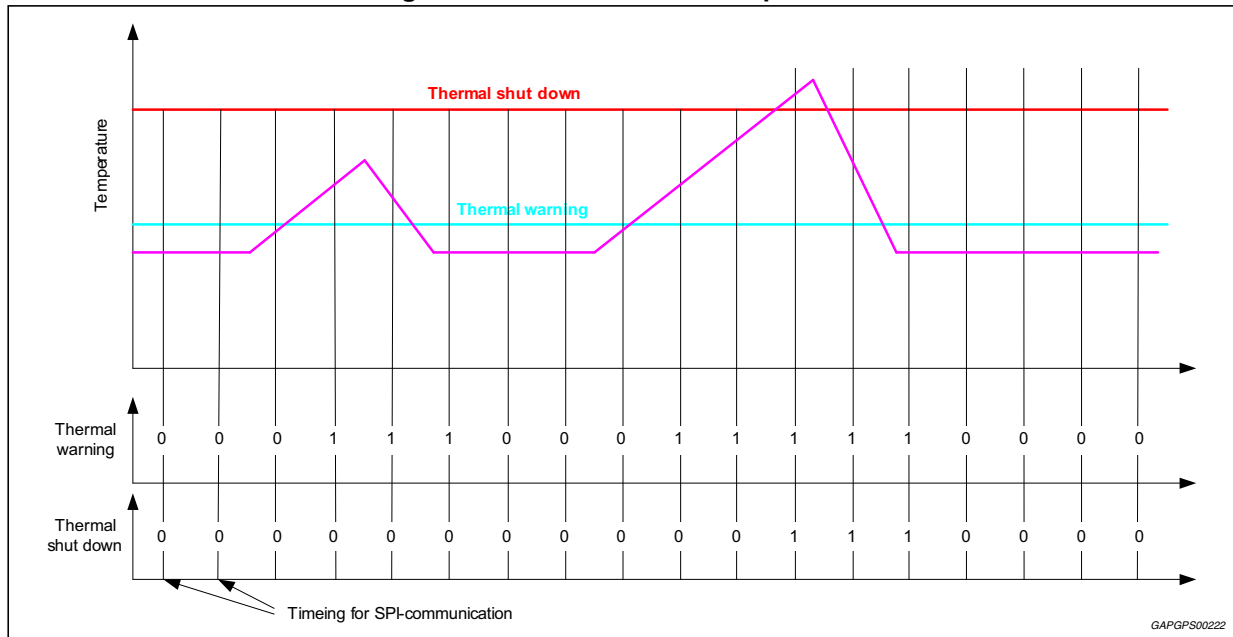
##### Thermal warning

If the measured value is higher than the thermal warning threshold,  $T_W$  ([Table 15](#)), for  $t_{TW}$  ([Table 18](#)) the appropriate thermal warning bit for that output is set in the SPI Status register (bit D8 of status registers 1 - 4, [Section 5.2.2](#)). No other action is taken. Reading the status registers clears the  $T_W$  bit(s) once the device is cooled sufficiently. This failure detection is used for all outputs.

##### Thermal shutdown

When the measured temperature exceeds the thermal shutdown threshold,  $T_{SD}$ , a failure is detected. This failure detection is filtered for  $t_{OT}$  (40  $\mu\text{s}$  typ., [Table 18](#)). After  $t_{OT}$  the output is shut down immediately and all of the set point and control variables are set to zero. This disables the output from further actuation until the over temperature condition is removed and appropriate status register(s) (status registers 1 - 4, [Section 5.2.2](#)) are read. Reading the status registers clears the  $T_{SD}$  bits once the device is cooled sufficiently. This failure detection is used for all outputs.

Figure 28. Thermal detection / protection behavior.



#### 4.8.5 Power ground loss (PGND-loss)

PGND-loss continuously monitors the voltage between SGND and PGNDxy. If the measured value is higher than  $V_{PG\_L}$  (Table 16) for longer than  $t_{PGND\_L}$  (Table 18) a failure is detected. This sets the PGNDL\_Qx bit (Section 5.2.2) and sets all of the set point and control variables to zero disabling the output. There is a power ground loss bit for each output even though Output 1 shares power ground with Output 2 and Output 3 shares power ground with Output 4. It is not possible to switch on the output as long as the failure is detected.

Once the power ground loss condition is removed the outputs are re-enabled by reading the appropriate status register (SPI Status register 1 - 4). This clears the failure bit in the status register and re-enables the output for use. This failure detection is used for all outputs.

The status of the failure is shown via SPI. PGND-loss is latched and can be reset only by accessing this register when the failure does not exist anymore.

#### 4.8.6 Signal ground loss (SGND-loss)

The SGND-loss monitors the voltage between SGND and PGNDxy. If the measured value is higher than  $V_{SG\_L}$  (Table 16) for  $t_{SGND\_L}$  (Table 18) a failure is detected. After this time ALL outputs are switched off immediately and the driver is shut down. The SPI communication is possible but there is a threshold shift at the logic output drivers due to an additional substrate diode in the ground path between PGNDxy and SGND (see Section 5.2.1).

#### 4.8.7 Freewheeling diode loss detection (Dx-loss)

Freewheeling diode loss is detected by measuring the current through the output clamping structure. If the clamping structure is used for more than  $t_{DX\_L}$  (Table 18) a Dx\_Loss is detected and the appropriate Status register bit (bit D5 of status registers 1 - 4, Section 5.2.2) is latched on. This bit can only be cleared once the failure is removed and the status register is read.

### 4.8.8 SPI-failure

There are 3 possible SPI-failures:

- parity failure (PARITY\_F)
- clock failure (SPICLK\_F)
- data failure (DATA\_F)

In case of any SPI-Failure the next transmission to the master contains the following data:

MSB														LSB	
received address				1	1	1	1	1	1	1	1	1	1	1	Parity
A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

#### Parity failure:

A parity failure is detected if the total number of '1's in the message is not odd. The PARITY\_F bit of status register 0 is set and master message is ignored (no change of the data). The corresponding status message returned to the master after a parity failure contains the received address and only '1's for the data bits. The PARITY\_F bit can be cleared by accessing address 0.

#### SPI clock failure:

The L9375 counts the number of SPICLK positive edges during SPICS actuations (SPICS='0'). If this number is unequal to 16 an error is detected and the message is not used (no change of the data) and the SPICLK\_F bit in the status address 0 is set. The corresponding status message returned to the master after a Clock failure contains the received address and only '1's for the data bits. The SPICLK\_F bit can be cleared by accessing address 0.

#### Data failure:

A SPI command with data content that is not allowed produces a data failure (DATA\_F).

The Data\_F bit in the SPI status register 0 is set if the master writes invalid data to the config-registers (address 2, 14 and 15). When this failure occurs all data in these addresses are not modified (no change in the content at these registers). The Data\_F bit can be cleared by accessing address 0.

### 4.8.9 CLKIN-failure

CLKIN-failure (CLKIN\_F) is detected if the input frequency ([Table 17](#)) at the CLKIN pin is out of the specified range for  $t_{CLK\_F}$  ([Table 18](#)). Once this failure is detected all outputs are switched off immediately, all set points, control variables, and counters are reset to zero and the sync\_counter is set to one. This frequency is monitored by an internal oscillator. This oscillator used to clock all internal nodes otherwise driven by CLKIN.

All failures which occur due to a CLKIN-failure are not reflected in any SPI-register. Only a sync failure will be reflected. Failures which occurred prior to a CLKIN failure are not deleted or overwritten.

The CLKIN\_F bit can be cleared by accessing address 0 once the failure is removed.

#### 4.8.10 Sync-failure

Sync failure detects a timing error in the output command synchronization. The master  $\mu\text{C}$  programs a timing window (STW, [Section 4.3](#)) where accessing to status address 0 is not allowed. If there is an access to Status address 0 when the STW flag is set then a sync-failure is generated (SYNC\_F = 1). Also, a SYNC\_F will be detected if there is no SPI traffic at all between two SYNC\_SIG events. This status will be read out on the subsequent SPI transfer.

Without a SYNC\_SIG or at sync-failure there is no effect for the actuation and setpoints

A sync-failure detection results in two consecutive error flags (SYNC\_F = 1).

To re-synchronize the L9374LF a SYNC\_TRIG signal must be sent.

#### 4.8.11 Current not reachable failure (Q3 & Q4)

The Current Not Reachable failure is detected when the current controller control variable is set to 1FF<sub>(Hex)</sub> or the current measurement sign\_bit is set ('1') for more than  $t_{\text{CURR\_F}}$  (8ms typ). Once a CNR is detected the CNRx bit for that output is set to '1' and the ISAT value is reset (see sections, [4.5.4](#), [4.6.1](#) and, [5.2.1](#)).

The Current Not Reachable detection is used for outputs Q3 and Q4 only.

**Table 36. Fault diagnostic summary**

Failure	Output state	Effect	Reset behavior
<b>Openload</b>	off	– bit is set (latched)	Access SPI-register
<b>Undercurrent</b>	on	– bit is set (filtered) see <a href="#">Section 4.8.1: Undercurrent / openload</a>	Access SPI-register
<b>Overload</b>	on	– bit is set (latched) – output is switched off – all set points / current / duty cycle / durations are kept at zero	Access SPI-register
<b>Over temperature</b>	on	– bit is set (latched) – output is switched off – all set points / current / duty cycle / durations are kept at zero	Access SPI-register
<b>PGND-loss</b>	on + off	– bit is set (latched) – output is switched off – all set points / current / duty cycle / durations are kept at zero	Access SPI-register
<b>SGND-loss</b>	on + off	– No constraints at all functions – SPI-communication has to be possible – The SPI-bit SGND_L is set after the filter time ( $t_{\text{SGND\_filt}}$ ) – All channels are switched off after $t_{\text{SGND\_filt}}$ and all current setpoints are deleted – The sync-parameters are not cleared; sync-counter is not reset	Access SPI-register
<b>Dx-loss</b>	on	– bit is set (latched)	Access SPI-register

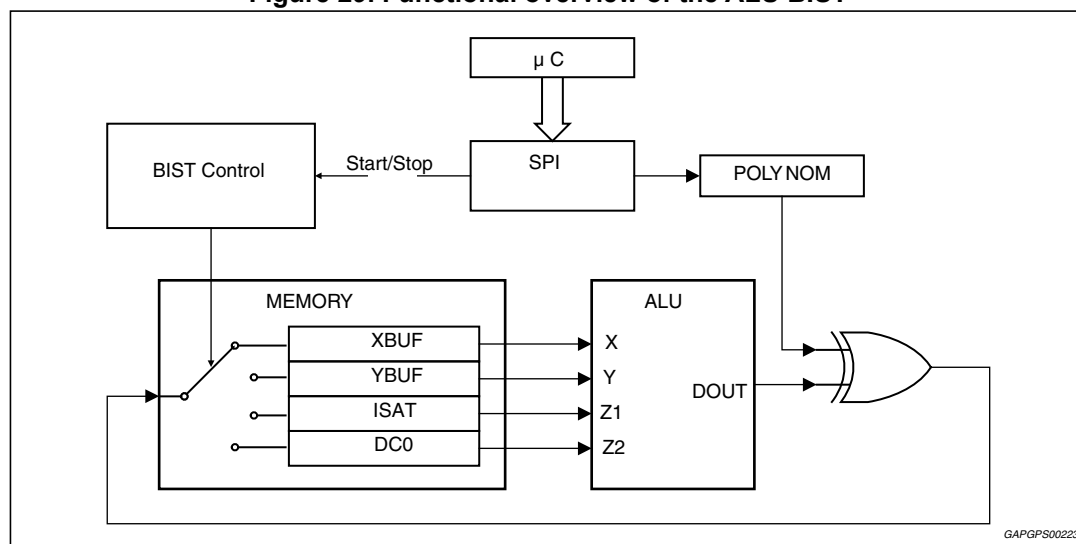
Table 36. Fault diagnostic summary (continued)

Failure	Output state	Effect	Reset behavior
<b>SPI: Parity failure</b> odd	on + off	<ul style="list-style-type: none"> <li>– bit is set (latched)</li> <li>– data are not used</li> </ul>	Access SPI-register
<b>SPI: SPICLK-failure</b> n <> 16	on + off	<ul style="list-style-type: none"> <li>– bit is set (latched)</li> <li>– data are not used</li> </ul>	Access SPI-register
<b>SPI: Data-failure</b>	on + off	<ul style="list-style-type: none"> <li>– bit is set (latched)</li> <li>– data are not used (within a register)</li> </ul>	Access SPI-register
<b>CLKIN-failure</b>	on + off	<ul style="list-style-type: none"> <li>– bit is set (latched)</li> <li>– all outputs switched off immediately</li> <li>– all set points / current / duty cycle / durations are kept at zero</li> <li>– all counters are kept at zero</li> <li>– all synchronization values are kept at zero (reset, sync, STW)</li> <li>– there is no influence at all status register</li> </ul>	Access SPI-register
<b>Sync-failure</b> STW_V_MIN < X < STW_V_MAX	on + off	<ul style="list-style-type: none"> <li>– bit is set (latched)</li> </ul>	Access SPI-register
<b>Under voltage @ VS</b>	on + off	<ul style="list-style-type: none"> <li>– all outputs switched off immediately</li> <li>– all set points / current / duty cycle /durations are kept zero</li> <li>– all counters are kept at zero</li> <li>– all synchronization values are kept at zero (reset, sync, STW)</li> <li>– all status register are kept at zero</li> <li>– all input, outputs and data buffer are kept at default</li> </ul>	-

### 4.8.12 ALU- BIST (Build in self test)

The ALU BIST is based on a Cyclic Redundancy Check (CRC) value calculation. For this reason it is possible to bring the sequencer, which controls the calculation of the current regulation ALU, into a special BIST mode. This mode is programmable via SPI using a special sequence of commands. The BIST is enabled when the fast switch off (FSOFF\_ALL = '10') command is given. The BIST then starts when the Res\_CCV command (Res\_CCV = '01') along with a characteristic polynomial is programmed via SPI into register 15 (see [Section 5.1.9](#)). The BIST is autonomous, once it is started, it cannot be interrupted. The internal registers are used to provide values to the ALU during the BIST. These registers will be reset at the start of the BIST. After the BIST has finished the BIST busy bit (status address 5, bit D9) is reset and the CRC checksum is available. The checksum can be read out via SPI from the ISAT\_Q3 register (status address 8, bits D0 - D9, [Section 5.2.5](#)). The BIST mode can then be exited when the fast switch off all command is reversed (FSOFF\_ALL = '01'). The used registers will be cleared to their power-on reset state when the L9374LF exits BIST mode.

Figure 29. Functional overview of the ALU BIST



To achieve test coverage higher than 97% with the BIST the following 4 polynomial values are recommended.

1. 194d (1100 0010)
2. 225d (1110 0001)
3. 212d (1101 0100)
4. 245d (1111 0101)

#### Sequence to perform the ALU built in self test during application:

1. Initiate the BIST sequencer; SPI command address: 2, FSOFF\_ALL = 10).  
Note: The sequencer is then waiting for the programming of the characteristic polynomial to start the BIST.
2. Program the characteristic polynomial (SPI command address 15 RL= xxxxxxxx) while setting Res\_CCV (= '01'). While the BIST is running BIST busy bit (BIST\_BUSY Status address 5, bit D9) is set to '1'.  
Note: Programming address 15 starts the BIST sequence. At the beginning of the



sequence the internal registers are reset. It's not possible to interrupt the BIST. When the BIST is completed, the BIST busy bit is reset to '0' and the checksum is available to be read.

The BIST\_BUSY bit reflects the actual status of the sequencer. 1: BIST is running or has been run previously and no current regulation is possible.

3. Readout the BIST checksum value located in status address 8, bits D0 - D9).
4. Repeat steps 2 and 3 until all of the polynomials have been run through the sequencer.
5. To exit the BIST mode write FSOFF\_ALL = '01' (command address 2, bits D4 & D5). At this point you must re-program a new RL value (SPI command address 15, RL = xxxxxxxx).

Note: Once leaving the BIST mode the internal registers are set to default values. After exiting the BIST mode and providing a new RL value the sequencer is ready to learn a new current regulation.

It is possible to program new current regulator set values in the same SPI access loop (Address. 0 to 15) where the BIST is stopped and a new RL value is written.

Affected internal registers from BIST:

<b>XBuf</b>	Register for intermediate results
<b>YBuf</b>	Register for intermediate results
<b>DC0</b>	Register for intermediate result of DC
<b>ISAT_Q3</b>	Integration register for Channel 3

The contents of these register are reset at the initiation and completion of the BIST.

Just using the fast switch off command alone (FSOFF\_ALL='10) does not initiate a BIST. This action will only initiate the sequencer into the BIST ready state. The BIST will not be started until programming a polynomial via SPI into address 15 is completed. Until that point the internal registers will not be reset. It is possible to leave the BIST ready state with by reversing the fast switch off command (Command address 2, FSOFF\_ALL = '01'). The sequencer is then ready for new current regulation commands.



Table 38. SVDT command

SVDT command (Address 2)	Bit 1	Bit 0
Not Possible	0	0
Normal Operation / No test	0	1
SVDT Active (in test mode)	1	0
Not Possible	1	1

When the SVDT has completed testing all of the outputs, the SVDT bits are reset '01' and the test is halted. To restart the test the SVDT bits must be rewritten as '10'. All of the results are stored within the SPI output status registers (SPI addresses 1 - 4, section 5.2.2). Accessing the output status registers after the SVDT is completed clears these registers. It is important to note that reading these addresses during an SVDT test also clears the status bits.

The SVDT sequence begins at the next SYNC\_SIG after initiating the SVDT command. It is important to disable edge shaping (Command Address 2, bits D8 & D7 = '10', section 5.1.3) during the SVDT test for accurate results. This can be done in the same command.

The SVDT will run in a loop until completed even if the programmed sync register cycle time (RESET\_VALUE) is shorter than the SVDT actuation time.

Figure 31. Timing between each output test

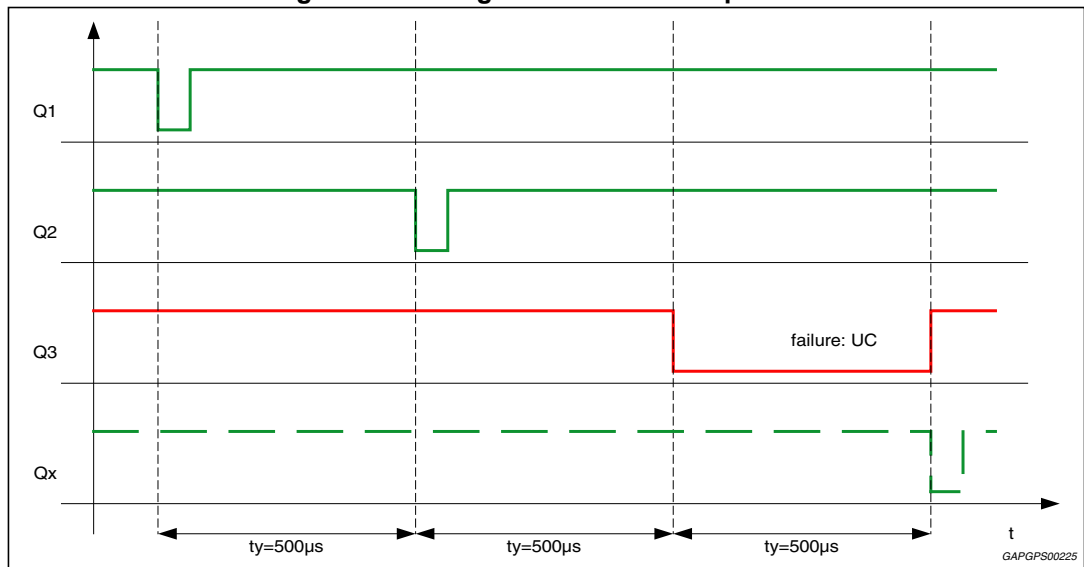
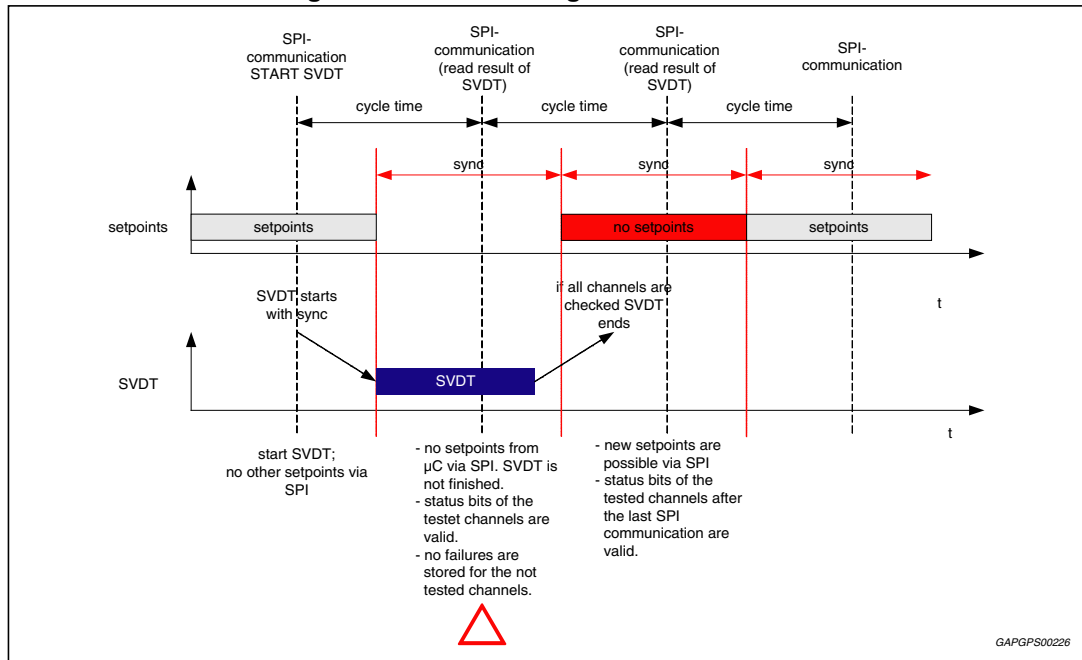


Figure 32. SVDT-Timing with SPI-transfer:



### SVDT test sequence

1. Disable Edge Shaping (Command address 2, bits D8 & D7 = '10')
2. Initiate SVDT (Command address 2; bits D1 & D0 = '10')
3. Qx switches on at the next sync-signal (sequence of actuation: Q1..Q4)
4. Because the output is actuated the output current increases.
5. At time  $t_x$ , if the output current has exceeded the under current value,  $I_{UC}$ , the output is switched off.
6. If the over current threshold ( $I_{OC}$ ) is achieved prior to  $t_x$  then the output is immediately disabled and an over current condition is detected.
7. The output will switch off any time prior to exceeding time,  $t_y$ , if the undercurrent threshold,  $I_{UC}$ , has been met.
8. After the output is disabled if the output clamps the voltage to  $V_Z$  (35V) a  $Dx\_Loss$  is detected.
9. If an Over temperature is not detected then the SDVT test is passed
10. The SVDT will then test at  $Q_{x+1}$  until all 4 outputs have been tested.

Criterion for passing:

- no overcurrent
- Current value increases and reached undercurrent value within time  $t_y$  ( $I_{Qx} > I_{UC}$ ) & ( $t_x < t_y$ ).
- Channels with a freewheeling diode does not have a clamping thus do not report a  $Dx\_Loss$  condition

SPI:

- no failure at all Output status registers (Status Addresses 1 - 4).
- $Qx\_ON = 1$

Figure 33. Passing test diagram

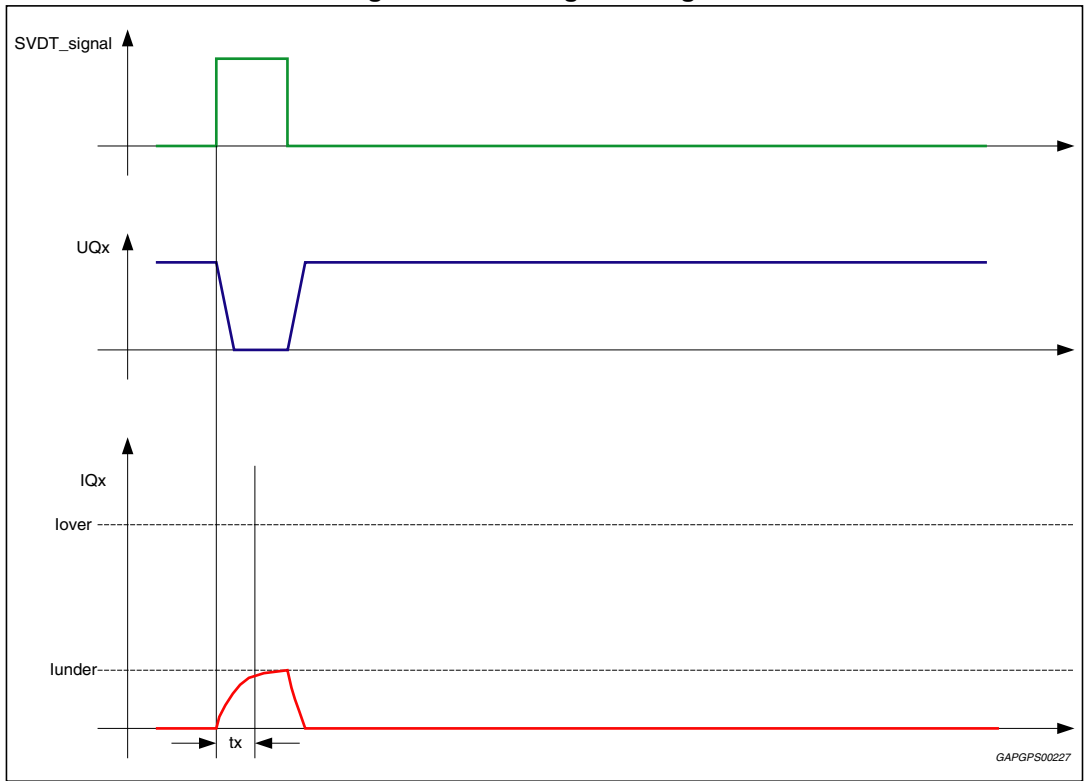
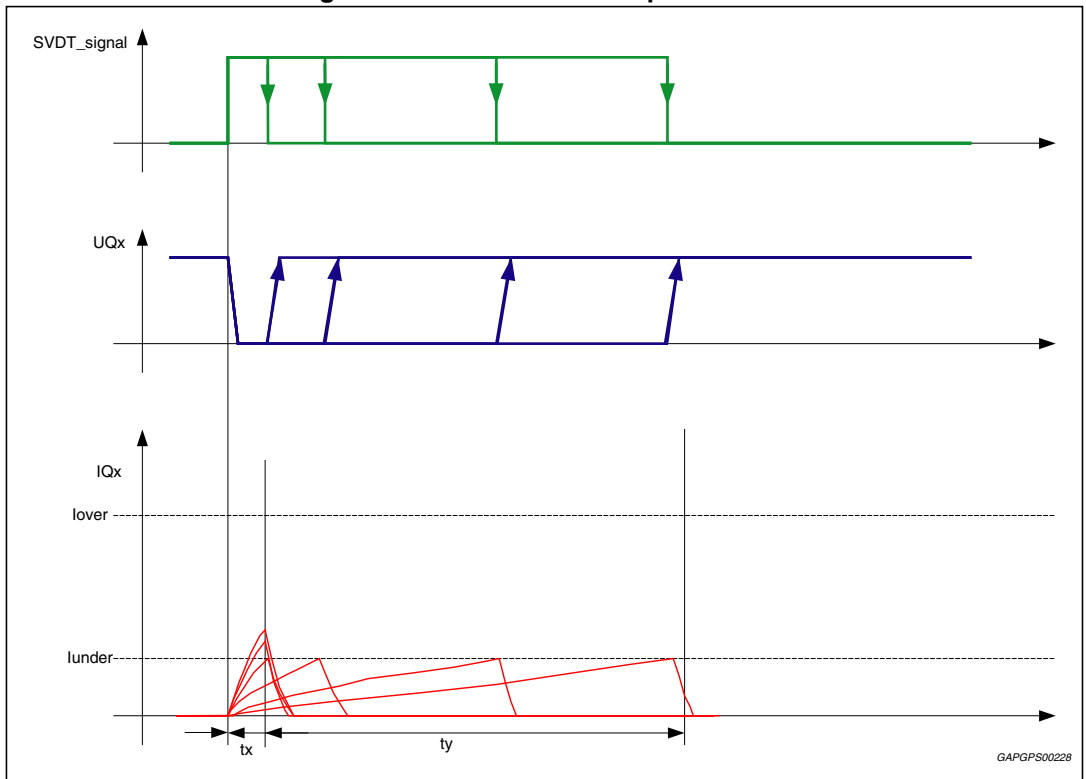
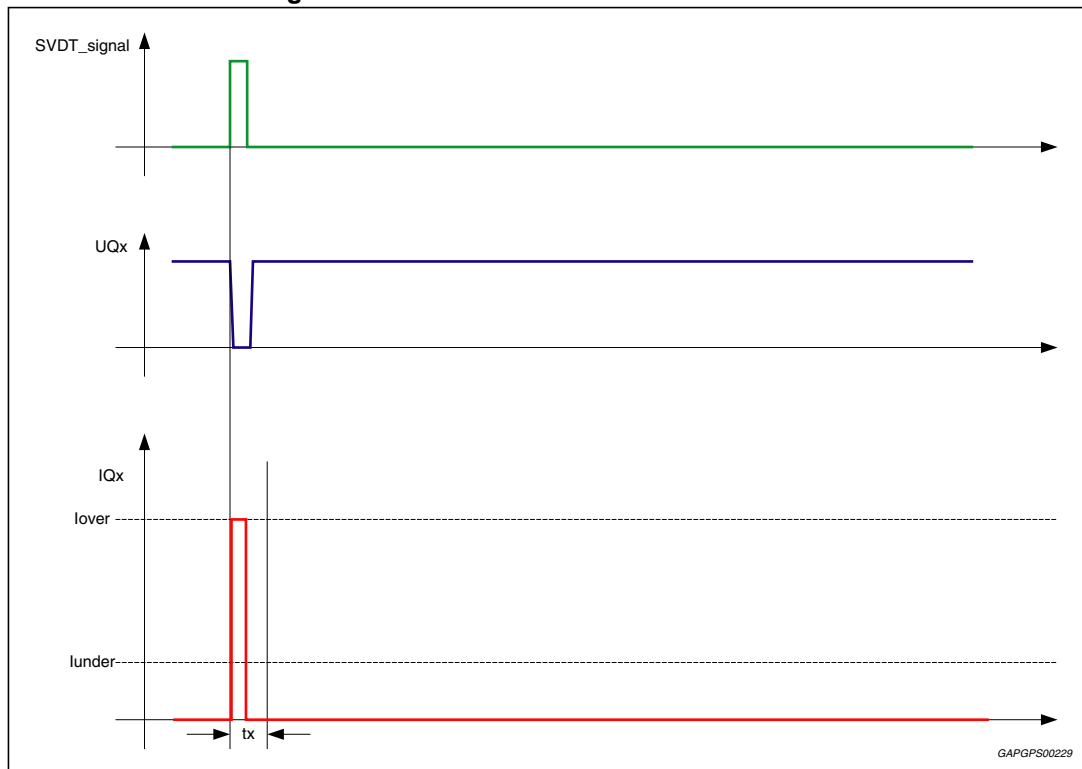


Figure 34. Possibilities of a passed test



## The SVDT test examples

Figure 35. Test failed: short circuit / overload

**A failed test sequence for overload condition:**

1. Disable Edge Shaping (Command address 2, bits D8 & D7 = '10')
2. Initiate SVDT (Command address 2; bits D1 & D0 = '10')
3. Qx switches on at the next sync-signal (sequence of actuation: Q1..Q4)
4. The output current increases and reached  $I_{OL}$  before tx is reached
5. Output Qx is switched off for overload protection and the overload bit (bit D0 of the status registers D1 - D4).
6. After the output is disabled if the output clamps the voltage to  $V_Z$  (35V) a  $Dx\_Loss$  is detected.
7. If an Over temperature is not detected then the SDVT test is passed
8. The SVDT will then test at Qx+1 until all 4 outputs have been tested.

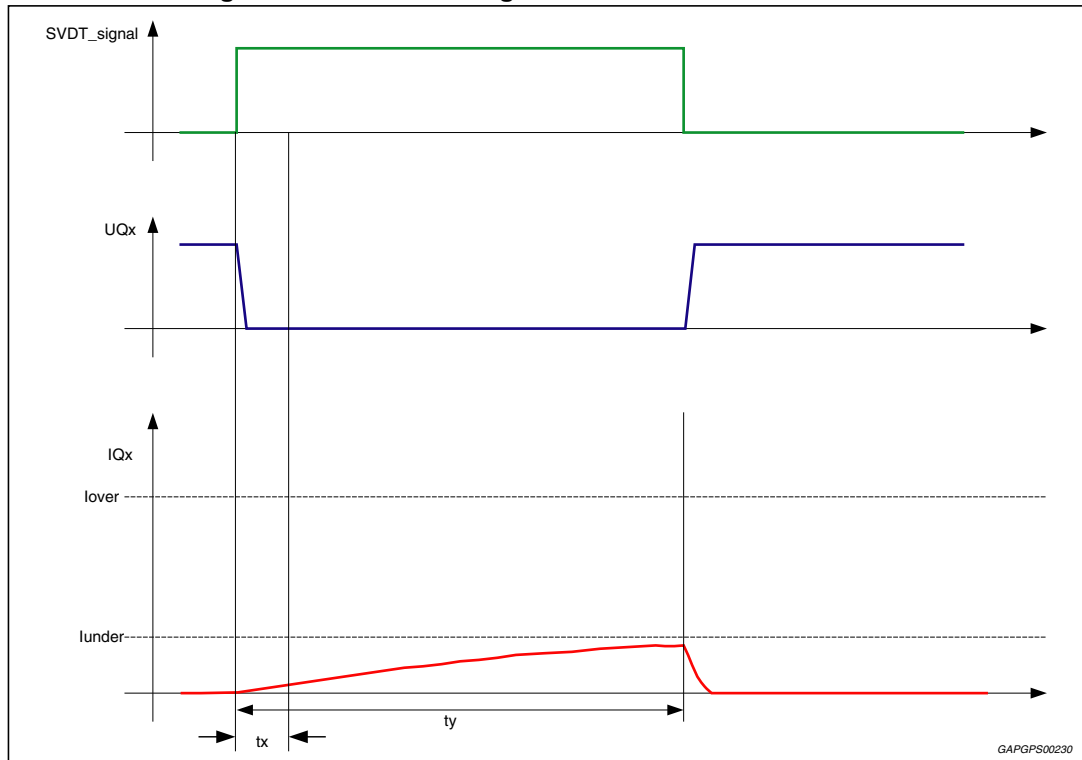
## Criterion:

- The output current increases and reaches overcurrent value within the test time tx

## SPI:

- Status registers 1 - 4, OL\_Qx bit is set.

Figure 36. Test failed: high resistive load / undercurrent



#### A failed test sequence for under current condition

The test sequence:

1. Disable Edge Shaping (Command address 2, bits D8 & D7 = '10')
2. Initiate SVDT (Command address 2; bits D1 & D0 = '10')
3. Qx switches on at the next sync-signal (sequence of actuation: Q1..Q4)
4. The output current increases but does not reach the undercurrent value,  $I_{UC}$ .
5. After  $t_y$  the output is switched off.
6. After the output is disabled if the output clamps the voltage to  $V_Z$  (35V) a  $Dx\_Loss$  is detected.
7. If an Over temperature is not detected then the SDVT test is passed
8. The SVDT will then test at  $Q_{x+1}$  until all 4 outputs have been tested.

Criterion:

- the current value does not reach the undercurrent value within time  $t_y$

SPI:

- Status registers 1 - 4, UC\_Qx bit is set.

Table 39. SVDT status

<b>Dx_loss</b>	<b>Overcurrent OC_Qx</b>	<b>Under Current UC_Qx</b>	<b>Description</b>
0	0	0	Test is passed
0	0	1	High resistive load or high inductive load
0	1	0	Overcurrent: short circuit to supply voltage or short circuit of the load
0	1	1	Not possible
1	0	0	Dx-loss
1	0	1	Dx-loss+ high resistive load or high inductive load
1	1	0	Dx-loss + short circuit to supply voltage or short circuit of the load
1	1	1	Not possible



## 5 Programmers guide

This programmers guide is a reference section intended to aid in the L9374LF interface software development. The L9374LF uses SPI messaging for all of its communication into or out of the device. The Command registers are written to and the Status registers are read.

### 5.1 Command registers

The Command Registers are registers written to by the MASTER  $\mu$ C to actuate the L9374LFs various functions. Each command consists of an address, data, and a parity bit (refer to [Chapter 4.1: SPI serial peripheral interface](#) for more details).

#### 5.1.1 Sync + Sync-trigger register (address 0)

MSB														LSB	
0	0	0	0	SYNC_TRIG	RESET_VALUE				SYNC_VALUE						Parity
A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 40. Sync + Sync-trigger register**

Sync + sync-trigger	Name	Bit Location	Number of bits	bit time
Synchronization value	SYNC_VALUE	D0-D5	6	250 $\mu$ s
Reset value (highest 4 Bits)	RESET_VALUE	D6-D9	4	1 ms
Sync-trigger	SYNC_TRIG	D10	1	-

For this section see [Chapter 4.3: Synchronization controller](#) for more details

#### Synchronization value:

This 6-bit-value represents a time value. At this time the new set points are processed.  
Resolution of LSB: 250  $\mu$ s

#### Reset value:

With this value the time base of the synchronization can be modified.  
Resolution of LSB: 1 ms

The MSB of the RESET\_VALUE (D9) affects the bit times for the Sync Trigger Window, the Duration x, and the Duration y parameters.

#### Sync-trigger:

The synchronization is re-triggered by setting this bit to '1'. After a re-synchronization the internal logic will clear this bit automatically.

If the SVDT is active and still running, it will be interrupted by setting the SYNC\_TRIG bit (See also [Chapter 4.3](#) section on [Synchronization controller programming](#)).

### 5.1.2 Sync tolerance window (STW) register (address 1)

MSB															LSB
0	0	0	1	0	STW_V_MAX					STW_V_MIN					Parity
A3	A2	A1	A0	free	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

**STW value:**

These two sets of 5 bits each define a window (between min and max) where accessing address '0' within this window will cause a sync failure indication (SYNC\_F).

To keep the resolution meaningful for the entire range of Sync Triggering the resolution is dependant on the RESET\_VALUE MSB. For programming the two values to the STW the master has to write both values (2 x 5 bit).

**Table 41. STW value**

STW value	Name	Bit location	Number of bits	bit time RESET_VALUE ≤ 0111 <sub>(2)</sub>	bit time RESET_VALUE ≥ 1000 <sub>(2)</sub>
STW value min.	STW_V_MIN	D0 - D4	5	250 μs	500 μs
STW value max.	STW_V_MAX	D5 - D9	5	250 μs	500 μs

For this section see [Chapter 4.3: Synchronization controller](#) for more details

### 5.1.3 Configuration register 1 (address 2)

MSB															LSB
0	0	1	0	x	x	EDGE_SH		FSON_EN	FSOFF_ALL		CLKIN_S	SVDT		Parity	
A3	A2	A1	A0	free	free	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 42. Configuration register 1**

Config register	Name	Bit location	Number of bits
Silent valve driver test	SVDT	D0 - D1	2 Bit
CLKIN frequency 1MHz / 250kHz	CLKIN_S	D2 - D3	2 Bit
Fast switch off all	FSOFF_ALL	D4 - D5	2 Bit
Fast switch on enable (general)	FSON_EN	D6	1 Bit
Edge shaping on / off	EDGE_SH	D7 - D8	2 Bit

**Silent valve driver test (SVDT):**

These two bits (D0 & D1) are normally set to '01'. Writing '10' to these two bits starts the silent valve driver test.

(for more details see [Chapter 4.8.13: Silent valve driver test \(SVDT\)](#))

**Table 43. Silent valve driver test (SVDT)**

Bit 1	Bit 0	Combination
0	0	Not valid
0	1	Normal condition / no test
1	0	Active
1	1	Not valid

Writing not valid bit combinations generates a SPI-data-failure and causes that specific SPI command to be ignored and subsequent returning Status Register data to be set to all '1's.

**CLKIN input frequency 1MHz / 250kHz (CLKIN\_S):**

These two bits set the ratio between internal and external clock (See [Chapter 4.2: Clock](#)).

**Table 44. CLKIN\_S**

Bit 1	Bit 0	Combination
0	0	Not valid
0	1	250 kHz
1	0	1 MHz
1	1	Not valid

Writing not valid bit combinations generates a SPI-data-failure and causes that specific SPI command to be ignored and subsequent returning Status Register data to be set to all '1's.

**Fast switch off (FSOFF\_ALL):**

These two bits (D4 & D5) are normally set to '01'. With these two bits set to '10' all outputs are switched off immediately (without regard to the synchronization). When set to active these bits clear the fast switch on enable (FSON\_EN) bit at address 3 and all set points. It is not possible to activate any output with status FSOFF\_ALL = '10' (active). This bit pattern is also used to initiate the ALU built in self test, or BIST, (for more details on the Built In Self Test see [Chapter 4.8.12: ALU- BIST \(Build in self test\)](#)).

**Table 45. Fast switch off**

Bit 1	Bit 0	Combination
0	0	Not Valid
0	1	Normal condition
1	0	Active → all outputs are off
1	1	Not Valid

Writing Not Valid bit combinations generates a SPI-data-failure and causes that specific SPI command to be ignored and subsequent returning Status Register data to be set to all '1's.

**Fast switch on enable (FSON\_EN):**

This bit (D6) is normally set to '0'. Setting this bit ('1') enables the SPI ability to drive outputs directly. With this bit set, writing to address 3 (bits D0 -D3) turns on or off outputs Q1 - Q4. All of the bits in Command Register 3 are reset when FSON\_EN is reset ('0').

### Edge shaping (EDGE\_SH)

Edge Shaping option allows the user to incorporate a slower more EMI sensitive slope to the output waveform. By setting these bits the user is able to turn on / off edge shaping for all outputs (see [Section 3.3.4: Output timing characteristics](#)). There is no option to select individual outputs for edge shaping. When performing the SVDT it is recommended that Edge Shaping be turned OFF.

**Table 46. Edge shaping**

Bit 1	Bit 0	Combination
0	0	Not Valid
0	1	Edge Shaping <b>ON</b> for all outputs
1	0	Edge Shaping <b>OFF</b> for all outputs
1	1	Not Valid

Writing Not Valid bit combinations generates a SPI-data-failure and causes that specific SPI command to be ignored and subsequent returning Status Register data to be set to all '1's.

### 5.1.4 Fast switch-on (FSON) register (address 3)

MSB											LSB				
0	0	1	1	x	x	x	x	x	x	x	ON <sub>4</sub>	ON <sub>3</sub>	ON <sub>2</sub>	ON <sub>1</sub>	Parity
A3	A2	A1	A0	free	free	free	free	free	free	free	D3	D2	D1	D0	P

**Table 47. Fast switch-on**

Configuration register	Bit Location	Name
Switch on Q1	D0	ON <sub>1</sub>
Switch on Q2	D1	ON <sub>2</sub>
Switch on Q3	D2	ON <sub>3</sub>
Switch on Q4	D3	ON <sub>4</sub>

If the fast switch on enable bit (FSON\_EN) is set, writing 1 to the bit ON<sub>x</sub> switches the output on 100%. A '0' written to the fast switch on enable pin will disable this function. Any outputs on as a result of an ON<sub>x</sub> bit being high will be turned off.

The fast switch off all bits (FSOFF\_ALL) turn off all channels immediately (it does not depend on the synchronization) and clear all bits at this address. The fast switch off all (FSOFF\_ALL) command has the highest priority.

### 5.1.5 Duration registers (address 4 and 5)

MSB															LSB
0	1	0	0	x	D_Q2					D_Q1					Parity
0	1	0	1	x	D_Q4					D_Q3					Parity
A3	A2	A1	A0	free	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

The output can be driven in two stages by one SPI transfer, a duty cycle for a duration and then a second duty cycle. These registers provide the initial duration information. Two duration values are available in each register.

**Table 48. Register duration value**

Register address	Duration parameter	Number of bits	Bit location	Output
4	D_Q1	5 Bit	D4 - D0	Q1
4	D_Q2	5 Bit	D9 - D5	Q2
5	D_Q3	5 Bit	D4 - D0	Q3
5	D_Q4	5 Bit	D9 - D5	Q4

The duration bit resolution depends on the synchronization timer RESET\_VALUE MSB:

**Table 49. Duration bit resolution**

RESET_VALUE MSB (add.0, bit D9)	Resolution of duration
0	250 $\mu$ s
1	500 $\mu$ s

### 5.1.6 Duty cycle register (address 6 to 9)

MSB															LSB
0	1	1	0	x	x	DUTY1_Q1									Parity
0	1	1	1	x	x	DUTY2_Q1									Parity
1	0	0	0	x	x	DUTY1_Q2									Parity
1	0	0	1	x	x	DUTY2_Q2									Parity
A3	A2	A1	A0	free	free	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

The value of these registers represent the outputs Q1 and Q2 set point duty cycles. Address 6 and 8 provide the initial duty cycle used during the duration specified in the duration register (address 4). Addresses 7 and 9 provide the duty cycles used after the duration specified in address 4 has expired.

**Table 50. Duty cycle register (address 6 to 9)**

Register address	Duty cycle register	Number of bits	Bit location	Name
6	Output 1 Duty cycle 1	9	D0 - D8	DUTY1_Q1
7	Output 1 Duty cycle 2	9	D0 - D8	DUTY2_Q1
8	Output 2 Duty cycle 1	9	D0 - D8	DUTY1_Q2
9	Output 2 Duty cycle 2	9	D0 - D8	DUTY2_Q2

The resolution is 0.2% per LSB.

000<sub>(H)</sub> = 0% Duty Cycle

1F4<sub>(H)</sub> = 100% Duty cycle.

To achieve the full diagnostic capability do not use a duty cycle of less than 5%(or 19<sub>(H)</sub>).

### 5.1.7 Current / duty cycle registers (address 10 to 13)

MSB														LSB	
1	0	1	0	x	x	CURRENT/DUTY1_Q3									Parity
1	0	1	1	x	x	CURRENT/DUTY2_Q3									Parity
1	1	0	0	x	x	CURRENT/DUTY1_Q4									Parity
1	1	0	1	x	x	CURRENT/DUTY2_Q4									Parity
A3	A2	A1	A0	free	free	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

These registers provide a numerical value that is either translated as a current regulation set point or a duty cycle set point. This depends on the Current Control / PWM (CCPWM\_Qx) bits found in Register 14. Either or both outputs can be set as either a current controlled output or a fixed PWM output independently (for details see [Chapter 3.3.6: Q3 / Q4 \(current controller\)](#)).

**Table 51. Current / duty cycle registers**

Register address	Duty cycle register	Number of bits	Bit location	Name
10	Output 1 Current / Duty cycle 1	9	D0 - D8	CURRENT/DUTY1_Q1
11	Output 1 Current / Duty cycle 2	9	D0 - D8	CURRENT/DUTY2_Q1
12	Output 2 Current / Duty cycle 1	9	D0 - D8	CURRENT/DUTY1_Q2
13	Output 2 Current / Duty cycle 2	9	D0 - D8	CURRENT/DUTY2_Q2

Resolution of LSB: 3.522mA

000<sub>(H)</sub> = 0 Amps

1FF<sub>(H)</sub> = 1.8 Amps

### 5.1.8 Configuration register 2 - current control / over-voltage threshold (address 14)

MSB														LSB	
1	1	1	0	x	x	x	OV_TH_Q2		OV_TH_Q1		CCPWM_Q4		CCPWM_Q3		Parity
A3	A2	A1	A0	free	free	free	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 52. Configuration register 2 - current control / over-voltage threshold**

Configuration register	Number of bits	Bit location	Name
Current Controller / PWM Switch Q3	2 bit	D1 - D0	CCPWM_Q3
Current Controller / PWM Switch Q4	2 bit	D3 - D2	CCPWM_Q4
Overload threshold Q1	2 bit	D5 - D4	OV_TH_Q1
Overload threshold Q2	2 bit	D7 - D6	OV_TH_Q2

#### Current controller / PWM enable

These two bits control the PWM or current regulation algorithm for outputs Q3 and Q4. When disabled the output reverts to a PWM only configuration as in outputs Q1 and Q2.

**Table 53. Current controller off Q3 / Q4**

Bit 1	Bit 0	Combination
0	0	Not Valid
0	1	Current controller enabled (PWM Control Off)
1	0	PWM Control Only (Current Control Off)
1	1	Not Valid

Writing Not Valid bit combinations generates a SPI-data-failure and causes that specific SPI command word to be ignored and subsequent returning Status Register data to be set to all '1's.

#### Overload threshold Qx:

These two bits change the threshold of the overload diagnosis of channel Q1 and Q2. (See [Table 15](#) for values and [4.8.3: Overload](#) for a functional description)

**Table 54. Overload threshold Q1 / Q2**

Bit 1	Bit 0	Combination
0	0	Not Valid
0	1	Overload threshold 1
1	0	Overload threshold 2
1	1	Not Valid

Writing Not Valid bit combinations generates a SPI-data-failure and causes that specific SPI command word to be ignored and subsequent returning Status Register data to be set to all '1's.

### 5.1.9 Configuration register 3 (CCV reset and load resistance values) (address 15)

<b>MSB</b>															<b>LSB</b>
1	1	1	1	x	Res_CCV		RL_SPI								Parity
A3	A2	A1	A0	free	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 55. Configuration register 3**

Configuration register	Number of bits	Bit location	Name
Reset current controller values	2 bit	D9 - D8	Res_CCV
RL_SPI	8 bit	D7 - D0	RL_SPI

#### Reset current controller values command (Res\_CCV):

The Current Controller values are reset and the new RL\_SPI is used after the reset time. During the reset phase the current controller regulation variable  $I_{SAT}$  is set to zero and no current regulation is possible. When changing the RL\_SPI it is necessary to reset the current controller by giving this command

**Table 56. Reset current controller values command**

Bit 1	Bit 0	Combination
0	0	Not Valid
0	1	Reset
1	0	Normal Condition
1	1	Not Valid

Writing Not Valid bit combinations generates a SPI-data-failure and causes that specific SPI command word to be ignored and subsequent returning Status Register data to be set to all '1's.

#### RL\_SPI:

RL\_SPI is an 8 bit value representing the expected load resistance driven by the current controller outputs (Q3 and Q4). This value is used for both current controllers. The controller performance is best with RL\_SPI close to the real value of the load resistor.

**Table 57. Load resistor value**

D7	D6	D5	D4	D3	D2	D1	D0	SPI - Bit
8 Ω	4 Ω	2 Ω	1 Ω	1/2 Ω	1/4 Ω	1/8 Ω	1/16 Ω	RL_SPI



## 5.2 Status registers

### 5.2.1 General status (address 0)

MSB										LSB					
0	0	0	0	0	SGND_L	FSON_S	CLKIN_State		EN	CLKIN_F	SYNC_F	DATA_F	SPICLK-F	PARITY_F	Parity
A3	A2	A1	A0	free	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 58. Status registers**

General status	Number of bits	Bit location	Name
Parity-failure	1 Bit	D0	PARITY_F
SPI-Clock-failure	1 Bit	D1	SPICLK_F
Data-failure	1 Bit	D2	DATA_F
Sync-Failure	1 Bit	D3	SYNC_F
CLKIN-failure	1 Bit	D4	CLKIN_F
EN Status	1 Bit	D5	EN
1MHz / 250kHz Status	2 Bits	D7 - D6	CLKIN_S
Fast Switch On Enable Status	1 Bit	D8	FSON_S
SGND loss	1 Bit	D9	SGND_L

#### Parity-failure:

If a parity-failure occurs during any command write this bit is set. It is cleared by accessing address 0.

#### SPI-Clock-failure:

This bit is set by a clock-failure (number of positive edges of SPICLK within SPICS = low is unequal 16) and is cleared by accessing address 0.

#### Data-failure:

This bit is set if the master writes invalid data to the configuration-register (Data: SVDT, CLKIN\_S and FSOFF\_ALL / CCPWM\_Qx / OV\_THx, EDGE\_SH\_OFF). Reset of this bit is done by accessing address 0. If the master tries to write invalid data to one of the input registers its content will not be changed (invalid write access is ignored, SPI data failure is set).

#### Sync-failure:

This bit is set by a Sync-failure and is cleared when the failure does not exist anymore. (shows the actual status)

(see [Synchronization failure](#))

**CLKIN-failure:**

If the frequency of CLKIN-signal is not in a specified range a CLKIN-failure occurs (CLKIN\_F = 1). The specification range can be changed via SPI (CLKIN\_STATE). This bit (CLKIN\_F) can be cleared by accessing this address.

**Hardware EN status:**

The EN Status bit reflects the level of the Enable (EN) pin. If the value of the Enable pin was low since the last access to this register the status EN is low (low sensitive signal). This bit is cleared by accessing this address.

**1 MHz / 250 kHz status:**

These bits reflect the two CLKIN\_S bits from the Command register 2 (bits D3 and D2). This is done to verify that the L9374LF has received the CLKIN\_S command.

**Table 59. CLKIN\_S command**

Bit 1	Bit 0	Combination
0	0	Not possible
0	1	250 kHz
1	0	1 MHz
1	1	Not possible

**Fast switch on enable (FSON\_EN) status**

This bit shows the actual status of Fast switch on enable (FSON\_EN) bit found in Command register 2, bit D6.

**SGND loss:**

After sensing a signal ground loss for  $t_{SGND\_filt}$  the SPI-bit SGND\_L is set, all channels are switched off, and all current set points are reset. The sync-parameters and the sync\_counter are not cleared. With SGND-loss a SPI-communication is still possible by using PGND as a ground reference. When the loss of SGND no longer exists the SGND\_L bit is reset after an access to address 0 (refer to section 4.8.6: *Signal ground loss (SGND-loss)*).

**5.2.2 Output status Q1... Q4 (address 1 to 4)**

**Outputs Q1 and Q2 (addresses 1 and 2):**

MSB										LSB					
0	0	0	1	0	OV_TH1	TW_1	Q1_OFF	Q1_ON	DL_1	PGNDL_12	TSD_1	OVER_1	UC_1	OL_1	Parity
0	0	1	0	0	OV_TH2	TW_2	Q2_OFF	Q2_ON	DL_1	PGNDL_12	TSD_1	OVER_2	UC_2	OL_2	Parity
A3	A2	A1	A0	free	D9	free	D7	D6	D5	D4	D3	D2	D1	D0	P



**Outputs Q3 and Q4 (addresses 3 and 4):**

MSB															LSB
0	0	1	1	0	CCPWM_3	TW_3	Q3_OFF	Q3_ON	DL_3	PGNDL_34	TSD_3	OVER_3	UC_3	OL_3	Parity
0	1	0	0	0	CCPWM_4	TW_4	Q4_OFF	Q4_ON	DL_4	PGNDL_34	TSD_4	OVER_4	UC_4	OL_X4	Parity
A3	A2	A1	A0	free	D9	free	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 60. Output status Q1... Q4**

Channel status	Number of bits	Name
Openload	1 Bit	OL_x
Undercurrent	1 Bit	UC_x
Overload	1 Bit	OVER_x
Thermal Shutdown	1 Bit	TSD_x
PGND-lost	1 Bit	PGNDL_xy
Dx-lost	1 Bit	DL_x
Output ON	1 Bit	Qx_ON
Output OFF	1 Bit	Qx_OFF
Current / PWM controller Select	1 Bit	CCPWM_x
overload threshold	1 Bit	OV_THx
Thermal warning	1 Bit	TW_x

(see section 4.8: *Diagnostics* for details for mot of the parameters in this section)

**Open load:**

The open load bit is set if the voltage at output Qx in off-state is lower than the failure-threshold  $V_{OL}$  (*Table 15*). This bit is cleared by accessing this address (Refer to section 4.8.1 for more details).

**Undercurrent:**

The undercurrent bit shows the status of the undercurrent detection ( $I_{UC}$ , *Table 15*). This bit is cleared by accessing this address (Refer to section 4.8.1 for more details).

**Overload:**

When the current through output Qx in on-state is higher than the failure-threshold ( $I_{OL}$ , *Table 15*) the overload bit is set and all set point and control variables for the offending output are set to zero. This bit can be cleared by accessing this address (Refer to section 4.8.3 for more details).

**Thermal shutdown:**

thermal shutdown is detected if the temperature of the DMOS is above  $T_{SD}$ , (*Table 15*) for  $t_{OVL}$  (*Table 18*) (refer to section 4.8.4 for more details).

**PGND-loss:**

This bit is set by a power ground loss and is cleared by accessing this address (Refer to section 4.8.5 for more details)

**Loss of freewheeling diode (Dx-loss):**

This bit is set by loss of the freewheeling diode and is cleared by accessing this address (refer to section 4.8.7 for more details).

**Gate voltage on status (Qx\_ON):**

This bit shows the status of the output driver gate. A comparator monitors the voltage of the gate.

If there is any actuation of the output between two SPI transfers the cycle time this bit is set. The bit is cleared by accessing this address (Refer to section: [Gate monitoring](#) for more information).

**Gate voltage off status (Qx\_OFF):**

This bit shows the status of the output driver gate. A comparator monitors the voltage of the gate.

If the output is disabled between two SPI transfers the cycle time this bit is set. The bit is cleared by accessing this address (Refer to section: [Gate monitoring](#) for more information).

**Current / PWM controller select:**

This bit is set when the Current Controlled is disabled and the PWM Control is active (refer to: [Current controller / PWM enable](#) for details).

**Table 61. Current / PWM controller select**

CCPWM	Status current controller off
0	Current Controller Enabled
1	PWM Control Enabled (Current Control disabled)

**Overload threshold:**

This bit shows the overload threshold selected in Configuration register 2 (Command address E) actual status of the threshold of the overload diagnosis (refer to [Table 15.](#))

**Table 62. Overload threshold**

OV_TH	Status overload threshold	Typical overload threshold value
0	Overload threshold 1	7.5 A
1	Overload threshold 2	8.5 A

### 5.2.3 VD (address 5)

MSB															LSB
0	1	0	1	0	BIST_BUSY	VD									Parity
A3	A2	A1	A0	free	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 63. VD / BIST BUSY general status**

General status	Number of bits	Name
VD	9	VD
BIST BUSY	1	BIST_BUSY

#### VD:

The value supply voltage at the D13 pin is measured and stored in Status Address 5 (refer to section [3.3.12: VD measurement](#) for more details)

**Table 64. VD value**

SPI - Bit	D8	D7	D6	D5	D4	D3	D2	D1	D0
VD-value	16 V	8 V	4 V	2 V	1 V	1/2 V	1/4 V	1/8 V	1/16 V

#### BIST BUSY:

This bit shows the status of the BIST state machine (details see [Chapter 4.8.12](#))

**Table 65. BIST BUSY status**

BIST_BUSY flag	BIST status
0	BIST not running
1	BIST is running

### 5.2.4 Output duty (address 6 and 7)

MSB															LSB
0	1	1	0	0	CNR3	Out_duty_Q3									Parity
0	1	1	1	0	CNR4	Out_duty_Q4									Parity
A3	A2	A1	A0	free	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 66. Output duty**

Output status	Number of bits	Name
Output duty	9 Bit	Out_duty_Qx
Current Not Reachable	1 Bit	CNRx

**Output duty:**

This value shows the duty cycle commanded by the current controller (9 bit control variable) just prior to the time of the SPI transfer. The resolution of LSB is that of the PWM command register of 0.2%.

**Timing example:**

- Time base: 5 ms between SPI transfers
- Output-frequency: 4 kHz → 250 μs

The Out\_Duty\_Qx value shows the duty cycle at 4,75 ms.

The maximum value read is 1FF<sub>(H)</sub>. This occurs when the output current cannot reach the commanded value (refer to section 3.3.6: Q3 / Q4 (current controller) for more information).

**Current Not Reachable (CNRx):**

This bit is set if the control variable of the current at output Qx shows the maximum value (1FF<sub>(H)</sub>) for more than 8 ms (typ.). This bit can be cleared by accessing this address, when the failure does not exist anymore (refer to section 3.3.6: Q3 / Q4 (current controller) for more information).

**5.2.5 ISAT-Qx (address 8 + 9)**

MSB															LSB
1	0	0	0	0	ISAT_Q3										Parity
1	0	0	0	1	ISAT_Q4										Parity
A3	A2	A1	A0	free	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 67. ISAT\_Qx**

Channel status	Number of bits	Name
ISAT_Qx	10 Bit	ISAT_Qx

**ISAT\_Qx:**

ISAT\_Qx is an internal value of the current controller. This is used by the current controller to provide accurate current regulation (refer to section 3.3.6: Q3 / Q4 (current controller) for more details).

### 5.2.6 Reference diode voltage measurement (V\_FWD) (address 10)

MSB														LSB	
1	0	1	0	0	0	V_FWD									Parity
A3	A2	A1	A0	free	free	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 68. Reference diode voltage measurement**

Description	Number of bits	Resolution per bit
Reference diode forward voltage drop	9 Bit	7.8 mV typ

#### Reference diode forward voltage (V\_FWD):

The V\_FWD value is a measurement of an internal reference diode using a fixed reference current. This corresponds to the forward voltage of one of the current controller output freewheeling diodes.

The resolution of the LSB is 7.8mV (typ.) and the parameter range is:

**Table 69. V\_FWD value**

SPI - Bit	D8	D7	D6	D5	D4	D3	D2	D1	D0
V_FWD	2 V	1 V	1/2 V	1/4 V	1/8 V	1/16 V	1/32 V	1/64 V	1/128 V

Note: Refer to section : [V\\_FWD](#) for more information.

### 5.2.7 Sense resistor measurement (Rs) (address 11)

MSB														LSB	
1	0	1	1	0	0	Rs									Parity
A3	A2	A1	A0	free	free	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 70. Sense resistor measurement**

Channel status	Number of bits	Name
Sense resistor measurement	9 Bit	Rs

Refer to [Section 4.5.2](#) for more information)

The resolution of the LSB is 8.7mΩ (typ.) and the parameter range is:

**Table 71. Rs value**

SPI - Bit	D8	D7	D6	D5	D4	D3	D2	D1	D0
Rs-value	4 Ω	2 Ω	1 Ω	1/2 Ω	1/4 Ω	1/8 Ω	1/16 Ω	1/32 Ω	1/64 Ω

### 5.2.8 Current controller status register (CC-STATUS) (address 12)

<b>MSB</b>															<b>LSB</b>
1	1	0	0	0	Res_CCV		RL_SPI								Parity
A3	A2	A1	A0	free	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 72. Current controller status register**

CC-register	Number of bits	name
Reset current controller values	2 Bit	Res_CCV
RL_SPI	8 Bit	RL_SPI

**Res\_CCV Feedback:**

Res\_CCV show the actual current controller reset state. This is not a copy of the bit received in the command register 15 (see 5.1.9). The bit combination '01' (reset) can only read via SPI if the communication runs during a current regulator reset.

**RL\_SPI feedback**

RL\_SPI is a copy of the received SPI-values (see 5.1.9: *Configuration register 3 (CCV reset and load resistance values) (address 15)*).



### 5.2.9 Error average (address 13 + 14)

MSB														LSB	
1	1	0	1	0	0	ERRORAVG_Q3								Parity	
1	1	1	0	0	0	ERRORAVG_Q4								Parity	
A3	A2	A1	A0	free	free	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

**Table 73. Error average**

Error average	Number of bits	Name
Error average	9 Bit	ERRORAVG_Qx

(refer to [Section 4.5.2 : Load current measurements](#) for detailed information)

### 5.2.10 Reserved (address 15)

This register is not used. Answer will always be 0xF001.

MSB														LSB	
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	Parity
A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	P

## 6 Register block functional overview

### 6.1 Input command register block overview (MOSI data)

Note: without address-bits and parity

Table 74. Overview input register block

address	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0 SYNC_REG	sync_ trig	RESET_VALUE				SYNC_VALUE					
		sync_ res_3	sync_ res_2	sync_ res_1	sync_ res_0	sync_ value_5	sync_ value_4	sync_ value_3	sync_ value_2	sync_ value_1	sync_ value_0
Power on reset status	0	0	0	0	0	0	0	0	0	0	0
1 STW_V	free	STW_V_MAX				STW_V_MIN					
		STW_ max_4	STW_ max_3	STW_ max_2	STW_ max_1	STW_ max_0	STW_ min_4	STW_ min_3	STW_ min_2	STW_ min_1	STW_ min_0
Power on reset status	0	0	0	0	0	0	0	0	0	0	0
2 CONFIG 1	free	free	EDGE_SH		FSON_ EN	FSOFF_ALL		CLKIN_S		SVDT	
			EDGE_SH_ OFF_1	EDGE_SH_ OFF_0		F <sub>SOFF_1</sub>	F <sub>SOFF_0</sub>	CLKIN_S_ 1	CLKIN_S_ 0	SVDT_1	SVDT_0
power on reset status	0	0	0	1	0	0	1	0	1	0	1
3 FSON	free	free	free	free	free	free	free	Q4_ON	Q3_ON	Q2_ON	Q1_ON
Power on reset status	0	0	0	0	0	0	0	0	0	0	0
4 Duration Q1/Q2	free	D_Q2				D_Q1					
		D <sub>Q2_4</sub>	D <sub>Q2_3</sub>	D <sub>Q2_2</sub>	D <sub>Q2_1</sub>	D <sub>Q2_0</sub>	D <sub>Q1_4</sub>	D <sub>Q1_3</sub>	D <sub>Q1_2</sub>	D <sub>Q1_1</sub>	D <sub>Q1_0</sub>
power on reset status	0	0	0	0	0	0	0	0	0	0	0
5 Duration Q3/Q4	free	D_Q4				D_Q3					
		D <sub>Q4_4</sub>	D <sub>Q4_3</sub>	D <sub>Q4_2</sub>	D <sub>Q4_1</sub>	D <sub>Q4_0</sub>	D <sub>Q3_4</sub>	D <sub>Q3_3</sub>	D <sub>Q3_2</sub>	D <sub>Q3_1</sub>	D <sub>Q3_0</sub>
power on reset status	0	0	0	0	0	0	0	0	0	0	0
6 DUTY1_Q1	free	free	DUTY1_Q1								
			DU1 <sub>Q1_8</sub>	DU1 <sub>Q1_7</sub>	DU1 <sub>Q1_6</sub>	DU1 <sub>Q1_5</sub>	DU1 <sub>Q1_4</sub>	DU1 <sub>Q1_3</sub>	DU1 <sub>Q1_2</sub>	DU1 <sub>Q1_1</sub>	DU1 <sub>Q1_0</sub>
Power on reset status	0	0	0	0	0	0	0	0	0	0	0
7 DUTY2_Q1	free	free	DUTY2_Q1								
			DU2 <sub>Q1_8</sub>	DU2 <sub>Q1_7</sub>	DU2 <sub>Q1_6</sub>	DU2 <sub>Q1_5</sub>	DU2 <sub>Q1_4</sub>	DU2 <sub>Q1_3</sub>	DU2 <sub>Q1_2</sub>	DU2 <sub>Q1_1</sub>	DU2 <sub>Q1_0</sub>

Table 74. Overview input register block (continued)

address	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
power on reset status	0	0	0	0	0	0	0	0	0	0	0
8 DUTY1_Q2	free	free	DUTY1_Q2								
			DU1Q2_8	DU1Q2_7	DU1Q2_6	DU1Q2_5	DU1Q2_4	DU1Q2_3	DU1Q2_2	DU1Q2_1	DU1Q2_0
power on reset status	0	0	0	0	0	0	0	0	0	0	0
9 DUTY2_Q2	free	free	DUTY2_Q2								
			DU2Q2_8	DU2Q2_7	DU2Q2_6	DU2Q2_5	DU2Q2_4	DU2Q2_3	DU2Q2_2	DU2Q2_1	DU2Q2_0
power on reset status	0	0	0	0	0	0	0	0	0	0	0
10 CUR/DTY1_Q3	free	free	CURRENT/DUTY1_Q3								
			CU1Q3_8	CU1Q3_7	CU1Q3_6	CU1Q3_5	CU1Q3_4	CU1Q3_3	CU1Q3_2	CU1Q3_1	CU1Q3_0
power on reset status	0	0	0	0	0	0	0	0	0	0	0
11 CUR/DTY2_Q3	free	free	CURRENT/DUTY2_Q3								
			CU2Q3_8	CU2Q3_7	CU2Q3_6	CU2Q3_5	CU2Q3_4	CU2Q3_3	CU2Q3_2	CU2Q3_1	CU2Q3_0
power on reset status	0	0	0	0	0	0	0	0	0	0	0
12 CUR/DTY1_Q4	free	free	CURRENT/DUTY1_Q4								
			CU1Q4_8	CU1Q4_7	CU1Q4_6	CU1Q4_5	CU1Q4_4	CU1Q4_3	CU1Q4_2	CU1Q4_1	CU1Q4_0
power on reset status	0	0	0	0	0	0	0	0	0	0	0
13 CUR/DTY2_Q4	free	free	CURRENT/DUTY2_Q4								
			CU2Q4_8	CU2Q4_7	CU2Q4_6	CU2Q4_5	CU2Q4_4	CU2Q4_3	CU2Q4_2	CU2Q4_1	CU2Q4_0
power on reset status	0	0	0	0	0	0	0	0	0	0	0
14 CONFIG_2	free	free	free	OV_TH_Q2		OV_TH_Q1		CCPWM_Q4		CCPWM_Q3	
				OV_TH_Q2_1	OV_TH_Q2_0	OV_TH_Q1_1	OV_TH_Q1_0	CCPWM_Q4_1	CCPWM_Q4_0	CCPWM_Q3_1	CCPWM_Q3_0
power on reset status	0	0	0	0	1	0	1	0	1	0	1
15 CONFIG_3	free	Res_CCV		RL_SPI							
		Res_CCV_1	Res_CCV_0	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
power on reset status	0	x	x	x	x	x	x	x	x	x	x

## 6.2 Status register block overview (MISO data)

Note: without address-bits and parity

Table 75. Overview answer register block

address	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0 G_INFO	free	SGND_L	STATE_FAST	CLKIN_State		HW_EN	CLKIN_F	SYNC_F	Data_F	SPICLK_F	PARITY_F
				CLKIN_S_1	CLKIN_S_0						
power on reset status	0	0	0	0	1	0	0	1	0	0	0
1 STATUS_Q_1	free	OV_TH	TW_1	Q1_OFF	Q1_ON	DL_Q1	PGND_L_Q1	TEMP_Q1	OVER_Q1	UC_Q1	OL_Q1
2 STATUS_Q_2	free	OV_TH	TW_2	Q2_OFF	Q2_ON	DL_Q2	PGND_L_Q2	TEMP_Q2	OVER_Q2	UC_Q2	OL_Q2
3 STATUS_Q_3	free	CCPWM_Q4	TW_3	Q3_OFF	Q3_ON	DL_Q3	PGND_L_Q3	TEMP_Q3	OVER_Q3	UC_Q3	OL_Q3
4 STATUS_Q_4	free	CCPWM_Q4	TW_4	Q4_OFF	Q4_ON	DL_Q4	PGND_L_Q4	TEMP_Q4	OVER_Q4	UC_Q4	OL_Q4
5 VD	free	BIST_BUSY	VD_8	VD_7	VD_6	VD_5	VD_4	VD_3	VD_2	VD_1	VD_0
6 OUT_DUTY_Q3	free	CNR_Q3	OUT_DUTY_Q3								
			OUTD_Q3_8	OUTD_Q3_7	OUTD_Q3_6	OUTD_Q3_5	OUTD_Q3_4	OUTD_Q3_3	OUTD_Q3_2	OUTD_Q3_1	OUTD_Q3_0
power on reset status	0	0	0	0	0	0	0	0	0	0	0
7 OUT_DUTY_Q4	free	CNR_Q4	OUT_DUTY_Q4								
			OUTD_Q4_8	OUTD_Q4_7	OUTD_Q4_6	OUTD_Q4_5	OUTD_Q4_4	OUTD_Q4_3	OUTD_Q4_2	OUTD_Q4_1	OUTD_Q4_0
power on reset status	0	0	0	0	0	0	0	0	0	0	0

Table 75. Overview answer register block (continued)

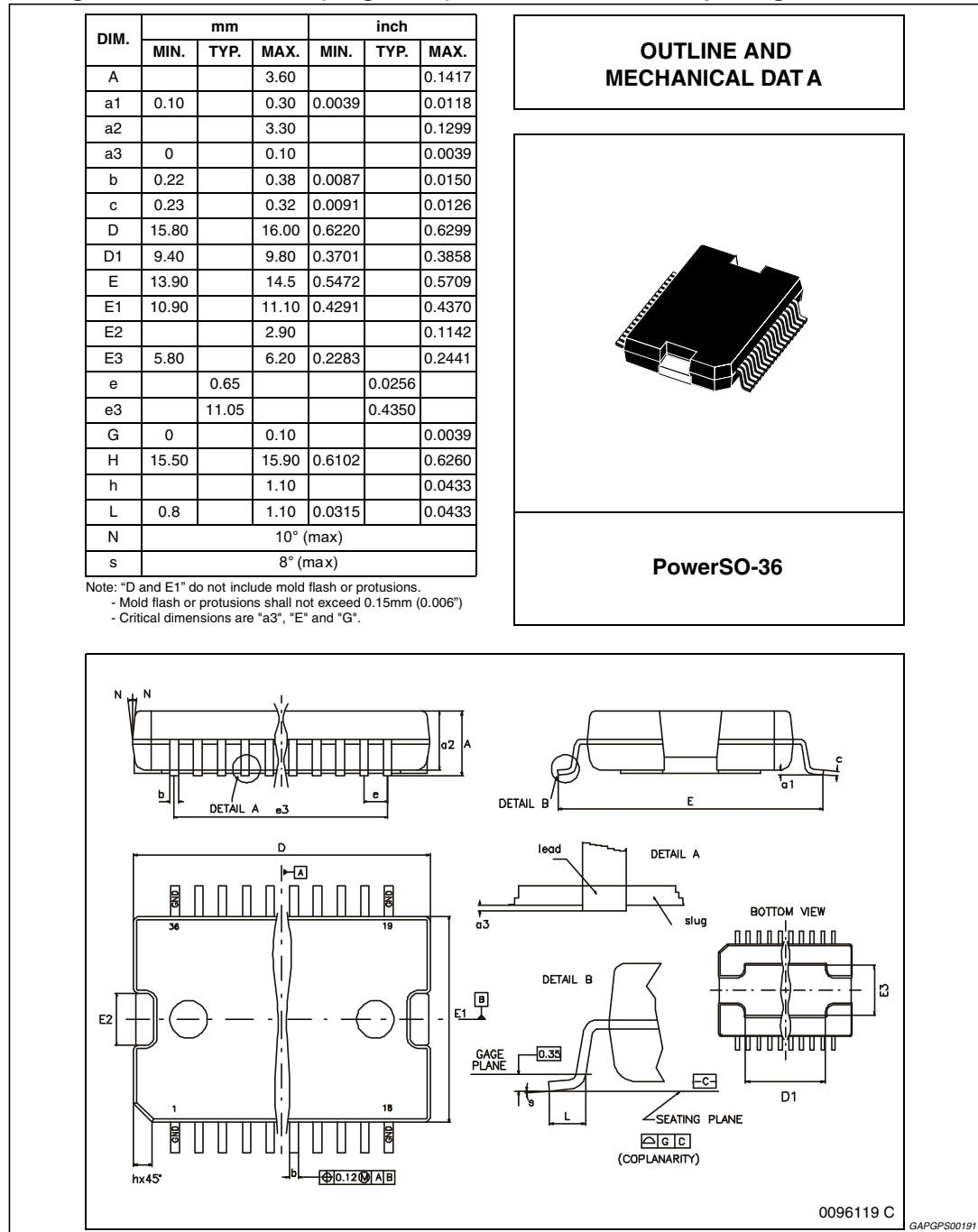
address	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8 ISAT_Q3	free	ISAT_Q3									
		ISAT_Q3_9	ISAT_Q3_8	ISAT_Q3_7	ISAT_Q3_6	ISAT_Q3_5	ISAT_Q3_4	ISAT_Q3_3	ISAT_Q3_2	ISAT_Q3_1	ISAT_Q3_0
power on reset status	0	0	0	0	0	0	0	0	0	0	0
9 ISAT_Q4	free	ISAT_Q4									
		ISAT_Q4_9	ISAT_Q4_8	ISAT_Q4_7	ISAT_Q4_6	ISAT_Q4_5	ISAT_Q4_4	ISAT_Q4_3	ISAT_Q4_2	ISAT_Q4_1	ISAT_Q4_0
power on reset status	0	0	0	0	0	0	0	0	0	0	0
10 V_FWD	free	free	V_FWD								
			V_FWD_8	V_FWD_7	V_FWD_6	V_FWD_5	V_FWD_4	V_FWD_3	V_FWD_2	V_FWD_1	V_FWD_0
power on reset status	0	0		x	x	x	x	x	x	x	x
11 RS	free	free	Rs								
			RS_8	RS_7	RS_6	RS_5	RS_4	RS_3	RS_2	RS_1	RS_0
power on reset status	0	0									
12 CC-STATUS	free	Res_CCV	RL_SPI	RL_SPI							
		Res_CC V_1	Res_CC V_0	RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0
power on reset status	0	0	1	0	1	0	0	0	0	0	0
13 ERRORAVG_Q3	free	free	ERRORAVG_Q3								
			ERROR_AVG_Q3_8	ERROR_AVG_Q3_7	ERROR_AVG_Q3_6	ERROR_AVG_Q3_5	ERROR_AVG_Q3_4	ERROR_AVG_Q3_3	ERROR_AVG_Q3_2	ERROR_AVG_Q3_1	ERROR_AVG_Q3_0
power on reset status	0	0	0	0	0	0	0	0	0	0	0
14 ERRORAVG_Q4	free	free	ERRORAVG_Q4								
			ERROR_AVG_Q4_8	ERROR_AVG_Q4_7	ERROR_AVG_Q4_6	ERROR_AVG_Q4_5	ERROR_AVG_Q4_4	ERROR_AVG_Q4_3	ERROR_AVG_Q4_2	ERROR_AVG_Q4_1	ERROR_AVG_Q4_0
power on reset status	0	0	0	0	0	0	0	0	0	0	0
15 RESERVED	RESERVED										
answer to access	0	0	0	0	0	0	0	0	0	0	0

# 7 Package information

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**Figure 37. PowerSO-36 (slug down) mechanical data and package dimensions**



## 8 Revision history

Table 76. Document revision history

Date	Revision	Changes
30-Oct-2013	1	Initial release.

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