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FAIRCHILD

October 2014

FDMS8558S(PCN)

N-Channel PowerTrench® SyncFET™

25 V, 90 A, 1.5 mΩ

Features

- Dual Cool™ PQFN package
- Max $r_{DS(on)}$ = 1.5 mΩ at V_{GS} = 10 V, I_D = 33 A
- Max $r_{DS(on)}$ = 1.7 mΩ at V_{GS} = 4.5 V, I_D = 31 A
- High performance technology for extremely low $r_{DS(on)}$
- SyncFET™ Schottky Body Diode
- RoHS Compliant

General Description

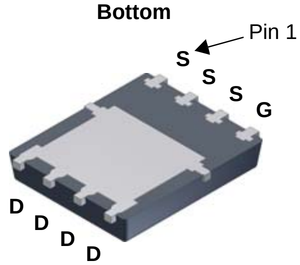
This N-Channel SyncFET™ is produced using Fairchild Semiconductor's advanced PowerTrench® process. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance. This device has the added benefit of an efficient monolithic Schottky body diode.

Applications

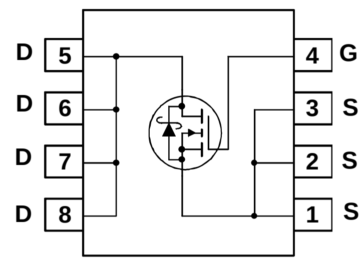
- Synchronous Rectifier for DC/DC Converters
- Telecom Secondary Side Rectification
- High End Server/Workstation Vcore Low Side

Top

Bottom



Power 56



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	12	V
I_D	Drain Current -Continuous (Package limited) T_C = 25 °C	90	A
	-Continuous T_A = 25 °C (Note 1a)	33	
	-Pulsed	140	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	145	mJ
P_D	Power Dissipation T_C = 25 °C	78	W
	Power Dissipation T_A = 25 °C (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case T_C = 25 °C	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient T_A = 25 °C (Note 1a)	50	

Package Marking and Ordering Information

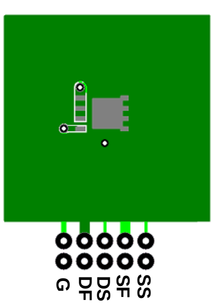
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
09OD	FDMS8558S	Power 56	13''	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

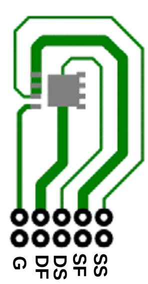
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25 °C		24		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 20 V, V_{GS} = 0 V			500	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = +12 V/-8 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 1 mA	1.1	1.4	2.2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25 °C		-3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 33 A		1.1	1.5	mΩ
		V_{GS} = 4.5 V, I_D = 31 A		1.3	1.7	
		V_{GS} = 10 V, I_D = 33 A, T_J = 125 °C		1.6	2.1	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 33 A		317		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 13 V, V_{GS} = 0 V, f = 1 MHz		5118		pF
C_{oss}	Output Capacitance			1508		pF
C_{rss}	Reverse Transfer Capacitance			195		pF
R_g	Gate Resistance			0.9		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 13 V, I_D = 33 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		14		ns
t_r	Rise Time			8		ns
$t_{d(off)}$	Turn-Off Delay Time			51		ns
t_f	Fall Time			7		ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 13 V, I_D = 33 A		81		nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 13 V, I_D = 33 A		38		nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 13 V, I_D = 33 A		10		nC
Q_{gd}	Gate to Drain “Miller” Charge			9.7		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2)		0.6	0.8	V
		V_{GS} = 0 V, I_S = 33 A (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	I_F = 33 A, di/dt = 300 A/μs		35		ns
Q_{rr}	Reverse Recovery Charge			49		nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. E_{AS} of 145 mJ is based on starting T_J = 25 °C, L = 0.9 mH, I_{AS} = 18 A, V_{DD} = 23 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 39 A.

Typical Characteristics T_J = 25 °C unless otherwise noted

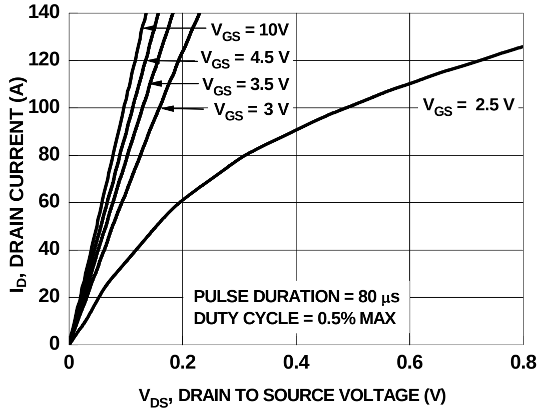


Figure 1. On Region Characteristics

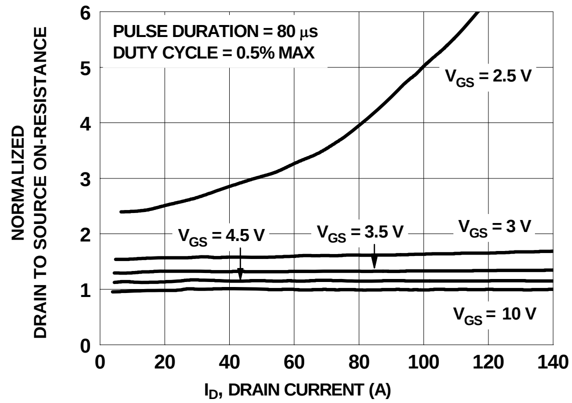


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

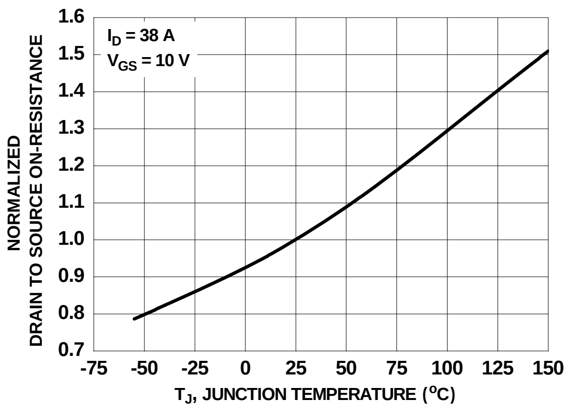


Figure 3. Normalized On Resistance vs Junction Temperature

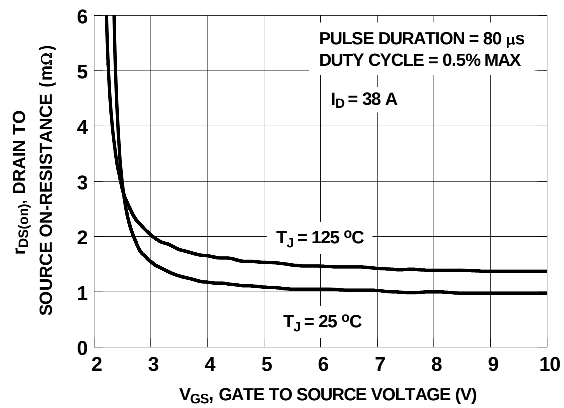


Figure 4. On-Resistance vs Gate to Source Voltage

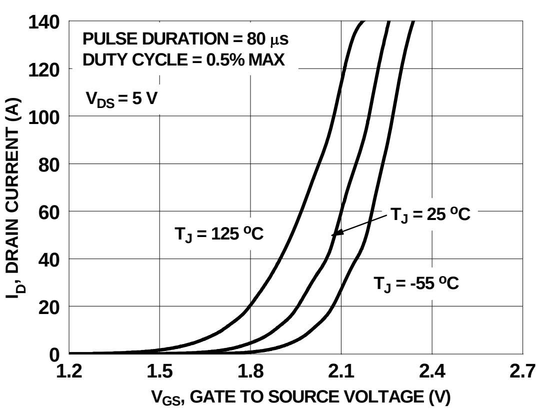


Figure 5. Transfer Characteristics

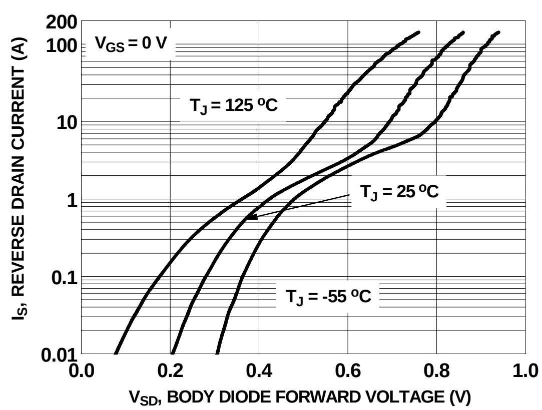


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

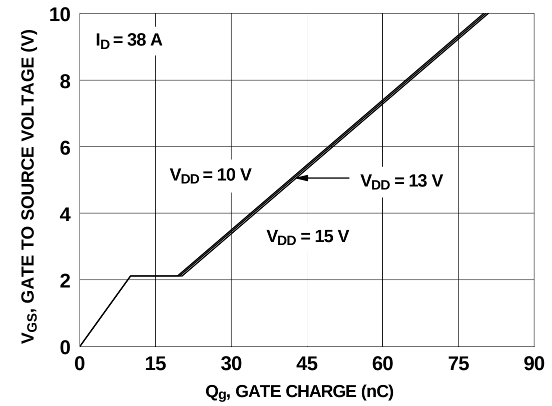


Figure 7. Gate Charge Characteristics

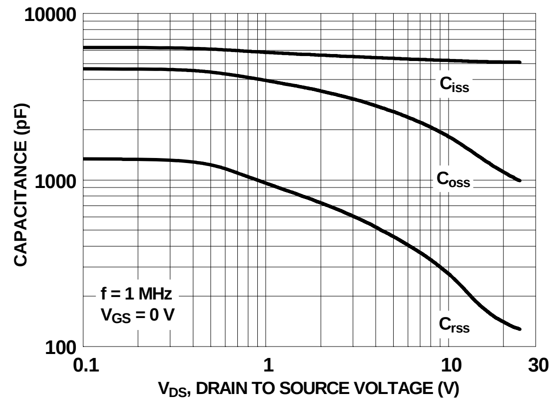


Figure 8. Capacitance vs Drain to Source Voltage

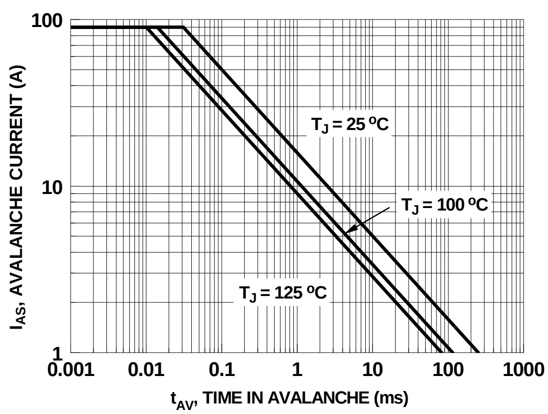


Figure 9. Unclamped Inductive Switching Capability

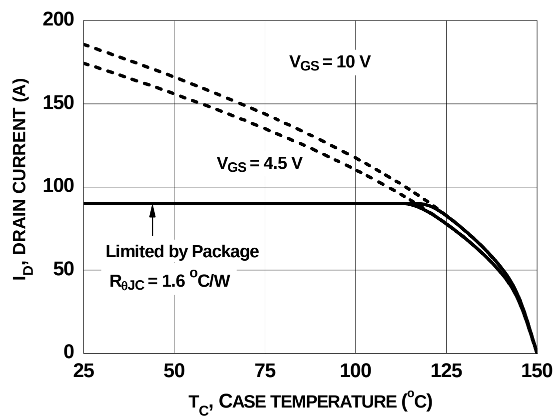


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

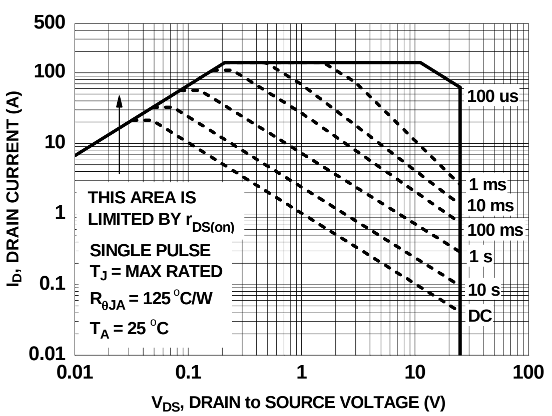


Figure 11. Forward Bias Safe Operating Area

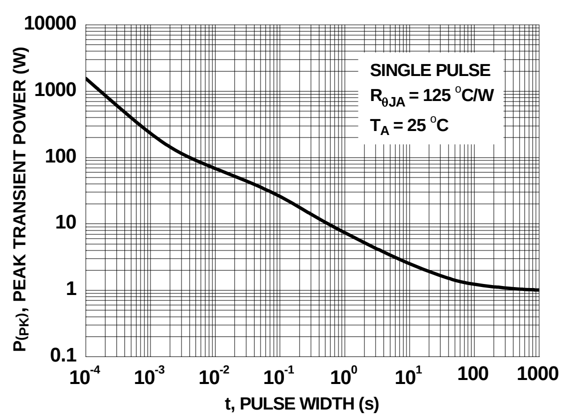


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

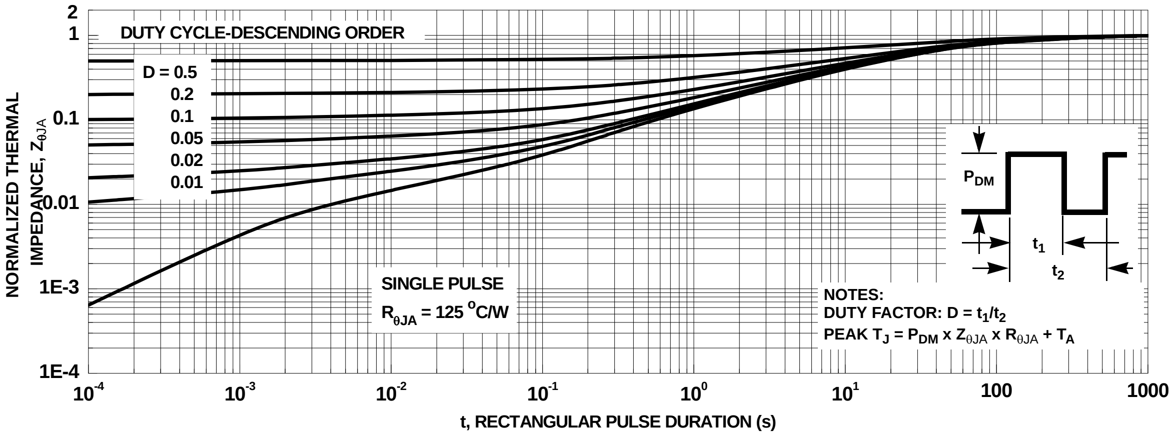


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET™ Schottky body diode Characteristics

Fairchild's SyncFET™ process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS8558S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

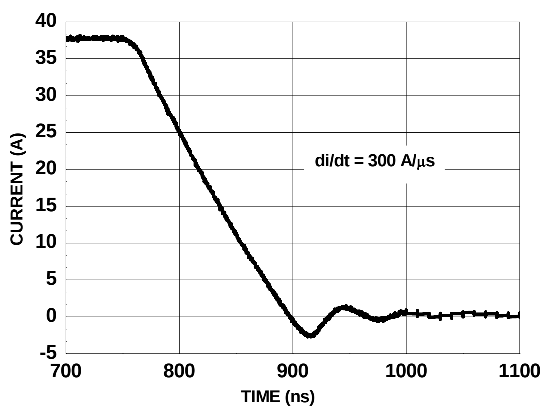


Figure 14. FDMS8558S SyncFET™ body diode reverse recovery characteristic

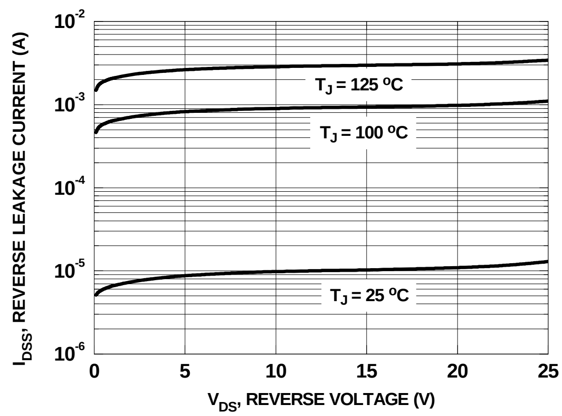
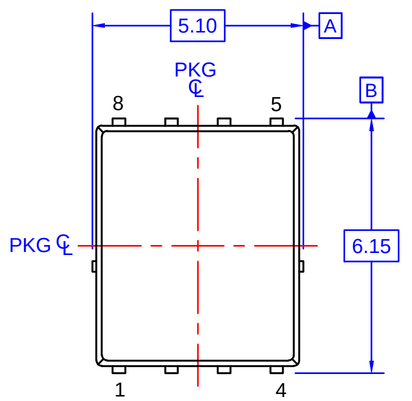
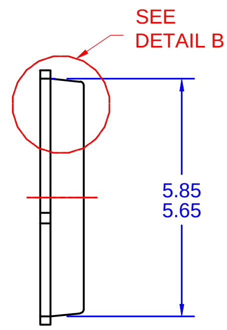


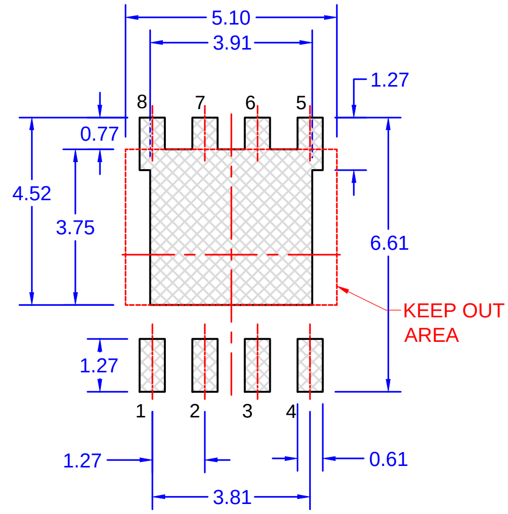
Figure 15. SyncFET™ body diode reverse leakage versus drain-source voltage

PQFN8 5X6, 1.27P
CASE 483AE
ISSUE A

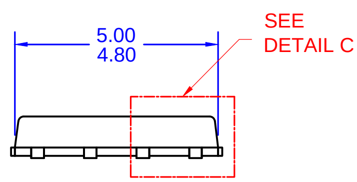


TOP VIEW

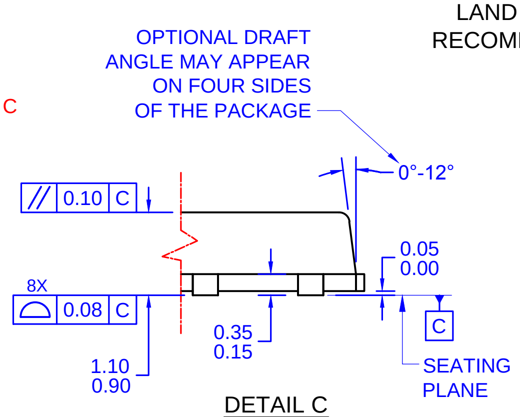




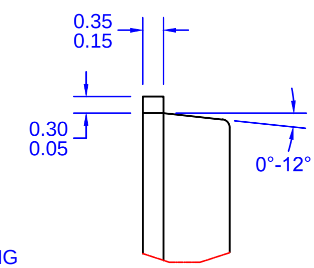
LAND PATTERN
RECOMMENDATION



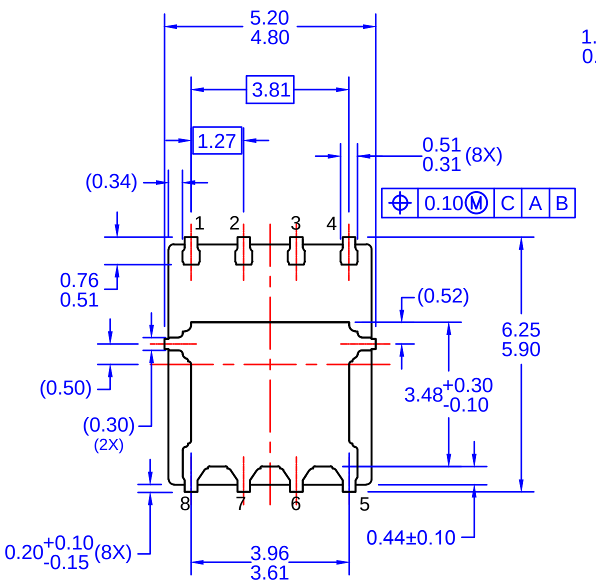
SIDE VIEW



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED
- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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