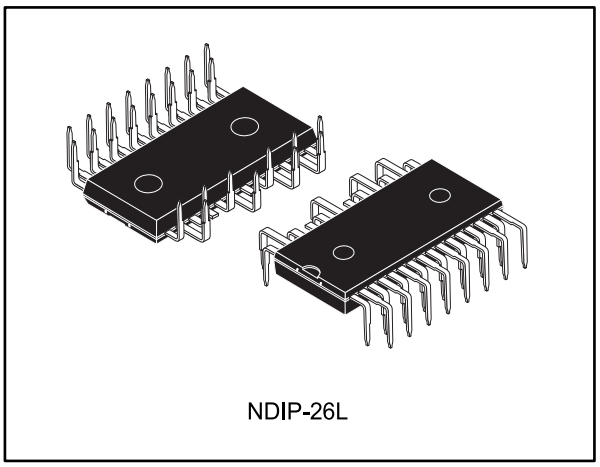
STGIPN3H60AT

SLLIMM™-nano small low-loss intelligent molded module IPM, 3 A, 600 V, 3-phase IGBT inverter bridge

Datasheet - production data



NDIP-26L

Features

- IPM 3 A, 600 V, 3-phase IGBT inverter bridge including control ICs for gate driving and freewheeling diodes
- Optimized for low electromagnetic interference
- $V_{CE(sat)}$ negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull-down resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Optimized pinout for easy board layout
- 85 kΩ NTC for temperature control (UL1434 CA 2 and 4)

Applications

- 3-phase inverters for motor drives
- Dish washers, refrigerator compressors, heating systems, air-conditioning fans, draining and recirculation pumps

Description

This intelligent power module implements a compact, high performance AC motor drive in a simple, rugged design. It is composed of six IGBTs with freewheeling diodes and three half-bridge HVICs for gate driving, providing low electromagnetic interference (EMI) characteristics with optimized switching speed. The package is optimized for thermal performance and compactness in built-in motor applications, or other low power applications where assembly space is limited. This IPM includes an operational amplifier, completely uncommitted, and a comparator that can be used to design a fast and efficient protection circuit. SLLIMM™ is a trademark of STMicroelectronics.

Table 1: Device summary

Order code	Marking	Package	Packing
STGIPN3H60AT	GIPN3H60AT	NDIP-26L	Tube

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1 Internal schematic diagram and pin configuration

Figure 1: Internal schematic diagram

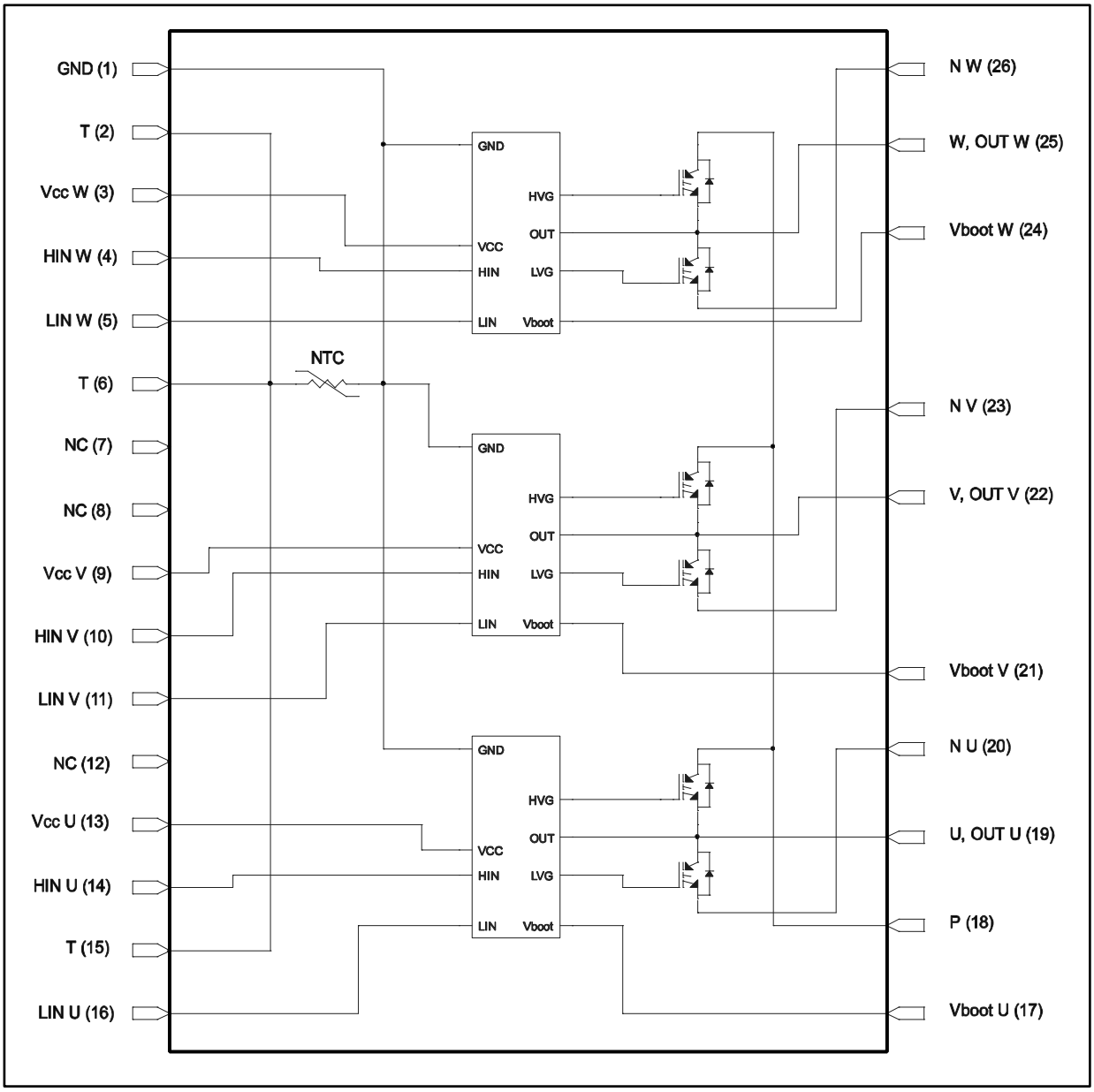
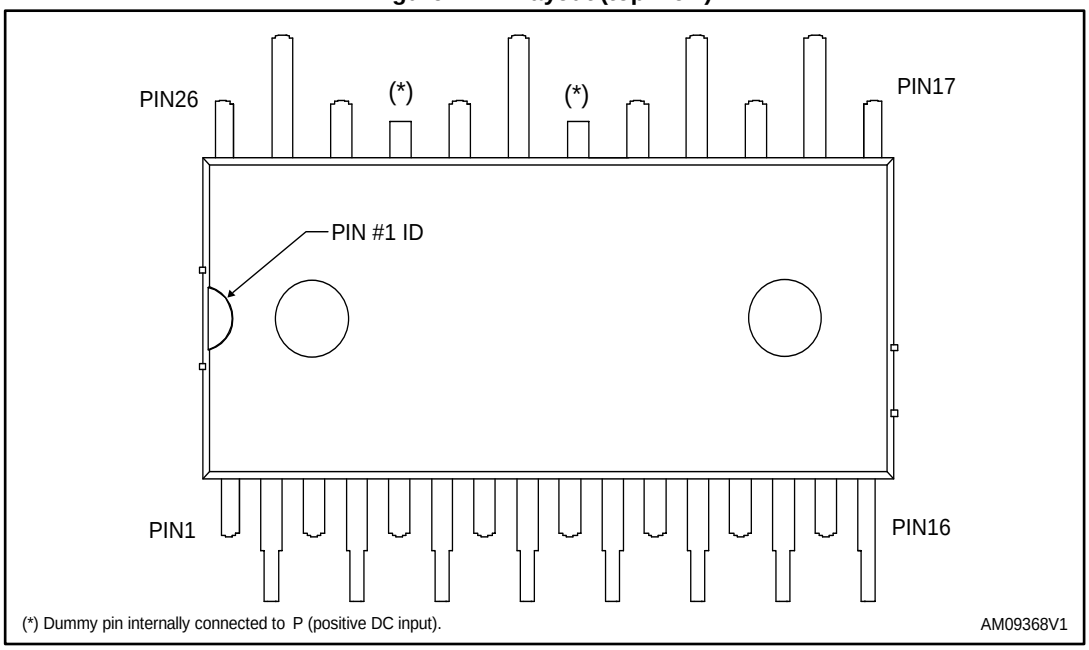


Table 2: Pin description

Pin	Symbol	Description
1	GND	Ground
2	T	NTC thermistor terminal
3	V_{CC} W	Low voltage power supply W phase
4	HIN W	High side logic input for W phase
5	LIN W	Low side logic input for W phase
6	T	NTC thermistor terminal
7	NC	Not connected
8	NC	Not connected
9	V_{CC} V	Low voltage power supply V phase
10	HIN V	High side logic input for V phase
11	LIN V	Low side logic input for V phase
12	NC	Not connected
13	V_{CC} U	Low voltage power supply for U phase
14	HIN U	High side logic input for U phase
15	T	NTC thermistor terminal
16	LIN U	Low side logic input for U phase
17	V_{BOOT} U	Bootstrap voltage for U phase
18	P	Positive DC input
19	U	U phase output
20	N_U	Negative DC input for U phase
21	V_{BOOT} V	Bootstrap voltage for V phase
22	V	V phase output
23	N_V	Negative DC input for V phase
24	V_{BOOT} W	Bootstrap voltage for W phase
25	W	W phase output
26	N_W	Negative DC input for W phase

Figure 2: Pin layout (top view)



2 Electrical ratings

2.1 Absolute maximum ratings

Table 3: Inverter part

Symbol	Parameter	Value	Unit
V_{CES}	Each IGBT collector emitter voltage (V_{IN}[(1)]= 0)	600	V
± I_C[(2)]	Each IGBT continuous collector current at T_C = 25°C	3	A
± I_{CP}[(3)]	Each IGBT pulsed collector current	18	A
P_{TOT}	Each IGBT total dissipation at T_C = 25°C	8	W

Notes:

(1)Applied between HIN_i, LIN_i and G_{ND} for i = U, V, W.

(2)Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

(3)Pulse width limited by max junction temperature.

Table 4: Control part

Symbol	Parameter	Min.	Max.	Unit
V_{OUT}	Output voltage applied between OUT_U, OUT_V, OUT_W - GND	V_{boot} - 18	V_{boot} + 0.3	V
V_{CC}	Low voltage power supply	- 0.3	18	V
V_{boot}	Bootstrap voltage	- 0.3	618	V
V_{IN}	Logic input voltage applied between HIN_i, LIN_i and G_{ND} for i = U, V, W	- 0.3	V_{CC} + 0.3	V
$\Delta V_{OUT/dT}$	Allowed output slew rate		50	V/ns

Table 5: Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 s.)	1000	V
T_j	Power chips operating junction temperature range	-40 to 150	°C
T_C	Module operation case temperature range	-40 to 125	°C

2.2 Thermal data

Table 6: Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	50	°C/W

3 Electrical characteristics

3.1 Inverter part

T_J = 25 °C unless otherwise specified.

Table 7: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{CC} = V_{boot} = 15 V, V_{IN}(1) = 0 to 5 V, I_C = 1 A	-	2.15	2.6	V
		V_{CC} = V_{boot} = 15 V, V_{IN}(1) = 0 to 5 V, I_C = 1 A, T_J = 125 °C	-	1.65		
I_{CES}	Collector-cut off current (V_{IN}(1) = 0 “logic state”)	V_{CE} = 550 V, V_{CC} = V_{Boot} = 15 V	-		250	µA
V_F	Diode forward voltage	V_{IN}(1) = 0 “logic state”, I_C = 1 A	-		1.7	V

Notes:

(1)Applied between HIN_i, LIN_i and G_{ND} for i = U, V, W (LIN inputs are active-low).

Table 8: Inductive load switching time and energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{on}(1)	Turn-on time	V_{DD} = 300 V, V_{CC} = V_{boot} = 15 V, V_{IN}(2) = 0 to 5 V, I_C = 1 A (see *Figure 4: "Switching time definition"*)	-	275	-	ns
$t_{c(on)}$(1)	Crossover time (on)		-	90	-	
t_{off}(1)	Turn-off time		-	890	-	
$t_{c(off)}$(1)	Crossover time (off)		-	125	-	
t_{rr}	Reverse recovery time		-	50	-	
E_{on}	Turn-on switching energy		-	18	-	µJ
E_{off}	Turn-off switching energy		-	13	-	

Notes:

(1)t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

(2)Applied between HIN_i, LIN_i and G_{ND} for i = U, V, W (LIN inputs are active-low).

Figure 3: Switching time test circuit

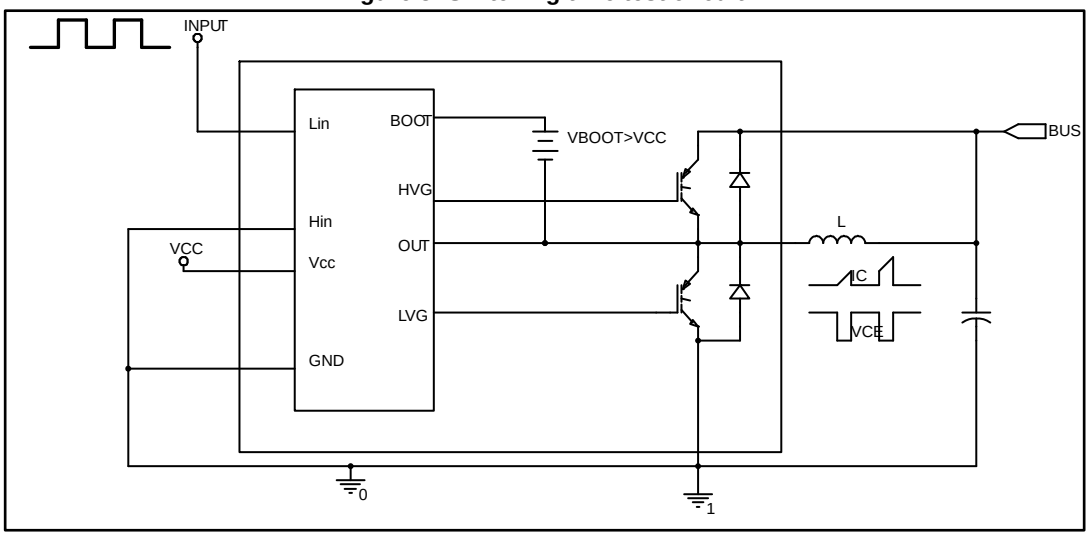
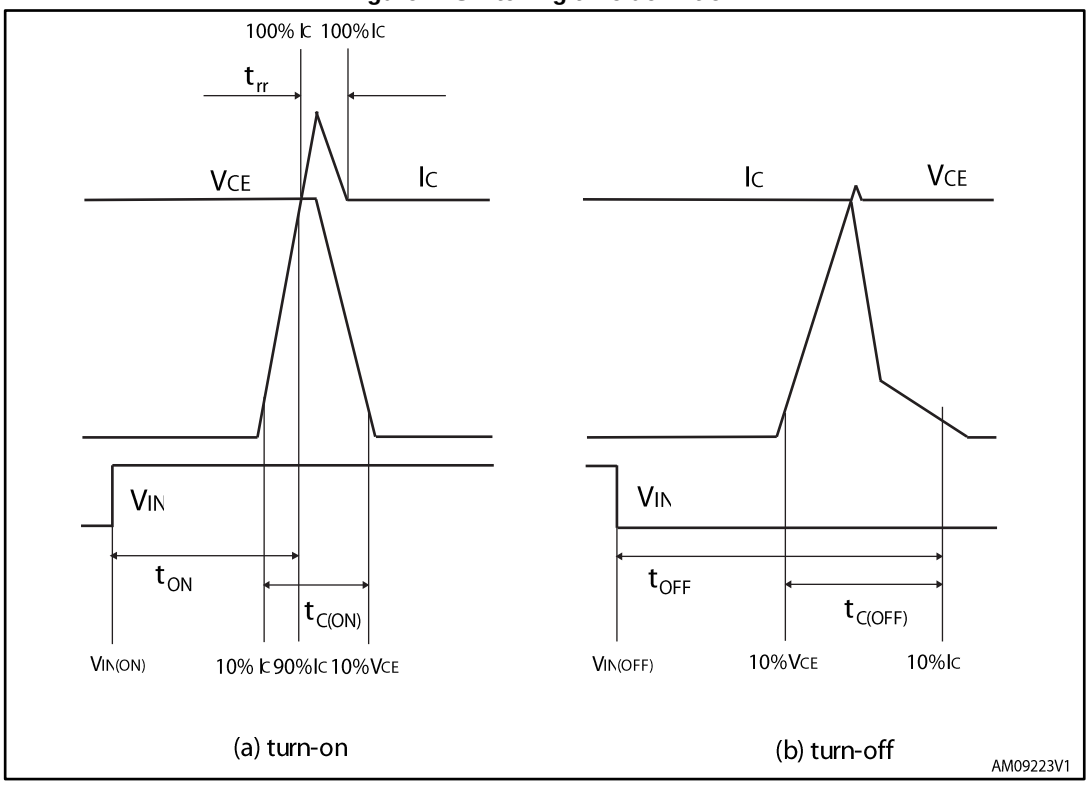


Figure 4: Switching time definition



3.2 Control part

Table 9: Low voltage power supply (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC_thON}	Undervoltage turn-on threshold		9.1	9.6	10.1	V
V_{CC_thOFF}	Undervoltage turn-off threshold		7.9	8.3	8.8	V
V_{CC_hys}	Undervoltage hystereses		0.9			V
I_{qccu}	Undervoltage quiescent supply current	V_{CC} < 7.9 V		250	330	µA
I_{qcc}	Quiescent current	V_{CC} = 15 V		350	450	µA

Table 10: Bootstrapped voltage (V_{CC} = 15 V unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{boot_thON}	Undervoltage turn-on threshold		8.5	9.5	10.5	V
V_{boot_thOFF}	Undervoltage turn-off threshold		7.2	8.3	9.2	V
$V_{boothys}$	Undervoltage hystereses		0.9			V
I_{qboot}	Quiescent current				250	µA
$R_{DS(on)}$	Bootstrap driver on-resistance	V_{CC} > 12.5 V		125		Ω

Table 11: Logic inputs (V_{CC} = 15 V unless otherwise specified)

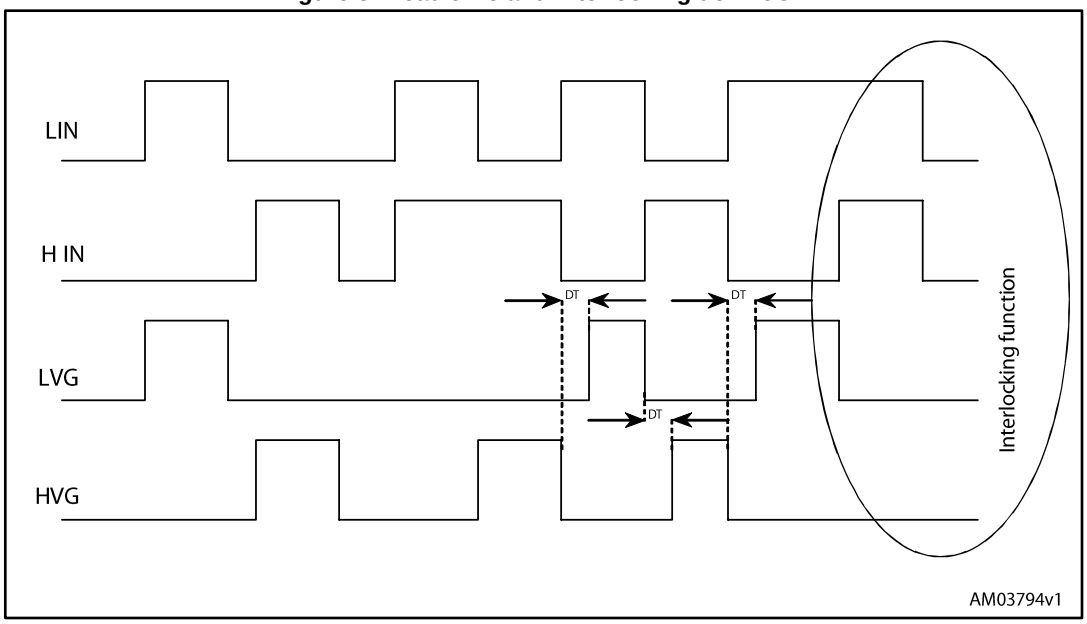
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low level logic input voltage				1.1	V
V_{ih}	High level logic input voltage		1.8			V
I_{il}	Low level logic input current (1)	V_{IN} = 0 V (1)	-1			µA
I_{ih}	High level logic input current (1)	V_{IN} = 15 V (1)		20	70	µA
Dt	Dead time(2)			320		ns

Notes:

(1)Applied between HIN_i, LIN_i and G_{ND} for i = U, V, W

(2)See *Figure 5: "Dead time and interlocking definition"*

Figure 5: Dead time and interlocking definition



3.2.1 NTC thermistor

Table 12: NTC thermistor

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R25	Resistance	T = 25 °C		85		kΩ
R100	Resistance	T = 100 °C		5388		Ω
B	B-constant	T = 25 °C to 100 °C		4092		K
T	Operating temperature		-25		125	°C

$$R(T) = R_{25} \times e^{B\left(\frac{1}{T}-\frac{1}{298}\right)}$$

Where T are temperatures in Kelvins

Figure 6: NTC resistance vs. temperature

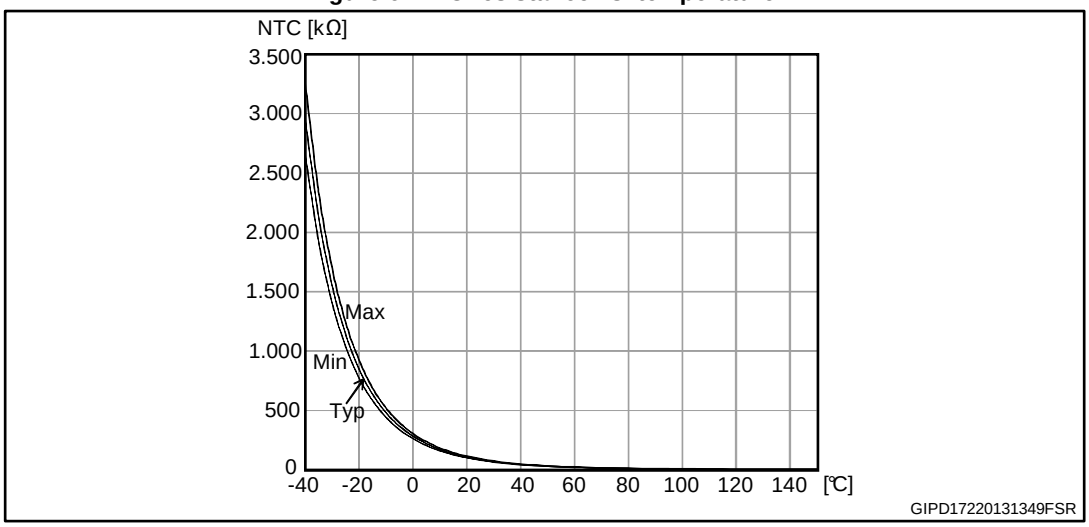
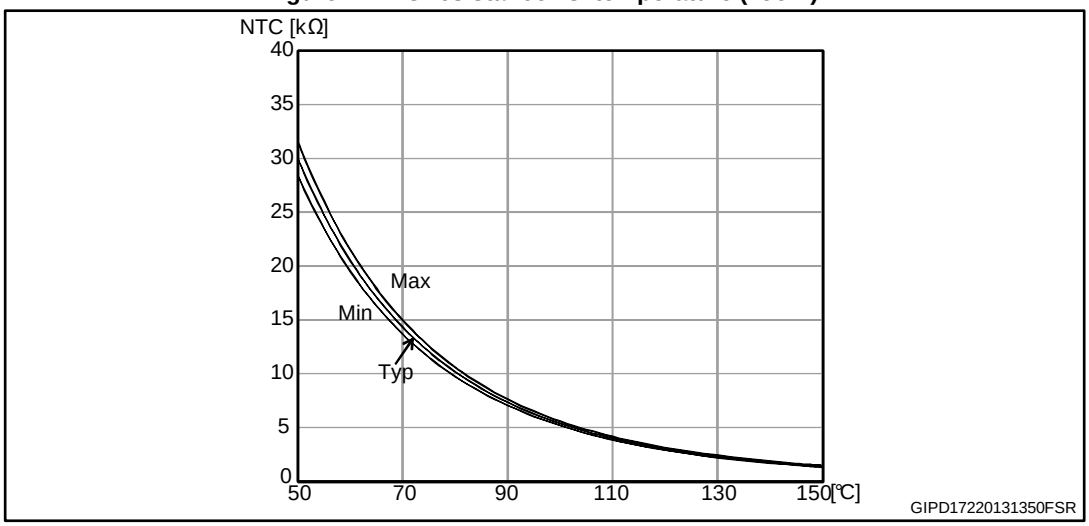
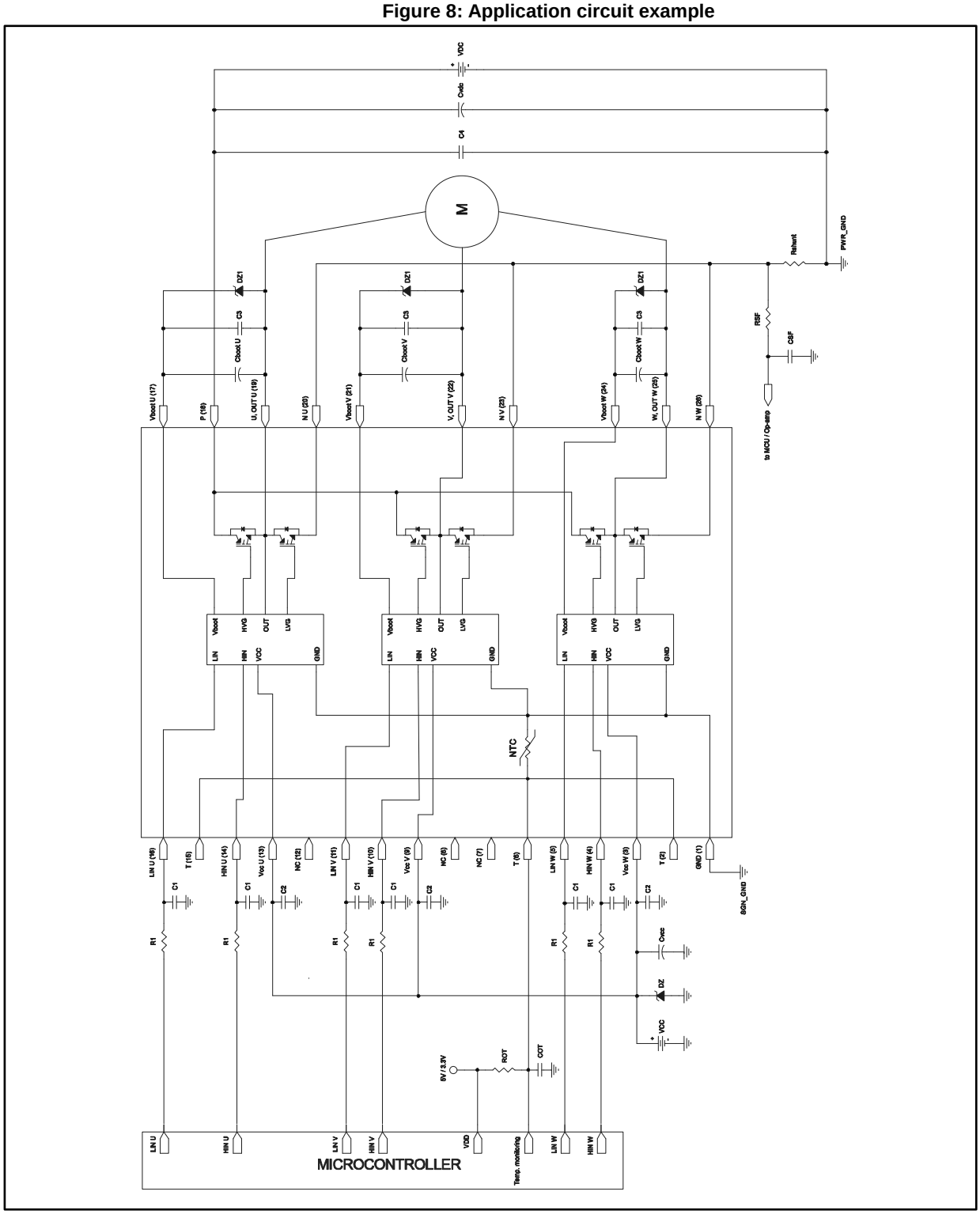


Figure 7: NTC resistance vs. temperature (zoom)



4 Application circuit example

Figure 8: Application circuit example



Application designers are free to use a different scheme according with the specifications of the device.

4.1 Guidelines

- Input signals HIN, LIN are active-high logic. A 500 kΩ (typ.) pull-down resistor is built-in for each input. To prevent input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters (R1, C1) on each input signal is suggested. The filters should be done with a time constant of about 100ns and must be placed as close as possible to the IPM input pins.
- The bypass capacitor Cvcc (aluminum or tantalum) is recommended to reduce the transient circuit demand on the power supply. In addition, a decoupling capacitor C2 (from 100 to 220 nF, ceramic with low ESR) is suggested, to reduce high frequency switching noise distributed on the power supply lines. It must be placed as close as possible to each Vcc pin and in parallel to the bypass capacitor.
- The use of RC filter (RSF, CSF) for current monitoring is recommended to improve noise immunity. The filter must be placed as close as possible to the microcontroller or to the Op-amp.
- The decoupling capacitor C3 (from 100 to 220 nF, ceramic with low ESR), in parallel to each C_{boot}, is recommended in order to filter high frequency disturbances.
- The Zener diodes DZ1 between the Vcc pins and GND and in parallel to each Cboot is suggested in order to prevent overvoltage.
- The decoupling capacitor C4 (from 100 to 220 nF, ceramic with low ESR) in parallel to the electrolytic capacitor Cvdc is recommended, in order to prevent surge destruction. Both capacitors C4 and Cvdc should be placed as close as possible to the IPM (C4 has priority over Cvdc).
- By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an opto-coupler is possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- In order to avoid malfunctions, the wiring between N pins, the shunt resistor and PWR_GND should be as short as possible.
- It is recommended to connect SGN_GND to PWR_GND at only one point (near the terminal of shunt resistor), in order to avoid any malfunction due to power ground fluctuation.

These guidelines are useful for application design to ensure the specifications of the device. For further details, please refer to the relevant application note AN4043.

Table 13: Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply voltage	Applied between P-Nu, Nv, Nw		300	500	V
V_{CC}	Control supply voltage	Applied between V_{CC}-GND	12	15	17	V
V_{BS}	High side bias voltage	Applied between V_{BOOTi}-OUT_i for i = U, V, W	11.5		17	V
t_{dead}	Blanking time to prevent Arm-short	For each input signal	1.5			µs
f_{PWM}	PWM input signal	-40°C < T_c < 100 °C -40°C < T_j < 125 °C			25	kHz
T_C	Case operation temperature				100	°C

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

5.1 NDIP-26L type C package information

Figure 9: NDIP-26L type C package outline

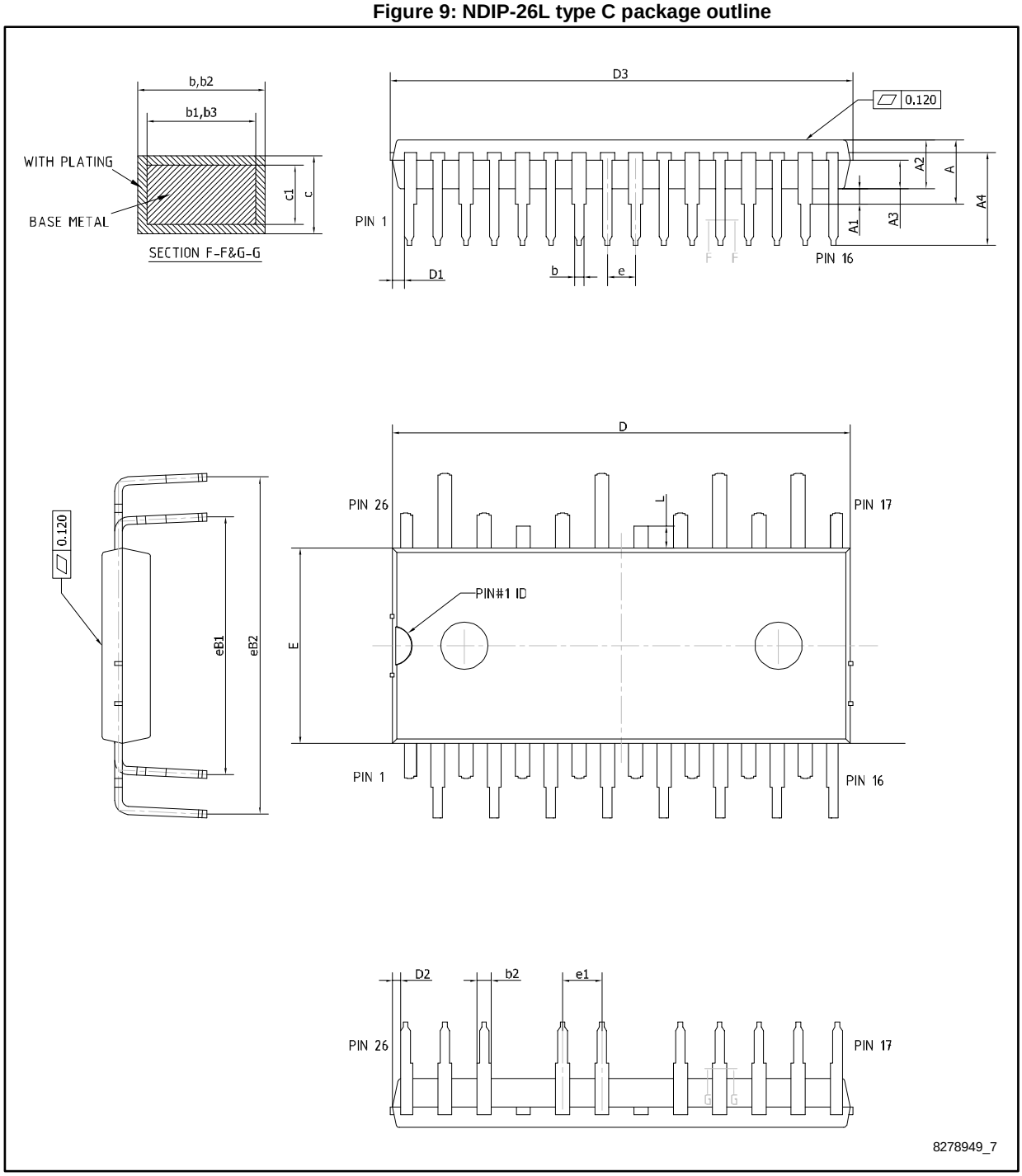


Table 14: NDIP-26L type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			4.40
A1	0.80	1.00	1.20
A2	3.00	3.10	3.20
A3	1.70	1.80	1.90
A4	5.70	5.90	6.10
b	0.53		0.72
b1	0.52	0.60	0.68
b2	0.83		1.02
b3	0.82	0.90	0.98
c	0.46		0.59
c1	0.45	0.50	0.55
D	29.05	29.15	29.25
D1	0.50	0.77	1.00
D2	0.35	0.53	0.70
D3			29.55
E	12.35	12.45	12.55
e	1.70	1.80	1.90
e1	2.40	2.50	2.60
eB1	16.10	16.40	16.70
eB2	21.18	21.48	21.78
L	1.24	1.39	1.54

5.2 NDIP-26L packing information

Figure 10: NDIP-26L tube dimensions (dimensions are in mm)

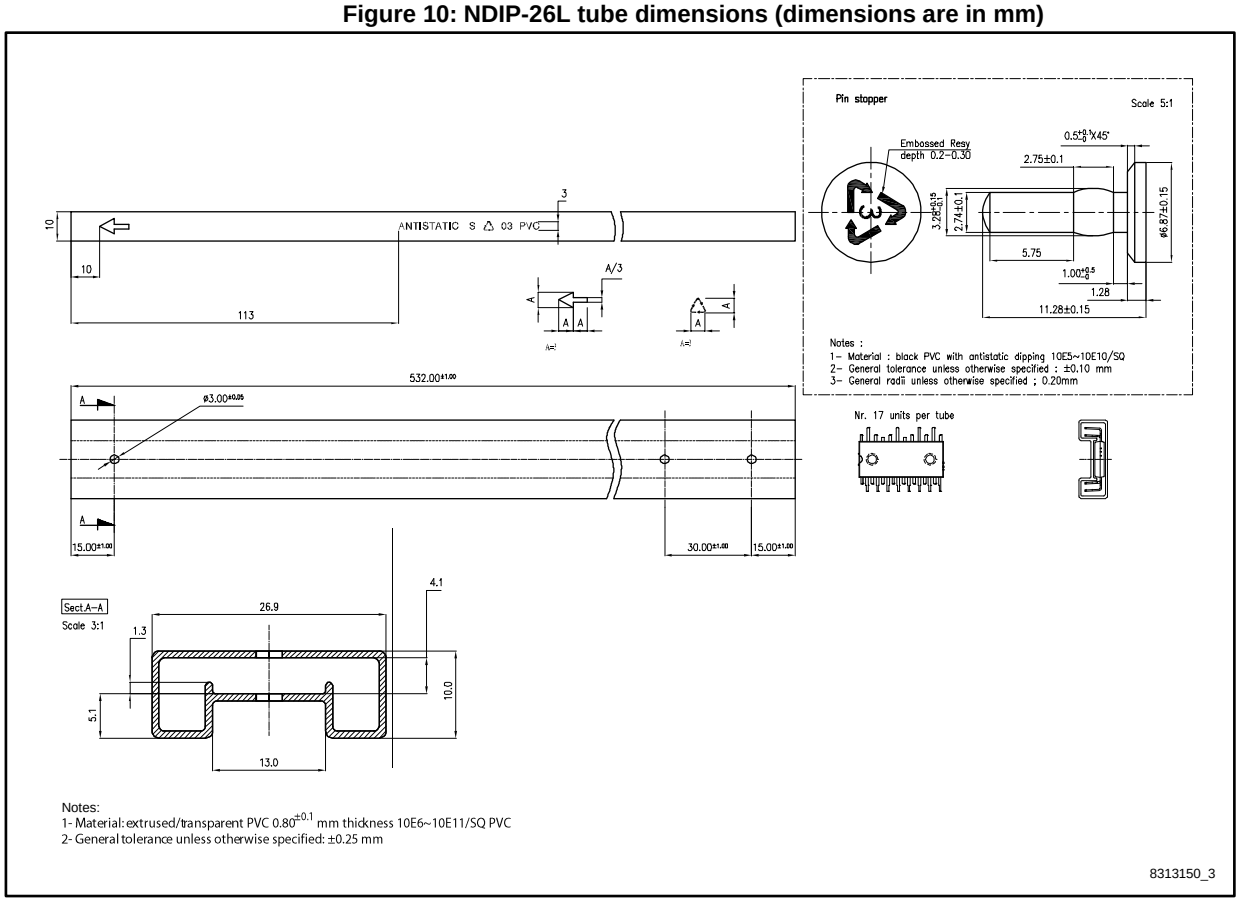


Table 15: Shipping details

Parameter	Value
Base quantity	17 pcs
Bulk quantity	476 pcs

6 Revision history

Table 16: Document revision history

Date	Revision	Changes
30-Sep-2014	1	Initial release.
13-Sep-2016	2	Updated *Section 5.1: "NDIP-26L type C package information"* and *Section 5.2: "NDIP-26L packing information"* Minor text changes

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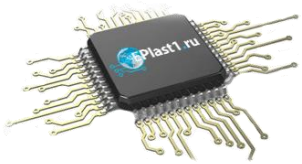

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