ADM6993/X

ADM6993/X HDLC to Fast Ethernet Converter

Communications

Never stop thinking.

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Previous Version:

Page/Date	Subjects (major changes since last revision)
2003-07-02	Rev. 1.0: First release of ADM6993
2003-10-13	Rev. 1.1: Added sections 4.3&4.4
2005-08-15	Changed to the new Infineo format
2005-09-09	Rev. 1.11: when changed to the new Infineon format
2005-11-28	Minor change. Included Green package information

Trademarks

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1 Product Overview

Features and the block diagram.

1.1 Overview

The ADM6993/X is a single chip integrating two 10/100 Mbps MDIX TX/FX transceivers, a three-port 10/100M Ethernet L2 switch controller, and features converter mode to meet demanding applications, including Fiber-to-Ethernet media converters, 2/3 port Ethernet switches, VoIP gateways, and NAT routers. The ADM6993X is the environmentally friendly “green” package version.

The ADM6993/X supports priority features on Port-Base priority, VLAN TAG priority and IP TOS precedence checking at individual ports. This is done through a small low-cost micro controller to initialize or on-the-fly to configure. The priority of packets can be tagged based on TCP port number for the multi-media application.

The 2nd MAC interface could be selected as TP/FX or MII/RMII/GPSI to connect with bridge devices for different media. The 3rd MAC interface could be selected as MII/RMII/GPSI/HDLC to connect with routing devices, and bridge devices for different media. The dedicated HDLC channel supports rate from 64Kbps to 50Mbps.

On the media side of port0/1, the ADM6993/X supports auto MDIX 10Base-T/100Base-TX and 100Base-FX as specified by the IEEE 802.3 committee through uses of digital circuitry and high speed A/D.

ADM6993/X supports serial management interface (SMI) for a small low-cost micro controller to initialize or configure. It also provides port status for remote agent monitor and smart counter for port statistics.

1.2 Features

Main features:

- 3-port10/100M switch integrated with a 2-port PHY (10/100TX and 100FX) and 3rd MAC port as GPSI/MII/RMII/HDLC.
- Provides TX<-->FX Converter modes with faulted propagation and redundant capability by using of two ADM6993/X.
- Short latency on the converter mode.
- Built-in data buffer 6Kx64bit SRAM.
- Up to 2k MAC Unicast addresses with a 4-way associative hashing table.
- MAC address learning table with aging function.
- Two queues per port for QoS purposes.
- Port-base, 802.1p and TCP/IP ToS priority.
- Store & forward architecture.
- 802.3x flow control for full duplex and back-pressure for half duplex in case the buffer is full.
- Supports Auto-Negotiation.
- Packet lengths up to 1536 bytes.
- Broadcast storming filter.
- Port-base VLAN/tag-base VLAN.
- 16 entries of packet classification and marking or filtering for TCP/UDP Port Numbering, IP Protocol ID and Ethernet Type.
- Serial Management Interface for low-end CPUs.
- Provides port status for remote agent monitoring .
- Provides smart counters for port statistics reporting.
- 128 PQFP packaging with 2.5 V/3.3 V power supply.

1.3 Block Diagram

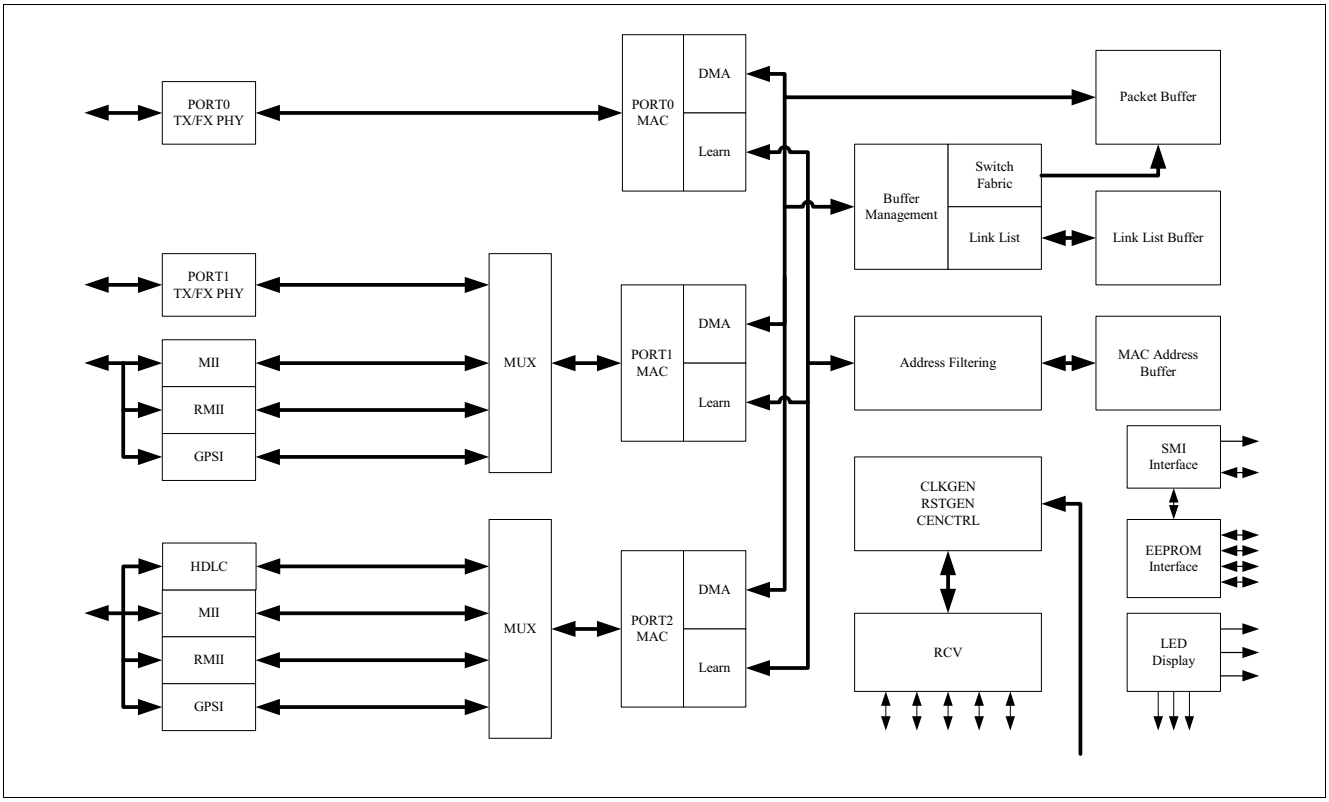


Figure 1 ADM6993/X Block Diagram

1.4 Data Lengths Conventions

Table 1 Data Lengths Conventions

qword	64 bits
dword	32 bits
word	16 bits
byte	8 bits
nibble	4 bits

2 Interface Description

This chapter describes Pin Diagram, Pin Type and Buffer Type Abbreviations, and Pin Descriptions.

2.1 Pin Diagram

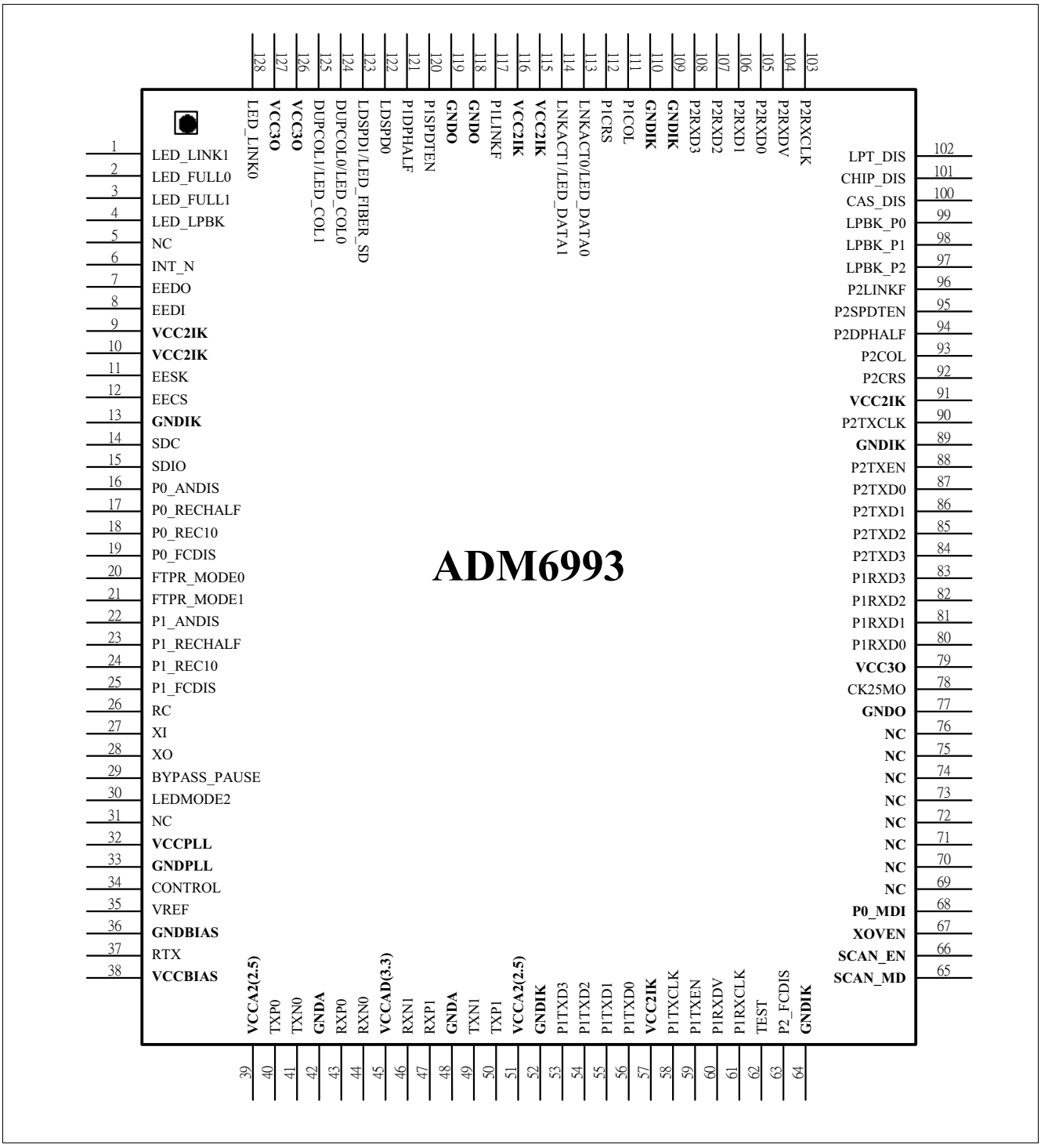


Figure 2 ADM6993/X Pin Assignment

2.2 Pin Type and Buffer Type Abbreviations

Standardized abbreviations:

Table 2 ADM6993/XAbbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 3 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 k Ω
PD1	Pull down, 10 k Ω
PD2	Pull down, 20 k Ω
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.3 Pin Descriptions

ADM6993/X pins are categorized into one of the following groups:

- Port 0/1 Twisted Pair Interface, 8 pins
- Port 2 (MII/RMII/GPSI) Interface, 17 pins
- Port 1 alternative MII Port Interface, 17 pins
- LED Interface, 13 pins
- EEPROM Interface, 4 pins
- Configuration Interface, 28 pins
- Ground/Power Interface, 27 pins
- Miscellaneous, 14 pins

Note: If not specified, all signals default to digital signals.

Table 4 Port 0/1 Twisted Pair Interface (8 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
40	TXP_0	AO		**Twisted Pair Transmit** Output Positive.
50	TXP_1	AO		
41	TXN_0	AO		**Twisted Pair Transmit** Output Negative.
49	TXN_1	AO		
43	RXP_0	AI		**Twisted Pair Receive** Input Positive.
47	RXP_1	AI		
44	RXN_0	AI		**Twisted Pair Receive** Input Negative.
46	RXN_1	AI		

Table 5 Port 2 (MII/RMII/GPSI) Interface (17 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
87	P2TXD0	I/O	TTL, PD, 8mA	**Port 2 MII Transmit Data bit 0** Synchronous to the rising edge of TXCLK.
	FXMODE0			**FXMODE0** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as bit 0 of FXMODE.
86	P2TXD1	I/O	TTL, PD, 8mA	**Port 2 MII Transmit Data bit 1** Synchronous to the rising edge of TXCLK.
	FXMODE1			**FXMODE1** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as bit 1 of FXMODE. FXMODE [1:0] Interface 00_B , Both Port0 & Port1 are TP port 01_B , Port0 is TP port and Port1 is FX port 10_B , Port0 is TP port and Port1 is FX port (converter mode) 11_B , Both Port0 & Port1 are FX port

Table 5 Port 2 (MII/RMII/GPSI) Interface (17 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
85	P2TXD2	I/O	TTL, PD, 8mA	**Port 2 MII Transmit Data bit 2** Synchronous to the rising edge of TXCLK.
	P2BUSMD0			**P2BUSMD0** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as P2BUSMD0.
84	P2TXD3	I/O	PD, 8mA	**Port 2 MII Transmit Data bit 3**
	P2BUSMD1			**P2BUSMD1** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as P2BUSMD1. BUSMD[1:0] Interface 00_B , MII(Default) 01_B , RMII 10_B , GPSI 11_B , HDLC
88	P2TXEN	I/O	PD, 8mA	**Port 2 MII Transmit Enable** Synchronous to the rising edge of TXCLK
	DISBP			**DISBP. Disable Back Pressure** 0_B , Enable back-pressure(Default) 1_B , Disable back-pressure
108	P2RXD_3	I	TTL, PD	**Port 2 MII Receive Data bit 3 ~ 0**
107	P2RXD_2			
106	P2RXD_1			
105	P2RXD_0			
104	P2RXDV	I	TTL, PD	**Port 2 MII Receive Data Valid**
93	P2COL	I	TTL, PD	**Port 2 MII Collision input**
92	P2CRS	I	TTL, PD	**Port 2 MII Carrier Sense**
103	P2RXCLK	I	TTL, PD	**Port 2 MII Receive Clock Input**
90	P2TXCLK	I	TTL, PD	**Port 2 MII Transmit Clock Input**
96	P2LINKF	I	TTL, PU	**P2LINKF** This pin will be used to input the Link Status of Port2 1_B , Link Fail
95	P2SPDTEN	I	TTL, PD	**P2SPDTEN** This pin will be used as Port 2 Speed Status input 1_B , 10M
94	P2DPHALF	I	TTL, PD	**P2DPHALF** This pin will be used as Port 2 Duplex Status input 1_B , Half Duplex

Table 6 Port 1 Alternative MII Port Interface (17 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
56	P1TXD0/CHIPID_0	I/O	TTL, PD, 8mA	**Port 1 MII Transmit Data bit 0/Chip ID Bit 0** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as CHIPID_0.This pin will become P1RXD0 if P1BUSMD[1:0] is 11. Synchronous to the rising edge of TXCLK.
55	P1TXD1/CHIPID_1	I/O	TTL, PD, 8mA	**Port 1 MII Transmit Data bit 1/Chip ID Bit 1** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as CHIPID_1.This pin will become P1RXD1 if P1BUSMD[1:0] is 11. Synchronous to the rising edge of TXCLK.
54	P1TXD2/P1BUSMD0	I/O	TTL, PU, 8mA	**Port 1 MII Transmit Data bit 2/ Port 1 Bus Mode bit 0** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as P1BUSMD0.This pin will become P1RXD2 if P1BUSMD[1:0] is 11. Synchronous to the rising edge of TXCLK. P1BUSMD[1:0] Interface 00_B , MII (Power Down TX Phy) 01_B , RMII (Power Down TX Phy) 10_B , GPSI (Power Down TX Phy) 11_B , TP/FX (default)
53	P1TXD3/P1BUSMD1	I/O	TTL, PU, 8mA	**Port 1 MII Transmit Data bit 3/ Port 1 Bus Mode bit 1** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as P1BUSMD1.This pin will become P1RXD3 if P1BUSMD[1:0] is 11. Synchronous to the rising edge of TXCLK. P1BUSMD[1:0] Interface 00_B , MII (Power Down TX Phy) 01_B , RMII (Power Down TX Phy) 10_B , GPSI (Power Down TX Phy) 11_B , TP/FX (default)
59	P1TXEN	O	TTL, PD, 8mA	**Port 1 MII Transmit Enable** This pin will become P1RXDV if P1BUSMD[1:0] is 11. Synchronous to the rising edge of TXCLK
	IDLE_MODE			**IDEL_MODE** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as HDLC IDLE frame control mode. IDLE_MODE IDLE Pattern 0_B , FF_H(Default) 1_B , $7E_H$

Table 6 Port 1 Alternative MII Port Interface (17 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
83	P1RXD_3	I	TTL, PD	**Port 1 MII Receive Data bit 3 ~ 0** These pins will become P1TXD[3:0] if P1BUSMD[1:0] is 11
82	P1RXD_2			
81	P1RXD_1			
80	P1RXD_0			
60	P1RXDV	I	TTL, PD	**Port 1 MII Receive Data Valid** This pin will become P1TXEN if P1BUSMD[1:0] is 11
111	P1COL	I/O	TTL, PD	**Port 1 MII Collision input** This pin will become P1COL if P1BUSMD[1:0] is 11 and becomes an output pin
112	P1CRS	I/O	TTL, PD	**Port 1 MII Carrier Sense** This pin will become P1CRS if P1BUSMD[1:0] is 11 and becomes an output pin
61	P1RXCLK	I/O	TTL, PD	**Port 1 MII Receive Clock Input** This pin will become P1CRS if P1BUSMD[1:0] is 11 and becomes an output pin
58	P1TXCLK	I/O	TTL, PD	**Port 1 MII Transmit clock Input** This pin will become P1CRS if P1BUSMD[1:0] is 11 and becomes an output pin.
117	P1LINKF	I	TTL, PU	**Port 1 Link Fail Status** This pin will be used to input the Link Status of Port1 if Port1 is not connected to internal PHY 1_B , Link Fail
120	P1SPDTEN	I	TTL, PD	**Port 1 Speed Status** This pin will be used as Port 1 Speed Status input if Port1 is not connected to internal PHY 1_B , 10M
121	P1DPHALF	I	TTL, PD	**Port 1 Duplex Status** This pin will be used as Port 2 Duplex Status input if Port1 is not connected to internal PHY 1_B , Half Duplex

Table 7 LED Interface (13 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
113	LNKACT_0	I/O	TTL PD 8mA	**PORT0 Link & Active LED/Link LED.** If LEDMODE_0 is 1, this pin indicates both link status and RX/TX activity. When link status is LINK_UP, LNKACT_0 will be turned on. While PORT0 is receiving/transmitting data, LNKACT_0 will be off for 100ms and then on for 100ms. If LEDMODE_0 is 0, this pin only indicates RX/TX activity.
	LED_DATA_0			**Port0 LED DATA**
	LEDMODE_0			**LED mode for LINK/ACT LED of PORT0.** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as LEDMODE_0.
114	LNKACT_1	I/O	TTL PD 8mA	**PORT1 Link & Active LED/Link LED.** If LEDMODE_2 is 1, this pin indicates both link status and RX/TX activity. When link status is LINK_UP, LNKACT_1 will be turned on. While PORT1 is receiving/transmitting data, LNKACT_1 will be off for 100ms and then on for 100ms. If LEDMODE_2 is 0, this pin only indicates RX/TX activity.
	LED_DATA_1			**Port1 LED DATA**
	LEDMODE_1			**LED mode DUPLEX/COL LED of PORT0 & PORT1.** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as LEDMODE_1. If LEDMODE_1 is 1, DUPCOL[1:0] will display both duplex condition and collision status. If LEDMODE_1 is 0, only collision status will be displayed.
30	LEDMODE_2	I	TTL PD	**LED mode for LINK/ACT LED of PORT1** 0_B , ACT 1_B , LINK/ACT
124	DUPCOL_0	I/O	TTL PD 8mA	**PORT0 Duplex LED** If LEDMODE_1 is 1, this pin indicates both duplex condition and collision status. When FULL_DUPLEX, this pin will be turned on for PORT0. When HALF_DUPLEX and no collision occurs, this pin will be turned off. When HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and then on for 100ms. If LEDMODE_1 is 0, this pin indicates collision status. When in HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and turn on for 100ms.
	LED_COL_0			**Port0 Collision LED**
	DIS_LEARN			**Disable Address Learning.** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as DIS_LEARN. If DIS_LEARN is 1, MAC address learning will be disabled.

Table 7 LED Interface (13 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
125	DUPCOL_1 /LED_COL_1	I/O	TTL PU 8mA	**PORT1 Duplex** If LEDMODE_1 is 1, this pin indicates both duplex condition and collision status. When FULL_DUPLEX, this pin will be turned on for PORT1. When HALF_DUPLEX and no collision occurs, this pin will be turned off. When HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and then on for 100ms. If LEDMODE_1 is 0, this pin indicates collision status. When HALF_DUPLEX and a collision occurs, this pin will be off for 100ms and turn on for 100ms.
122	LDSPD_0	I/O	TTL PU 8mA	**PORT0 Speed LED** Used to indicate speed status of PORT0. When operating in 100Mbps this pin is turned on, and when operating in 10Mbps this pin is off.
	RDNT_EN			**Enable Redundant Capability** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as RDNT_EN. If RDNT_EN is 0, "REDUNDANT" capability will be disabled. For TS1000 application this pin should have a value of 0.
123	LDSPD_1	I/O	TTL PU 8mA	**PORT1 Speed LED** Used to indicate speed status of PORT1. When operating in 100Mbps this pin is turned on, and when operating in 10Mbps this pin is off.
	LED_FIBER_SD			**LED_FIBER_SD** Used to indicate signal status of PORT1 when ADM6993/X is operating in converter mode.
	SNP_EN			**Enable Snooping Mode** During power on reset, value will be latched by ADM6993/X at the rising edge of RESETL as SNP_EN. If SNP_EN is 0, "SNOOPING" capability will be disabled.
1	LED_LINK_1	O	TTL 8mA	**PORT[1:0] Link LED** These pins indicate link status. When link status is LINK_UP, these pins will be turned on for relevant port.
128	LED_LINK_0			
3	LED_FULL_1	O	TTL 8mA	**PORT[1:0] Full Duplex LED** These pins indicate current duplex condition of PORT0. When FULL_DUPLEX, these pins will be turned on for relevant port. When HALF_DUPLEX these pins will be turned off for relevant port.
2	LED_FULL_0			
4	LED_LPBK	O	TTL 8mA	**Loop Back Test LED** While performing loop back test this pin is turned on.

Table 8 EEPROM Interface (4 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
7	EEDO	I	TTL PU	**EEPROM Data Output** Serial data input from EEPROM. This pin is internal pull-up.
12	EECS	I/O	PD 4mA	**EEPROM Chip Select** This pin is active high chip enabled for EEPROM. When RESETL is low, it will be tristate.
11	EECK	I/O	TTL PU 4mA	**Serial Clock** This pin is the EEPROM clock source. When RESETL is low, it will be tristate. This pin is internal pull-up.
8	EEDI	I/O	TTL PU 4mA	**EEPROM Serial Data Input** This pin is the output for serial data transfer. When RESETL is low, it will be tristate.

Table 9 Configuration Interface (28 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
16	P0_ANDIS	I	TTL PD	**Auto-Negotiation Disable for PORT0** 0_B **E**, Enable 1_B **D**, Disable
17	P0_RECHALF	I	TTL PD	**Recommend Half Duplex Communication for PORT0** 0_B **F**, Full 1_B **H**, Half
18	P0_REC10	I	TTL PD	**Recommend 10M for PORT0** 0_B **100**, 100M 1_B **10**, 10M
19	P0_FCDIS	I	TTL PD	**Flow Control Disable for PORT0** 0_B **E**, Enable 1_B **D**, Disable
22	P1_ANDIS	I	TTL PD	**Auto-Negotiation Disable for PORT1** 0_B **E**, Enable 1_B **D**, Disable
23	P1_RECHALF	I	TTL PD	**Recommend Half Duplex Communication for PORT1** 0_B **F**, Full 1_B **H**, Half
24	P1_REC10	I	TTL PD	**Recommend 10M for PORT1** 0_B **100**, 100M 1_B **10**, 10M
25	P1_FCDIS	I	TTL PD	**Flow Control Disable for PORT1** 0_B **E**, Enable 1_B **D**, Disable
63	P2_FCDIS	I	TTL PD	**Flow Control Disable for PORT2** 0_B **E**, Enable 1_B **D**, Disable

Table 9 Configuration Interface (28 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
67	XOVEN	I	TTL PD	**Auto-MDIX Enable.** 0_B **D**, Disable 1_B **E**, Enable
68	P0_MDI	I	TTL PU	**MDI/MDIX Control for PORT0** This setting will be ignore if enable Auto-MDIX. 0_B **MDIX**, MDIX 1_B **MDI**, MDI
21, 20	FTPR_MODE[1:0	I	TTL PD	**Fault Propagation Mode** 00_B **R**, Reserved 01_B **Fx**, FX fail -> UTP fail, UTP fail -> FX transmit FEFI 10_B **R**, Reserved 11_B **D**, Disable
99	LPBK_P0	I	TTL PD	**Enable Loop Back Test for PORT0** 0_B **D**, Disable 1_B **E**, Enable
98	LPBK_P1	I	TTL PD	**Enable Loop Back Test for PORT1** 0_B **D**, Disable 1_B **E**, Enable
97	LPBK_P2	I	TTL PD	**Enable Loop Back Test for PORT2** 0_B **D**, Disable 1_B **E**, Enable
101	CHIP_DIS	I	TTL PD	**Chip Disable** 0_B **D**, Disable 1_B **E**, Enable
100	CAS_DIS	O	TTL 4mA	**Disable Cascaded Chip** 0_B **D**, Disable 1_B **E**, Enable
102	LPT_DIS	I	TTL PD	**Link Pass Through Disable** 0_B **E**, Enable 1_B **D**, Disable
29	BYPASS_PAUSE	I	TTL PD	**Bypass Frame** The destination address is reserved IEEE MAC address 0_B **D**, Disable 1_B **E**, Enable

Table 10 Ground/Power Interface (27 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
42, 48	GNDTR	GND, A		**Ground** Used by AD receiver/transmitter block.
39, 51	VCCA2	PWR, A		**2.5 V used for Analogue block**
45	VCCAD	PWR, A		**3.3 V used for TX line driver**

Table 10 Ground/Power Interface (27 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
36	GNDBIAS	GND, A		**Ground used by digital substrate**
38	VCCBIAS	PWR, A		**3.3 V used for bios block**
33	GNDPLL	GND, A		**Ground used by PLL**
32	VCCPLL	PWR, A		**2.5 V used for PLL**
13, 52, 64, 89, 109, 110	GNDIK	GND, D		**Ground used by digital core and pre-driver**
9, 10, 57, 91, 115, 116	VCCIK	PWR, D		**2.5 V used for digital core and pre-driver**
77, 118, 119	GNDO	GND, D		**Ground used by digital pad**
79, 126, 127	VCC3O	PWR, D		**3.3 V used for digital pad.**

Table 11 Miscellaneous (14 Pins)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
6	$\overline{\text{INT}}$	O	TTL OD 4mA	**Interrupt** This pin will be used to interrupt external management device. This is a low active and open drain pin.
15	SDIO	I/O	TTL PU 8mA	**Serial Management Data** This pin is in/out to PHY. When RESETL is low, this pin will be tristate.
14	SDC	I	TTL 8mA	**Serial Management Data Clock**
78	CKO25M	O	TTL PU 8mA	**50M output for RMII and 25M Clock output for others**
34	CONTROL	AO		**FET Control Signal** The pin is used to control FET for 3.3 V to 2.5 V regulator.
37	RTX	A		**TX Resistor**
35	VREF	A		**Analog Power Failure Detected**
26	RC	I	TTL ST	**RC Input for Power On Reset** ADM6993/X sample pin RC as RESETL with the clock input from pin XI.
27	XI	AI		**25M Crystal Input** 25M Crystal Input. Variation is limited to +/- 50ppm.

Table 11 Miscellaneous (14 Pins) (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
28	XO	AO		**25M Crystal Output** When connected to oscillator, this pin should left unconnected.
5, 31, 62, 65, 66, 69, 70, 71, 72, 73, 74, 75, 76	NC			**No Connection**

2.4 Port 2 MII/RMII/GPSI/HDLC Interfaces Comparison

Table 12 Port 2 MII/RMII/GPSI/HDLC Interfaces Comparison

Pin No.	MII	RMII	GPSI	HDLC
87	P2TXD0(O)	P2TXD0(O)	P2TXD0(O)	P2TXD0(O)
86	P2TXD1(O)	P2TXD1(O)		
85	P2TXD2(O)			
84	P2TXD3(O)			
88	P2TXEN(O)	P2TXEN(O)	P2TXE(O)	
No Support	P2TXER(O)			
90	P2TXCLK(I)		P2RXCLK(I)	P2RXCLK(I)
105	P2RXD0(I)	P2RXD0(I)	P2RXD0(I)	P2RXD0(I)
106	P2RXD1(I)	P2RXD1(I)		
107	P2RXD2(I)			
108	P2RXD3(I)			
104	P2RXDV(I)	P2CRS_DV(I)	P2RXE/CRS(I)	
No Support	P2RXER(I)	P2RXER(I)		
93	P2COL(I)		P2COL(I)	
92	P2CRS(I)			
103	P2RXCLK(I)	P2REFCLK(I)	P2RXCLK(I)	P2RXCLK(I)
Port Status				
96	P2LINKF(I)	P2LINKF(I)	P2LINKF(I)	P2LINKF(I)='0'
95	P2SPDTEN(I)	P2SPDTEN(I)	P2SPDTEN(I)	
94	P2DPHALF(I)	P2DPHALF(I)	P2DPHALF(I)	

ADM6993/X doesn't provide MDC/MDIO to access external PHY, but provides PxLINKF, PxSPDTEN, and PxDPHALF to update MAC status from external PHY LINK/SPEED/DUPLEX LED pin.PxLINKF, Input = 1_B means unlink, 0_B means link.PxSPDTEN, Input = 1_B means 10Mbps, 0_B means 100Mbps.PxDPHALF, Input = 1_B means Half Duplex, 0_B means Full Duplex.

3 Function Description

The ADM6993/X integrates a two 100Base-X physical layer device (PHY), two complete 10Base-T modules, a 3-port 10/100 switch controller and memory into a single chip for both 10 Mbps and 100 Mbps Ethernet switch operations. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full-Duplex or Half-Duplex mode in both 10 Mbps and 100 Mbps operations. Operation modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The ADM6993/X consists of four major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in 6Kx64 SSRAM

3.1 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- 100Base-X physical medium dependent (PMD)

The 10Base-T section of the device implements the following functional blocks:

- 10Base-T physical layer signaling (PLS)
- 10Base-T physical medium attachment (PMA)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

The interfaces used for the communication between the PHY block and the switch core is a MII interface.

An Auto MDIX function is supported. This function can be Enabled/Disabled by using the hardware pin. A digital approach for the integrated PHY of the ADM6993/X has been adopted.

3.2 Auto Negotiation and Speed Configuration

3.2.1 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operations supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM6993/X supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

The auto negotiation function within the ADM6993/X can be controlled either by internal register access or by the use of configuration pins. If disabled, auto negotiation will not occur until software enables bit 12 in MII Register 0. If auto negotiation is enabled, the negotiation process will commence immediately.

When auto negotiation is enabled, the ADM6993/X transmits the abilities programmed into the auto negotiation advertisement register at address 04_H via FLP bursts. Any combination of 10 Mbps, 100 Mbps, half duplex, and full duplex modes may be selected. Auto negotiation controls the exchange of configuration information. Upon successfully auto negotiating, the abilities reported by the link partner are stored in the auto negotiation link partner ability register at address 05_H.

The contents of the “auto negotiation link partner ability register” are used to automatically configure the highest performance protocol between the local and far-end nodes. Software can determine which mode has been configured by auto negotiation, by comparing the contents of register 04_H and 05_H and then selecting the technology whose bit is set in both registers of highest priority relative to the following list:

1. 100Base-TX full duplex (highest priority)
2. 100Base-TX half duplex
3. 10Base-T full duplex
4. 10Base-T half duplex (lowest priority)

The basic mode control register at address 0_H controls the enabling, disabling and restarting of the auto negotiation function. When auto negotiation is disabled, the speed selection bit (bit 13) controls switching between 10 Mbps or 100 Mbps operation, while the duplex mode bit (bit 8) controls switching between full duplex operation and half duplex operation. The speed selection and duplex mode bits have no effect on the mode of operations when the auto negotiation enable bit (bit 12) is set.

The basic mode status register at address 1_H indicates the set of available abilities for technology types (bit 15 to bit 11), auto negotiation ability (bit 3), and extended register capability (bit 0). These bits are hardwired to indicate the full functionality of the ADM6993/X. The BMSR also provides status on:

- Whether auto negotiation is complete (bit 5)
- Whether the Link Partner is advertising that a remote fault has occurred (bit 4)
- Whether a valid link has been established (bit 2)

The auto negotiation advertisement register at address 4_H indicates the auto negotiation abilities to be advertised by the ADM6993/X. All available abilities are transmitted by default, but writing to this register or configuring external pins can suppress any ability.

The auto negotiation link partner ability register at address 05_H indicates the abilities of the Link Partner as indicated by auto negotiation communication. The contents of this register are considered valid when the auto negotiation complete bit (bit 5, register address 1_H) is set.

3.2.2 Speed Configuration

The twelve sets of four pins listed in **Table 13** configure the speed capability of each channel of the ADM6993/X. The logic states of these pins are latched into the advertisement register (register address 4_H) for auto negotiation

purpose. These pins are also used for evaluating the default value in the base mode control register (register 0_H) according to Table 13.

In order to make these pins with the same Read/Write priority as software, they should be programmed to 11111111_B in case a user wishes to update the advertisement register through software.

Table 13 Speed Configuration

Advertise all capability	Advertise single capability	Parallel detect follow IEEE std.	Auto Negoti-ation (Pin & EEPROM)	Speed (Pin & EEPROM)	Duplex (Pin & EEPROM)	Auto Negotiation	Advertise Capability				Parallel Detect Capability			
							10 0F	10 0H	10 F	10 H	10 0F	10 0H	10 F	10 H
1	0	0	1	X	X	1	1	1	1	1	1	0	1	0
1	0	1	1	X	X	1	1	1	1	1	0	1	0	1
1	1	0	1	X	X	1	1	0	0	0	1	0	0	0
1	1	1	1	X	X	1	1	0	0	0	0	1	0	0
0	0	0	1	1	1	1	1	1	1	1	1	0	1	0
0	0	1	1	1	1	1	1	1	1	1	0	1	0	1
0	1	0	1	1	1	1	1	0	0	0	1	0	0	0
0	1	1	1	1	1	1	1	0	0	0	0	1	0	0
0	0	X	1	1	0	1	0	1	0	1	0	1	0	1
0	1	X	1	1	0	1	0	1	0	0	0	1	0	0
0	0	0	1	0	1	1	0	0	1	1	0	0	1	0
0	0	1	1	0	1	1	0	0	1	1	0	0	0	1
0	1	0	1	0	1	1	0	0	1	0	0	0	1	0
0	1	1	1	0	1	1	0	0	1	0	0	0	0	1
0	X	X	1	0	0	1	0	0	0	1	0	0	0	1
X	X	X	0	1	1	0	1	—	—	—	—	—	—	—
X	X	X	0	1	0	0	—	1	—	—	—	—	—	—
X	X	X	0	0	1	0	—	—	1	—	—	—	—	—
X	X	X	0	0	0	0	—	—	—	1	—	—	—	—

3.3 Switch Functional Description

The ADM6993/X uses a “store & forward” switching approach for the following reason:

Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffer especially bridging between a server on a 100Mbps network and clients on a 10Mbps segment.

Store & forward switches improve overall network performance by acting as a “network cache”

Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.3.1 Basic Operation

The ADM6993/X receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within the same VLAN group, if appropriate. If the destination address is not found in the address table, the ADM6993/X treats the packet as a broadcast packet and forwards the packet to the other ports which in the same VLAN group.

The ADM6993/X automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the table.

3.3.2 Address Learning

The ADM6993/X uses a hash algorithm to learn the MAC address and can learn up to 2K MAC addresses. Address is stored in the Address Table. The ADM6993/X searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

If the SA was not found in the Address Table (a new address), the ADM6993/X waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then aging value of each corresponding entry will be reset to 0.

When the DA is PAUSE command, then the learning process will be disabled automatically by ADM6993/X.

3.3.3 Address Recognition and Packet Forwarding

The ADM6993/X forwards the incoming packets between bridged ports according to the Destination Address (DA) as below. All the packet forwarding will check VLAN first. A forwarding port must be within the same VLAN as the source port.

1. If the DA is an UNICAST address and the address was found in the Address Table, the ADM6993/X will check the port number and acts as follows:
   a) If the port number is equal to the port on which the packet was received, the packet is discarded.
   b) If the port number is different, the packet is forwarded across the bridge.
2. If the DA is an UNICAST address and the address was not found, the ADM6993/X treats it as a multicast packet and forwards across the bridge.
3. If the DA is a Multicast address, the packet is forwarded across the bridge.
4. If the DA is PAUSE Command (01-80-C2-00-00-01), then this packet will be dropped by ADM6993/X. ADM6993/X can issue and learn PAUSE command.
5. ADM6993/X will forward by defaulted or filtering out the packet with DA of (01-80-C2-00-00-00), discarding the packet with DA of (01-80-C2-00-00-01), filtering out the packet with DA of (01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F), and forwarding the packet with DA of (01-80-C2-00-00-10 ~ 01-80-C2-00-00-FF) decided by EEPROM Reg.7_H.

3.3.4 Address Aging

Address aging is supported for topology changes such as an address moving from one port to the other. When this happens, the ADM6993/X internally has a 300 seconds timer will aged out (remove) the address from the address table. Aging function can be enabled/disabled by user. Normally, disabling aging function is for security purpose.

3.3.5 Buffers and Queues

The ADM6993/X incorporates transmitted queues and the receiving buffer area for the three ETHERNET ports. The receiving buffers as well as the transmitted queues are located within the ADM6993/X along with the switch fabric. The buffers are divided into 192 blocks of 256 bytes each. The queues of each port are managed according to each port's read/write pointer.

3.3.6 Back off Algorithm

The ADM6993/X implements the truncated exponential back off algorithm compliant to the IEEE802.3 CSMA/CD standard. ADM6993/X will restart the back off algorithm by choosing 0-9 collision counts. The ADM6993/X resets the collision counter after 16 consecutive retransmit trials.

3.3.7 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96-bits time. The value is 9.6μs for 10Mbps ETHERNET, and 960ns for 100Mbps fast ETHERNET. ADM6993/X provides the option of a 92-bit gap in EEPROM to prevent packet lost when Flow Control is turned off and clock P.P.M. value differs.

3.3.8 Illegal Frames

The ADM6993/X will discard all illegal frames such as runt packet (less than 64 bytes), oversize packet (greater than 1518 or 1522 bytes) and bad CRC. Dribbling packing with good CRC value will accept by ADM6993/X. In case of bypass mode enabled, ADM6993/X will support tagged up to 1522bytes, and untagged packets up to 1518 bytes. In case of non-bypass mode, ADM6993/X will support tagged packets up to 1522 bytes, and untagged packets up to 1518 bytes.

3.3.9 Half Duplex Flow Control

Back Pressure function is supported for half-duplex operation. When the ADM6993/X cannot allocate a receiving buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is enabled by the BPEN set during RESET asserting. An Infineon-ADMtek Co Ltd proprietary algorithm is implemented inside the ADM6993/X to prevent back pressure function causing HUB partitioned under heavy traffic environment and reduce the packet lost rate to increase the whole system performance.

3.3.10 Full Duplex Flow Control

When full duplex port runs out of its receiving buffer, a PAUSE packet command will be issued by ADM6993/X to notice the packet sender to pause the transmission. This frame based flow control is totally compliant to IEEE 802.3x. ADM6993/X can issue or receive pause packet.

3.3.11 Broadcast Storm Filter

If Broadcast Storming filter is enable, the broadcast packets over the rising threshold within 50 ms will be discarded by the threshold setting. See EEPROM Reg.5_H.

Broadcast storm mode after initial:

Time interval: 50 ms

The max. packet number = 7490 in 100Base, 749 in 10Base

Table 14 Port Rising/Falling Threshold

Per Port Rising Threshold				
	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

Per Port Falling Threshold				
	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

Table 15 Drop Scheme for each queue

Drop Scheme for each queue				
Discard Mode Utilization	00	01	10	11
00	0%	0%	0%	0%
01	0%	0%	25%	50%
11	0%	25%	50%	75%

3.3.12 Auto TP MDIX Function

At normal application which Switch connect to NIC card is by one by one TP cable. If Switch connects other device such as another Switch must by two way. First one is Cross Over TP cable. Second way is to use extra RJ45 which crossover internal TX+- and RX+- signal. By second way customers can use one by one cable to connect two Switch devices. All these efforts need extra cost and are not good solutions. ADM6993/X provides Auto MDIX function which can adjust TX+- and RX+- at correct pin. Users can use one by one cable between ADM6993/X and other device either switches or NICs.

3.4 Converter Functional Description

3.4.1 Fault Propagation

The ADM6993/X Media Converter incorporates a Fault Propagation feature, which allows indirect sensing of a Fiber Link Loss via the 10/100Base-TX UTP connection. Whenever the ADM6993/X Media Converter detects a Link Loss condition on the Receive fiber (Fiber LNK OFF), it disables its UTP link pulse so that a Link Loss condition will be sensed on the UTP port to which the ADM6993/X Media Converter is connected. This link loss can then be sensed and reported by a Network Management agent in the remote UTP port's host equipment. This feature will affect the ADM6993/X UTP LNK LED.

The ADM6993/X Media Converter also incorporates a Far End Fault feature, which allows the stations on both ends of a pairs of fibers to be informed when there is a problem with one of the fibers. Without Far End Fault, it is impossible for a fiber interface to detect a problem that affects only its Transmitting fiber.

When Far End Fault is supported and enabled, a loss of received signal (link) will cause the transmitter to generate a Far End Fault pattern in order to inform the device at the far end of the fiber pair that a fault has occurred. Unless Fiber Link Loss occurred, if the UTP port link failed, the ADM6993/X Media Converter will also generate a Far End Fault pattern in order to inform the device at the far end of the fiber pair that a fault has occurred.

3.4.2 Redundant Link

The ADM6993/X Media Converter incorporates a Redundant Link feature, which allows designing a cost-effective Redundant TX FX Media Converter to provide a more reliable fiber link.

At converter mode (FXMODE[1:0]=10 and RDNT_EN=1), pin CAS_DIS of primary ADM6993/X connects to pin CHIP_DIS of secondary ADM6993/X.

- While FX port works well, pin CAS_DIS will output “1” to disable 2nd ADM6993/X
- While FX fiber link loss or the remote fault detection happens, pin CAS_DIS will output “0” to enable 2nd ADM6993/X.
- While ADM6993/X disable, TX port will become Hi-Z state.

3.4.3 Loop-Back mode

The ADM6993/X Media Converter incorporates a Loop-Back mode, which allows users or ISP to diagnose the local or the remote network equipment. The loop-back is used to check the operation of the switch and ensure the device's connection on the media side.

- While LPBK_P0=1, the received data from Port 1/Port 2 will be routed through the receiving path back to the transmitting path on Port 0 MII interface (between switch core and embedded port 0 PHY).
- While LPBK_P1=1, the received data from Port 0/Port 2 will be routed through the receiving path back to the transmitting path on Port 1 MII interface (between switch core and embedded port 1 PHY).
- While LPBK_P2=1, the received data from Port 0/Port 1 will be routed through the receiving path back to the transmitting path on Port 2 MII interface.

Note: The address learning, packet filter, CRC check, length check and loop-back function are not performed in snooping mode.

3.4.4 Snooping mode

The ADM6993/X Media Converter incorporates a Snooping mode, which allows packets perform cut-through between TX<-->FX while both TX and FX ports operate on 100M Full mode. On snooping mode, the packets will not enter the switch core to perform store and forward mechanisms.

- While SNP_EN=1, the ADM6993/X TX FX Media Converter will act TX<-->FX bridge while both TX and FX ports operate on 100M mode.
- While SNP_EN=0, the ADM6993/X TX FX Media Converter will force all packets to enter the switch core to perform store and forward mechanisms.

3.4.5 Fiber_SD LED

The ADM6993/X Media Converter provides a Fiber_SD LED on original LDSPD_1 pin. Fiber_SD is used to indicate the signal status of the fiber port.

3.5 Serial Management Interface (SMI) Register Access

The SMI consists of two pins, management data clock (SDC) and management data input/output (SDIO). The ADM6993/X is designed to support an SDC frequency up to 25 MHz. The SDIO line is bi-directional and may be shared with other devices.

The SDIO pin requires a 1.5 KΩ pull-up which, during idle and turn around periods, will pull SDIO to a logic “1“ state. ADM6993/X requires a single initialization sequence of 35 bits of preamble following power-up/hardware reset. The first 35 bits are preamble consisting of 35 contiguous logic “1“bits on SDIO and 35 corresponding cycles on SDC. Following preamble, the start-of-frame field is indicated by a <01> pattern. The next field signals the operation code (OP): <10> indicates read from management register operation, and <01> indicates write to management register operation. The next field is management register address. It is 10 bits wide and the most significant bit is transferred first.

Table 16 SMI Read/Write Command Format

Operation	Preamble	SFD	OP	CHIPID[1:0]	Unused	Register Address	TA	Data
Read	35”1”s	01	10	2 bits	000	5 bits Address	Z0	32 bits Data Read
Write	35”1”s	01	01	2 bits	000	5 bits Address	10	32 bits Data Write

During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the SDIO to avoid contention. Following the turnaround time, a 32-bit data stream is read from or written into the management registers of the ADM6993/X.

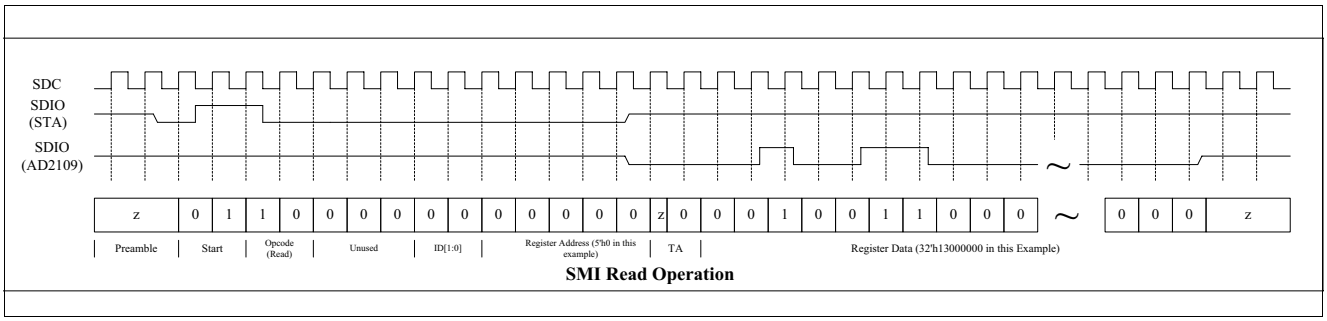


Figure 3 SMI Read Operation

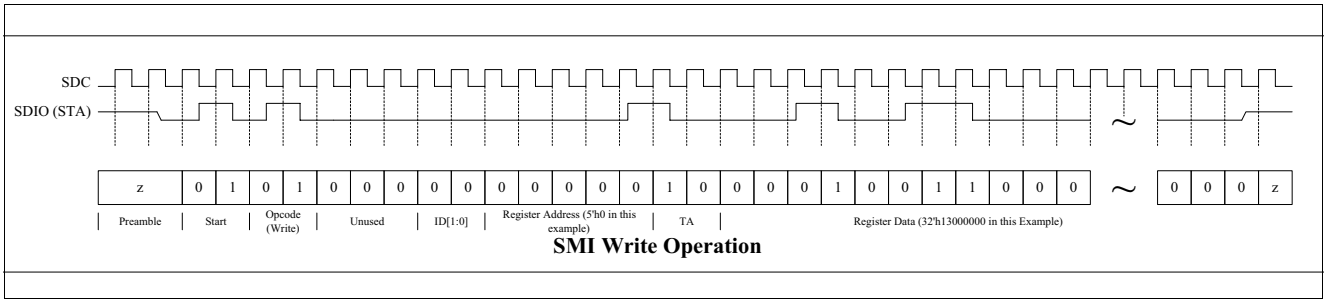


Figure 4 SMI Write Operation

3.5.1 Preamble Suppression

The SMI of ADM6993/X supports a preamble suppression mode. If the station management entity (i.e. MAC or other management controller) determines that all devices which are connected to the same SDC/SDIO in the system support preamble suppression, then the station management entity needs not generate preamble for each management transaction. The ADM6993/X requires a single initialization sequence of 35 bits of preamble following power-up/hardware reset. This requirement is generally met by pulling-up the resistor of SDIO. While the ADM6993/X will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required.

When ADM6993/X detects that there is address match, then it will enable Read/Write capability for external access. When an address is mismatched, then ADM6993/X will tri-state the SDIO pin.

3.5.2 Read EEPROM Register via SMI Register

The following 2 steps are for reading the data of EEPROM Register via SMI Interface.

Write the address of the desired EEPROM Register and READ command to SMI Register 04_H

EX. <35”1”s><01><01><00000><00100><10><000 0000000 000001 0000000000000000>

CMD ADDRESS DATA

Read ADM6993/X Internal EEPROM mapping Reg.1_H. Read SMI Register 04. The data of desired EEPROM Register will be in bit [15:0].

EX. <35”1”s><01><10><00000><00100><z0><000 0000000 000000 1000001000001111>

CMD ADDRESS DATA

Get ADM6993/X Internal EEPROM mapping Reg.1_H. value 820f.

3.5.3 Write EEPROM Register via SMI Register

To write data into desired EEPROM Register, write the address of the EEPROM Register.

EX. <35”1”s><01><01><00000><00100><10><001 0000000 000001 1000001000001111>

CMD ADDRESS DATA

Write ADM6993/X Internal EEPROM mapping Reg.1_H. with value 820f.

3.6 HDLC Controller

The ADM6993/X has an interface to HDLC. The main function is to forward Ethernet Packet from local LAN to WAN.

3.6.1 HDLC Frame Receiver

A received packet consists of an opening flag, data bytes, a 16-bit CRC, and a closing flag. The received cycle starts with the detection of data after the opening flag in the packet. After a flag is detected, the HDLC checks the data bit stream for minimum (less then 62 bytes including CRC-16) and maximum (more than 1534 bytes including CRC-16) packet lengths, zero deletion, abort characters, and idle characters. HDLC Controller will remove CRC-16 2 byte in the received packet before writing to BUFFER.

Clocking The HDLC Controller Receiver gets data from HDLC_RXD at the positive edge of HDLC_RXCLK.

Flag Detection The HDLC supports the following received flag (01111110) sequence:

Multiple flags between packets

(.....0111111001111110.....)

A flag shared as the closing and opening flags between two packets

(.....Data CRC 01111110 Data.....)

A shared zero between flags

(.....011111101111110.....)

All incoming flags are ignored and discarded by the HDLC. The first bit received, which is not a part of the flag character, signifies the start of the packet. If a flag is received during a packet, it indicates the end of the packet.

The CRC is checked (the last two bytes of the packet), and a decision is generated to forward or not.

Zero Deletion Each bit received between the opening and closing flag is checked for zero bit insertion. A zero that follows five contiguous ones is discarded from the incoming bit stream. HDLC is defined this feature to avoid the occurrence of flags in user data field.

Cyclic Redundancy Check (CRC) The frame check sequence (FCS) consists of 16 bits immediately preceding the closing flag. The 16-bit FCS detects data errors through the use of a cycle redundancy check (CRC) code. The CRC is generated from the incoming data and compared against the received CRC (remainder), carried in the FCS field of the packet. If the comparison does not match because of a bit error or burst error, the HDLC discards the packet by flushing the memory buffer regions, and waits for the next packet to be received. The CRC check polynomials are as follows:

CRC-16: $X^{16}+X^{12}+X^5+1$

3.6.2 HDLC Frame Transmitter

A transmitted packet consists of an opening flag, data bytes, 16-bit CRC, and a closing flag. The transmitter timing is asynchronous in relationship with the receive timing.

Clocking The HDLC Controller Transmitter send data to HDLC_TXD at the positive edge of external HDLC_TXCLK.

Flag Generation The HDLC Controller generates either (01111110) or multiple flags (0111111001111110...), depending on the packet data present in the BUFFER stored by LAN interface.

Zero Insertion The data in the packet read from the BUFFER is checked for the number of contiguous ones prior to the transmission. A zero is inserted into the transmitted bit stream after five contiguous ones are detected, excluding Flags or Abort characters. By this, HDLC can avoid the confusion between flag and data, which has the same value with flag.

Cyclic Redundancy Check (CRC) Generation The Frame Check Sequence (FCS) consists of 16 bits immediately preceding the closing flag. The 16-bit FCS detects data errors through the use of a cycle redundancy check (CRC) code. When all user data is transmitted, the calculated value is transmitted after the last data byte, and encloses the frame with a closing flag. The CRC check polynomials are as follows:

CRC-16: $X^{16}+X^{12}+X^{5}+1$

3.7 Reset Operation

The ADM6993/X can be reset either by hardware or software. A hardware reset is accomplished by applying a negative pulse, with the duration of at least 100 ms to the RC pin of the ADM6993/X during normal operation to guarantee internal SSRAM is reset well.

Hardware reset operation samples the pins and initializes all registers to their default values. This process includes re-evaluation of all hardware configurable registers. A hardware reset affects all embedded PHYs in the device.

Software reset can reset all embedded PHY and it does not latch the external pins nor reset the registers to their respective default value. This can be achieved by writing FF to EEPROM Reg.$3F_H$.

Logic levels on several I/O pins are detected during a hardware reset to determine the initial functionality of ADM6993/X. Some of these pins are used as output ports after reset operation.

Care must be taken to ensure that the configuration setup will not interfere with normal operations. Dedicated configuration pins can be tied to VCC or Ground directly. Configuration pins multiplexed with logic level output functions should be either weakly pulled up or weakly pulled down through external resistors.

3.7.1 Write EEPROM Register via EEPROM Interface

To write data into desired EEPROM Register via EEPROM interface:

If external EEPROM 93C46 or 93C66 exists, any WRITE programming instructions after EWEN instruction be executed can be updated effectively on EEPROM content and ADM6993/X internal mapping register on the same time.

If no external EEPROM exists, EECS/EECK/EEDI must be kept tri-state at least 100ms after hardware reset. Any WRITE programming instructions after EWEN instruction be executed can be updated effectively on ADM6993/X internal mapping register. Please notice that ADM6993/X can only identify 93C66-programming instructions if no external EEPROM.

4 Registers Description

This chapter describes descriptions of EEPROM Registers and SMI Registers.

4.1 EEPROM Registers

Table 17 EEPROM Register Map

Register	Bit 15-8		Bit 7-0		Default Value
00_H	Signature				4154_H
01_H	Port 0 Configuration				$820F_H$
02_H	Port 1 Configuration				$820F_H$
03_H	Port 2 Configuration				$820F_H$
04_H	TOS priority Map Low		VLAN priority Map Low		$F0F0_H$
05_H	Miscellaneous Configuration 0				C0
06_H	Miscellaneous Configuration 1				$82E8_H$
07_H	Miscellaneous Configuration 2				1480
08_H		Port 2 To Port Map	Port 1 To Port Map	Port 0 To Port Map	777_H
09_H	Filter Control Register 1		Filter Control Register 0		0_H
$0A_H$	Filter Control Register 3		Filter Control Register 2		0_H
$0B_H$	Filter Control Register 5		Filter Control Register 4		0_H
$0C_H$	Filter Control Register 7		Filter Control Register 6		0_H
$0D_H$	Filter Control Register 9		Filter Control Register 8		0_H
$0E_H$	Filter Control Register 11		Filter Control Register 10		0_H
$0F_H$	Filter Control Register 13		Filter Control Register 12		0_H
10_H	Filter Control Register 15		Filter Control Register 14		0_H
11_H	Filter Type Register 0				0_H
12_H	Filter Type Register 1				0_H
13_H	Filter Register 0				0_H
14_H	Filter Register 1				0_H
15_H	Filter Register 2				0_H
16_H	Filter Register 3				0_H
17_H	Filter Register 4				0_H
18_H	Filter Register 5				0_H
19_H	Filter Register 6				0_H
$1A_H$	Filter Register 7				0_H
$1B_H$	Filter Register 8				0_H
$1C_H$	Filter Register 9				0_H
$1D_H$	Filter Register 10				0_H
$1E_H$	Filter Register 11				0_H
$1F_H$	Filter Register 12				0_H
20_H	Filter Register 13				0_H
21_H	Filter Register 14				0_H

Table 17 EEPROM Register Map (cont'd)

Register	Bit 15-8	Bit 7-0	Default Value
22_H	Filter Register 15		0_H
23_H	PVID and PCID MASK of Port 0		1_H
24_H	PVID and PCID MASK of Port 0		0_H
25_H	PVID and PCID MASK of Port 1		1_H
26_H	PVID and PCID MASK of Port 1		0_H
27_H	PVID and PCID MASK of Port 2		1_H
28_H	PVID and PCID MASK of Port 2		0_H
29_H	Tag Rule 0		$F000_H$
$2A_H$	Tag Rule 0		$00FF_H$
$2B_H$	Tag Rule 1		$F000_H$
$2C_H$	Tag Rule 1		$00FF_H$
$2D_H$	Tag Rule 2		$F000_H$
$2E_H$	Tag Rule 2		$00FF_H$
$2F_H$	Tag Rule 3		$F000_H$
30_H	Tag Rule 3		$00FF_H$
31_H	Tag Rule 4		$F000_H$
32_H	Tag Rule 4		$00FF_H$
33_H	Tag Rule 5		$F000_H$
34_H	Tag Rule 5		$00FF_H$
35_H	Tag Rule 6		$F000_H$
36_H	Tag Rule 6		$00FF_H$
37_H	Tag Rule 7		$F000_H$
38_H	Tag Rule 7		$00FF_H$
39_H	Miscellaneous Configuration 2		0000_H
$3A_H$	Vendor Code[15:0]		0000_H
$3B_H$	Model Number [7:0]	Vendor Code [23:16]	0000_H
$3C_H$	Vendor Code[23:8]		0000_H

4.2 EEPROM Register Descriptions

Table 18 Registers Address Space

Module	Base Address	End Address	Note
EEPROM	00_H	$3C_H$	

Table 19 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
SR	Signature Register	00_H	36
PCR_0	Port Configuration Register 0	01_H	36
PCR_1	Port Configuration Register 1	02_H	37
PCR_2	Port Configuration Register 2	03_H	38
VLAN_TOS_PMR	VLAN(TOS) Priority Map Register	04_H	39
MC_0	Miscellaneous Configuration 0	05_H	40
MCR_1	Miscellaneous Configuration Register 1	06_H	41
MCR_2	Miscellaneous Configuration Register 2	07_H	42
PBVLAN_MR	Port Base VLAN port Map Register	08_H	42
PCFC_1_0	Packet Filter Control Register 1 and 0	09_H	44
TFTR_0	Filter Type Register 0	11_H	45
TFTR_1	Filter Type Register 1	12_H	45
FR_0	Filter Register 0	13_H	46
FR_1	Filter Register 1	14_H	46
FR_2	Filter Register 2	15_H	46
FR_3	Filter Register 3	16_H	46
FR_4	Filter Register 4	17_H	46
FR_5	Filter Register 5	18_H	46
FR_6	Filter Register 6	19_H	46
FR_7	Filter Register 7	$1A_H$	46
FR_8	Filter Register 8	$1B_H$	46
FR_9	Filter Register 9	$1C_H$	47
FR_10	Filter Register 10	$1D_H$	47
FR_11	Filter Register 11	$1E_H$	47
FR_12	Filter Register 12	$1F_H$	47
FR_13	Filter Register 13	20_H	47
FR_14	Filter Register 14	21_H	47
FR_15	Filter Register 15	22_H	47
PB_ID_0_0	Port Base VLAN ID and Mask 0 of Port 0	23_H	48
PB_ID_1_0	Port Base VLAN ID and Mask 1 of Port 0	24_H	48
PB_ID_0_1	Port Base VLAN ID and Mask 0 of Port 1	25_H	49
PB_ID_1_1	Port Base VLAN ID and Mask 1 of Port 1	26_H	49
PB_ID_0_2	Port Base VLAN ID and Mask 0 of Port 2	27_H	50
PB_ID_1_2	Port Base VLAN ID and Mask 1 of Port 2	28_H	50

Table 19 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
TPR_0_0	Tag Port Rule 0 Register 0	29_H	51
TPR_1_0	Tag Port Rule 1 Register 0	$2A_H$	51
TPR_0_1	Tag Port Rule 0 Register 1	$2B_H$	51
TPR_1_1	Tag Port Rule 1 Register 1	$2C_H$	52
TPR_0_2	Tag Port Rule 0 Register 2	$2D_H$	51
TPR_1_2	Tag Port Rule 1 Register 2	$2E_H$	52
TPR_0_3	Tag Port Rule 0 Register 3	$2F_H$	51
TPR_1_3	Tag Port Rule 1 Register 3	30_H	52
TPR_0_4	Tag Port Rule 0 Register 4	31_H	51
TPR_1_4	Tag Port Rule 1 Register 4	32_H	52
TPR_0_5	Tag Port Rule 0 Register 5	33_H	51
TPR_1_5	Tag Port Rule 1 Register 5	34_H	52
TPR_0_6	Tag Port Rule 0 Register 6	35_H	51
TPR_1_6	Tag Port Rule 1 Register 6	36_H	52
TPR_0_7	Tag Port Rule 0 Register 7	37_H	51
TPR_1_7	Tag Port Rule 1 Register 7	38_H	52
MCR_3	Miscellaneous Configuration Register 3	39_H	52
MCR_4	Miscellaneous Configuration 4	$3A_H$	54
MCR_5	Miscellaneous Configuration Register 5	$3B_H$	54
MCR_6	Miscellaneous Configuration Register 6	$3C_H$	54

The register is addressed wordwise.

Table 20 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)

Table 20 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

Table 21 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

4.2.1 EEPROM Register Format

Signature Register

SR	Offset	Reset Value
Signature Register	00_H	4154_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Signature															
ro															

Field	Bits	Type	Description
Signature	15:0	ro	**Signature** 4154_H **SIG**, Default (AT)

Port Configuration Register 0

PCR_0 | **Offset** | **Reset Value**

Port Configuration Register 0 | **01_H** | **$820F_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BM	**LTM**					**ANPD**	**ANSC**	**PBP**	**PR**			**DX**	**SP**	**ANE**	**FC**
rw	rw					rw	rw	rw	rw			rw	rw	rw	rw

Field	Bits	Type	Description
BM	15	rw	**Bypass Mode(TX packets same as RX)** 1_B **E**, Enable
LTM	14:10	rw	**Limit Total MAC** 00000_B, Disable $Others_B$, Maximum total MAC
ANPD	9	rw	**Port 0 Auto-Negotiation Parallel Detect Follow IEEE802.3** 0_B **B**, Both 1_B **H**, Half Only (Default)
ANSC	8	rw	**Port 0 Auto-Negotiation Advertise Single Capability** 0_B **E**, Expand(Default) 1_B **S**, Single
PBP	7	rw	**Port-base priority**
PR	6:4	rw	**Priority Rule/000** 000_B , port base priority 001_B , [TCP,TOS,TAG] 010_B , [TCP,TAG,TOS] 011_B , [TAG,TCP,TOS] 100_B , [TOS,TAG] 101_B , [TAG,TOS]
DX	3	rw	**Duplex** This bit is unused if corresponding port is not connected to internal PHY 0_B **HD**, Half Duplex 1_B **FD**, Full Duplex (Default)
SP	2	rw	**Speed** This bit is unused if corresponding port is not connected to internal PHY 0_B **10M**, 10Base-T 1_B **100M**, 100TX
ANE	1	rw	**Auto negotiation Enable** This bit is unused if corresponding port is not connected to internal PHY 0_B **D**, Disable Auto-negotiation 1_B **E**, Enable Auto-negotiation. (Default)
FC	0	rw	**802.3x Flow Control Command Ability**

Port Configuration Register 1

PCR_1 **Offset** **Reset Value**

Port Configuration Register 1 **02_H** **$820F_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BM	**LTM**					**ANPD**	**ANSC**	**PBP**	**PR**			**DX**	**SP**	**ANE**	**FC**
rw	rw					rw	rw	rw	rw			rw	rw	rw	rw

Field	Bits	Type	Description
BM	15	rw	**Bypass Mode(TX packets same as RX)** 1_B **E**, Enable
LTM	14:10	rw	**Limit Total MAC** 00000_B, Disable $Others_B$, Maximum total MAC
ANPD	9	rw	**Port 1 Auto-Negotiation Parallel Detect Follow IEEE802.3** 0_B **B**, Both 1_B **H**, Half Only (Default)
ANSC	8	rw	**Port 1 Auto-Negotiation Advertise Single Capability** 0_B **E**, Expand(Default) 1_B **S**, Single
PBP	7	rw	**Port-base priority**
PR	6:4	rw	**Priority Rule/000** 000_B , port base priority 001_B , [TCP,TOS,TAG] 010_B , [TCP,TAG,TOS] 011_B , [TAG,TCP,TOS] 100_B , [TOS,TAG] 101_B , [TAG,TOS]
DX	3	rw	**Duplex** This bit is unused if corresponding port is not connected to internal PHY 0_B **HD**, Half Duplex 1_B **FD**, Full Duplex (Default)
SP	2	rw	**Speed** This bit is unused if corresponding port is not connected to internal PHY 0_B **10M**, 10Base-T 1_B **100M**, 100TX
ANE	1	rw	**Auto negotiation Enable** This bit is unused if corresponding port is not connected to internal PHY 0_B **D**, Disable Auto-negotiation 1_B **E**, Enable Auto-negotiation. (Default)
FC	0	rw	**802.3x Flow Control Command Ability**

Port Configuration Register 2

PCR_2	Offset	Reset Value
Port Configuration Register 2	03_H	$820F_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BM	LTM					HM	HCM	PBP	PR			DX	SP	ANE	FC
rw	rw					??	??	rw	rw			rw	rw	rw	rw

Field	Bits	Type	Description
BM	15	rw	**Bypass Mode(TX packets same as RX)** 1_B **E**, Enable
LTM	14:10	rw	**Limit Total MAC** 00000_B, Disable $Others_B$, Maximum total MAC
HM	9	rw	**HDLC Mode** 0_B , By-pass pre/SFD 1_B , Remove pre/SFD(Default)
HCM	8	rw	**HDLC CRC Mode** 0_B , 16 bits CRC(Default) 1_B , 32 bits CRC
PBP	7	rw	**Port-base priority**
PR	6:4	rw	**Priority Rule/000** 000_B , port base priority 001_B , [TCP,TOS,TAG] 010_B , [TCP,TAG,TOS] 011_B , [TAG,TCP,TOS] 100_B , [TOS,TAG] 101_B , [TAG,TOS]
DX	3	rw	**Duplex** This bit is unused if corresponding port is not connected to internal PHY 0_B **HD**, Half Duplex 1_B **FD**, Full Duplex (Default)
SP	2	rw	**Speed** This bit is unused if corresponding port is not connected to internal PHY 0_B **10M**, 10Base-T 1_B **100M**, 100TX
ANE	1	rw	**Auto negotiation Enable** This bit is unused if corresponding port is not connected to internal PHY 0_B **D**, Disable Auto-negotiation 1_B **E**, Enable Auto-negotiation. (Default)
FC	0	rw	**802.3x Flow Control Command Ability**

VLAN(TOS) priority Map Register

VLAN_TOS_PMR **Offset** **Reset Value**

VLAN(TOS) Priority Map Register **04_H** **$F0F0_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	TAG7	TAG6	TAG5	TAG4	TAG3	TAG2	TAG1	TAG0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
IP7	15	rw	**Priority of the packet which the precedence field of IP header is 7**
IP6	14	rw	**Priority of the packet which the precedence field of IP header is 6**
IP5	13	rw	**Priority of the packet which the precedence field of IP header is 5**
IP4	12	rw	**Priority of the packet which the precedence field of IP header is 4**
IP3	11	rw	**Priority of the packet which the precedence field of IP header is 3**
IP2	10	rw	**Priority of the packet which the precedence field of IP header is 2**
IP1	9	rw	**Priority of the packet which the precedence field of IP header is 1**
IP0	8	rw	**Priority of the packet which the precedence field of IP header is 0**
TAG7	7	rw	**Priority of the packet which the priority field of TAG is 7**
TAG6	6	rw	**Priority of the packet which the priority field of TAG is 6**
TAG5	5	rw	**Priority of the packet which the priority field of TAG is 5**
TAG4	4	rw	**Priority of the packet which the priority field of TAG is 4**
TAG3	3	rw	**Priority of the packet which the priority field of TAG is 3**
TAG2	2	rw	**Priority of the packet which the priority field of TAG is 2**
TAG1	1	rw	**Priority of the packet which the priority field of TAG is 1**
TAG0	0	rw	**Priority of the packet which the priority field of TAG is 0**

Note: 0_B: low priority queue. Q0; 1_B: High priority queue. Q1. The weight ratio is 1:N. The default is Q0 for un-tag and none IP frame.

Miscellaneous Configuration 0

MC_0 **Offset** **Reset Value**

Miscellaneous Configuration 0 **05_H** **$C0_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM				VLAN	PL	PQR		MAD	SC	IPG	ECC	DBO	BSE	BST	
rw				rw	rw	rw		??	??	rw	??	??	rw	rw	

Field	Bits	Type	Description
DM	15:12	rw	**Discard Mode (drop scheme for each queue)**
VLAN	11	rw	**Enable Replace VLAN ID 0 &1 by PVID**
PL	10	rw	**Packet Length** 0_B , 1536 1_B , 1518
PQR	9:8	rw	**Priority Queue ratio** 00_B , 1:2 01_B , 1:4 10_B , 1:8 11_B , 1:16
MAD	7	rw	**Disable MCC_AVERAGE** 1_B **D**, Disable MCC Average
SC	6	rw	**SWCLK(Switch RXCLK to TXCLK for 7-wire)**
IPG	5	rw	**IPG Leveling** 0_B , 96BT(Default) 1_B , 92BT
ECC	4	rw	**XCRC** 0_B **XCRCCHK**, Enable CRC Check
DBO	3	rw	**Disable Back-Off** 1_B **D**, Disable Back-Off
BSE	2	rw	**Broadcast Storming Enable**
BST	1:0	rw	**Broadcast Storming Threshold[1:0]**

Miscellaneous Configuration Register 1

MCR_1	Offset	Reset Value
Miscellaneous Configuration Register 1	06_H	$82E8_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					**ET**	**CDP**	Res						**DFFE**	**DP**	**AD**
ro					rw	rw	ro						rw	rw	rw

Field	Bits	Type	Description
Res	15:11	ro	**Reserved**
ET	10	rw	**Enable TENLMT** 1_B **E**, Enable
CDP	9	rw	**Check The Destination Port is in the same VLAN Group** 1_B **E**, Enable
Res	8:3	ro	**Reserved**
DFFE	2	rw	**DISFEFI(Disable Far End Fault/0)**

Field	Bits	Type	Description
DP	1	rw	**Discard Packet after 16th Collision** 0_B **D**, Don't discard
AD	0	rw	**Aging Disable** 0_B **E**, Enable Aging

Miscellaneous Configuration Register2

MCR_2	Offset	Reset Value
Miscellaneous Configuration Register 2	**07_H**	**1480_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PFM1		**PFM2**		**PFM3**		**PFM4**		**CPN**		**LM2**		**LM1**		**LM0**	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
PFM1	15:14	rw	**Packet Filtering Mode for Received DA= 01 80 c2 00 00 10 ~ 01 80 c2 00 00 ff**
PFM2	13:12	rw	**Packet Filtering Mode for Received DA= 01 80 c2 00 00 02 ~ 01 80 c2 00 00 0f**
PFM3	11:10	rw	**Packet Filtering Mode for Received DA= 01 80 c2 00 00 01 and OPCODE!= PAUSE**
PFM4	9:8	rw	**Packet Filtering Mode for Received DA= 01 80 c2 00 00 00**
CPN	7:6	rw	**CPU Port Number**
LM2	5:4	rw	**Learning Mode of Port 2**
LM1	3:2	rw	**Learning Mode of Port 1**
LM0	1:0	rw	**Learning Mode of Port 0**

Note:

1. *Learning Mode: 00_B : group 0(default), 01_B : group 1, $1x_B$: according to bit 0 of received VID(bit 0 is used to set the learning group of untag packet*
2. *Packet Filtering Mode: 00_B : forward, 01_B : discard, 10_B : forward the packet to CPU port(defined in Bit [7:6] of register 07_H). if this packet is received from CPU Port, this packet will be forward to the VLAN group. 11_B : forward the packet to CPU port. if this packet is received from CPU Port, this packet will be discard.*

Port Base VLAN port Map Register

PBVLAN_MR	Offset	Reset Value
Port Base VLAN port Map Register	**08_H**	**777_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LED	Res		**LP**	Res	**PM2**			Res	**PM1**			Res	**PM0**		
rw	ro		rw	ro	rw			ro	rw			ro	rw		

Field	Bits	Type	Description
LED	15	rw	**Put Off LEDs of UTP port** 0_B , always put off LEDs of UTP port when UTP link down 1_B , LEDs of UTP port show DIPSW setting when auto-negotiation disable and link down
Res	14:13	ro	**Reserved**
LP	12	rw	**Link Partner** 0_B , if auto-negotiation enable, follow speed and duplex setting to negotiate with link partner. 1_B , if auto-negotiation enable, always advertise full capability to its link partner.
Res	11	ro	**Reserved**
PM2	10:8	rw	**Port 2 To port Map**
Res	7	ro	**Reserved**
PM1	6:4	rw	**Port 1 To port Map**
Res	3	ro	**Reserved**
PM0	2:0	rw	**Port 0 To port Map**

Packet Filter Control Registers 1 and 0

PCFC_1_0	Offset	Reset Value
Packet Filter Control Register 1 and 0	09_H	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
APR2	APR1	APR0	OP14					APR2	APR1	APR0	OP13				
rw	rw	rw	rw					rw	rw	rw	rw				

Field	Bits	Type	Description
APR2	15	rw	**Apply to Port 2 Rx** 0_B **DNA**, Do not apply 1_B **APL**, Apply
APR1	14	rw	**Apply to Port 1 Rx** 0_B **DNA**, Do not apply 1_B **APL**, Apply
APR0	13	rw	**Apply to Port 0 Rx** 0_B **DNA**, Do not apply 1_B **APL**, Apply
OP14	12:8	rw	**OP Code for Filter** Defined in Register 14_H (16_H, 18_H, $1A_H$, $1C_H$, $1E_H$, 20_H, 22_H)
APR2	7	rw	**Apply to Port 2 Rx** 0_B **DNA**, Do not apply 1_B **APL**, Apply
APR1	6	rw	**Apply to Port 1 Rx** 0_B **DNA**, Do not apply 1_B **APL**, Apply
APR0	5	rw	**Apply to Port 0 Rx** 0_B **DNA**, Do not apply 1_B **APL**, Apply
OP13	4:0	rw	**OP Code for Filter** which defined in Register 13_H (15_H, 17_H, 19_H, $1B_H$, $1D_H$, $1F_H$, 21_H)

Note:

OP Code bit[4:3]

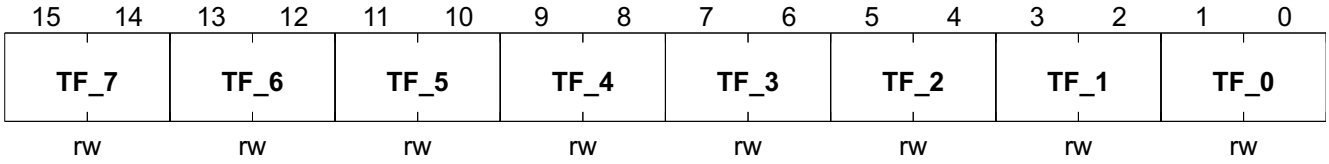
00_B : Priority. Priority is defined in OP Code bit[2:0] ;

01_B : Discard. OP Code bit[2:0] is RESERVED and SHOULD keep always 0;

$1x_B$: RESERVED.

Filter Type Register 0

TFTR_0	Offset	Reset Value
Filter Type Register 0	11_H	0000_H



Field	Bits	Type	Description
TF_7	15:14	rw	**Type of Filter 7**
TF_6	13:12	rw	**Type of Filter 6**
TF_5	11:10	rw	**Type of Filter 5**
TF_4	9:8	rw	**Type of Filter 4**
TF_3	7:6	rw	**Type of Filter 3**
TF_2	5:4	rw	**Type of Filter 2**
TF_1	3:2	rw	**Type of Filter 1**
TF_0	1:0	rw	**Type of Filter 0**

Note:

00_B : TCP/UDP Port Number;

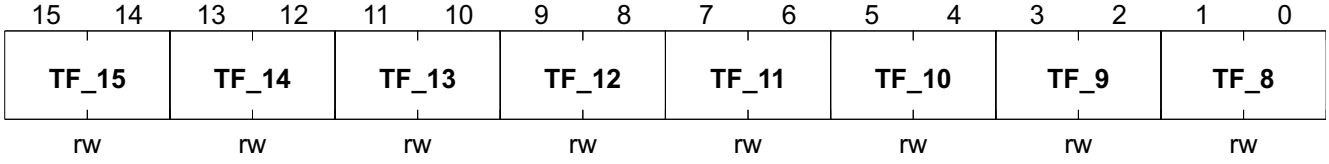
01_B : IP Protocol ID;

10_B : Ethernet Type;

11_B : RESERVED

Filter Type Register 1

TFTR_1	Offset	Reset Value
Filter Type Register 1	12_H	0000_H



Field	Bits	Type	Description
TF_15	15:14	rw	**Type of Filter 15**
TF_14	13:12	rw	**Type of Filter 14**

Field	Bits	Type	Description
TF_13	11:10	rw	**Type of Filter 13**
TF_12	9:8	rw	**Type of Filter 12**
TF_11	7:6	rw	**Type of Filter 11**
TF_10	5:4	rw	**Type of Filter 10**
TF_9	3:2	rw	**Type of Filter 9**
TF_8	1:0	rw	**Type of Filter 8**

Note:

00_B : TCP/UDP Port Number;

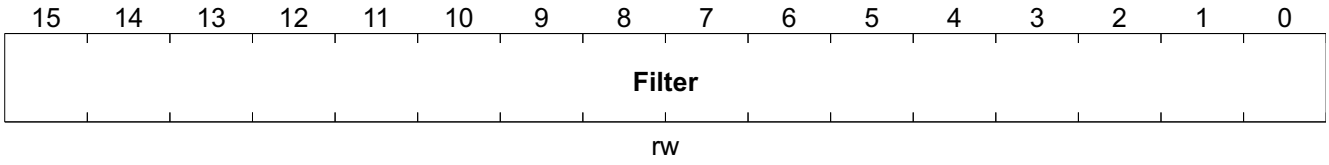
01_B : IP Protocol ID;

10_B : Ethernet Type;

11_B : RESERVED

Filter Register 0

FR_0	Offset	Reset Value
Filter Register 0	**13_H**	**0000_H**



Field	Bits	Type	Description
Filter	15:0	rw	**Filter**

Other Filter Registers have the same structure and characteristics as **Filter Register 0**; the offset addresses are listed in **Table 22**.

Table 22 Other Filter Regsiters

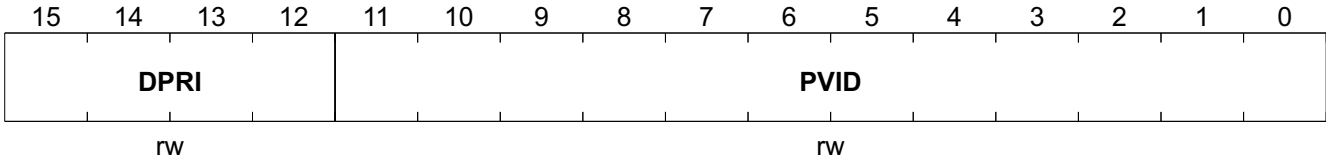
Register Short Name	Register Long Name	Offset Address	Page Number
FR_1	Filter Register 1	14_H	
FR_2	Filter Register 2	15_H	
FR_3	Filter Register 3	16_H	
FR_4	Filter Register 4	17_H	
FR_5	Filter Register 5	18_H	
FR_6	Filter Register 6	19_H	
FR_7	Filter Register 7	$1A_H$	
FR_8	Filter Register 8	$1B_H$	

Table 22 Other Filter Regsiters (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
FR_9	Filter Register 9	$1C_H$	
FR_10	Filter Register 10	$1D_H$	
FR_11	Filter Register 11	$1E_H$	
FR_12	Filter Register 12	$1F_H$	
FR_13	Filter Register 13	20_H	
FR_14	Filter Register 14	21_H	
FR_15	Filter Register 15	22_H	

Port Base VLAN ID and Mask 0 of Port 0

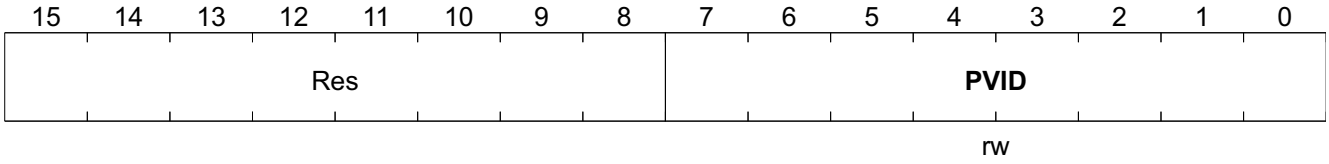
PB_ID_0_0	Offset	Reset Value
Port Base VLAN ID and Mask 0 of Port 0	23_H	0001_H



Field	Bits	Type	Description
DPRI	15:12	rw	**PVID Mask[3:0]** Default Priority
PVID	11:0	rw	**PVID** Port base VLAN ID

Port Base VLAN ID and Mask 1 of Port 0

PB_ID_1_0	Offset	Reset Value
Port Base VLAN ID and Mask 1 of Port 0	24_H	0000_H



Field	Bits	Type	Description
PVID	7:0	rw	**PVID Mask[11:4]**

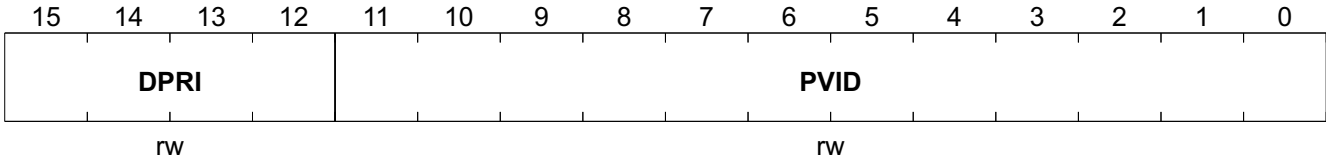
Note:

If (Tag Packet) then Tag = {TAGIN[15:12], ((TAGIN[11:0] & ~MASK) | (PVID & MASK))}

If (UnTag Packet) then Tag = {PKT_PRT[2:0], 0_B, PVID}

Port Base VLAN ID and Mask 0 of Port 1

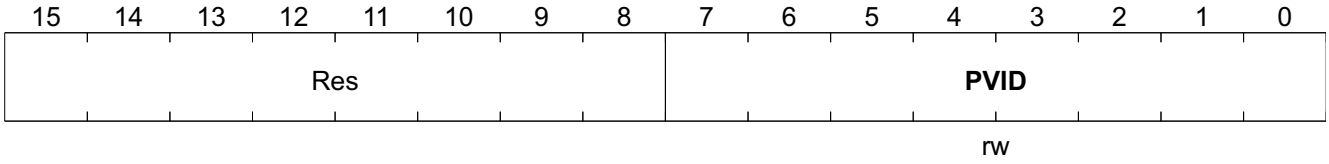
PB_ID_0_1	Offset	Reset Value
Port Base VLAN ID and Mask 0 of Port 1	25_H	0001_H



Field	Bits	Type	Description
DPRI	15:12	rw	**PVID Mask[3:0]** Default Priority
PVID	11:0	rw	**PVID** Port base VLAN ID

Port Base VLAN ID and Mask 1 of Port 1

PB_ID_1_1	Offset	Reset Value
Port Base VLAN ID and Mask 1 of Port 1	26_H	0000_H



Field	Bits	Type	Description
PVID	7:0	rw	**PVID Mask[11:4]**

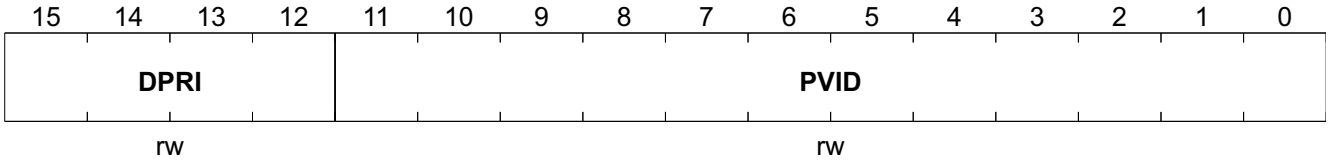
Note:

If (Tag Packet) then Tag = {TAGIN[15:12], ((TAGIN[11:0] & ~MASK) | (PVID & MASK))}

If (UnTag Packet) then Tag = {PKT_PRT[2:0], 0_B, PVID}

Port Base VLAN ID and Mask 0 of Port 2

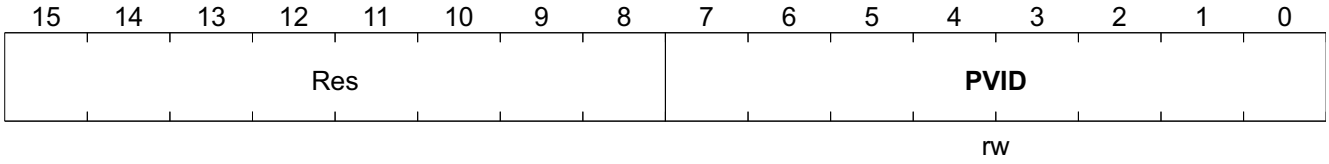
PB_ID_0_2	Offset	Reset Value
Port Base VLAN ID and Mask 0 of Port 2	**27_H**	**0001_H**



Field	Bits	Type	Description
DPRI	15:12	rw	**PVID Mask[3:0]** Default Priority
PVID	11:0	rw	**PVID** Port base VLAN ID

Port Base VLAN ID and Mask 1 of Port 2

PB_ID_1_2	Offset	Reset Value
Port Base VLAN ID and Mask 1 of Port 2	**28_H**	**0000_H**



Field	Bits	Type	Description
PVID	7:0	rw	**PVID Mask[11:4]**

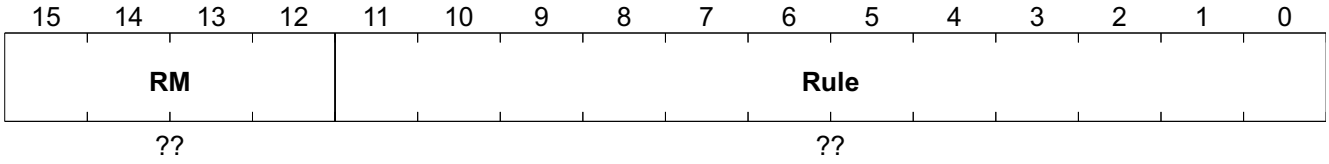
Note:

If (Tag Packet) then Tag = {TAGIN[15:12], ((TAGIN[11:0] & ~MASK) | (PVID & MASK))}

If (UnTag Packet) then Tag = {PKT_PRT[2:0], 0_B, PVID}

Tag Port Rule 0 Register 0

TPR_0_0 | **Offset** | **Reset Value**
Tag Port Rule 0 Register 0 | **29_H** | **$F000_H$**



Field	Bits	Type	Description
RM	15:12	rw	**Rule Mask[3:0]**
Rule	11:0	rw	**Rule**

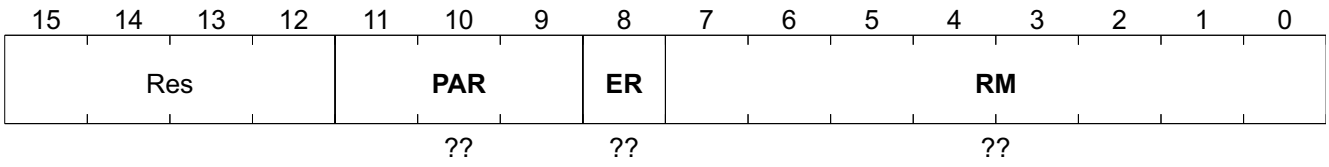
Other Tag Port Rule 0 Registers have the same structure and characteristics as **Tag Port Rule 0 Register 0**; the offset addresses are listed in **Table 23**.

Table 23 Other Tag Port Rule 0 Registers

Register Short Name	Register Long Name	Offset Address	Page Number
TPR_0_1	Tag Port Rule 0 Register 1	$2B_H$	
TPR_0_2	Tag Port Rule 0 Register 2	$2D_H$	
TPR_0_3	Tag Port Rule 0 Register 3	$2F_H$	
TPR_0_4	Tag Port Rule 0 Register 4	31_H	
TPR_0_5	Tag Port Rule 0 Register 5	33_H	
TPR_0_6	Tag Port Rule 0 Register 6	35_H	
TPR_0_7	Tag Port Rule 0 Register 7	37_H	

Tag Port Rule 1 Register 0

TPR_1_0 | **Offset** | **Reset Value**
Tag Port Rule 1 Register 0 | **$2A_H$** | **$00FF_H$**



Field	Bits	Type	Description
PAR	11:9	rw	**Port to apply the rule**
ER	8	rw	**Exclude Rule**

Field	Bits	Type	Description
RM	7:0	rw	**Rule Mask[11:4]**

Other Tag Port Rule 1 Registers have the same structure and characteristics as **Tag Port Rule 1 Register 0**; the offset addresses are listed in **Table 24**.

Table 24 Other Tag Port Rule 1 Regsiters

Register Short Name	Register Long Name	Offset Address	Page Number
TPR_1_1	Tag Port Rule 1 Register 1	$2C_H$	
TPR_1_2	Tag Port Rule 1 Register 2	$2E_H$	
TPR_1_3	Tag Port Rule 1 Register 3	30_H	
TPR_1_4	Tag Port Rule 1 Register 4	32_H	
TPR_1_5	Tag Port Rule 1 Register 5	34_H	
TPR_1_6	Tag Port Rule 1 Register 6	36_H	
TPR_1_7	Tag Port Rule 1 Register 7	38_H	

Miscellaneous Configuration Register 3

MCR_3	Offset	Reset Value
Miscellaneous Configuration Register 3	**39_H**	**0000_H**

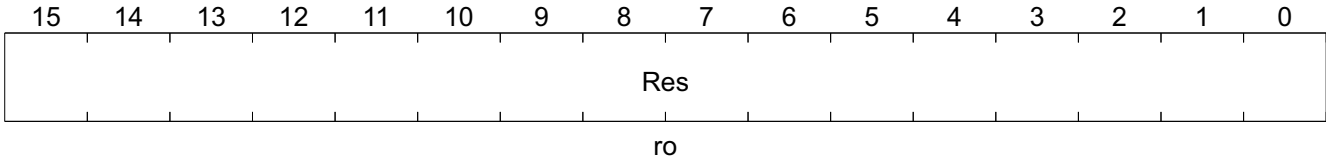
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		**CLC**	**RL**	**FP**	**100S**	**AP_P**			**LLB**			**PN_V**	**TAG**		
ro		rw	rw	rw	rw	rw			rw			rw	rw		

Field	Bits	Type	Description
Res	15:14	ro	**Reserved**
CLC	13	rw	**Check of the Length of CRS** 0_B , Enable the checking of the length of CRS (default) 1_B , Disable the checking of the length of CRS
RL	12	rw	**Redundant Link** 0_B , Enable Redundant Link in converter mode(default) 1_B , Disable Redundant Link
FP	11	rw	**Fault Propagation** 0_B , Enable Fault Propagation in converter mode(default) 1_B , Disable Fault Propagation
100S	10	rw	**100M Snooping** 0_B , Enable 100M snooping in converter mode(default) 1_B , Disable snooping
AP_P	9:7	rw	**All Packet/PPPOE** 0_B , all packet 1_B , PPPOE only

Field	Bits	Type	Description
LLB	6:4	rw	**Local Loop-back for Port2/Port1/Port0** 0_B , Normal Operation(default) 1_B , Local Loop-back for Port2/Port1/Port0
PN_V	3	rw	**Port Number/VLAN ID Base Grouping** 0_B , Port Number base grouping(default) 1_B , Received VLAN ID base grouping
TAG	2:0	rw	**VLAN TAG** 0_B , Recognize VLAN TAG automatically(default) 1_B , Disable

Miscellaneous Configuration Register 4

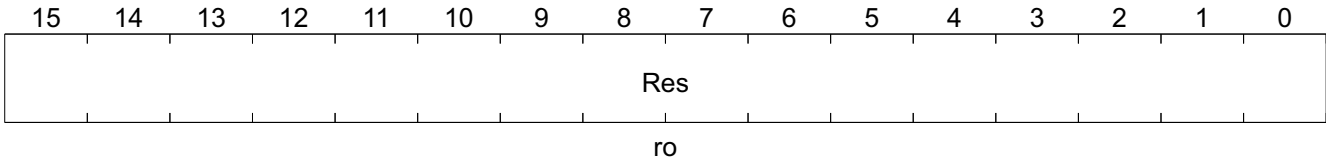
MCR_4	Offset	Reset Value
Miscellaneous Configuration 4	$3A_H$	0000_H



Field	Bits	Type	Description
Res	15:0	ro	**Reserved**

Miscellaneous Configuration Register 5

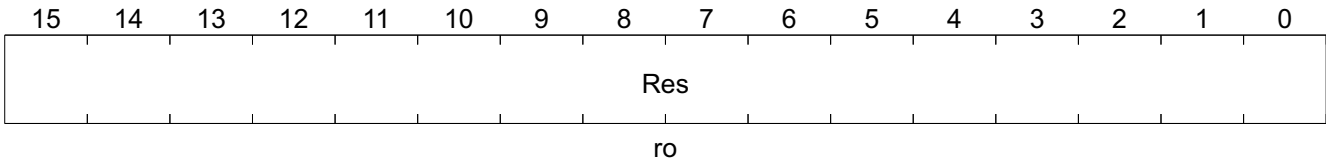
MCR_5	Offset	Reset Value
Miscellaneous Configuration Register 5	$3B_H$	0000_H



Field	Bits	Type	Description
Res	15:0	ro	**Reserved**

Miscellaneous Configuration Register 6

MCR_6	Offset	Reset Value
Miscellaneous Configuration Register 6	$3C_H$	0000_H



Field	Bits	Type	Description
Res	15:0	ro	**Reserved**

4.3 Default Value of SMI Register

Table 25 Default Value of SMI Register

Register	Bit 31-0	Mode	Default
00_H	Chip Identifier	ro	21143_H
01_H	Hardware Settings	ro	pin
02_H	Interrupt Register	lh/roc	0_H
03_H	Port Status	ro	Real time status
04_H	EEPROM Register File Access Control	rw	0_H
05_H	Port Control Register	rw	0_H
06_H	Over Flow Flag	lh/roc	0_H
07_H	P0 Receive Packets	rw	0_H
08_H	P0 Reveive Byte Count	rw	0_H
09_H	P0 Transmit Packets	rw	0_H
$0A_H$	P0 Transmit Byte Count	rw	0_H
$0B_H$	P0 Error Count	rw	0_H
$0C_H$	P0 Collision Count	rw	0_H
$0D_H$	P1 Receive Packets	rw	0_H
$0E_H$	P1 Reveive Byte Count	rw	0_H
$0F_H$	P1 Transmit Packets	rw	0_H
10_H	P1 Transmit Byte Count	rw	0_H
11_H	P1 Error Count	rw	0_H
12_H	P1 Collision Count	rw	0_H
13_H	P2 Receive Packets	rw	0_H
14_H	P2 Reveive Byte Count	rw	0_H
15_H	P2 Transmit Packets	rw	0_H
16_H	P2 Transmit Byte Count	rw	0_H
17_H	P2 Error Count	rw	0_H
18_H	P2 Collision Count	rw	0_H
19_H	Per Port Counter Reset	wr	

Note: Any write activity to counter register will reset the counter and the overflow flag of this counter.

4.4 SMI Register Descriptions

Table 26 Registers Address Space

Module	Base Address	End Address	Note
SMI	00_H	19_H	

Table 27 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
CI	Chip Identifier	00_H	**57**
HSS	Hardware Setting Status	01_H	**58**
Interrupt	Interrupt Register	02_H	**58**
PSR	Port Status Register	03_H	**60**
EEPROM_FAC	EEPROM Register File Access Control	04_H	**62**
PCR	Port Control Register	05_H	**62**
Overflow_Flag	Overflow Flag	06_H	**63**
PerPortCounter0	Per Port Counter 0	07_H	**64**
PerPortCounter1	Per Port Counter Register 1	08_H	**65**
PerPortCounter2	Per Port Counter Register 2	09_H	**65**
PerPortCounter3	Per Port Counter Register 3	10_H	**65**
PerPortCounter4	Per Port Counter Register 4	11_H	**65**
PerPortCounter5	Per Port Counter Register 5	12_H	**65**
PerPortCounter6	Per Port Counter Register 6	13_H	**65**
PerPortCounter7	Per Port Counter Register 7	14_H	**65**
PerPortCounter8	Per Port Counter Register 8	15_H	**65**
PerPortCounter9	Per Port Counter Register 9	16_H	**65**
PerPortCounterReset	Per Port Counter Reset	19_H	**65**

The register is addressed wordwise.

Table 28 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register

Table 28 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

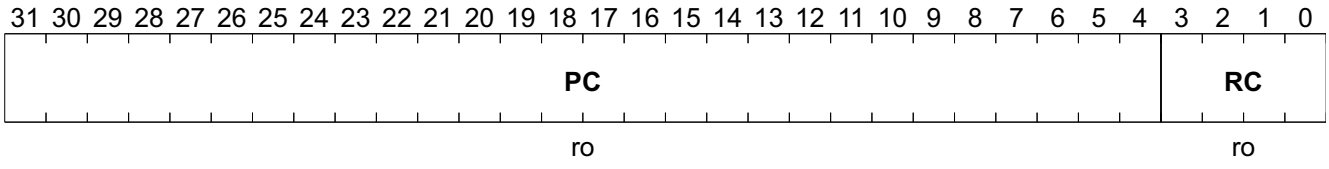
Table 29 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

4.4.1 SMI Register Format

Chip Identifier

CI	Offset	Reset Value
Chip Identifier	**00_H**	**21143_H**

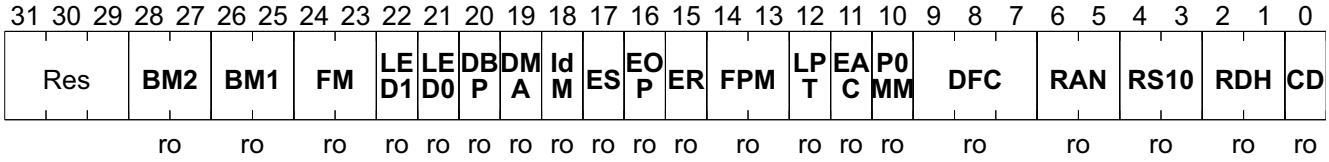


Field	Bits	Type	Description
PC	31:4	ro	**Project Code**

Field	Bits	Type	Description
RC	3:0	ro	**Revision Code**

Hardware Setting Status

HSS	Offset	Reset Value
Hardware Setting Status	**01_H**	**pin_H**



Field	Bits	Type	Description
BM2	28:27	ro	**Bus Mode of Port 2**
BM1	26:25	ro	**Bus Mode of Port 1**
FM	24:23	ro	**Fiber Mode**
LED1	22	ro	**LEDMODE 1**
LED0	21	ro	**LEDMODE 0**
DBP	20	ro	**Disable Back Preasure**
DMA	19	ro	**Disable MAC address learning**
IdM	18	ro	**Idle Mode**
ES	17	ro	**Enable Snooping**
EOP	16	ro	**Enable OAM Processor**
ER	15	ro	**Enable Redundant**
FPM	14:13	ro	**Fault Propagation Mode**
LPT	12	ro	**Disable Link Pass Through**
EAC	11	ro	**Enable Auto-Crossover**
P0MM	10	ro	**P0 MDI/MDIX**
DFC	9:7	ro	**Disable Flow Control**
RAN	6:5	ro	**Recommend Auto-Negotiation Ability for TP Port**
RS10	4:3	ro	**Recommend Speed 10 for TP Port**
RDH	2:1	ro	**Recommend Duplex Half for TP/FX Port**
CD	0	ro	**Chip Dis**

Interrupt Register

Interrupt	Offset	Reset Value
Interrupt Register	**02_H**	**$0000\ 0000_H$**

31–19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	CO	RCE2	RCE1	RCE0	BF2	BF1	BF0	FCA2	DC2	SC2	LSC2	FCA1	DC1	SC1	LSC1	FCA0	DC0	SC0	LSC0

lh/cbr/cbr/cbr/cbr/cbr/cbr/cbr/cbr/cbr/cbr/cbr/cbr/cbr/cbr/cbr/cbr/cbr/cbr/cc

Field	Bits	Type	Description
CO	18	lh/roc	**Counter Overflow** 0_B , Normal 1_B , Any counter defined in register 7_H~18_H overflow
RCE2	17	lh/roc	**Port 2 Receive CRC Error Packet** 0_B , Normal 1_B , Reveive CRC error packet
RCE1	16	lh/roc	**Port 1 Receive CRC Error Packet** 0_B , Normal 1_B , Reveive CRC error packet
RCE0	15	lh/roc	**Port 0 Receive CRC Error Packet** 0_B , Normal 1_B , Reveive CRC error packet
BF2	14	lh/roc	**Port 2 Buffer Full** 0_B , Normal 1_B , Buffer Full
BF1	13	lh/roc	**Port 1 Buffer Full** 0_B , Normal 1_B , Buffer Full
BF0	12	lh/roc	**Port 0 Buffer Full** 0_B , Normal 1_B , Buffer Full
FCA2	11	lh/roc	**Port 2 Flow Control Ability Change** 0_B , Normal 1_B , Status Change
DC2	10	lh/roc	**Port 2 Duplex Change** 0_B , Normal 1_B , Status Change
SC2	9	lh/roc	**Port 2 Speed Change** 0_B , Normal 1_B , Status Change
LSC2	8	lh/roc	**Port 2 Link Status Change** 0_B , Normal 1_B , Status Change
FCA1	7	lh/roc	**Port 1 Flow Control Ability Change** 0_B , Normal 1_B , Status Change
DC1	6	lh/roc	**Port 1 Duplex Change** 0_B , Normal 1_B , Status Change

Field	Bits	Type	Description
SC1	5	lh/roc	**Port 1 Speed Change** 0_B , Normal 1_B , Status Change
LSC1	4	lh/roc	**Port 1 Link Status Change** 0_B , Normal 1_B , Status Change
FCA0	3	lh/roc	**Port 0 Flow Control Ability Change** 0_B , Normal 1_B , Status Change
DC0	2	lh/roc	**Port 0 Duplex Change** 0_B , Normal 1_B , Status Change
SC0	1	lh/roc	**Port 0 Speed Change** 0_B , Normal 1_B , Status Change
LSC0	0	lh/roc	**Port 0 Link Status Change** 0_B , Normal 1_B , Status Change

Port Status Register

PSR	Offset	Reset Value
Port Status Register	**03_H**	**Real Time Status$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res											CBL1		CB1	CBL0		CB0	BF2	BF1	BF0	FC2	Dup2	Spe2	LS2	FC1	Dup1	Spe1	LS1	FC0	Dup0	Spe0	LS0
											ro		ro	ro		ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

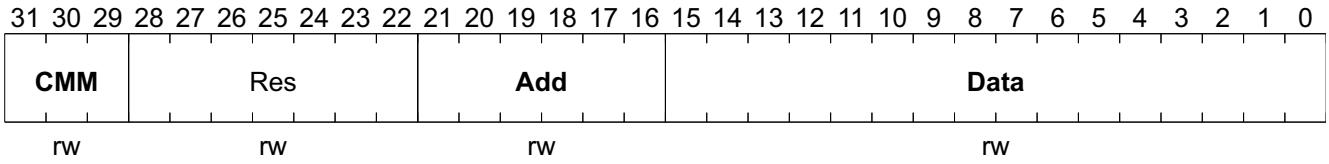
Field	Bits	Type	Description
CBL1	20:19	ro	**CBBRK_LENGTH of P1** 00_B , 0~60m 01_B , 60~90m 10_B , 90~130m 11_B , 130~170m
CB1	18	ro	**CBBRK of P1** 0_B , Normal 1_B , Cable Broken
CBL0	17:16	ro	**CBBRK_LENGTH of P0** 00_B , 0~60m 01_B , 60~90m 10_B , 90~130m 11_B , 130~170m

Field	Bits	Type	Description
CB0	15	ro	**CBBRK of P0** 0_B , Normal 1_B , Cable Broken
BF2	14	ro	**Buffer Full Status of Port 2** 0_B , Normal 1_B , Buffer Full
BF1	13	ro	**Buffer Full Status of Port 1** 0_B , Normal 1_B , Buffer Full
BF0	12	ro	**Buffer Full Status of Port 0** 0_B , Normal 1_B , Buffer Full
FC2	11	ro	**Flow Control of Port 2** 0_B , Disable 1_B , Enable
Dup2	10	ro	**Duplex of Port 2** 0_B , Half Duplex 1_B , Full Duplex
Spe2	9	ro	**Speed of Port 2** 0_B , 10M 1_B , 100M
LS2	8	ro	**Link Status of Port 2** 0_B , Link Down 1_B , Link Up
FC1	7	ro	**Flow Control of Port 1** 0_B , Disable 1_B , Enable
Dup1	6	ro	**Duplex of Port 1** 0_B , Half Duplex 1_B , Full Duplex
Spe1	5	ro	**Speed of Port 1** 0_B , 10M 1_B , 100M
LS1	4	ro	**Link Status of Port 1** 0_B , Link Down 1_B , Link Up
FC0	3	ro	**Flow Control of Port 0** 0_B , Disable 1_B , Enable
Dup0	2	ro	**Duplex of Port 0** 0_B , Half Duplex 1_B , Full Duplex
Spe0	1	ro	**Speed of Port 0** 0_B , 10M 1_B , 100M

Field	Bits	Type	Description
LS0	0	ro	**Link Status of Port 0** 0_B , Link Down 1_B , Link Up

EEPROM Register File Access Control

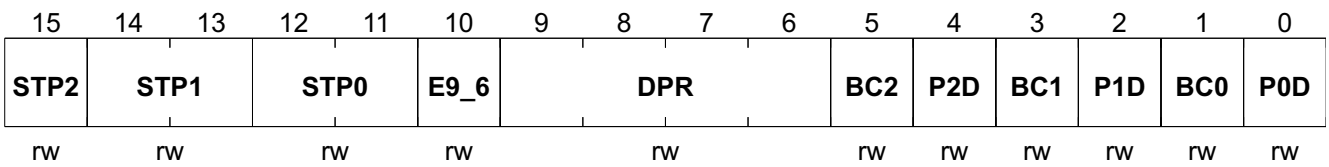
EEPROM_FAC	Offset	Reset Value
EEPROM Register File Access Control	**04_H**	**$0000\ 0000_H$**



Field	Bits	Type	Description
CMM	31:29	rw	**Command** 000_B , Read 001_B , Write $Others_B$, Reserved
Res	28:22	rw	**Reserved** Should be always 0000000_B
Add	21:16	rw	**Address** 00_H~$3F_H$
Data	15:0	rw	**Data**

Port Control Register

PCR	Offset	Reset Value
Port Control Register	**05_H**	**00000_H**

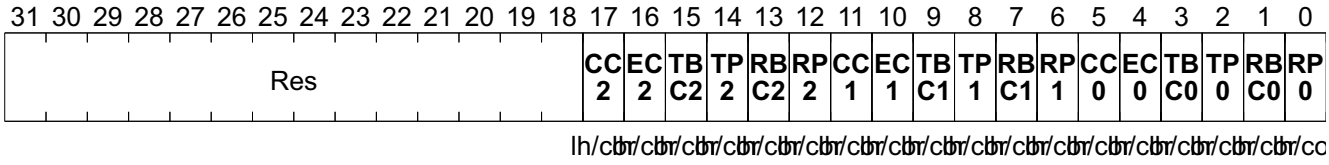


Field	Bits	Type	Description
STP2	16:15	rw	**STP State of Port 2** $0x_B$, Forwarding 10_B , Learning 11_B , Blocking & listening

Field	Bits	Type	Description
STP1	14:13	rw	**STP State of Port 1** $0x_B$, Forwarding 10_B , Learning 11_B , Blocking & listening
STP0	12:11	rw	**STP State of Port 0** $0x_B$, Forwarding 10_B , Learning 11_B , Blocking & listening
E9_6	10	rw	**Enable Bit[9:6]** 0_B , Disable 1_B , Enable
DPR	9:6	rw	**Destination of the packet received from CPU port** Bit [8:6] : Bit[6] is for P0, Bit[7] is for P1 and Bit[8] is for P2. If the bit is set to 1, the packet received from CPU port defined in EEPROM register 7_H bit [7:6] will be forward to the corresponding port.Bit [9]: If the total number of 1 in Bit [8:6] is greater than 1, this bit should set to 1 too.
BC2	5	rw	**P2 Bandwidth Control ON/OFF** 0_B , Normal 1_B , Force P2 issue PAUSE packet for full duplex and back pressure for half duplex
P2D	4	rw	**P2 Disable** 0_B , Normal 1_B , P2 Disable Receiving/Transmitting
BC1	3	rw	**P1 Bandwidth Control ON/OFF** 0_B , Normal 1_B , Force P1 issue PAUSE packet for full duplex and back pressure for half duplex
P1D	2	rw	**P1 Disable** 0_B , Normal 1_B , P1 Disable Receiving/Transmitting
BC0	1	rw	**P0 Bandwidth Control ON/OFF** 0_B , Normal 1_B , Force P0 issue PAUSE packet for full duplex and back pressure for half duplex
P0D	0	rw	**P0 Disable** 0_B , Normal 1_B , P0 Disable Receiving/Transmitting

Overflow Flag

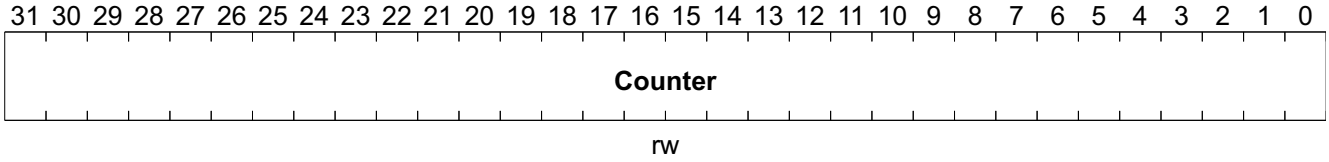
Overflow_Flag	Offset	Reset Value
Overflow Flag	**06_H**	**00000_H**



Field	Bits	Type	Description
CC2	17	lh/roc	**P2 Collision Count** 1_B , P2 Collision Count
EC2	16	lh/roc	**P2 Error Count** 1_B , P2 Error Count
TBC2	15	lh/roc	**P2 Transmit Byte Count** 1_B , P2 Transmit Byte Count
TP2	14	lh/roc	**P2 Transmit Packets** 1_B , P2 Transmit Packets
RBC2	13	lh/roc	**P2 Receive Byte Count** 1_B , P2 Receive Byte Count
RP2	12	lh/roc	**P2 Receive Packets** 1_B , P2 Receive Packets
CC1	11	lh/roc	**P1 Collision Count** 1_B , P1 Collision Count
EC1	10	lh/roc	**P1 Error Count** 1_B , P1 Error Count
TBC1	9	lh/roc	**P1 Transmit Byte Count** 1_B , P1 Transmit Byte Count
TP1	8	lh/roc	**P1 Transmit Packets** 1_B , P1 Transmit Packets
RBC1	7	lh/roc	**P1 Receive Byte Count** 1_B , P1 Receive Byte Count
RP1	6	lh/roc	**P1 Receive Packets** 1_B , P1 Receive Packets
CC0	5	lh/roc	**P0 Collision Count** 1_B , P0 Collision Count
EC0	4	lh/roc	**P0 Error Count** 1_B , P0 Error Count
TBC0	3	lh/roc	**P0 Transmit Byte Count** 1_B , P0 Transmit Byte Count
TP0	2	lh/roc	**P0 Transmit Packets** 1_B , P0 Transmit Packets
RBC0	1	lh/roc	**P0 Receive Byte Count** 1_B , P0 Receive Byte Count
RP0	0	lh/roc	**P0 Receive Packets** 1_B , P0 Receive Packets

Per Port Counter 0

PerPortCounter0	Offset	Reset Value
Per Port Counter 0	07_H	$0000\ 0000_H$



Field	Bits	Type	Description
Counter	31:0	rw	**Counter**

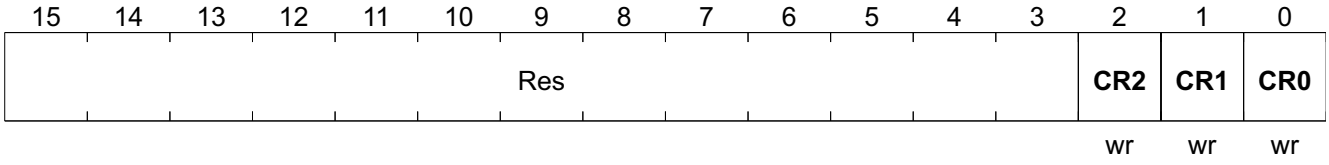
Other Per Port Counter Registers have the same structure and characteristics as **Per Port Counter 0**; the offset addresses are listed in **Table 30**.

Table 30 Other Per Port Counter Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PerPortCounter1	Per Port Counter Register 1	08_H	
PerPortCounter2	Per Port Counter Register 2	09_H	
PerPortCounter3	Per Port Counter Register 3	10_H	
PerPortCounter4	Per Port Counter Register 4	11_H	
PerPortCounter5	Per Port Counter Register 5	12_H	
PerPortCounter6	Per Port Counter Register 6	13_H	
PerPortCounter7	Per Port Counter Register 7	14_H	
PerPortCounter8	Per Port Counter Register 8	15_H	
PerPortCounter9	Per Port Counter Register 9	16_H	

Per Port Counter Reset

PerPortCounterReset	Offset	Reset Value
Per Port Counter Reset	19_H	$??_H$



Field	Bits	Type	Description
CR2	2	wr	**Counter Reset of Port2** 1_B , Reset All Counter of Port 2

Field	Bits	Type	Description
CR1	1	wr	**Counter Reset of Port1** 1_B , Reset All Counter of Port 1
CR0	0	wr	**Counter Reset of Port0** 1_B , Reset All Counter of Port 0

5 Electrical Specification

DC and AC.

5.1 DC Characterization

Table 31 Electrical Absolute Maximum Rating

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	V_{CC}	-0.3		2.7	V	
Input Voltage	V_{IN}	-0.3		V_{CC} + 0.3	V	
Output Voltage	*Vout*	-0.3		V_{CC} + 0.3	V	
Storage Temperature	*TSTG*	-55		155	°C	
Power Dissipation	*PD*			990	mW	
ESD Rating	*ESD*			2	KV	

Table 32 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply[1)]	*Vcc*	3.135	3.3	3.465	V	
Input Voltage	*Vin*	0	-	Vcc	V	
Junction Operating Temperature	*Tj*	0	25	115	°C	

1) VCC3O. VCCBIAS

Table 33 DC Electrical Characteristics for 3.3 V Operation[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Low Voltage	*VIL*			0.8	V	TTL
Input High Voltage	*VIH*	2.0			V	TTL
Output Low Voltage	*VOL*			0.4	V	TTL
Output High Voltage	*VOH*	2.4			V	TTL
Input Pull_up/down Resistance	*RI*		50		KΩ	VIL = 0 V or VIH = Vcc

1) Under VCC = 3.0 V~ 3.6 V, Tj = °C ~ 115 °C

5.2 AC Characterization

Power on Reset Timing, EEPROM Interface Timing, 10Base-Tx MII Timing, 100Base-Tx MII Timing, Reduce MII Timing, GPSI(7-wire) Timing, HDLC Timing, and SMI Timing.

Power on Reset Timing

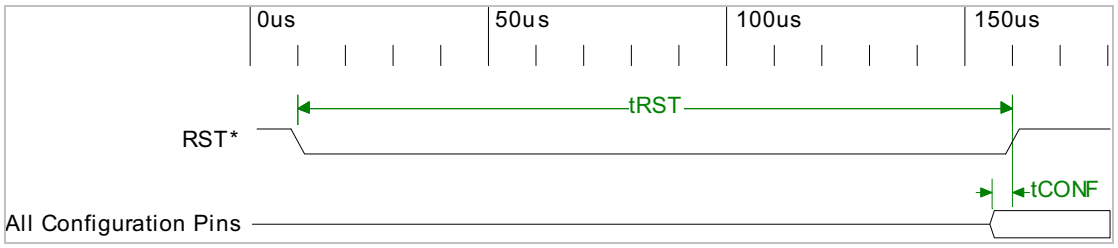


Figure 5 Power on Reset Timing

Table 34 Power on Reset Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RST Low Period	t_{RST}	100			ms	TTL
Start of Idle Pulse Width	t_{CONF}	100			ns	TTL

EEPROM Interface Timing

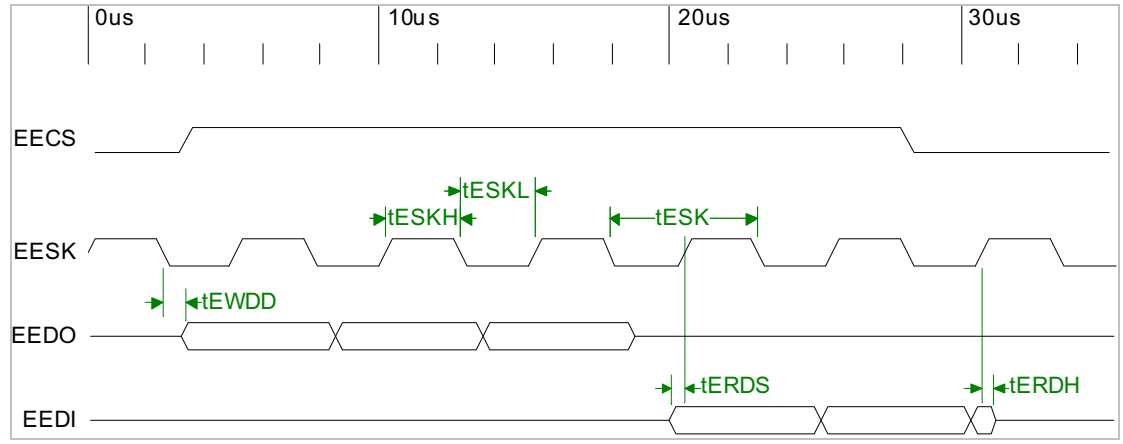


Figure 6 EEPROM Interface Timing

Table 35 EEPROM Interface Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Period	t_{ESK}		5120		ns	
EESK Low Period	t_{ESKL}	2550		2570	ns	
EESK High Period	t_{ESKH}	2550		2570	ns	
EEDI to EESK Rising Setup Time	t_{ERDS}	10			ns	

Table 35 EEPROM Interface Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EEDI to EESK Rising Hold Time	t_{ERDH}	10			ns	
EESK Falling to EEDO Output Delay Time	t_{EWDD}			20	ns	

10Base-Tx MII Input Timing

10Base-Tx Input timing conditions

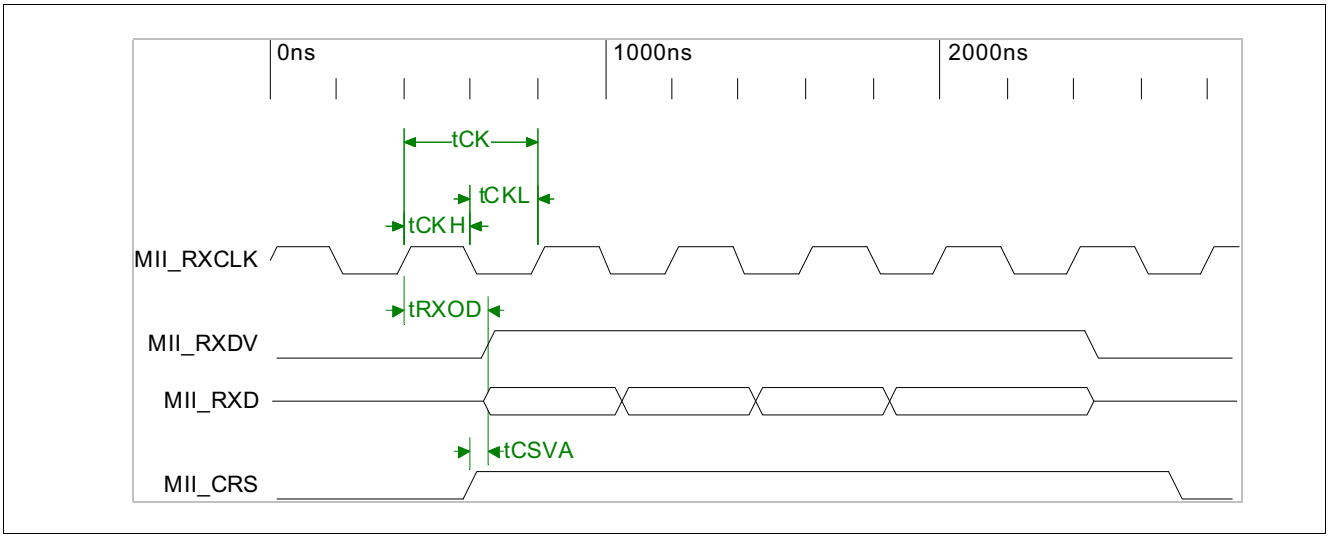


Figure 7 10Base-Tx MII Input Timing

Table 36 10Base-Tx MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	t_{CK}		400		ns	
MII_RXCLK Low Period	t_{CKL}	160		240	ns	
MII_RXCLK High Period	t_{CKH}	160		240	ns	
MII_CRS Rising to MII_RXDV Rising	t_{CSVA}	0		10	ns	
MII_RXCLK Rising to MII_RXD, MII_RXDV, MII_CRS Output Delay	t_{RXOD}	200			ns	

10Base-TX MII Output Timing

10Base-TX MII Output timing conditions

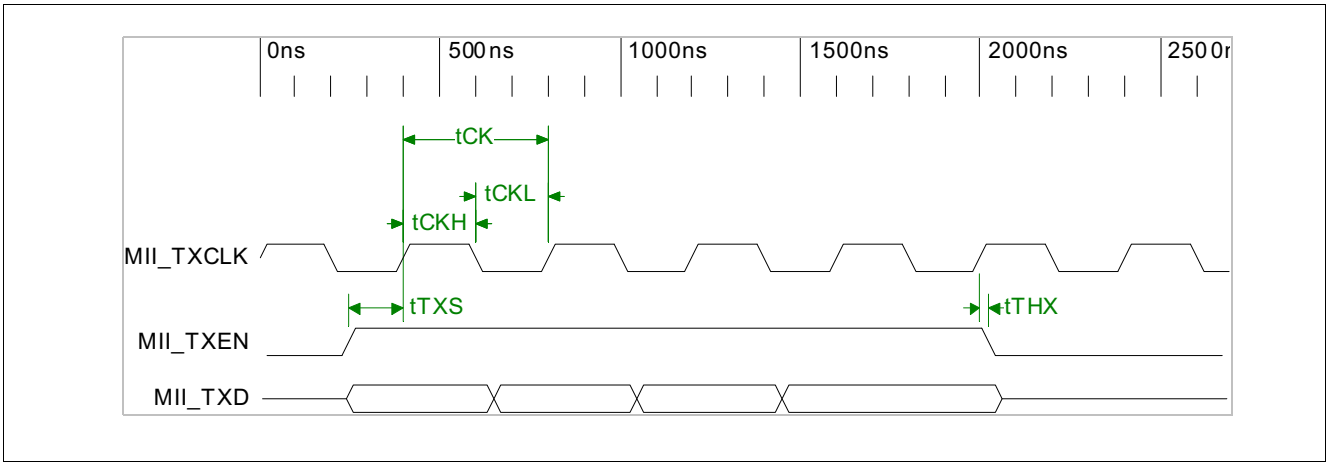


Figure 8 10Base-TX MII Output Timing

Table 37 10Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	t_{CK}		400		ns	
MII_TXCLK Low Period	t_{CKL}	160		240	ns	
MII_TXCLK High Period	t_{CKH}	160		240	ns	
MII_TXD, MII_TXEN to MII_TXCLK Rising Setup Time	t_{TXS}	10			ns	
MII_TXD, MII_TXEN to MII_TXCLK Rising Hold Time	t_{TXH}	10			ns	

100Base-Tx MII Input Timing

100Base Tx MII Input timing conditions

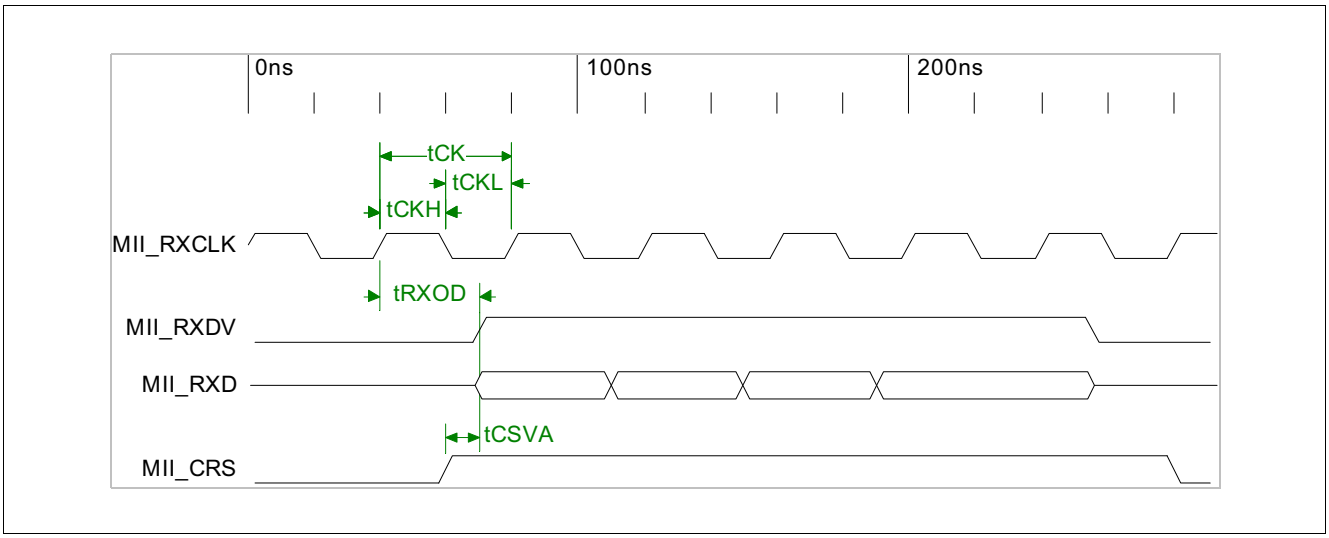


Figure 9 100Base-TX MII Input Timing

Table 38 100Base-TX MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	t_{CK}		40		ns	
MII_RXCLK Low Period	t_{CKL}	16		24	ns	
MII_RXCLK High Period	t_{CKH}	16		24	ns	
MII_CRS Rising to MII_RXDV Rising	t_{CSVA}	0		10	ns	
MII_RXCLK Rising to MII_RXD, MII_RXDV, MII_CRS Output Delay	t_{RXOD}	20		30	ns	

100Base-TX MII Output Timing

100Base-TX MII Output timing conditions

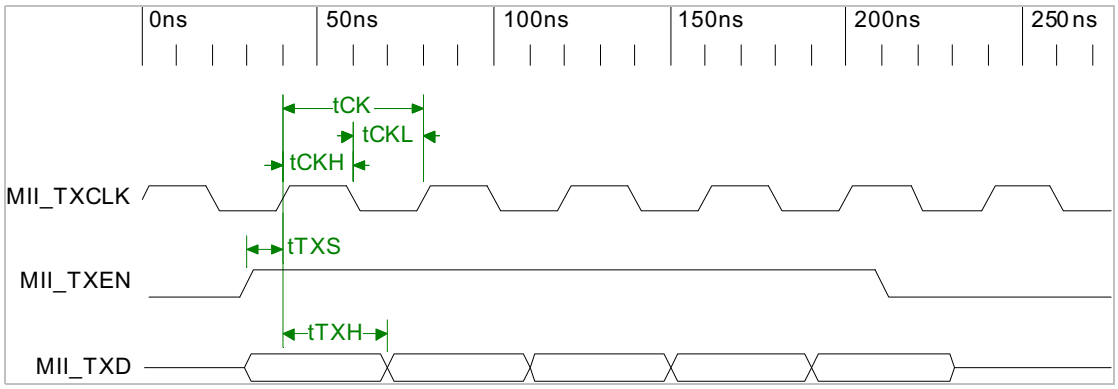


Figure 10 100Base-TX MII Output Timing

Table 39 100Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	t_{CK}		40		ns	
MII_TXCLK Low Period	t_{CKL}	16		24	ns	
MII_TXCLK High Period	t_{CKH}	16		24	ns	
MII_TXD, MII_TXEN to MII_TXCLK Rising Setup Time	t_{TXS}	10			ns	
MII_TXD, MII_TXEN to MII_TXCLK Rising Hold Time	t_{TXH}	10			ns	

Reduce MII Timing

Reduce MII timing conditions

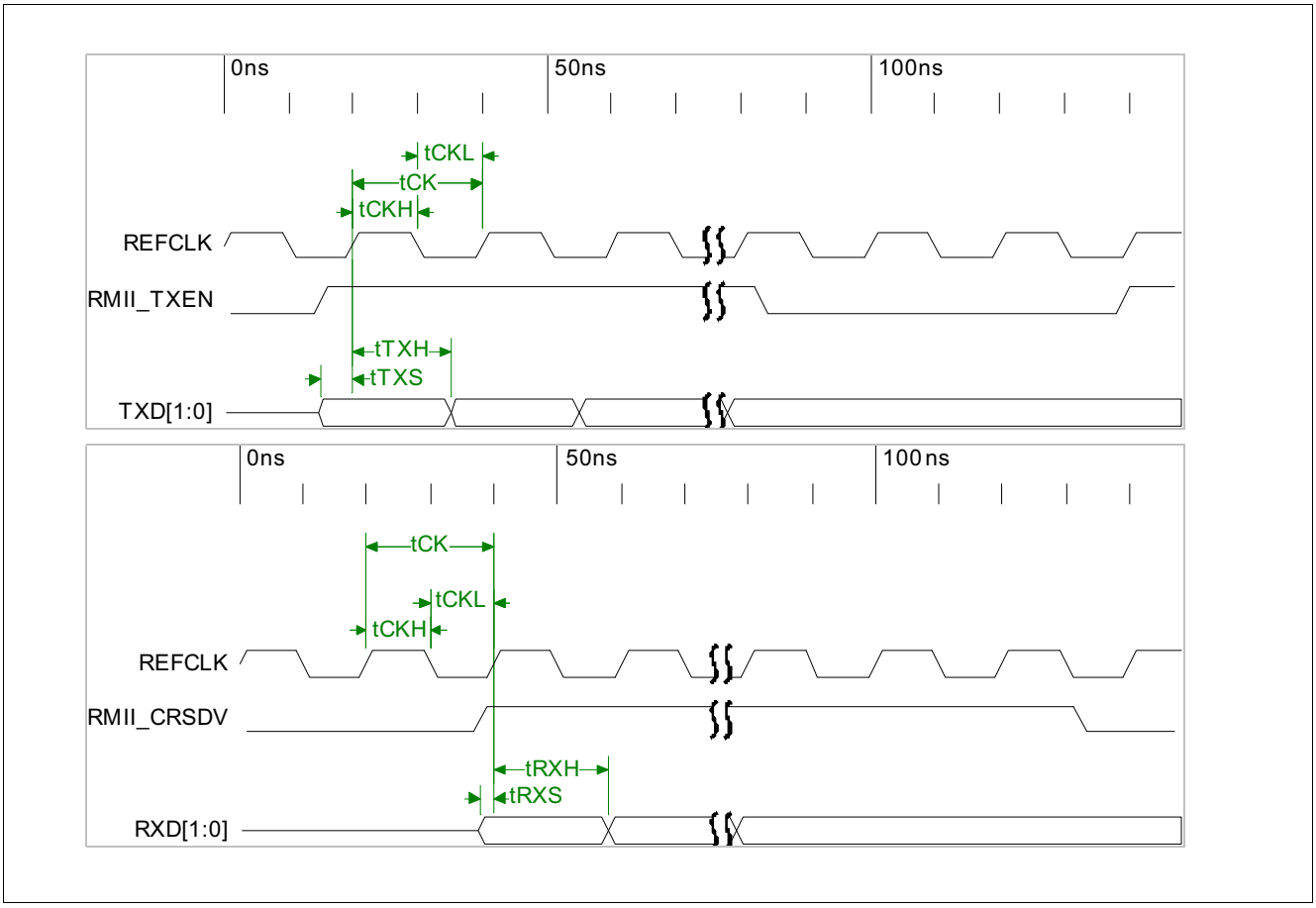


Figure 11 Reduce MII Timing

Table 40 100Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RMII_REFCLK Period	t_{CK}		20		ns	
RMII_REFCLK Low Period	t_{CKL}		10		ns	
RMII_REFCLK High Period	t_{CKH}		10		ns	
TXEN, TXD to REFCLK rising setup time	t_{TXS}	4			ns	
TXE, TXD to REFCLK rising hold time	t_{TXH}	2			ns	
CSRDV, RXD to REFCLK rising setup time	t_{RXS}	4			ns	
CRSDV, RXD to REFCLK rising hold time	t_{RXH}	2			ns	

GPSI (7-wire) Input Timing

GPSI (7-wire) Input timing conditions

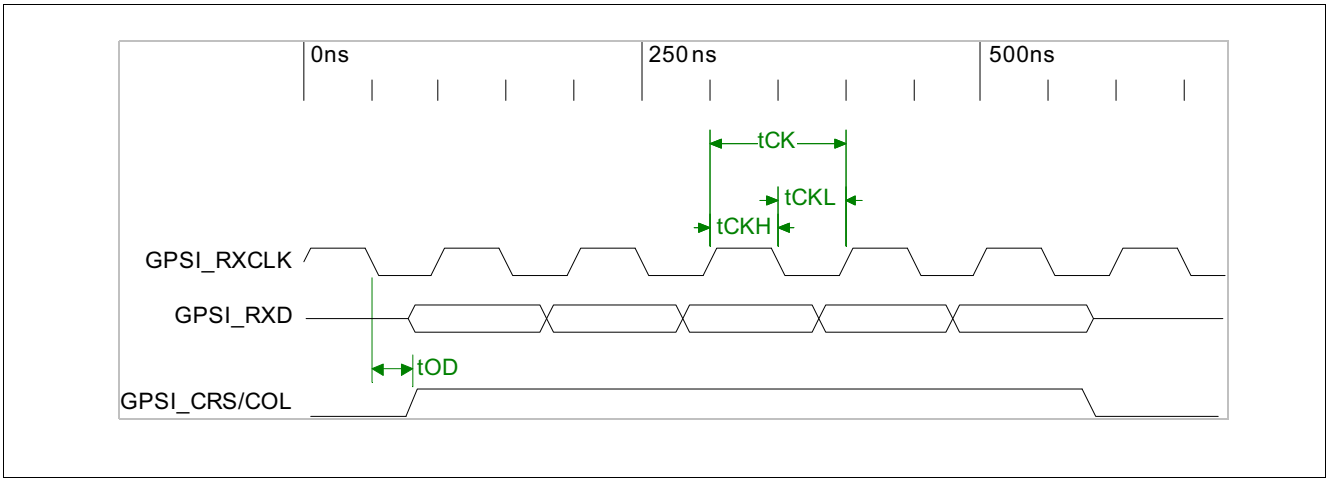


Figure 12 GPSI (7-wire) Input Timing

Table 41 GPSI (7-wire) Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GPSI_RXCLK Period	T_{CK}		100		ns	
GPSI_RXCLK Low Period	T_{CKL}	40		60	ns	
GPSI_RXCLK High Period	T_{CKH}	40		60	ns	
GPSI_RXCLK Rising to GPSI_CRS/GPSI_COL Output Delay	T_{OD}	50		70	ns	

GPSI (7-wire) Output Timing

GPSI (7-wire) Output timing conditions

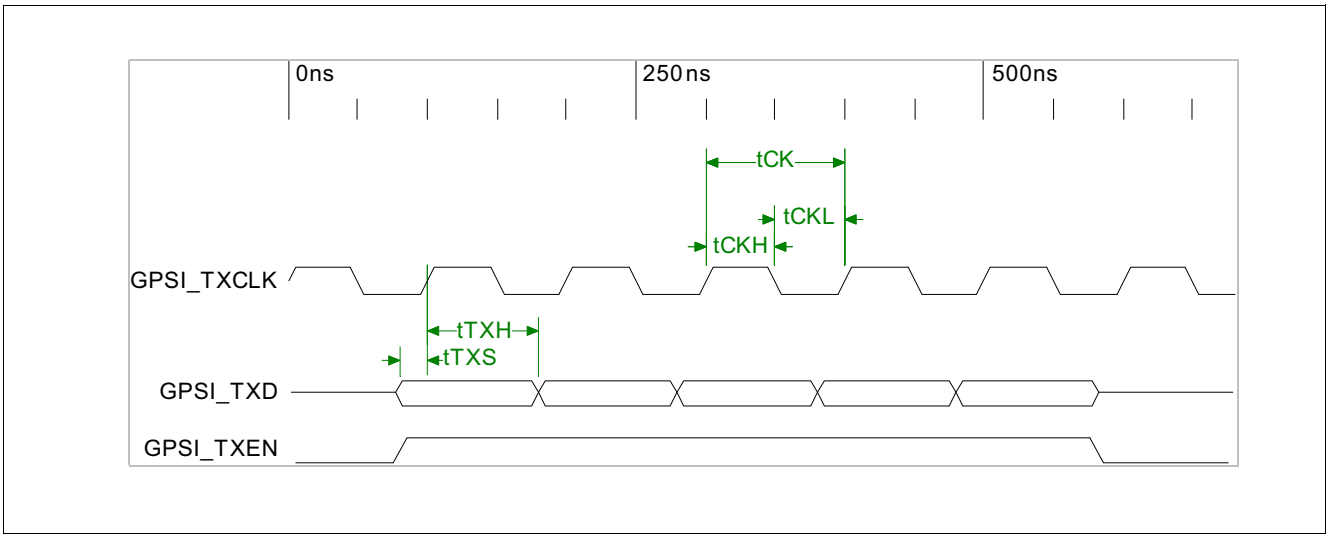


Figure 13 GPSI (7-wire) Output Timing

Table 42 GPSI (7-wire) Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GPSI_TXCLK Period	T_{CK}		100		ns	
GPSI_TXCLK Low Period	T_{CKL}	40		60	ns	
GPSI_ T XCLK High Period	T_{CKH}	40		60	ns	
GPSI_TXD, GPSI_TXEN to GPSI_TXCLK Rising Setup Time	T_{TXS}	10			ns	
GPSI_TXD, GPSI_TXEN to GPSI_TXCLK Rising Hold Time	T_{TXH}	10			ns	

HDLC Timing

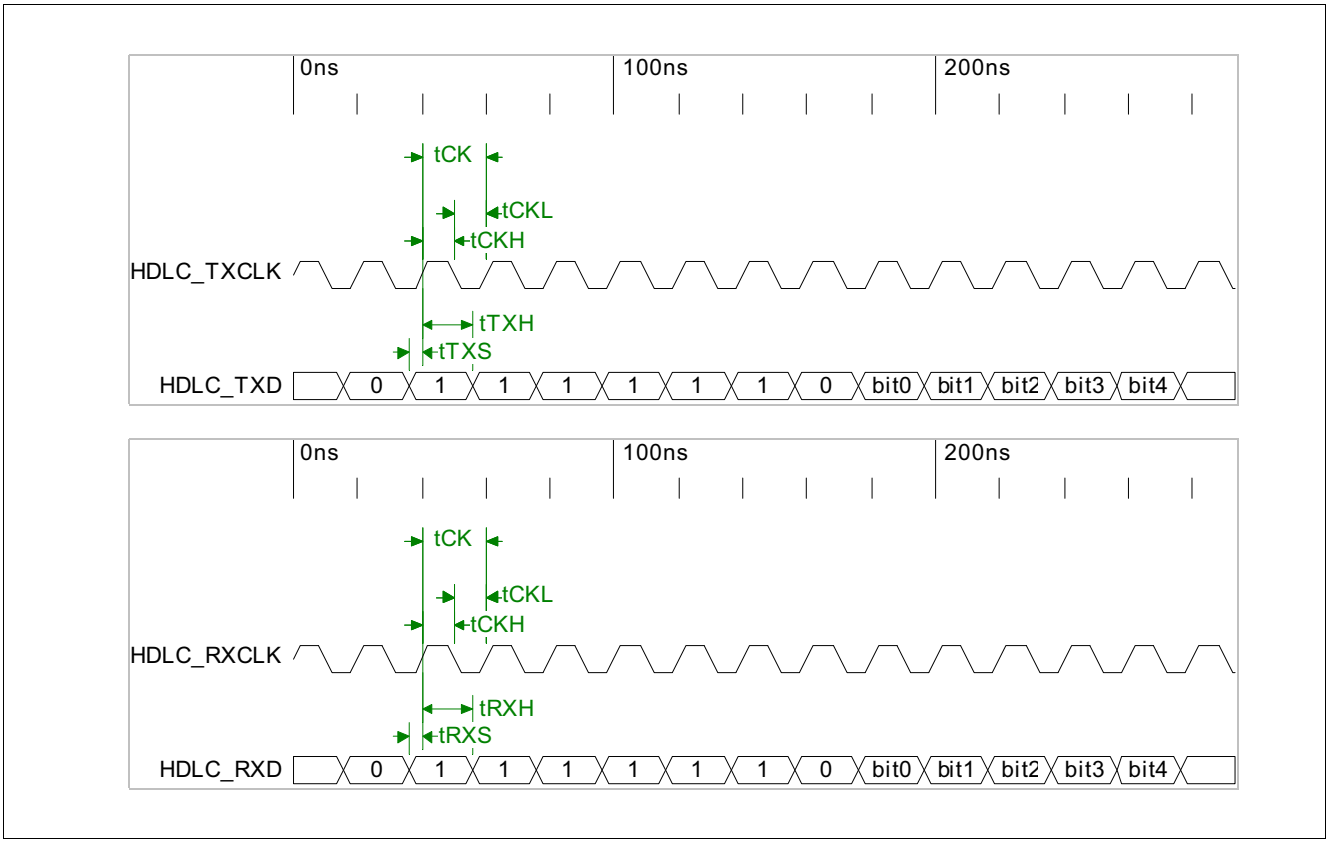


Figure 14 HDLC Timing

Table 43 HDLC Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
HDLC_REFCLK Period	T_{CK}	20			ns	
HDLC_REFCLK Low Period	T_{CKL}	10			ns	

Table 43 HDLC Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
HDLC_REFCLK High Period	T_{CKH}	10			ns	
TXD to TXCLK rising setup time	T_{TXS}	0			ns	
TXD to TXCLK rising hold time	T_{TXH}	5			ns	
RXD to RXCLK rising setup time	T_{RXS}	0			ns	
RXD to RXCLK rising hold time	T_{RXH}	5			ns	

SMI Timing

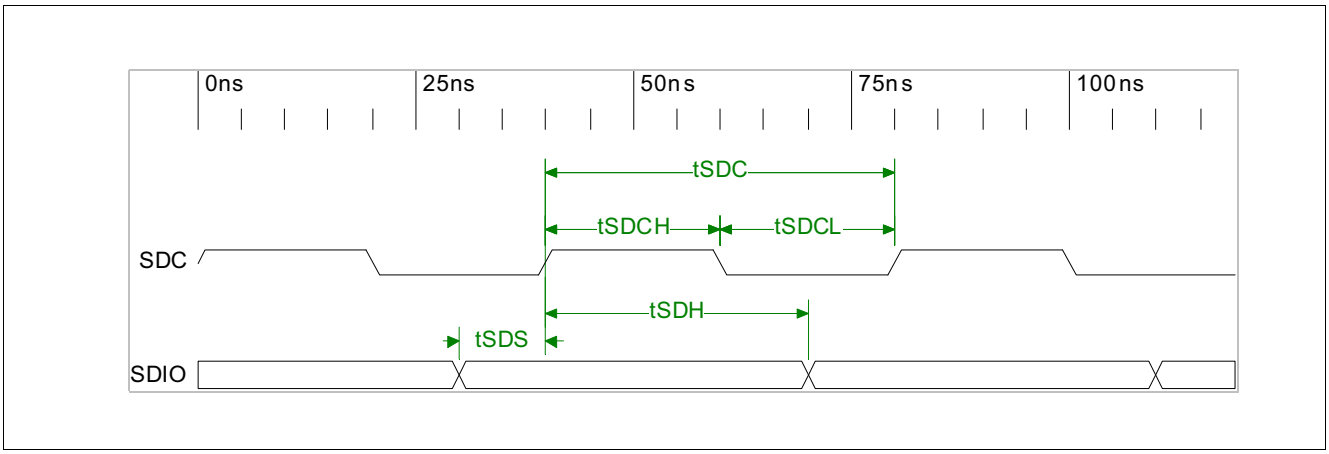


Figure 15 SMI Timing

Table 44 SMI Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDC Period	T_{CK}	20			ns	
SDC Low Period	T_{CKL}	10			ns	
SDC High Period	T_{CKH}	10			ns	
SDIO to SDC rising setup time on read/write cycle	T_{SDS}	4			ns	
SDIO to SDC rising hold time on read/write cycle	T_{SDH}	2			ns	

6 Packaging

128 PQFP packaging for ADM6993/X

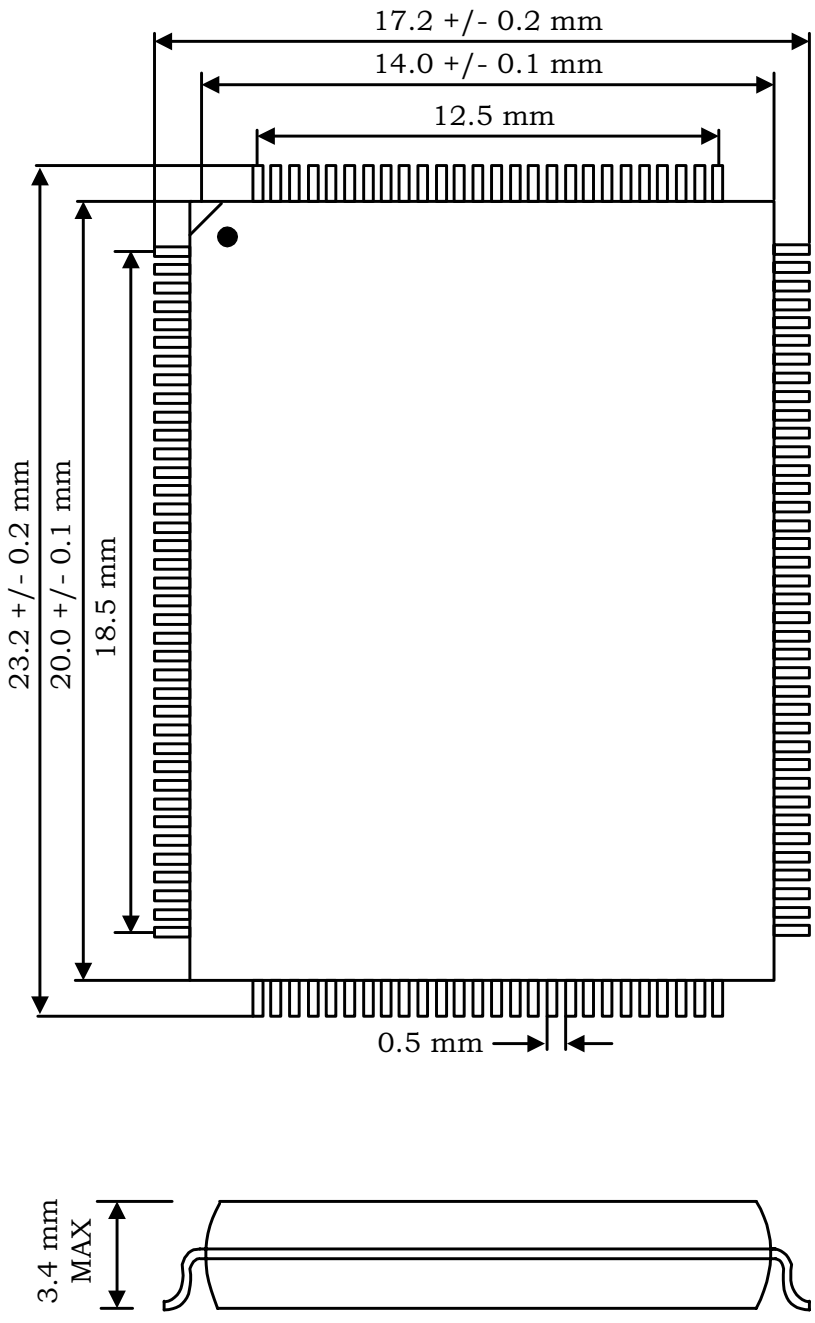


Figure 16 128 PQFP packaging for ADM6993/X

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- Техническая поддержка проекта;
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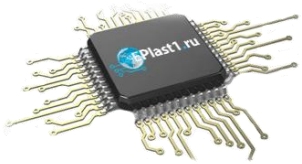

Как с нами связаться

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