DEMO MANUAL DC1945A

LTC2185 and LTC6409 16-Bit, 125Msps Dual ADC Combo Board

DESCRIPTION

Demonstration circuit 1945A supports the LTC®2185 125Msps dual ADC and a LTC6409 low noise amplifier. The assembly may be modified to evaluate other members of the pin-compatible 16-bit LTC2185 and 14-bit/12-bit LTC2145 dual ADC families.

DC1945A supports the LTC2185, DDR LVDS output mode. The circuitry on the analog inputs is optimized for analog input frequencies from DC to 100MHz. The DC1945A can also be used as a direct receiver board by attaching the analog inputs to a demodulator like the LTC5585. Refer to the data sheet for proper input networks for different input frequencies.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage: ADC	Depending on sampling rate and the A/D converter provided, this supply must provide up to 150mA	4.5		6	V
Supply Voltage: Amplifier	Depending on supply voltage used, this supply must provide up to 150mA	2.7		5.2	V
Analog Input Range	Depending on SENSE Pin Voltage	62		125	mV
Logic Input Voltages	Minimum Logic High Maximum Logic Low		1.3 0.6		V V
Logic Output Voltages (OV_{DD} = 1.8V)	Minimum High Level Output Voltage Maximum Low Level Output Voltage		1.395 1.065		V V
Sampling Frequency (Convert Clock Frequency)	Depending on ADC, this can vary between 20Msps and 125Msps	1		125	Msps
Convert Clock Level	Single-Ended Encode Mode (ENC^- Tied to GND)	0		3.6	V
Convert Clock Level	Differential Encode Mode (ENC^- Not Tied to GND)	0.2		3.6	V
Resolution			16		Bits
Input Frequency Range		DC		100	MHz
SFDR	See Applicable Data Sheet				
SNR	See Applicable Data Sheet				

QUICK START PROCEDURE

DC1945A is easy to set up to evaluate the performance of the LTC2185 family of A/D converters. Refer to Figure 1 for proper measurement equipment setup and follow the procedure in the Setup section.

SETUP

If a DC890 QuikEval™ II Data Acquisition and Collection System was supplied with the DC1945A demonstration circuit, follow the DC890 Quick Start Guide to install the required software and for connecting the DC890 to the DC1945A and to a PC.

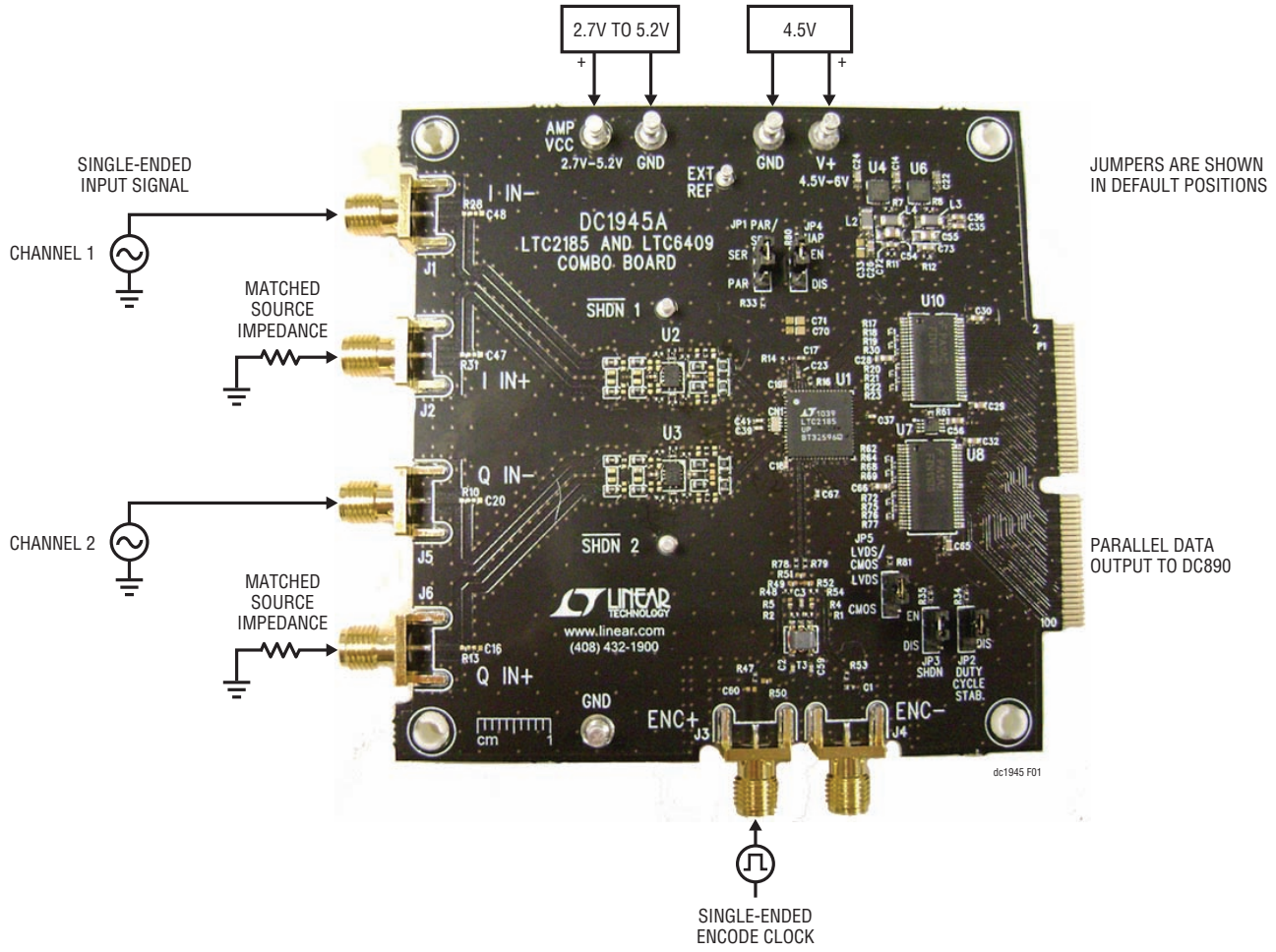


Figure 1. DC1945A Setup

HARDWARE SETUP

SMAs:

J1 I IN$^-$: Negative analog input for channel 1. Apply the analog signal of interest to this SMA. For a single-ended signal a matching impedance should be connected on the positive input of channel 1 (J2) for proper balance. Use this channel when using a single-ended input.

J2 I IN$^+$: Positive analog input for channel 1. Apply the analog signal of interest to this SMA. Terminate this channel to an impedance that matches I IN$^-$ when using a single-ended input on J1. If J2 is being driven single-ended, a matching impedance should be connected on the negative input of channel 1 (J1) for proper balance.

J5 Q IN$^-$: Negative analog input for channel 2. Apply the analog signal of interest to this SMA. For a single-ended signal a matching impedance should be connected on the positive input of channel 2 (J6) for proper balance. Use this channel when using a single-ended input.

J6 Q IN$^+$: Positive analog input for channel 2. Apply the analog signal of interest to this SMA. Terminate this channel to an impedance that matches Q IN$^-$ when using a single-ended input on J5. If J6 is being driven single-ended, a matching impedance should be connected on the negative input of channel 2 (J5) for proper balance.

J3 ENC$^+$: Positive encode clock input. As a default the demo board is populated to accept a single-ended clock input from a DC1075A demo board, or an equivalent CMOS signal. For other population options see the encode clock section of this manual.

J4 ENC$^-$: Negative encode clock input. As a default this input port is grounded to accommodate the single-ended clock drive. For other population options see the encode clock section of this manual.

Turrets:

V$^+$: Positive input voltage for the ADC and digital buffers. This voltage feeds a regulator that supplies the proper voltages for the ADC and buffers. The voltage range for this turret is 4.5V up to 6V.

AMP V_{CC}: Voltage supply for the amplifiers. This voltage input is unregulated, and supplies the two amplifiers directly. The voltage range for this turret is 2.7V to 5.2V. The recommended voltage is 3.3V.

EXT REF: Optional reference programming voltage. This pin is connected directly to the SENSE pin of the ADC. If no external voltage is supplied this pin will be pulled to V_{DD} through a weak pull-up resistor. This will select the ±1V input range. Connect to GND to select the ±0.5V input range, an external reference between 0.625V and 1.3V will select an input range of ±0.8 • V_{SENSE}.

$\overline{\text{SHDN1}}$: Shutdown pin for the U2. As a default this pin is tied to Amp V_{CC} through 100kΩ. Connect this pin to GND to manually shutdown U2.

$\overline{\text{SHDN2}}$: Shutdown pin for the U3. As a default this pin is tied to Amp V_{CC} through 100kΩ. Connect this pin to GND to manually shutdown U3.

GND: Ground connection. This demo board only has a single ground plane. This turret should be tied to the GND terminal of the power supply being used.

Jumpers:

The DC1945A demonstration circuit board should have the following jumper settings as default positions (as per Figure 1) which configures the ADC in serial programming mode. In the default configuration JP3 to JP6 should be left in the default locations. This will pull those pins high through weak pull-up resistors so that the SPI commands can be sent from the PC. When JP2 is set to PAR, then jumpers JP3 to JP6 can be configured manually.

JP1 PAR/SER: Selects parallel or serial programming mode. (Default: serial)

JP2 Duty Cycle Stab: In parallel programming mode enables or disables duty cycle stabilizer. In serial programming mode, pull up to V_{DD}. (Default: Enable or pull-up)

JP3 SHDN: In parallel programming mode enables or disables LTC2185. In serial programming mode, pull-up to V_{DD}. (Default: Enable or pull-up)

JP4 NAP: In parallel programming mode enables or disables NAP mode. In serial programming mode, pull up to V_{DD}. (Default: Enable or pull-up)

JP5 LVDS/CMOS: In parallel programming mode selects between LVDS or CMOS output signaling. In serial programming mode, pull up to V_{DD}. (Default: LVDS or pull-up) Note: CMOS mode not supported on the DC1945 demo board.

APPLYING POWER & SIGNALS TO THE DC1945A DEMONSTRATION CIRCUIT

If a DC890 is used to acquire data from the DC1945A, the DC890 must FIRST be connected to a powered USB port or provided an external 6V to 9V. Make this connection BEFORE applying 4.5V to 6V across the pins marked V^+ and GND, or 2.7V to 5.2V on the AMP_VCC pin on the DC1945A. DC1945A requires 4.5V on the ADC input for proper operation, regulators on the board produce the voltages required for the ADC. **The voltage applied to the amplifier is not regulated.** The DC1945A demonstration circuit requires up to 150mA on the ADC input depending on the sampling rate and the A/D converter supplied, and up to 150mA on the amplifier power input.

The DC890 data collection board is powered by the USB cable and does not require an external power supply unless it must be connected to the PC through an unpowered hub—in which case, it must be supplied an external 6V to 9V on turrets G7(+) and G1(–) or the adjacent 2.1mm power jack.

ANALOG INPUT NETWORK

The input network of the DC1945 can be modified to accommodate various applications. In the default setup both of the inputs are brought out to SMA connectors so the demo board can be driven with a differential source. To drive the demo board with a single-ended source simply drive J1 or J5 and terminate J2 or J6 with the matched source impedance of the signal source.

As a default the DC1945 is populated with no filtering between the input SMAs and the ADC. This allows a custom filter to be designed and installed between the amplifier and ADC. There are also pads for a filter before the amplifier itself. The gain of the amplifier can also be changed by varying the feedforward and feedback resistors. For optimal distortion and noise performance, the filter network can be implemented for different analog input frequencies after the LTC6409. Be sure not to overdrive the ADC by setting the gain too high; refer to the LTC6409 data sheet for resistor value considerations.

The DC1945 can also be used to sample I and Q channels of a signal, and through the PScope software these channels can be processed to get image rejection in one of the channels. This requires the I channel (J1 and J2) and the Q channel (J5 and J6) be driven with the same demodulated signal.

In almost all cases, off-board filters will be required on both analog input and encode clock to produce maximum SNR.

The off-board filters should be located close to the SMA inputs to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to obtain low distortion.

ENCODE CLOCK

Apply an encode clock to the SMA connector on the DC1945A demonstration circuit board marked J3. As a default, the DC1945A is populated to have a single-ended input.

For the best noise performance, the ENCODE INPUT must be driven with a very low jitter, square wave source. The amplitude should be large, up to $3V_{PP}$ or 13dBm. When using a sinusoidal signal generator, a squaring circuit can be used. Linear Technology also provides DC1075A, a demo board that divides a high frequency sine wave by four, producing a low jitter square wave for best results with the LTC2185.

Using bandpass filters on the clock and the analog input will improve the noise performance by reducing the wideband noise power of the signals. In the case of the DC1945A, a bandpass filter used for the clock should be used prior to the DC1075A. Data sheet FFT plots are taken with 10 pole LC filters made by TTE (Los Angeles, CA) to suppress signal generator harmonics, nonharmonically related spurs and broadband noise. Low phase noise Agilent 8644B generators are used with TTE bandpass filters for both the clock input and the analog input.

An internally generated conversion clock output is available on P1, which could be collected via a logic analyzer, or other data collection system if populated with a SAMTEC MEC8-150 type connector or collected by the DC890 QuikEval II data acquisition board using PScope™ software.

The clock network on the DC1945 can support a variety of clock inputs. As a default it is populated to accept a single-ended square wave clock from a DC1075 or appropriate signal generator. This will drive the ENC^+ pin single-ended and the ENC^- pin on the ADC is tied to GND.

When using a single-ended sine wave generator to drive the encode input of the ADC, it is best to use a single-ended to differential translation circuit. To modify the DC1945 to accommodate this first move the 0Ω resistor populated in position R47 to position R50, and move R54 and R48 to the R4 and R5 locations. This will direct the signal through the transformer T3 which will do the single-ended to differential translation.

When using a PECL or LVDS clock you can drive the DC1945 differentially through J3 and J4. From the default population, remove the 0Ω resistor in the C1 position and add the appropriate termination for your clock signal. R46, R55, R49, R51 and R52 are available to provide the proper termination for LVDS, PECL, or CML signaling. Blocking capacitors can be installed in the R78 and R79 positions if the common mode voltage of the clock is not compatible with the LTC2185.

SOFTWARE

The DC890 is controlled by the PScope system software provided or downloaded from the Linear Technology website at http://www.linear.com/software/. If a DC890 was provided, follow the DC890 Quick Start Guide and the instructions below.

To start the data collection software if PScope.exe is installed (by default) in \Program Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC1945A demonstration circuit is properly connected to the DC890, PScope should automatically detect the DC1945A, and configure itself accordingly. If necessary, the following procedure explains how to manually configure PScope.

Under the Configure menu, go to ADC Configuration. Check the Config Manually box and use the following configuration options (see Figure 2).

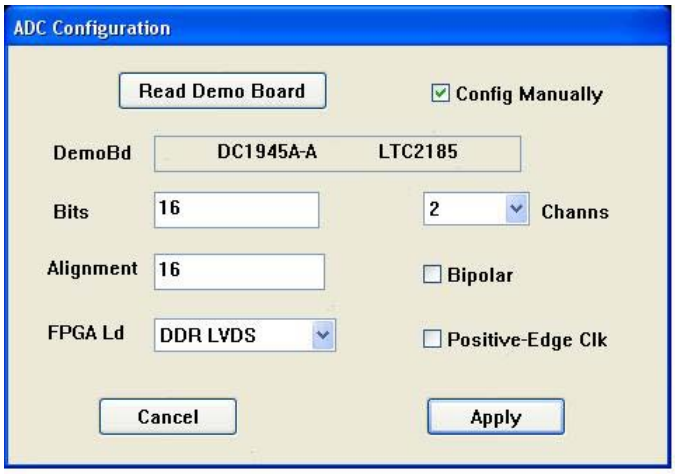


Figure 2. ADC Configuration

Manual Configuration Settings:

Bits: 16

Alignment: 16

FPGA Ld: DDR LVDS

Channs: 2

Bipolar: Unchecked

Positive-Edge Clk: Unchecked

Figure 2: ADC configuration

If everything is hooked up properly, powered and a suitable encode clock is present, clicking the Collect button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC890B Quick Start Guide and in the online help available within the PScope program itself.

SERIAL PROGRAMMING

PScope has the ability to program the DC1945A board serially through the DC890. There are several options available in the LTC2185 family that are only available through serially programming. PScope allows all of these features to be tested.

These options are available by first clicking on the Set Demo Bd Options icon on the PScope toolbar (Figure 3).

Figure 3. PScope Toolbar

SOFTWARE

This will bring up the menu shown in Figure 4.

This menu allows any of the options available for the LTC2185 family to be programmed serially. The LTC2185 family has the following options:

Power Control: Selects between normal operation, nap and sleep modes

- Normal (default): Entire ADC is powered and active
- Nap: ADC core powers down while references stay active
- Shutdown: The entire ADC is powered down

Clock Inversion: Selects the polarity of the CLKOUT signal

- Normal (default): Normal CLKOUT polarity
- Inverted: CLKOUT polarity is inverted

Clock Delay: Selects the phase delay of the CLKOUT signal

- 0 Deg (default): No CLKOUT delay
- 45 Deg: CLKOUT delayed by 45 degrees
- 90 Deg: CLKOUT delayed by 90 degrees
- 135 Deg: CLKOUT delayed by 135 degrees

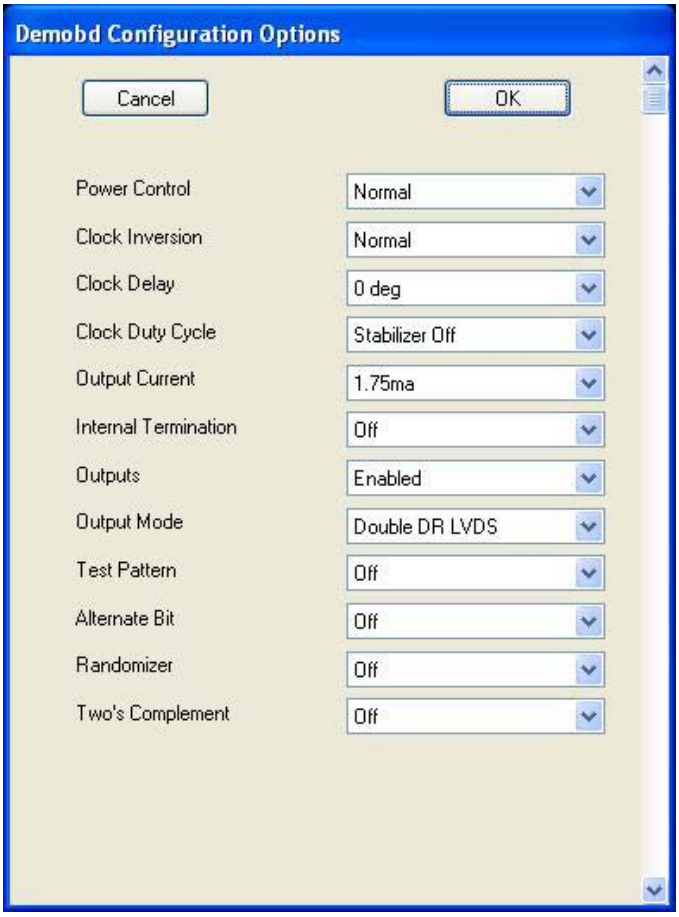


Figure 4. Demobd Configuration Options

SOFTWARE

Clock Duty Cycle: Enable or disables duty cycle stabilizer

- Stabilizer off (default): Duty cycle stabilizer disabled
- Stabilizer on: Duty cycle stabilizer enabled

Output Current: Selects the LVDS output drive current.

- 1.75mA (default): LVDS output driver current
- 2.1mA: LVDS output driver current
- 2.5mA: LVDS output driver current
- 3mA: LVDS output driver current
- 3.5mA: LVDS output driver current
- 4mA: LVDS output driver current
- 4.5mA: LVDS output driver current

Internal Termination: Enables LVDS internal termination.

- Off (default): Disables internal termination
- On: Enables internal termination

Outputs: Enables Digital Outputs

- Enabled (default): Enables digital outputs
- Disabled: Disables digital outputs

Output Mode: Selects digital output mode

- Full Rate: Full rate CMOS output mode. This mode is not supported by the DC1945A.
- Double LVDS (default): Double data rate LVDS output mode
- Double CMOS: Double data rate CMOS output mode. This mode is not supported by the DC1945A.

Test Pattern: Selects digital output test patterns

- Off (default): ADC data presented at output
- All Out =1: All digital outputs are 1
- All Out = 0: All digital outputs are 0
- Checkerboard: OF and D13-D0 alternate between 101 0101 1010 0101 and 010 1010 0101 1010 on alternating samples
- Alternating: Digital outputs alternate between all 1's and all 0's on alternating samples

Alternate Bit: Alternate bit polarity (ABP) mode

- Off (default): Disables alternate bit polarity
- On: Enables alternate bit polarity. Before enabling ABP, be sure the part is in offset binary mode

Randomizer: Enables data output randomizer

- Off (default): Disables data output randomizer
- On: Enables data output randomizer

Two's complement: Enables two's complement mode

- Off (default): Selects offset binary mode
- On: Selects two's complement mode

Once the desired settings are selected, hit OK and PScope will automatically update the register of the device on the DC1945A demo board.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	CN1	CAPACITOR ARRAY, 4 ELEMENT, 2.2µF, 4V, 20%, X7S	AVX, W2L14Z225MAT1A
2	7	C1, R47, R48, R53, R54, R78, R79	RES., CHIP, 0Ω, 1/16W, 0402	YAGEO, RC0402JR-070RL
3	5	C2, C3, C13, C59, C61	CAP., X7R, 0.01µF, 16V, 10%, 0402	AVX, 0402YC103KAQ2A, 2rls
4	19	C4, C15, C16, C20, C21, C25, C42-C44, C47-C52, C57, C58, C60, C62	CAP., OPT, 0402	OPTION
5	2	C5, C53	CAP., X7R, 0.01µF, 50V, 10%, 0402	TDK, C1005X7R1H103K
6	15	C6, C7, C26, C27-C32, C34-C36, C56, C65, C66	CAP., X7R, 0.1µF, 50V, 10%, 0603	TDK, C1608X7R1H104K
7	4	C8, C9, C10, C11	CAP., COG, 0.5pF, 50V, ±0.1pF, 0201	TDK, C0603C0G1H0R5B
8	1	C12	CAP., X5R, 4.7µF, 16V, 10%, 1210	MURATA, GRM32RR61C475KC01L
9	4	C14, C22, C72, C73	CAP., X7R, 1µF, 16V, 10%, 0603	NIC, NMC0603X7R105K16TRPF
10	2	C17, C23	CAP., X5R, 2.2µF, 6.3V, 20%, 0402	AVX, 04026D225MAT2A
11	5	C18, C19, C37, C39, C41	CAP., X5R, 0.1µF, 10V, 10%, 0402	TDK, C1005X5R1A104K
12	1	C24	CAP., X5R, 4.7µF, 6.3V, 20%, 0603	TDK, C1608X5R0J475MT
13	0	C33, C70, C71	CAP., OPT, 0603	OPTION
14	4	C45, C46, C63, C64	CAP., X7R, 0.1µF, 50V, 10%, 0402	TDK, C1005X7R1H104K
15	2	C54, C55 (BAL TO 1466B)	CAP., X5R, 10µF, 16V, 10%, 0805	AVX, 0805YD106KAT2A
16	3	C67, C68, C69	CAP., NPO, 22pF, 16V, 5%, 0402	AVX, 0402YA220JAT2A
17	3	E1, E7, E8	TEST POINT, TURRET, 0.061"	MILL-MAX, 2308-2-00-80-00-00-07-0
18	8	E2, E3, E4, E5, E6	TESTPOINT, TURRET, 0.094"	MILL-MAX, 2501-2-00-80-00-00-07-0
19	5	JP1, JP2, JP3, JP4, JP5	HEADER, 3 PIN, 0.079	SAMTEC, TMM-103-02-L-S
20	6	J1, J2, J3, J4, J5, J6	CON., SMA, 50Ω, EDGE-LAUNCH	EMERSON, 142-0701-851
21	0	L1, L5, L10, L13, L21	INDUCTOR, OPTION, 0603	OPTION
22	3	L2, L3, L4	FERRITE BEAD, 33Ω at 100MHz, 1206	MURATA, BLM31PG330SN1L
23	8	L6, L7, L8, L9, L16, L19, L20, L22	RES., CHIP, 0Ω, 1/10W, 0603	VISHAY, CRCW06030000Z0EA
24	4	L11, L12, L17, L18	RES., CHIP, 49.9Ω, 1/10W, 1%, 0603	NIC, NRC06F49R9TRF
25	4	L14, L15, L23, L24,	RES., CHIP, 100Ω, 1/10W, 1%, 0603	NIC, NRC06F1000TRF
26	4	MH1, MH2, MH3, MH4	STANDOFF, SNAP-ON	KEYSTONE, 8831
27	1	RN2	4 RES. ARRAY, 33Ω, 5%, 1/16W	VISHAY, CRA04S08333R0JTD
28	10	R1, R2, R38, R41, R42, R44, R65, R66, R73, R85	RES., CHIP, 49.9Ω, 1/16W, 1%, 0402	VISHAY, CRCW040249R9FKED
29	0	R3, R4, R5, R9, R10, R13, R15, R27, R28, R31, R37, R40, R43, R49-R52, R57, R60, R63, R74, R82, R84, R86, R87, R88	RES., CHIP, OPT, 0402	OPTION
30	1	R6	RES., CHIP, 10k, 1/16W, 5%, 0402	NIC, NRC04J103TRF
31	1	R7	RES., CHIP, 180k, 1/16W, 1%, 0402	VISHAY, CRCW0402180KFKED
32	1	R8	RES., CHIP, 330k, 1/16W, 1%, 0402	YAGEO, RC0402FR-07330KL
33	2	R11, R12	RES., CHIP, 3k, 1/16W, 1%, 0402	VISHAY, CRCW04023K00FKED
34	6	R14, R33, R34, R35, R80, R81	RES., CHIP, 1k, 1/16W, 5%, 0402	VISHAY, CRCW04021K00JNED
35	3	R16, R46, R55	RES., CHIP, 100Ω, 1/16W, 1%, 0402	VISHAY, CRCW0402100RFKED

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
36	17	R17-R23, R30, R61, R62, R64, R68, R69, R72, R75-R77	RES., CHIP, 100Ω, 1/20W, 5%, 0201	VISHAY, CRCW0201100RJNED
37	3	R24, R32, R36 (BAL TO 1968A)	RES., CHIP, 100k, 1/16W, 1%, 0402	YAGEO, RC0402FR-07100KL
38	3	R25, R26, R29 (BAL TO 1466B)	RES., CHIP, 4.99k, 1/10W, 1%, 0603	NIC, NRC06F4991TRF
39	4	R39, R45, R70, R71	RES., CHIP, 402Ω, 1/16W, 1%, 0402	VISHAY, CRCW0402402RFKED
40	4	R56, R59, R83, R89	RES., CHIP, 27.4Ω, 1/16W, 1%, 0402	VISHAY, CRCW040227R4FKED
41	2	R58, R67	RES., CHIP, 51.1Ω, 1/16W, 1%, 0402	VISHAY, CRCW040251R1FKED
42	1	T3	TRANSFORMER, RF~SMT~1:1 BALUN	MACOM, MABA-007159-000000
43	1	U1	I.C., 16-BIT ADC, QFN	LINEAR TECHNOLOGY, LTC2185IUP#PBF
44	2	U2, U3	I.C., HIGH SPEED DIFF. AMP./DRIVER, QFN	LINEAR TECHNOLOGY, LTC6409IUDB#PBF
45	2	U4, U6	I.C., LOW DROPOUT REGULATOR, 3×3mm, DFN	LINEAR TECHNOLOGY, LT3080EDD-1#PBF
46	1	U5	I.C., REMOTE 8-BIT I/O EXPANDER, SSOP-20	NXP, PCF8574TS/3,118
47	1	U7	I.C., LVDS REPEATER, US8	FAIRCHILD, FIN1101K8X
48	2	U8, U10	I.C., LVDS 8 PORT REPEATER, TSSOP	FAIRCHILD, FIN1108MTDX
49	1	U9 (BAL TO 1876A, 1074A & 1685A)	I.C., EEPROM, 2kB, 400kHz, 8TSSOP	MICROCHIP, 24LC025-I/ST
50	5	XJP1, XJP2, XJP3, XJP4, XJP5	SHUNT, 2mm	SAMTEC, 2SN-BK-G
51	1		FAB, PRINTED CIRCUIT BOARD	DEMO CIRCUIT 1945A (REV 1)
52	1		STENCIL SET (TOP & BOTTOM)	STENCIL DC1945A

SCHEMATIC DIAGRAM

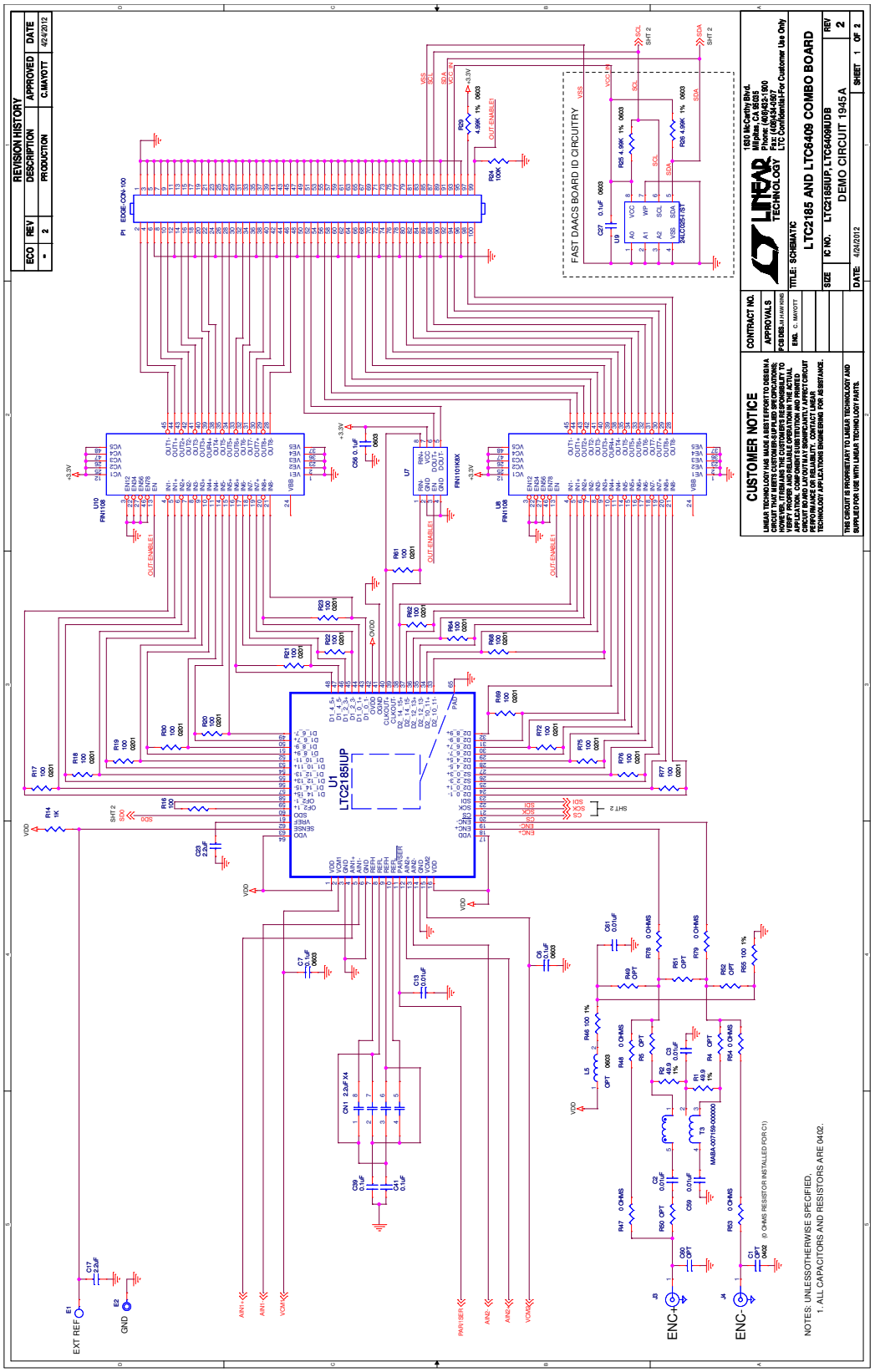


Figure 5. LTC2185 and LTC6409 Combo Board

SCHEMATIC DIAGRAM

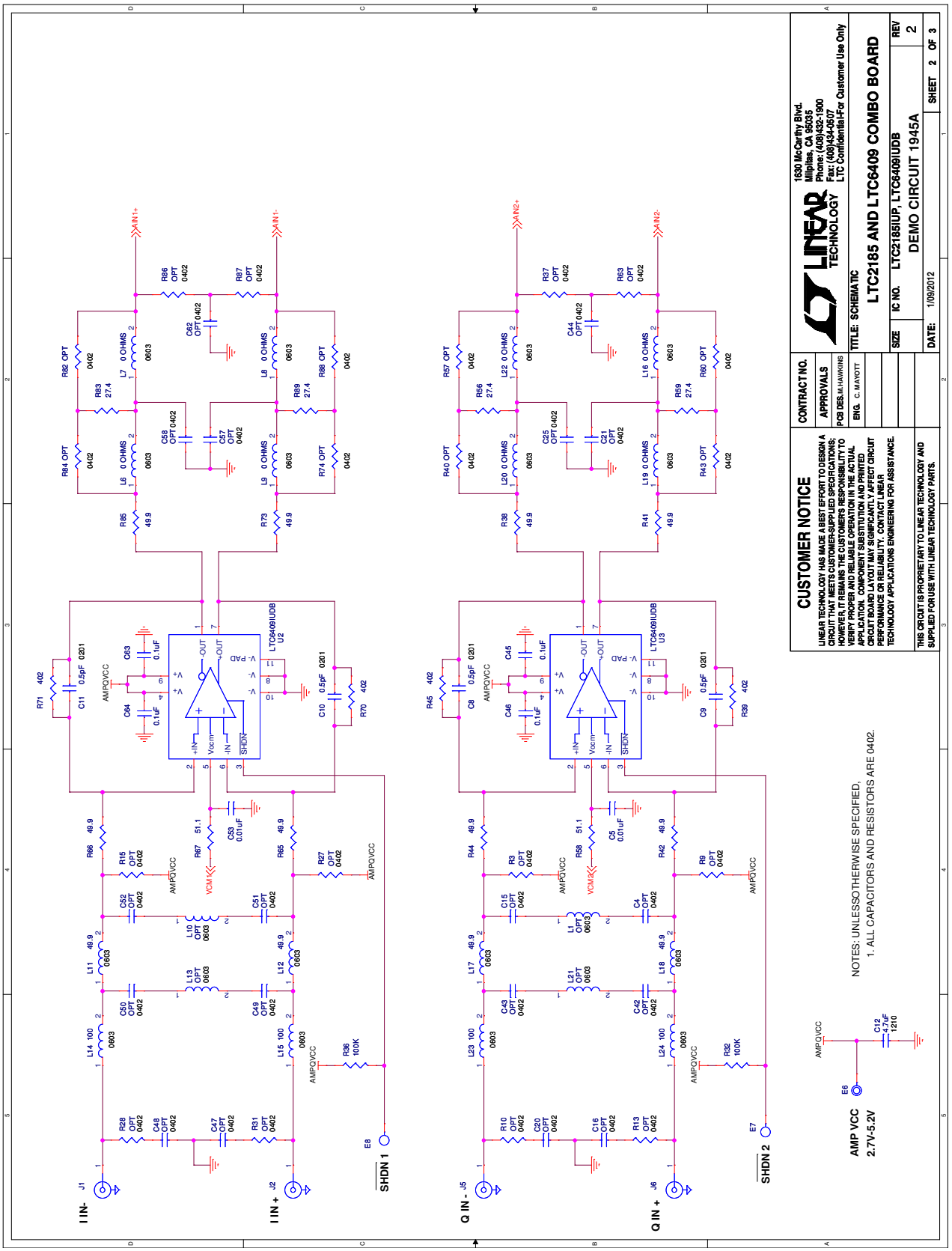


Figure 6. LTC2185 and LTC6409 Combo Board

SCHEMATIC DIAGRAM

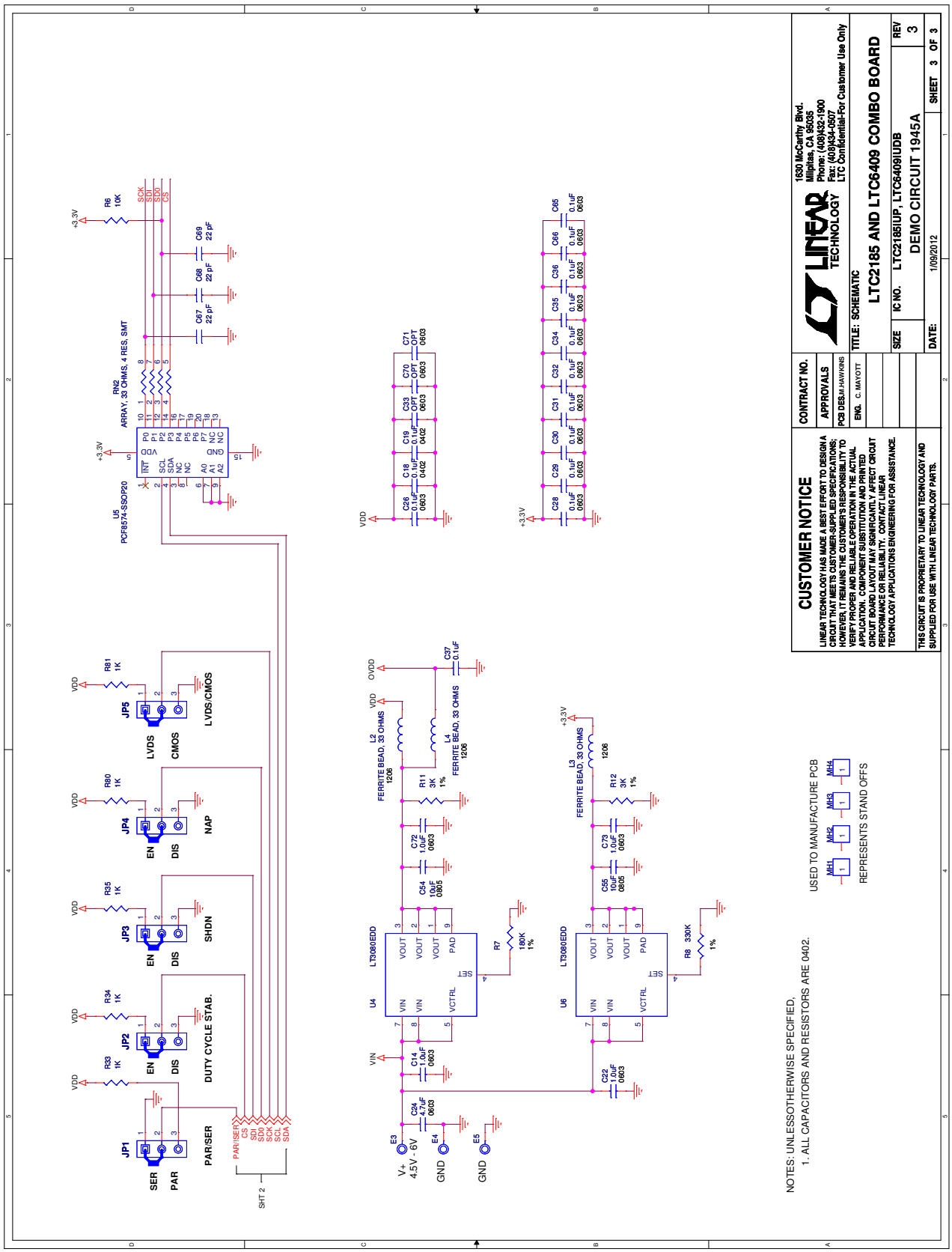


Figure 7. LTC2185 and LTC6409 Combo Board

DEMONSTRATION BOARD IMPORTANT NOTICE

Linear Technology Corporation (LTC) provides the enclosed product(s) under the following **AS IS** conditions:

This demonstration board (DEMO BOARD) kit being sold or provided by Linear Technology is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not provided by LTC for commercial use. As such, the DEMO BOARD herein may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including but not limited to product safety measures typically found in finished commercial goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may or may not meet the technical requirements of the directive, or other regulations.

If this evaluation kit does not meet the specifications recited in the DEMO BOARD manual the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY THE SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THIS INDEMNITY, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user releases LTC from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge. Also be aware that the products herein may not be regulatory compliant or agency certified (FCC, UL, CE, etc.).

No License is granted under any patent right or other intellectual property whatsoever. **LTC assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or any other intellectual property rights of any kind.**

LTC currently services a variety of customers for products around the world, and therefore this transaction **is not exclusive**.

Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

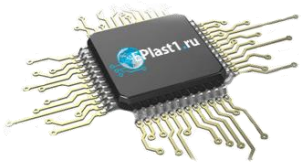
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.