Asymmetric Dual N-Channel 30V (D-S) Power MOSFET

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

APPLICATIONS

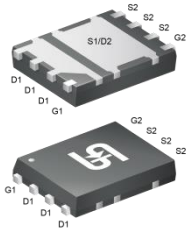
- IPC
- VGA
- NB VCORE

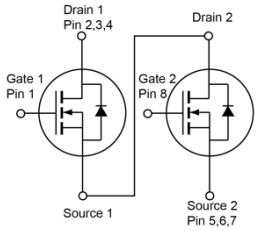
KEY PERFORMANCE PARAMETERS

PARAMETER		TYPE	VALUE	UNIT
V_{DS}		Q1	30	V
		Q2	30	
$R_{DS(on)}$ (max)	V_{GS} = 10V	Q1	11.7	mΩ
	V_{GS} = 4.5V		14.9	
	V_{GS} = 10V	Q2	3.6	
	V_{GS} = 4.5V		5.5	
Q_g		Q1	4.6	nC
		Q2	25	

Pb-Free RoHS COMPLIANT HALOGEN FREE

PDFN56 Asymmetric Dual





Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETER		SYMBOL	Q1	Q2	UNIT
Drain-Source Voltage		V_{DS}	30	30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	38	107	A
	T_A = 25°C		10	20	
Pulsed Drain Current		I_{DM}	152	428	A
Single Pulse Avalanche Current (Note 2)		I_{AS}	16	26	A
Single Pulse Avalanche Energy (Note 2)		E_{AS}	38	101	mJ
Total Power Dissipation	T_C = 25°C	P_D	30	69	W
	T_C = 125°C		6	14	
Total Power Dissipation	T_A = 25°C	P_D	2.2	2.4	W
	T_A = 125°C		0.4	0.5	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150		°C

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT		UNIT
		Q1	Q2	
Thermal Resistance – Junction to Case	$R_{\Theta JC}$	4.2	1.8	°C/W
Thermal Resistance – Junction to Ambient	$R_{\Theta JA}$	56	52	

Thermal Performance Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)							
PARAMETER	**CONDITIONS**	**SYMBOL**	**TYPE**	**MIN**	**TYP**	**MAX**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	BV_{DSS}	Q1	30	--	--	V
	V_{GS} = 0V, I_D = 250μA		Q2	30	--	--	
Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	$V_{GS(TH)}$	Q1	1.2	1.9	2.5	V
	V_{GS} = V_{DS}, I_D = 250μA		Q2	1.2	1.6	2.5	
Gate-Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	Q1	--	--	±100	nA
	V_{GS} = ±20V, V_{DS} = 0V		Q2	--	--	±100	nA
Drain-Source Leakage Current	V_{GS} = 0V, V_{DS} = 30V	I_{DSS}	Q1	--	--	1	μA
	V_{GS} = 0V, V_{DS} = 30V T_J = 125°C			--	--	100	
	V_{GS} = 0V, V_{DS} = 30V		Q2	--	--	1	
	V_{GS} = 0V, V_{DS} = 30V T_J = 125°C			--	--	100	
Drain-Source On-State Resistance (Note 3)	V_{GS} = 10V, I_D = 10A	$R_{DS(on)}$	Q1	--	8.8	11.7	mΩ
	V_{GS} = 4.5V, I_D = 9A			--	12.8	14.9	
	V_{GS} = 10V, I_D = 20A		Q2	--	2.7	3.6	
	V_{GS} = 4.5V, I_D = 16A			--	3.7	5.5	
Forward Transconductance (Note 3)	V_{DS} = 5V, I_D = 10A	g_{fs}	Q1	--	27	--	S
	V_{DS} = 5V, I_D = 20A		Q2	--	47	--	
Dynamic (Note 4)							
Total Gate Charge	Q1 V_{DS} = 15V, I_D = 10A Q2 V_{DS} = 15V, I_D = 20A	$Q_{g(VGS=10V)}$	Q1	--	9.3	--	nC
			Q2	--	49	--	
Total Gate Charge	Q1 V_{DS} = 15V, I_D = 9A Q2 V_{DS} = 15V, I_D = 16A	$Q_{g(VGS=4.5V)}$	Q1	--	4.6	--	
			Q2	--	25	--	
Gate-Source Charge		Q_{gs}	Q1	--	2.1	--	
			Q2	--	7.3	--	
Gate-Drain Charge		Q_{gd}	Q1	--	1.8	--	
			Q2	--	12	--	
Input Capacitance	Q1 V_{GS} = 0V, V_{DS} = 15V f = 1.0MHz Q2 V_{GS} = 0V, V_{DS} = 15V f = 1.0MHz	C_{iss}	Q1	--	555	--	pF
			Q2	--	2550	--	
Output Capacitance		C_{oss}	Q1	--	142	--	
			Q2	--	388	--	
Reverse Transfer Capacitance		C_{rss}	Q1	--	26	--	
			Q2	--	276	--	
Gate Resistance	f = 1.0MHz	R_g	Q1	0.5	1.6	3.2	Ω
			Q2	0.5	1.5	3	

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)							
PARAMETER	**CONDITIONS**	**SYMBOL**	**TYPE**	**MIN**	**TYP**	**MAX**	**UNIT**
Switching (Note 4)							
Turn-On Delay Time	Q1 V_{GS} = 10V, V_{DS} = 15V, I_D = 10A, R_G = 2Ω Q2 V_{GS} = 10V, V_{DS} = 15V, I_D = 20A, R_G = 2Ω	$t_{d(on)}$	Q1	--	4.8	--	ns
			Q2	--	11	--	
Turn-On Rise Time		t_r	Q1	--	65	--	
			Q2	--	79	--	
Turn-Off Delay Time		$t_{d(off)}$	Q1	--	8.2	--	
			Q2	--	32	--	
Turn-Off Fall Time		t_f	Q1	--	14	--	
			Q2	--	49	--	
Source-Drain Diode							
Forward Voltage (Note 3)	V_{GS} = 0V, I_S = 10A	V_{SD}	Q1	--	--	1.2	V
	V_{GS} = 0V, I_S = 20A		Q2	--	--	1	
Reverse Recovery Time	Q1 I_S = 10A, dI/dt = 100A/μs Q2 I_S = 20A, dI/dt = 100A/μs	t_{rr}	Q1	--	33	--	ns
			Q2	--	14	--	
Reverse Recovery Charge		Q_{rr}	Q1	--	19	--	nC
			Q2	--	8	--	

Notes:

1. Silicon limited current only.
2. Q1 : L = 0.3mH, V_{GS} = 10V, V_{DD} = 30V, R_G = 25Ω, I_{AS} = 16A, Starting T_J = 25°C
   Q2 : L = 0.3mH, V_{GS} = 10V, V_{DD} = 30V, R_G = 25Ω, I_{AS} = 26A, Starting T_J = 25°C
3. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
4. Switching time is essentially independent of operating temperature.

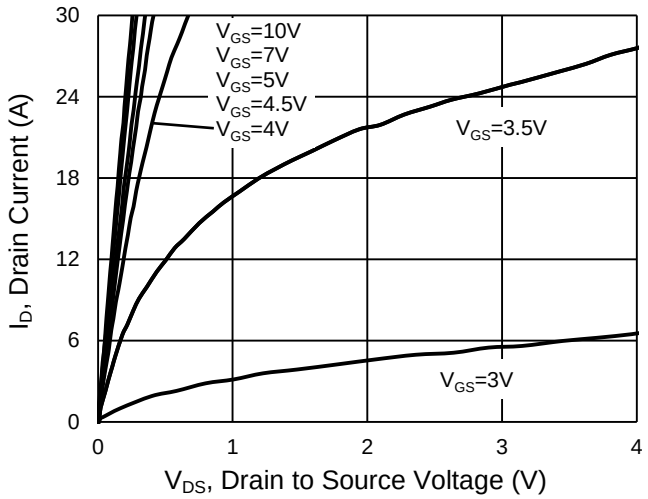
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM5055DCR RLG	PDFN56 Asymmetric Dual	2,500pcs / 13” Reel

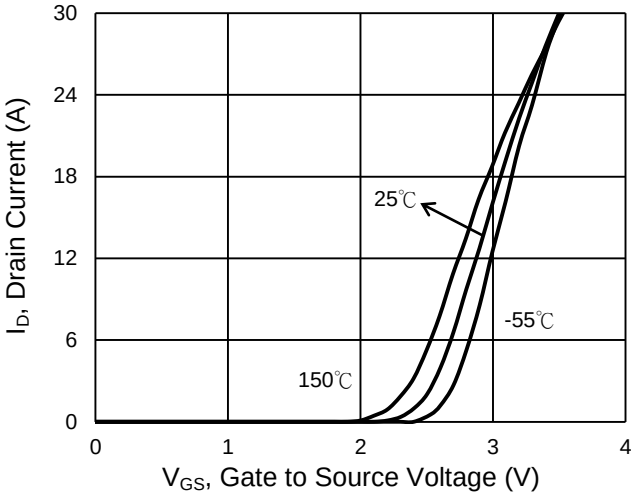
CHARACTERISTICS CURVES (Q1)

(T_A = 25°C unless otherwise noted)

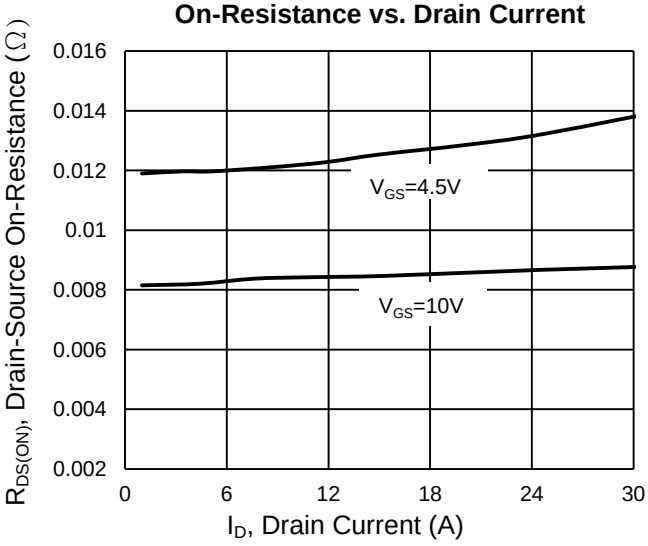
Output Characteristics



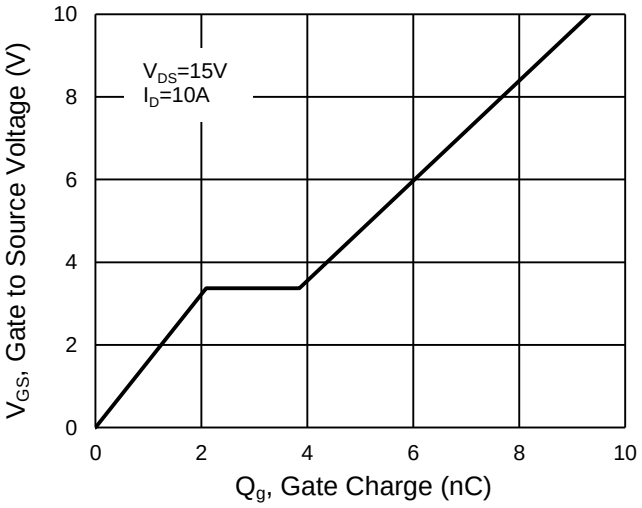
Transfer Characteristics



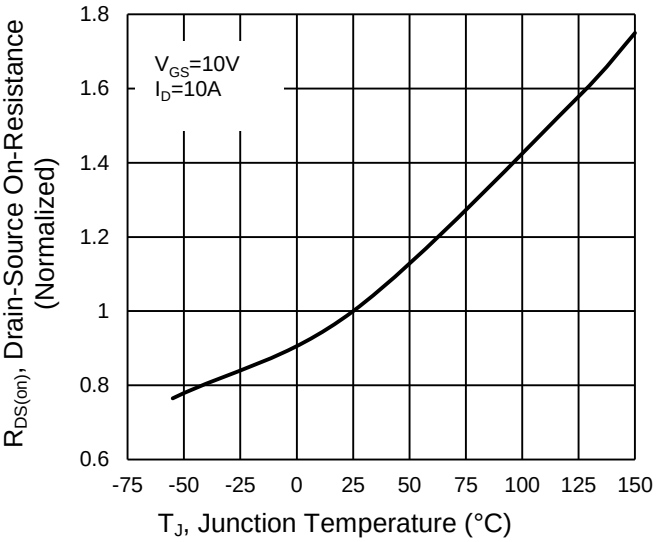
On-Resistance vs. Drain Current



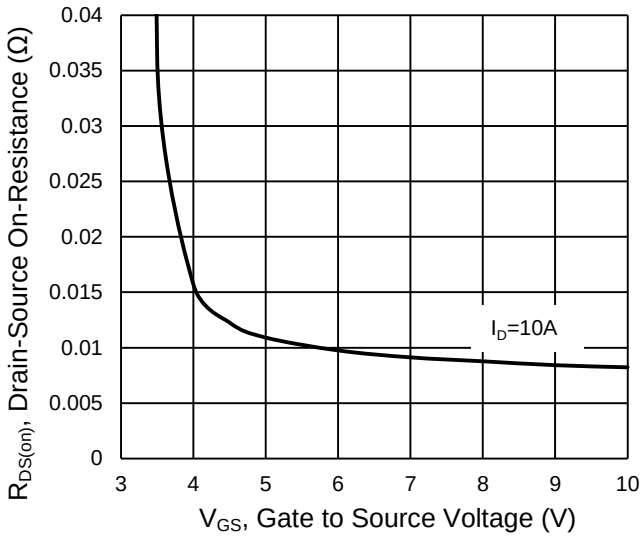
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



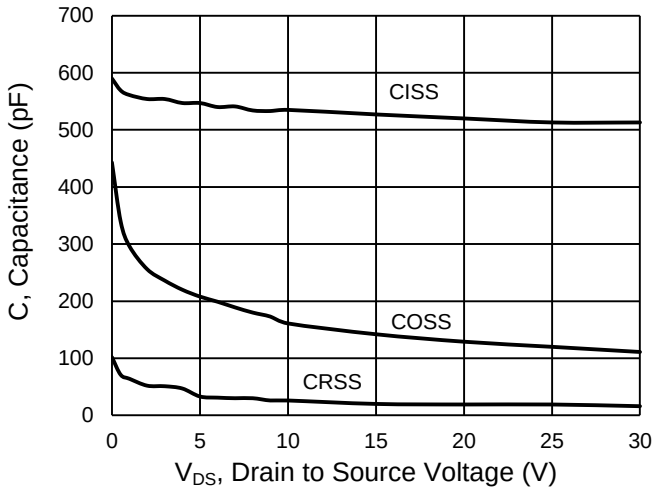
On-Resistance vs. Gate-Source Voltage



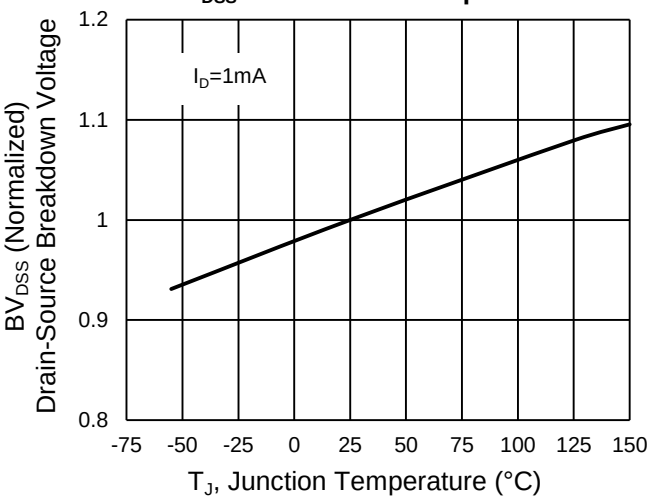
CHARACTERISTICS CURVES (Q1)

(T_A = 25°C unless otherwise noted)

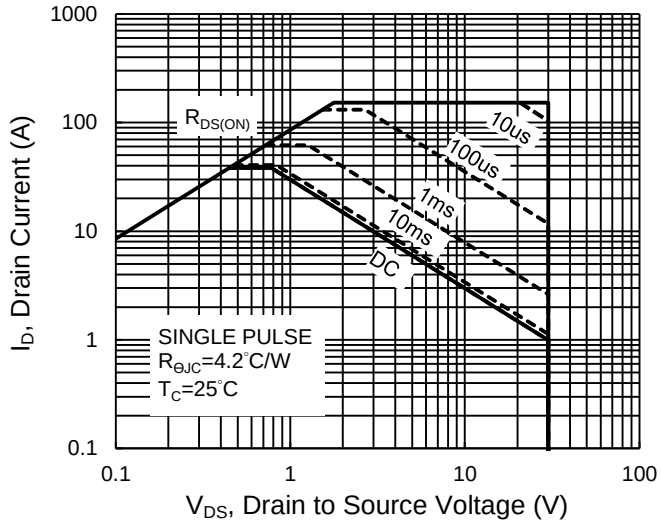
Capacitance vs. Drain-Source Voltage



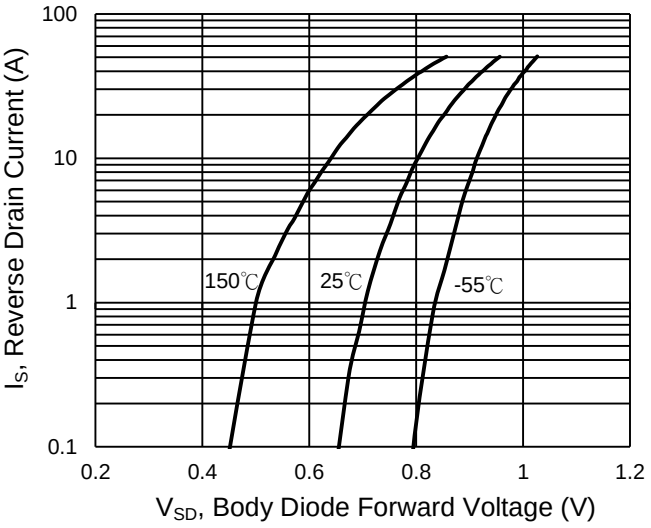
BV_{DSS} vs. Junction Temperature



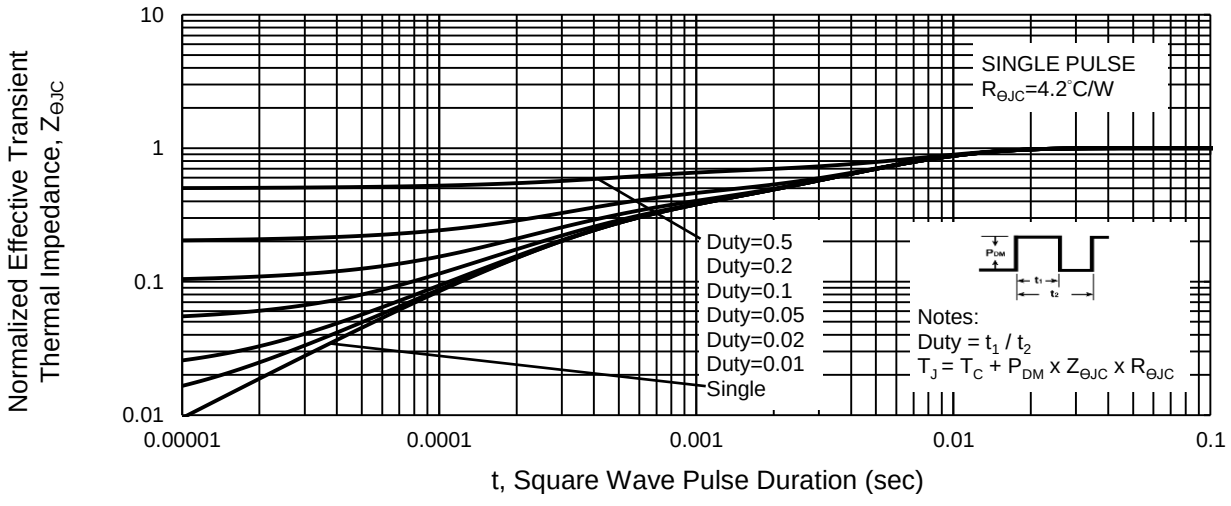
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



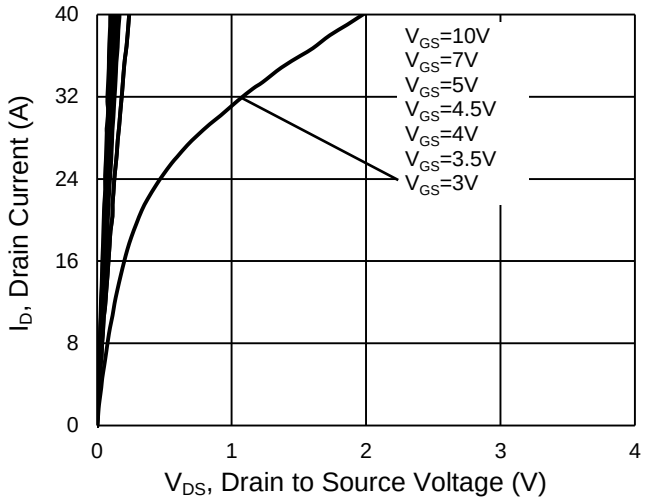
Normalized Thermal Transient Impedance, Junction-to-Case



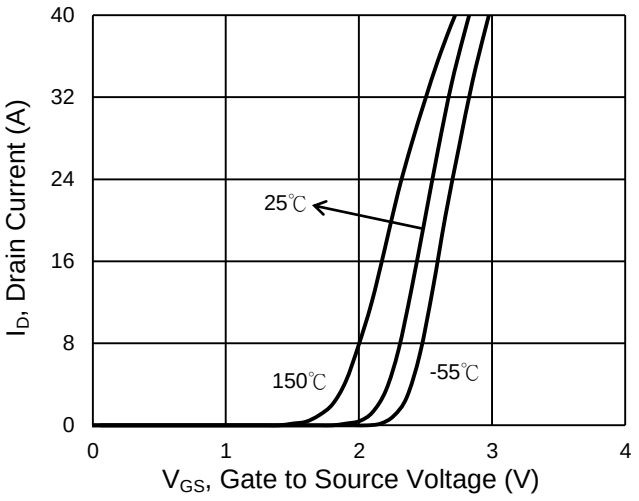
CHARACTERISTICS CURVES (Q2)

(T_A = 25°C unless otherwise noted)

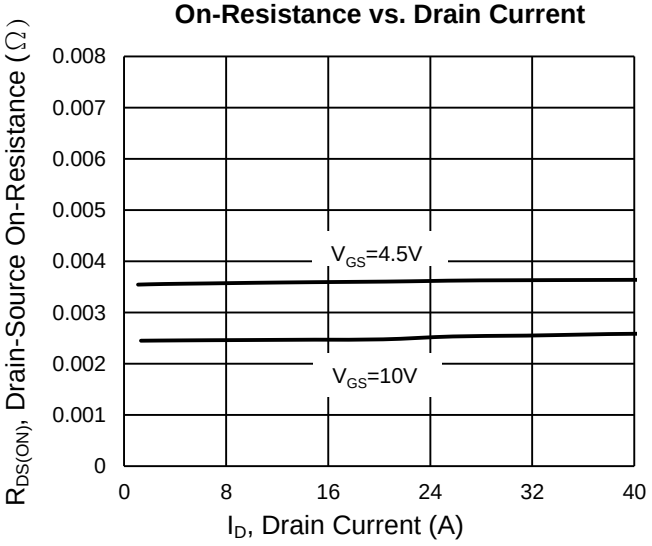
Output Characteristics



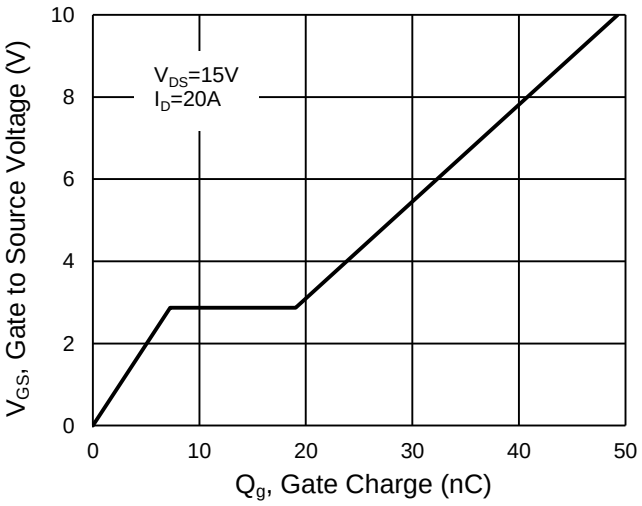
Transfer Characteristics



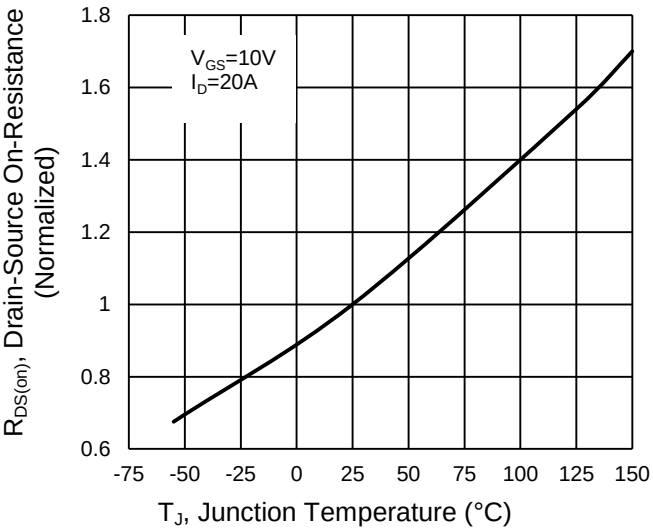
On-Resistance vs. Drain Current



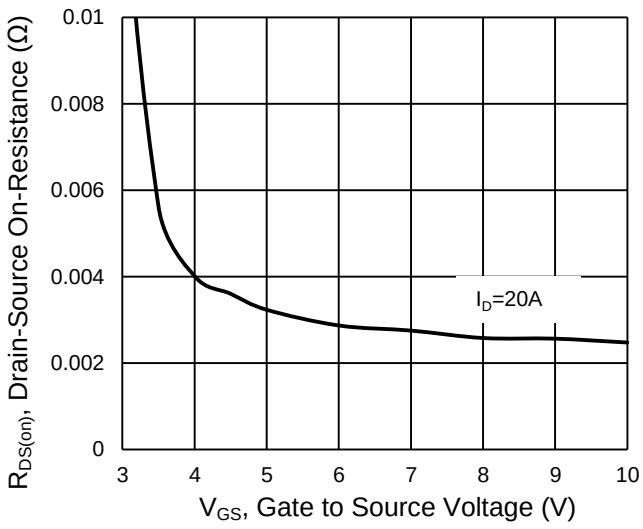
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



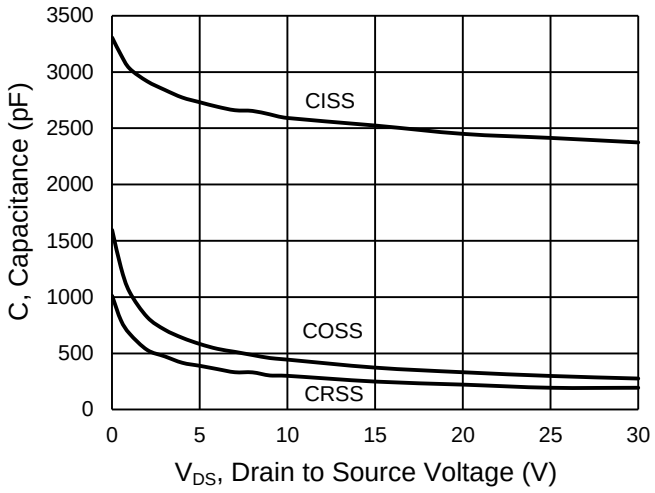
On-Resistance vs. Gate-Source Voltage



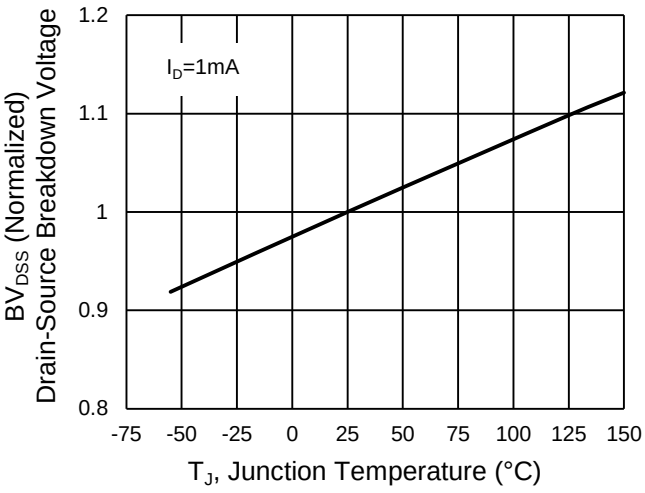
CHARACTERISTICS CURVES (Q2)

(T_A = 25°C unless otherwise noted)

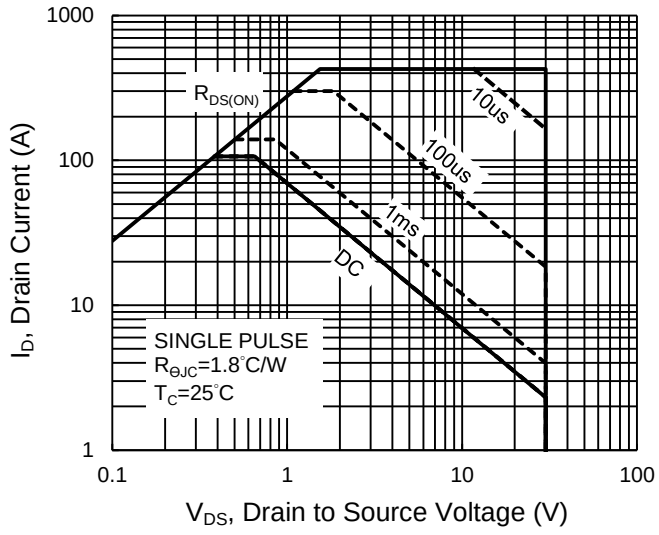
Capacitance vs. Drain-Source Voltage



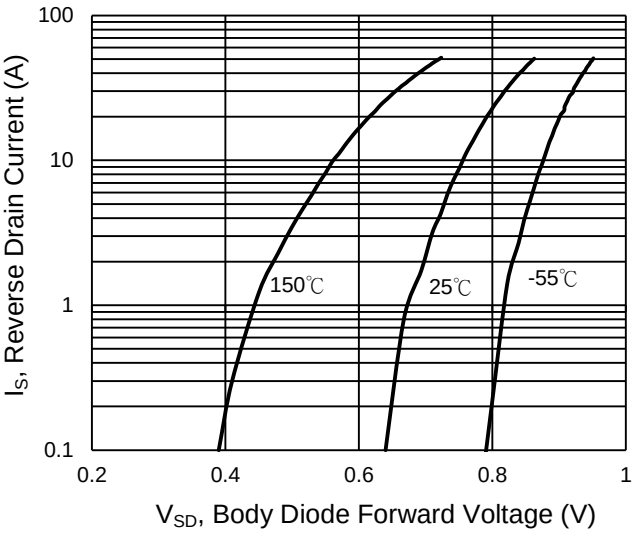
BV_{DSS} vs. Junction Temperature



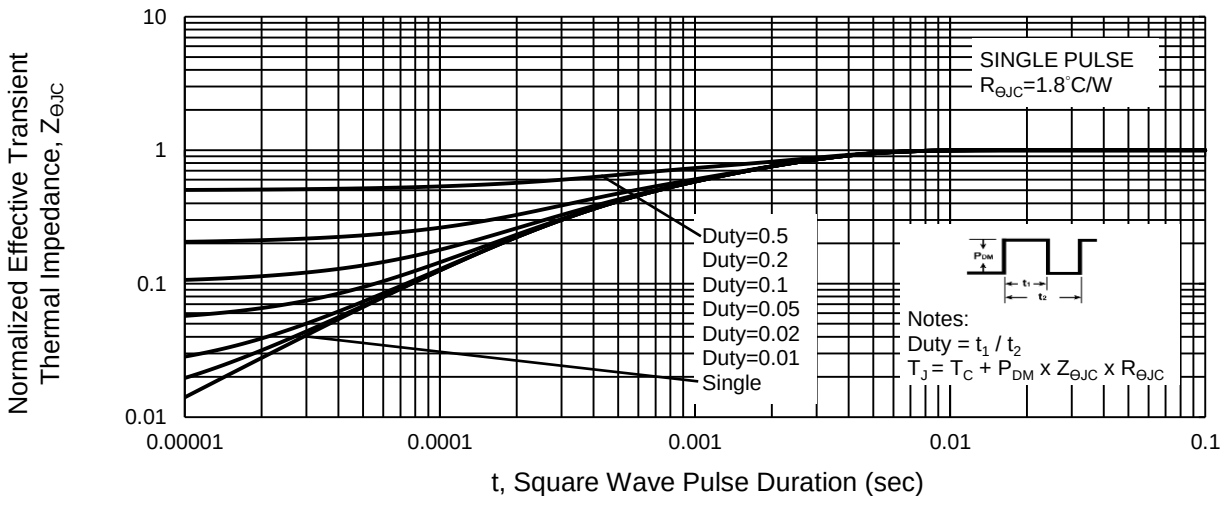
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

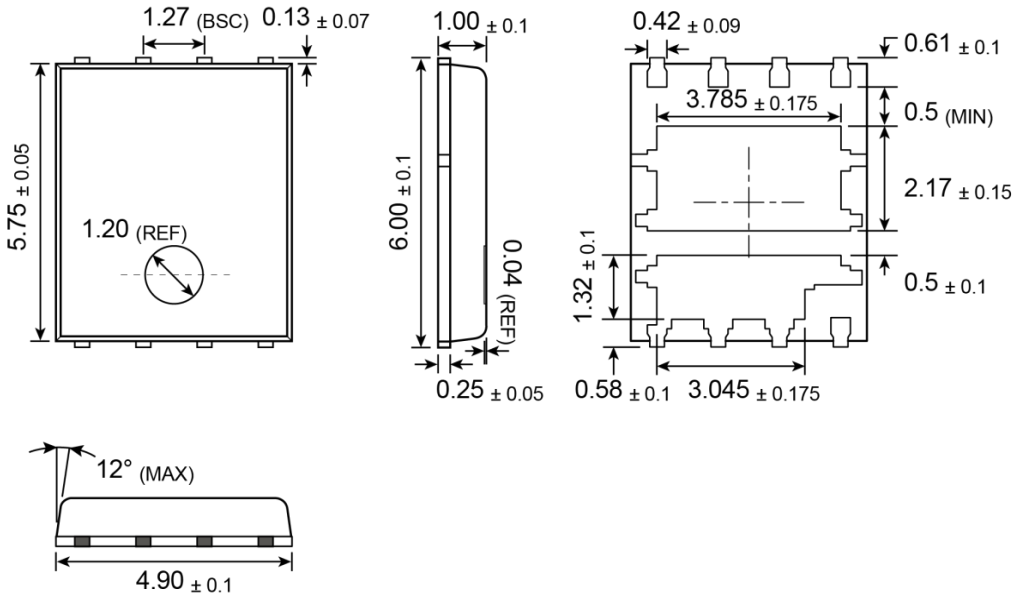


Normalized Thermal Transient Impedance, Junction-to-Case

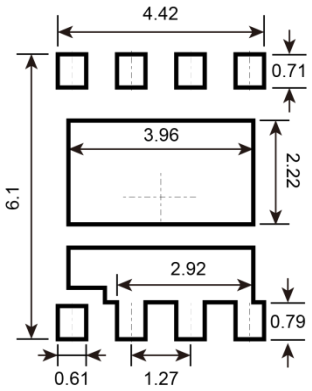


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56 Asymmetric Dual



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM

G = Halogen Free
Y = Year Code
WW = Week Code (01~52)
F = Factory Code

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- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
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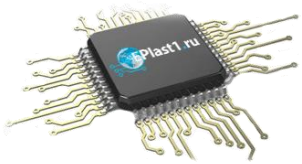
- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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