# **DISCRETE SEMICONDUCTORS**

# DATA SHEET

# BTA216X series D, E and F Three quadrant triacs guaranteed commutation

**Product specification** 

September 2018



# Three quadrant triacs guaranteed commutation

# BTA216X series D, E and F

#### **GENERAL DESCRIPTION**

Passivated guaranteed commutation triacs in a full pack, plastic envelope intended for use in motor control circuits or with other highly inductive loads. These devices balance the requirements of commutation performance and gate sensitivity. The "sensitive gate" E series and "logic level" D series are intended for interfacing with low power drivers, including micro controllers.

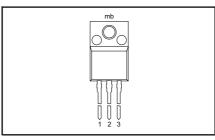
### **QUICK REFERENCE DATA**

SYMBOL	PARAMETER	MAX.	UNIT
V <sub>DRM</sub>	BTA216X- BTA216X- BTA216X- Repetitive peak off-state voltages	600D 600E 600F 600	V
I <sub>T(RMS)</sub>	RMS on-state current Non-repetitive peak on-state current	16 140	A A

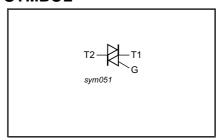
#### **PINNING - SOT186A**

PIN	DESCRIPTION			
1	main terminal 1			
2	main terminal 2			
3	gate			
case	isolated			

### PIN CONFIGURATION



### **SYMBOL**



#### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DRM}$	Repetitive peak off-state voltages		-	600¹	v
I <sub>T(RMS)</sub>	RMS on-state current Non-repetitive peak	full sine wave; $T_{hs} \le 38 ^{\circ}C$ full sine wave;	-	16	A
l²t dl <sub>⊤</sub> /dt	on-state current  I <sup>2</sup> t for fusing Repetitive rate of rise of on-state current after	$\begin{split} & T_{\rm j} = 25~^{\circ}\text{C prior to} \\ & \text{surge} \\ & t = 20~\text{ms} \\ & t = 16.7~\text{ms} \\ & t = 10~\text{ms} \\ & l_{\text{TM}} = 20~\text{A;} \ l_{\rm G} = 0.2~\text{A;} \\ & dl_{\rm G}/\text{dt} = 0.2~\text{Å/}\mu\text{s} \end{split}$		140 150 98 100	Α Α Α²s Α/μs
$\begin{matrix} I_{GM} \\ P_{GM} \\ P_{G(AV)} \end{matrix}$	triggering Peak gate current Peak gate power Average gate power Storage temperature Operating junction temperature	over any 20 ms period	- - -40 -	2 5 0.5 150 125	A W C C

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<sup>1</sup> Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15 A/ $\mu$ s.

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## **ISOLATION LIMITING VALUE & CHARACTERISTIC**

 $T_{hs}$  = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>isol</sub>	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65%; clean and dustfree	-	-	2500	V
C <sub>isol</sub>	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

## **THERMAL RESISTANCES**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R <sub>th j-hs</sub>	Thermal resistance junction to heatsink	full or half cycle with heatsink compound without heatsink compound	1 1		4.0 5.5	K/W K/W
R <sub>th j-a</sub>	Thermal resistance junction to ambient	in free air	-	55	-	K/W

### STATIC CHARACTERISTICS

T<sub>i</sub> = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.		MAX.		UNIT
		BTA216X-		D	Е	F	
I <sub>GT</sub>	Gate trigger current <sup>2</sup>	$V_{D} = 12 \text{ V}; I_{T} = 0.1 \text{ A}$					_
		T2+ G+   T2+ G-	-	5 5 5	10 10	25 25	mA mA
		T2- G-	_	5	10	25	mA
I <sub>L</sub>	Latching current	$V_D = 12 \text{ V}; I_{GT} = 0.1 \text{ A}$		15	05	20	A
		T2+ G+   T2+ G-	-	15 25	25 30	30 40	mA mA
		T2- G-	-	25	30	40	mA
I <sub>H</sub>	Holding current	$V_D = 12 \text{ V}; I_{GT} = 0.1 \text{ A}$	-	15	25	30	mA
					D, E, F	1	
$V_T$	On-state voltage	$I_{T} = 20 \text{ A}$	-		1.5		V
V <sub>GT</sub>	Gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}$	- 0.25		1.5		V
		$V_D = 400 \text{ V}; I_T = 0.1 \text{ A}; I_T = 125 °C$	0.23		-		
$I_D$	Off-state leakage current	$V_D = V_{DRM(max)}$ ; $T_j = 125  ^{\circ}C$	-		0.5		mA

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<sup>2</sup> Device does not trigger in the T2-, G+ quadrant.

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## **DYNAMIC CHARACTERISTICS**

T<sub>i</sub> = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS		MIN.		MAX.	UNIT
		BTA216X-	D	Е	F		
dV <sub>D</sub> /dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)};$ $T_j = 110  ^{\circ}C;$ exponential waveform; gate open	30	60	70	-	V/μs
dl <sub>com</sub> /dt	Critical rate of change of commutating current	circuit $V_{DM} = 400 \text{ V}; T_j = 125 ^{\circ}\text{C};$ $I_{T(RMS)} = 16 \text{ A};$ $dV_{com}/dt = 10 \text{V}/\mu\text{s};$ gate open circuit	2.5	6.2	18	-	A/ms
dI <sub>com</sub> /dt	Critical rate of change of commutating current	$\begin{array}{l} \text{Open circuit} \\ \text{V}_{\text{DM}} = 400 \text{ V; T}_{j} = 125 \text{ °C;} \\ \text{I}_{\text{T(RMS)}} = 16 \text{ A;} \\ \text{dV}_{\text{com}}/\text{dt} = 0.1 \text{V/}\mu\text{s; gate} \\ \text{open circuit} \end{array}$	12	20	50	1	A/ms

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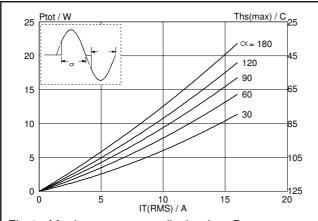


Fig.1. Maximum on-state dissipation,  $P_{tot}$ , versus rms on-state current,  $I_{T(RMS)}$ , where  $\alpha$  = conduction angle.

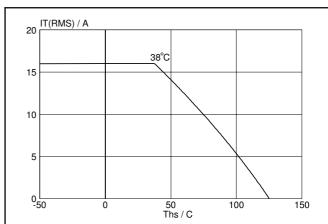


Fig.4. Maximum permissible rms current  $I_{T(RMS)}$ , versus heatsink temperature  $T_{hs}$ .

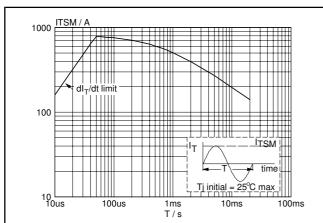


Fig.2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \le 20$ ms.

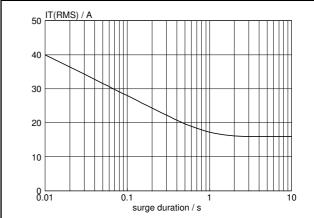


Fig.5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents, f = 50 Hz;  $T_{hs} \le 38 \, ^{\circ}\text{C}$ .

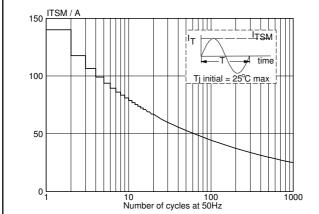


Fig.3. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents, f = 50 Hz.

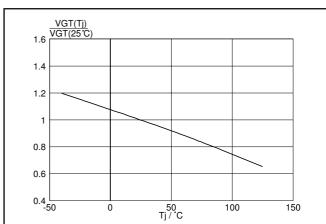
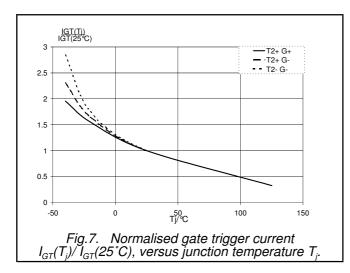


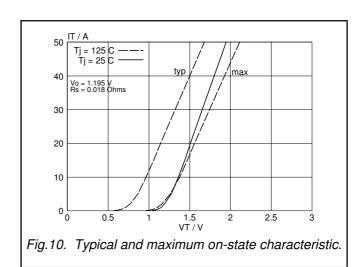
Fig.6. Normalised gate trigger voltage  $V_{GT}(T_j)/V_{GT}(25^{\circ}C)$ , versus junction temperature  $T_{j}$ .

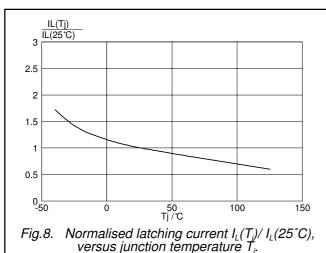
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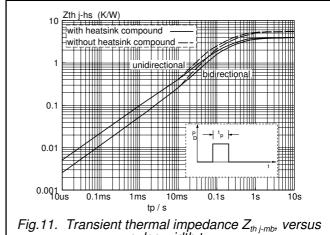
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IH(Tj) 3 IH(25°C) 0.5 0<sub>-50</sub> 50 Tj /℃ 150

pulse width t<sub>o</sub>.

 F TYPE E TYPE D TYPE

140

dlcom/dt (A/ms)

100

20



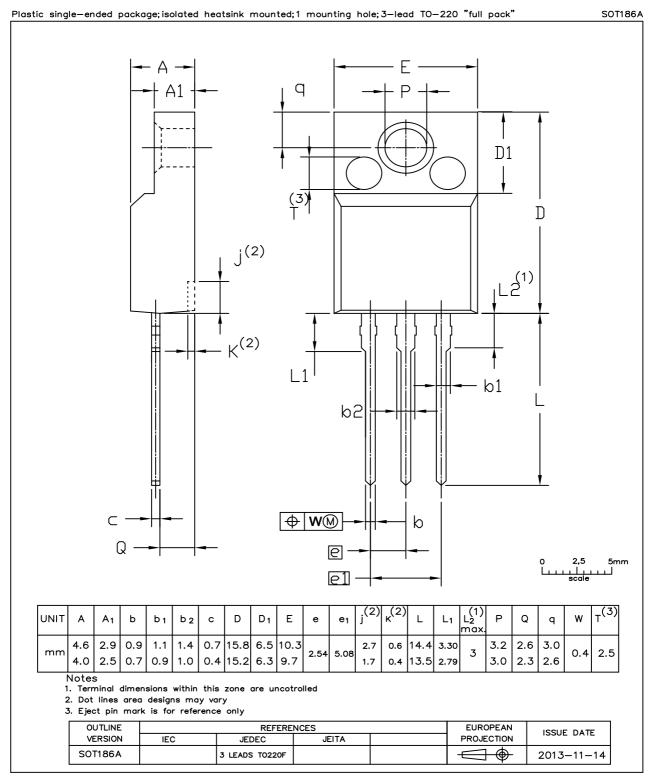
Tj/°C

Fig.9. Normalised holding current  $I_H(T_i)/I_H(25^{\circ}C)$ , versus junction temperature  $T_i$ .

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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