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FAIRCHILD SEMICONDUCTOR®

January 2013

# FDN537N

## Single N-Channel Power Trench® MOSFET

### 30 V, 6.5 A, 23 mΩ

### Features

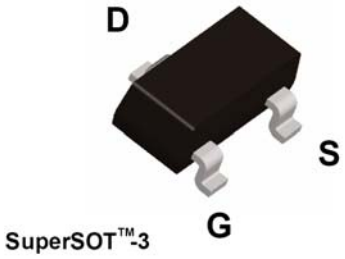
- Max $r_{DS(on)}$ = 23 mΩ at $V_{GS}$ = 10 V, $I_D$ = 6.5 A
- Max $r_{DS(on)}$ = 36 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 6.0 A
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL Tested
- RoHS Compliant

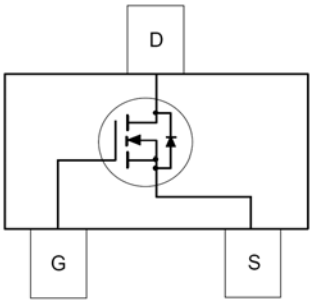
### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

### Application

- Primary DC-DC Switch




## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | 30 | V |
| $V_{GS}$ | Gate to Source Voltage | (Note 3) | ±20 | V |
| $I_D$ | Drain Current -Continuous (Package limited) $T_C$ = 25 °C | | 8.0 | A |
| | -Continuous $T_A$ = 25 °C | (Note 1a) | 6.5 | |
| | -Pulsed | | 25 | |
| $P_D$ | Power Dissipation | (Note 1a) | 1.5 | W |
| | Power Dissipation | (Note 1b) | 0.6 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | -55 to +150 | °C |

### Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1a) | 80 | °C/W |
| | Thermal Resistance, Junction to Ambient | (Note 1b) | 180 | |

### Package Marking and Ordering Information

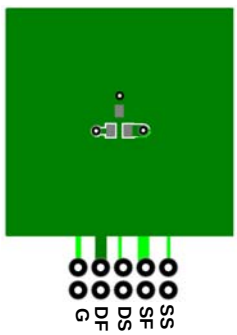
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| 537 | FDN537N | SSOT-3 | 7 ” | 8 mm | 3000 units |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | 18 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1.2 | 1.8 | 3.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | -6 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 6.5 A | | 19 | 23 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 6.0 A | | 25 | 36 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 6.5 A, $T_J$ = 125 °C | | 25 | 30 | |
| $g_{FS}$ | Forward Transconductance | $V_{DD}$ = 5 V, $I_D$ = 6.5 A | | 24 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1 MHz | | 360 | 465 | pF |
| $C_{oss}$ | Output Capacitance | | | 143 | 180 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 22 | 35 | pF |
| $R_g$ | Gate Resistance | | | 1.0 | | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 6.5 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 5 | 10 | ns |
| $t_r$ | Rise Time | | | 1 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 11 | 19 | ns |
| $t_f$ | Fall Time | | | 1 | 10 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V; $V_{DD}$ = 15 V, $I_D$ = 6.5 A | | 6.0 | 8.4 | nC |
| | Total Gate Charge | $V_{GS}$ = 0 V to 4.5 V; $V_{DD}$ = 15 V, $I_D$ = 6.5 A | | 3.0 | 4.2 | nC |
| $Q_{gs}$ | Total Gate Charge | $V_{DD}$ = 15 V, $I_D$ = 6.5 A | | 1.2 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | $V_{DD}$ = 15 V, $I_D$ = 6.5 A | | 1.1 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 6.5 A (Note 2) | | 0.86 | 1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 6.5 A, di/dt = 100 A/μs | | 14 | 22 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 3 | 10 | nC |

NOTES:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.




a) 80 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper


b) 180 °C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

3. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

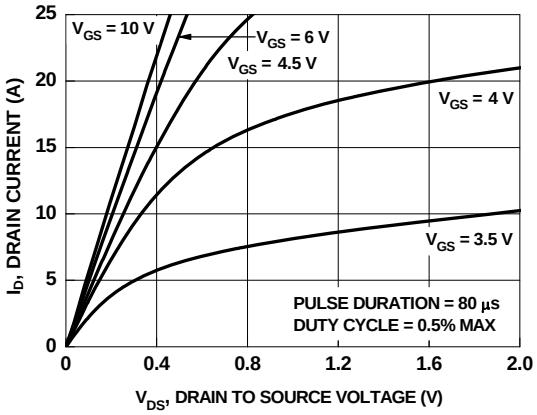



**Figure 1. On Region Characteristics**

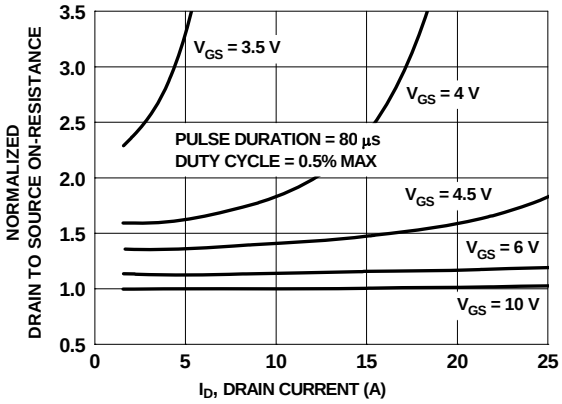



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

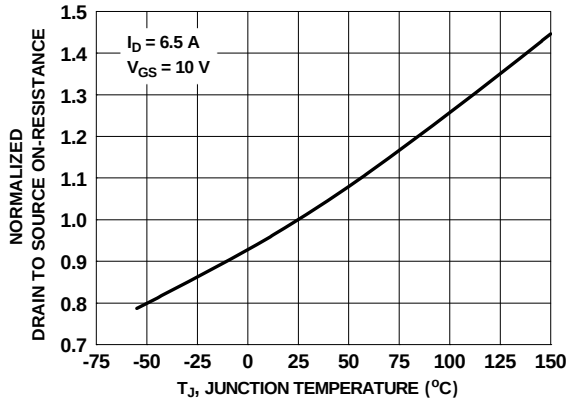



**Figure 3. Normalized On Resistance vs Junction Temperature**

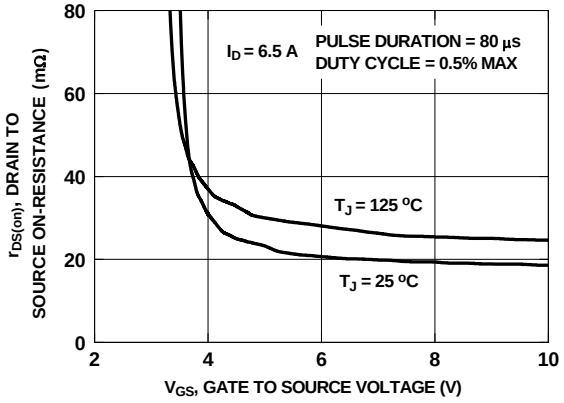



**Figure 4. On-Resistance vs Gate to Source Voltage**

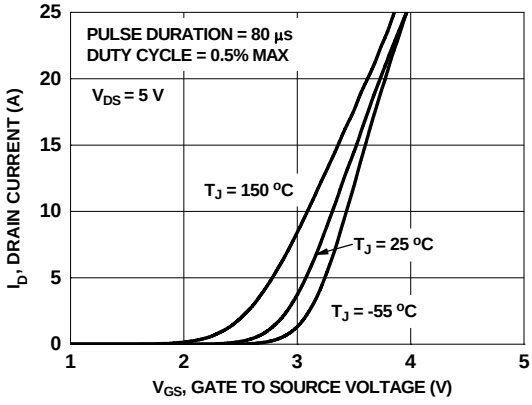



**Figure 5. Transfer Characteristics**

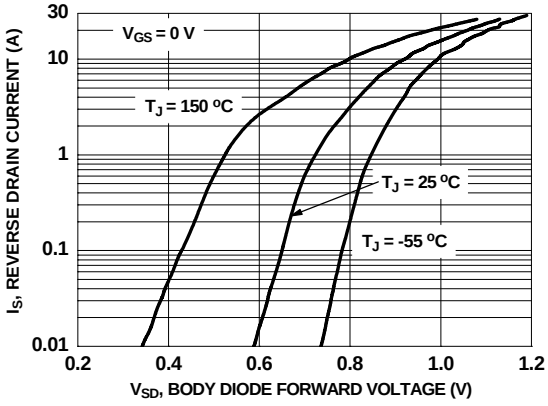



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

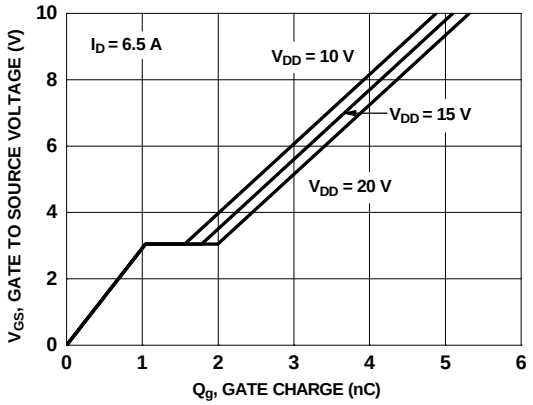



**Figure 7. Gate Charge Characteristics**

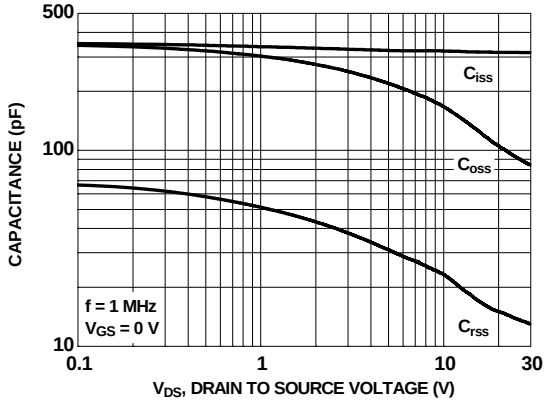



**Figure 8. Capacitance vs Drain to Source Voltage**

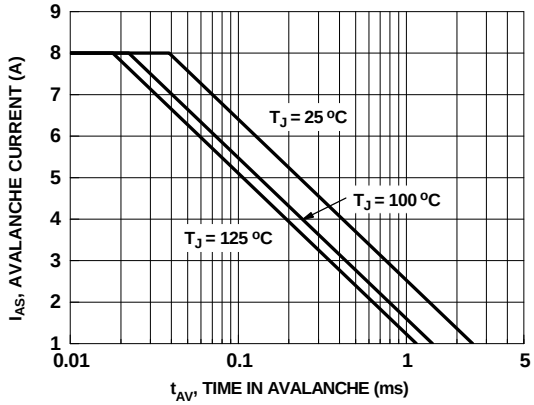



**Figure 9. Unclamped Inductive Switching Capability**

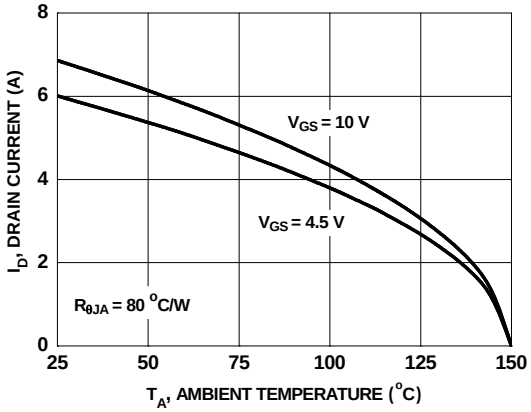



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

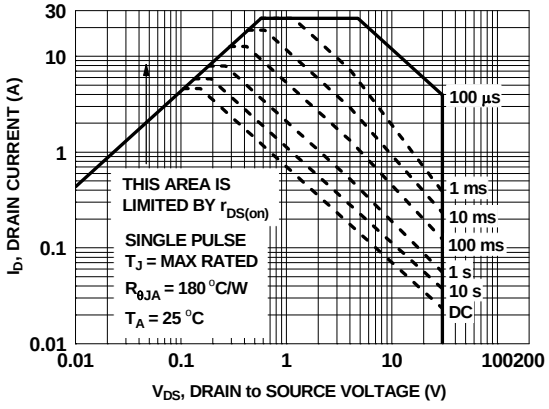



**Figure 11. Forward Bias Safe Operating Area**

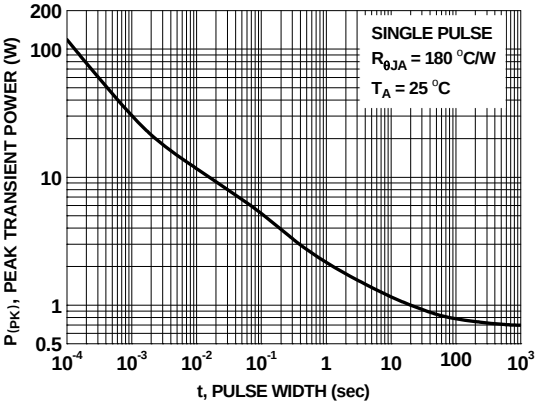



**Figure 12. Single Pulse Maximum Power Dissipation**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

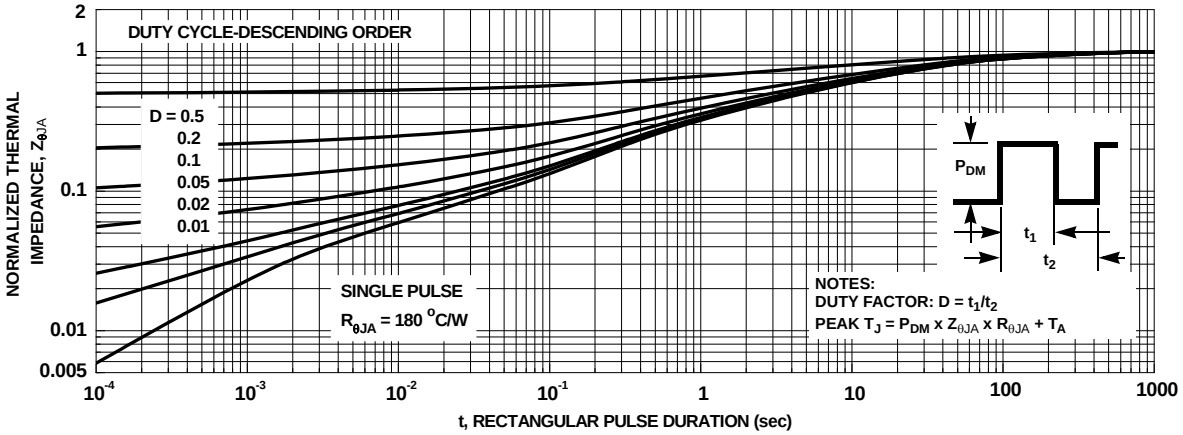



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

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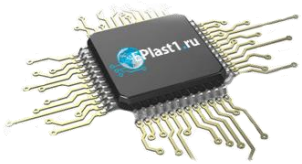


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