2-BIT BIDIRECTIONAL 1MHz, I²C BUS AND SMBUS VOLTAGE-LEVEL TRANSLATOR WITH 8kV HBM ESD

Check for Samples: TCA9406

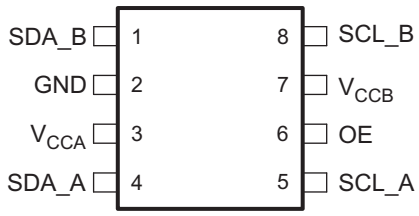
FEATURES

- 2-Bit Bidirectional Translator for SDA and SCL Lines in Mixed-Mode I²C Applications
- 5.5-V Tolerant OE Input
- Level Translation Range
  - 1.8 V to 2.5 V/3.3 V/5 V
  - 2.5 V to 2.5 V/3.3 V/5 V
  - 3.3 V to 3.3 V/5 V
- Internal10-kΩ Pullup Resistor on Each Port and Option to Add External Pullup Resistor if Required
- Provides Bidirectional Voltage Translation With No Direction Pin
- I_{off} Support Partial Power Down (V_{CC}= 0 V) With 2 mA
- High-Impedance Output SCL1, SDA1, SCL2, and SDA2 Pins When OE = Low or V_{CC}= 0 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port
    - 2500-V Human-Body Model (A114-B)
    - 250-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)
  - B Port
    - 8-kV Human-Body Model (A114-B)
    - 250-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)

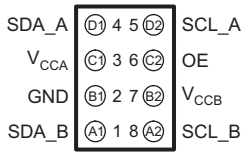
TYPICAL LEVEL-SHIFTER APPLICATIONS

- I²C/SMBus
- UART
- GPIO

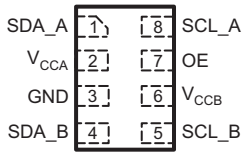
DCU PACKAGE
(TOP VIEW)



YZP PACKAGE
(BOTTOM VIEW)



DQM PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TCA9406 is a dual bidirectional I²C-Bus and SMBus Voltage-Level translator with enable (OE) Input. It is operational from 1.65 V to 3.6 V on A-Port and 2.3 V to 5.5 V on B-port. The Output Enable (OE) input is referenced to V_{CCA}, but is 5.5V tolerant

The device can also be used as a general purpose level-translator, supporting push-pull driving of the A and B ports. When driven with push-pull devices on both sides the TCA9406 can support up to 24Mps.

Under normal I2C and SMBus operation or other open drain configurations, the device can support up to 2Mbps. It is compatible with a standard I²C bus 100 kHz, 400 kHz and 1 MHz at both sides of A-Port and B-Port.

The TCA9406 features internal 10kOHM pullup resistors. Additional external pullup resistors can be added to the bus to reduce total pullup resistance.

The TCA9406 is not a bus buffer like the PCA9515B and PCA9517. The OE feature can be utilized to isolate one side of the bus from the other by placing both sides into a high impedence state.

The Enable (OE) should be tied to GND through a pulldown resistor to ensure the high-impedance state during power up or power down. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

ORDERING INFORMATION(1)

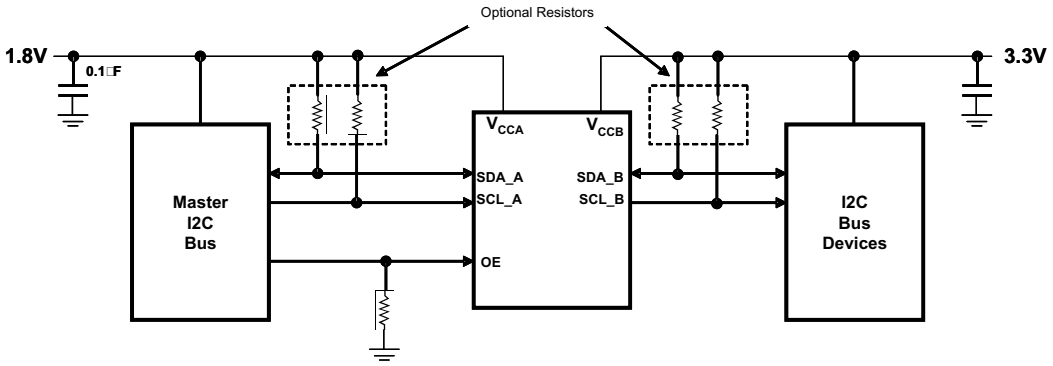
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP	Reel of 3000	TCA9406YZPR	
	MicroQFN – DQM	Reel of 3000	TCA9406DQMR	
	VSSOP – DCU	Reel of 3000	TCA9406DCUR	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DQM: The actual top-side marking has three additional characters that designate the year, month, and wafer fab/assembly site.
DCU: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

PIN DESCRIPTION

NO.		NAME	TYPE	FUNCTION
DQM, DCU	YZP			
1	A1	SDA_B	I/O	Input/output B. Referenced to V_{CCB}. Allow I2C_SDA configured to 2.5V/3.3V/5V
2	B1	GND	GND	Ground
3	C1	V_{CCA}	PWR	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}. Configuration for SDA_A, SCL_A, and OE
4	D1	SDA_A	I/O	Input/output A. Referenced to V_{CCA}. Allows I2C_SDA configured to 1.8V, 2.5V, 3.3V
5	D2	SCL_A	I/O	Input/output A. Referenced to V_{CCA}. Allows I2C_SCL configured to 1.8V, 2.5V, 3.3V
6	C2	OE	Input	Output enable (active High). Referenced to V_{CCA}. Pull OE to LOW to place all outputs in tri-state mode.
7	B2	V_{CCB}	PWR	B-port supply voltage. 2.3 V ≤ V_{CCB} ≤ 5.5 V for SDA_B, SCL_B
8	A2	SCL_B	I/O	Input/output B. Referenced to V_{CCB}. Allow I2C_SCL configured to 2.5V/3.3V/5V

TYPICAL OPERATING CIRCUIT



Design Notes:
OE can be tied directly to 1.8V (V_{CCA}) to always be in ENABLE mode.

ABSOLUTE MAXIMUM RATINGS(1)

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4.6	V
V_{CCB}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)	A port	–0.5	4.6	V
		B port	–0.5	6.5	
		OE input	–0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
θ_{JA}	Package thermal impedance(4)	DQM package		220	°C/W
		DCU package		227	
		YZP package		102	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1) (2)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage(3)				1.65	3.6	V
V_{CCB}	Supply voltage				2.3	5.5	V
V_{IH}	High-level input voltage	A-port I/Os	1.65 V to 1.95 V	2.3 V to 5.5 V	V_{CCI} – 0.2	V_{CCI}	V
			2.3 V to 3.6 V		V_{CCI} – 0.4	V_{CCI}	
		B-port I/Os	1.65 V to 3.6 V	2.3 V to 5.5 V	V_{CCI} – 0.4	V_{CCI}	
		OE input			V_{CCA} × 0.65	5.5	
V_{IL} (4)	Low-level input voltage	A-port I/Os	1.65 V to 3.6 V	2.3 V to 5.5 V	0	0.15	V
		B-port I/Os			0	0.15	
		OE input			0	V_{CCA} × 0.35	
Δt/Δv	Input transition rise or fall rate	A-port I/Os, push-pull driving	1.65 V to 3.6 V	2.3 V to 5.5 V		10	ns/V
		B-port I/Os, push-pull driving				10	
		Control input				10	
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.
(4) The maximum V_{IL} value is provided to ensure that a valid V_{OL} is maintained. The V_{OL} value is V_{IL} plus the voltage drop across the pass-gate transistor.

ELECTRICAL CHARACTERISTICS(1) (2) (3)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OHA}		I_{OH} = –20 µA, V_{IB} ≥ V_{CCB} – 0.4 V	1.65 V to 3.6 V	2.3 V to 5.5 V				V_{CCA} × 0.67		V
V_{OLA}		I_{OL} = 1 mA, V_{IB} ≤ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V					0.4	V
V_{OHB}		I_{OH} = –20 µA, V_{IA} ≥ V_{CCA} – 0.2 V	1.65 V to 3.6 V	2.3 V to 5.5 V				V_{CCB} × 0.67		V
V_{OLB}		I_{OL} = 1 mA, V_{IA} ≤ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V					0.4	V
I_I	OE		1.65 V to 3.6 V	2.3 V to 5.5 V			±1		±2	µA
I_{off}	A port		0 V	0 to 5.5 V			±1		±2	µA
	B port		0 to 3.6 V	0 V			±1		±2	µA
I_{OZ}	A or B port		1.65 V to 3.6 V	2.3 V to 5.5 V			±1		±2	µA
I_{CCA}		V_I = V_O = open, I_O = 0	1.65 V to V_{CCB}	2.3 V to 5.5 V					2.4	µA
			3.6 V	0 V					2.2	
			0 V	5.5 V					–1	
I_{CCB}		V_I = V_O = open, I_O = 0	1.65 V to V_{CCB}	2.3 V to 5.5 V					12	µA
			3.6 V	0 V					–1	
			0 V	5.5 V					1	
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.65 V to V_{CCB}	2.3 V to 5.5 V					14.4	µA
C_I	OE		3.3 V	3.3 V		2.5			3.5	pF
C_{io}	A or B port		3.3 V	3.3 V		10				pF
	A port					5		6		
	B port					6		7.5		

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

				V_{CCB} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate	Push-pull driving			21		22		24	Mbps
		Open-drain driving			2		2		2	
t_w	Pulse duration	Push-pull driving	Data inputs	47		45		41		ns
		Open-drain driving		500		500		500		

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

				V_{CCB} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate	Push-pull driving			20		22		24	Mbps
		Open-drain driving			2		2		2	
t_w	Pulse duration	Push-pull driving	Data inputs	50		45		41		ns
		Open-drain driving		500		500		500		

TIMING REQUIREMENTS

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

				V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
	Data rate	Push-pull driving			23		24	Mbps
		Open-drain driving			2		2	
t_w	Pulse duration	Push-pull driving	Data inputs	43		41		ns
		Open-drain driving		500		500		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	A	B	Push-pull driving		5.3		5.4		6.8	ns
			Open-drain driving	2.3	8.8	2.4	9.6	2.6	10	
t_{PLH}			Push-pull driving		6.8		7.1		7.5	
			Open-drain driving	45	260	36	208	27	198	
t_{PHL}	B	A	Push-pull driving		4.4		4.5		4.7	ns
			Open-drain driving	1.9	5.3	1.1	4.4	1.2	4	
t_{PLH}			Push-pull driving		5.3		4.5		0.5	
			Open-drain driving	45	175	36	140	27	102	
t_{en}	OE	A or B			200		200		200	ns
t_{dis}	OE	A or B			50		40		35	ns
t_{rA}	A-port rise time		Push-pull driving	3.2	9.5	2.3	9.3	2	7.6	ns
			Open-drain driving	38	165	30	132	22	95	
t_{rB}	B-port rise time		Push-pull driving	4	10.8	2.7	9.1	2.7	7.6	ns
			Open-drain driving	34	145	23	106	10	58	
t_{fA}	A-port fall time		Push-pull driving	2	5.9	1.9	6	1.7	13.3	ns
			Open-drain driving	4.4	6.9	4.3	6.4	4.2	6.1	
t_{fB}	B-port fall time		Push-pull driving	2.9	13.8	2.8	16.2	2.8	16.2	
			Open-drain driving	6.9	13.8	7.5	16.2	7	16.2	
$t_{SK(O)}$	Channel-to-channel skew				0.7		0.7		0.7	ns
Max data rate			Push-pull driving	21		22		24		Mbps
			Open-drain driving	2		2		2		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	A	B	Push-pull driving		3.2		3.7		3.8	ns
			Open-drain driving	1.7	6.3	2	6	2.1	5.8	
t_{PLH}			Push-pull driving		3.5		4.1		4.4	
			Open-drain driving	43	250	36	206	27	190	
t_{PHL}	B	A	Push-pull driving		3		3.6		4.3	ns
			Open-drain driving	1.8	4.7	2.6	4.2	1.2	4	
t_{PLH}			Push-pull driving		2.5		1.6		1	
			Open-drain driving	44	170	37	140	27	103	
t_{en}	OE	A or B			200		200		200	ns
t_{dis}	OE	A or B			50		40		35	ns
t_{rA}	A-port rise time		Push-pull driving	2.8	7.4	2.6	6.6	1.8	5.6	ns
			Open-drain driving	34	149	28	121	24	89	
t_{rB}	B-port rise time		Push-pull driving	3.2	8.3	2.9	7.2	2.4	6.1	ns
			Open-drain driving	35	151	24	112	12	64	
t_{fA}	A-port fall time		Push-pull driving	1.9	5.7	1.9	5.5	1.8	5.3	ns
			Open-drain driving	4.4	6.9	4.3	6.2	4.2	5.8	
t_{fB}	B-port fall time		Push-pull driving	2.2	7.8	2.4	6.7	2.6	6.6	ns
			Open-drain driving	5.1	8.8	5.4	9.4	5.4	10.4	
$t_{SK(O)}$	Channel-to-channel skew				0.7		0.7		0.7	ns
Max data rate			Push-pull driving	20		22		24		Mbps
			Open-drain driving	2		2		2		

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 3.3 V ± 0.3 V		V_{CCB} = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	
t_{PHL}	A	B	Push-pull driving		2.4		3.1	ns
			Open-drain driving	1.3	4.2	1.4	4.6	
t_{PLH}			Push-pull driving		4.2		4.4	
			Open-drain driving	36	204	28	165	
t_{PHL}	B	A	Push-pull driving		2.5		3.3	ns
			Open-drain driving	1	124	1	97	
t_{PLH}			Push-pull driving		2.5		2.6	
			Open-drain driving	3	139	3	105	
t_{en}	OE	A or B			200		200	ns
t_{dis}	OE	A or B			40		35	ns
t_{rA}	A-port rise time		Push-pull driving	2.3	5.6	1.9	4.8	ns
			Open-drain driving	25	116	19	85	
t_{rB}	B-port rise time		Push-pull driving	2.5	6.4	2.1	7.4	ns
			Open-drain driving	26	116	14	72	
t_{fA}	A-port fall time		Push-pull driving	2	5.4	1.9	5	ns
			Open-drain driving	4.3	6.1	4.2	5.7	
t_{fB}	B-port fall time		Push-pull driving	2.3	7.4	2.4	7.6	ns
			Open-drain driving	5	7.6	4.8	8.3	
$t_{SK(O)}$	Channel-to-channel skew				0.7		0.7	ns
Max data rate			Push-pull driving	23		24		Mbps
			Open-drain driving	2		2		

PRINCIPLES OF OPERATION

Application Notes

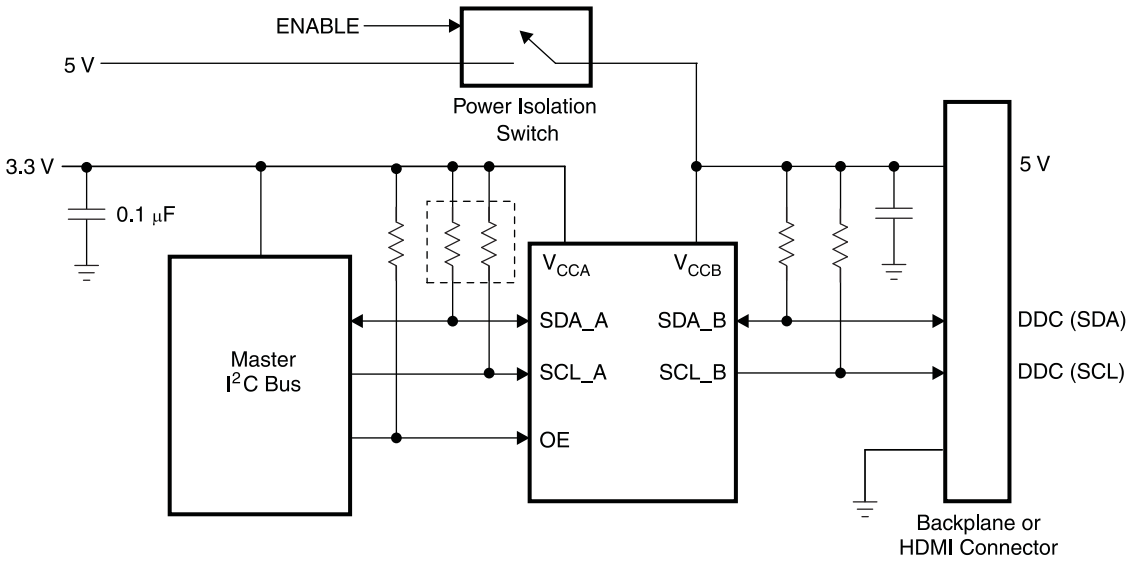


Figure 1. Typical Design Example

The TCA9406 has a V_{CC} isolation feature known as I_{off} partial power down and backdrive protection. If a cable is connected, and the connected external system is still powered own, the system can be put into standby mode by shutting down the power rail. In this state, the TCA9406 has a leakage current of approximately 2 μA caused by current flow from powered-on system.

Power Up, Power Down

One advantage of the TCA9406 translator is that either power supply can be ramped up first. Another advantage is that either power supply can be set to 0 V, and the outputs are in high-impedance state.

The recommended power up sequence is:

1. Apply power to the first V_{CC} and apply the second V_{CC}
2. Drive the OE input high to enable the device

The recommended power down sequence is:

1. Drive OE input low to disable the device
2. Switch Off the power from either V_{CC} and remove power from other V_{CC}.

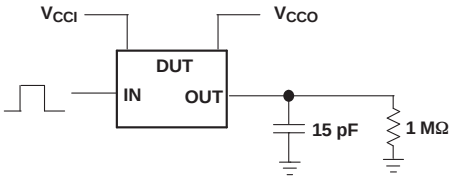
Enable/Disable

The TCA9406 has an OE input that is used to disable the device by setting OE low, which place all I/Os in the high-impedance state. The control OE is referenced to the V_{CCA} supply. A pulldown resistor tying OE to ground should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power up and power down. The value of resistor is based upon the current sinking capability of the device.

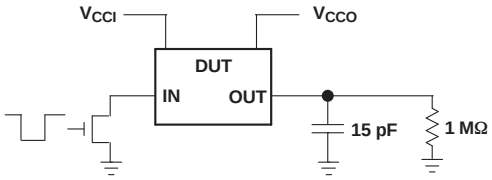
Integrated Pullup Resistors on the I/Os (A-Ports/B-Ports)

Each A-port I/O has an internal 10-kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10-kΩ resistors). Adding lower value pull-up resistors may effect V_{OL} levels. The internal pullups of the TCA9406 are disabled when the OE pin is low.

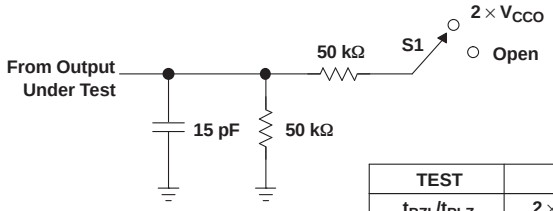
PARAMETER MEASUREMENT INFORMATION



DATA RATE, PULSE DURATION, PROPAGATION DELAY, OUTPUT RISE AND FALL TIME MEASUREMENT USING A PUSH-PULL DRIVER

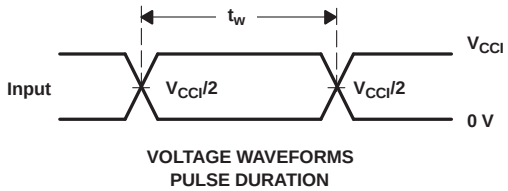


DATA RATE, PULSE DURATION, PROPAGATION DELAY, OUTPUT RISE AND FALL TIME MEASUREMENT USING AN OPEN-DRAIN DRIVER

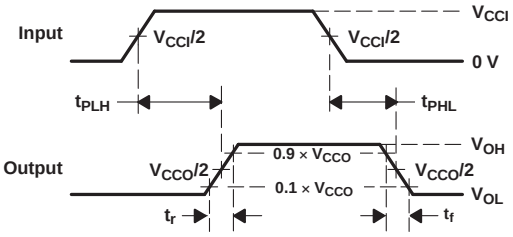


TEST	S1
t_{PZL}/t_{PLZ} t_{PHZ}/t_{PZH}	$2 \times V_{CCO}$ Open

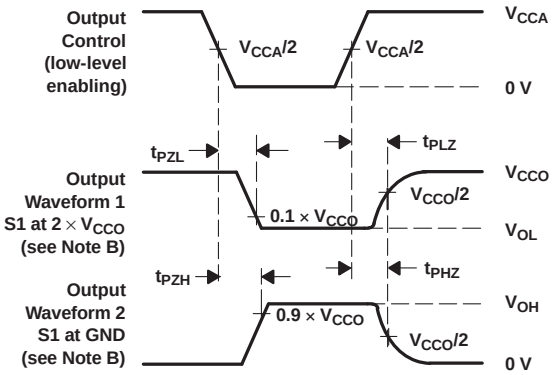
LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
HPA02270YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85		Samples
TCA9406DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NF9 Z	Samples
TCA9406DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	NF9R	Samples
TCA9406YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

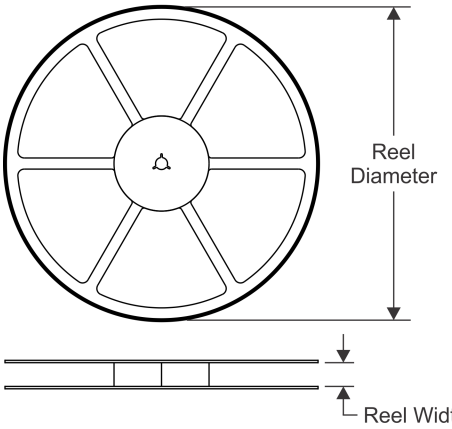
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

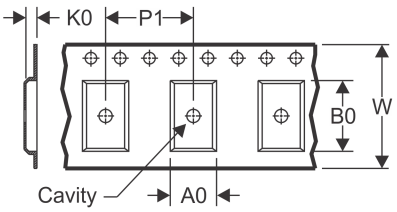
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

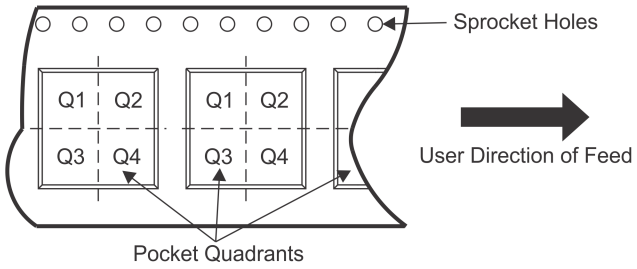


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

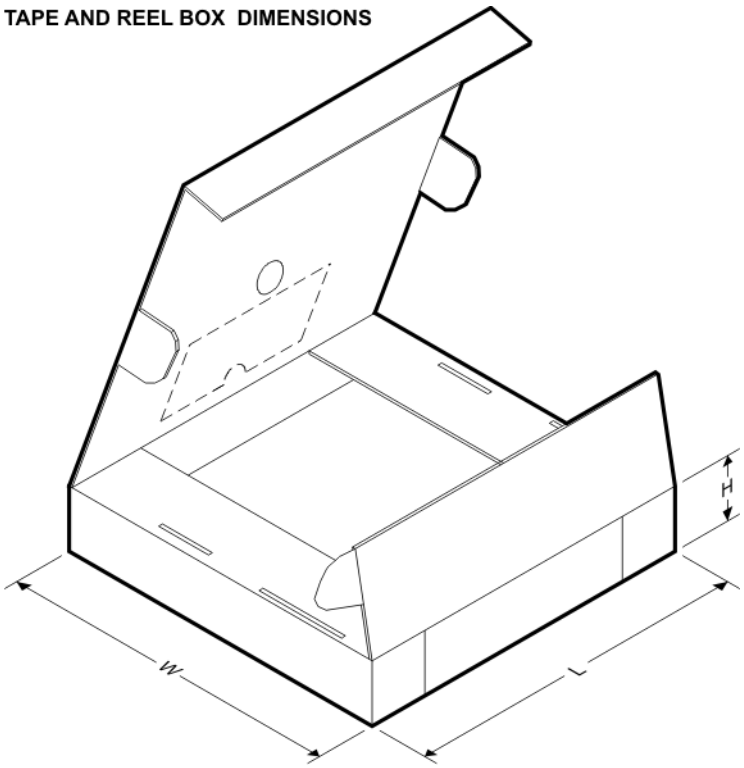
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9406DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
TCA9406DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TCA9406YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.11	2.1	0.56	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

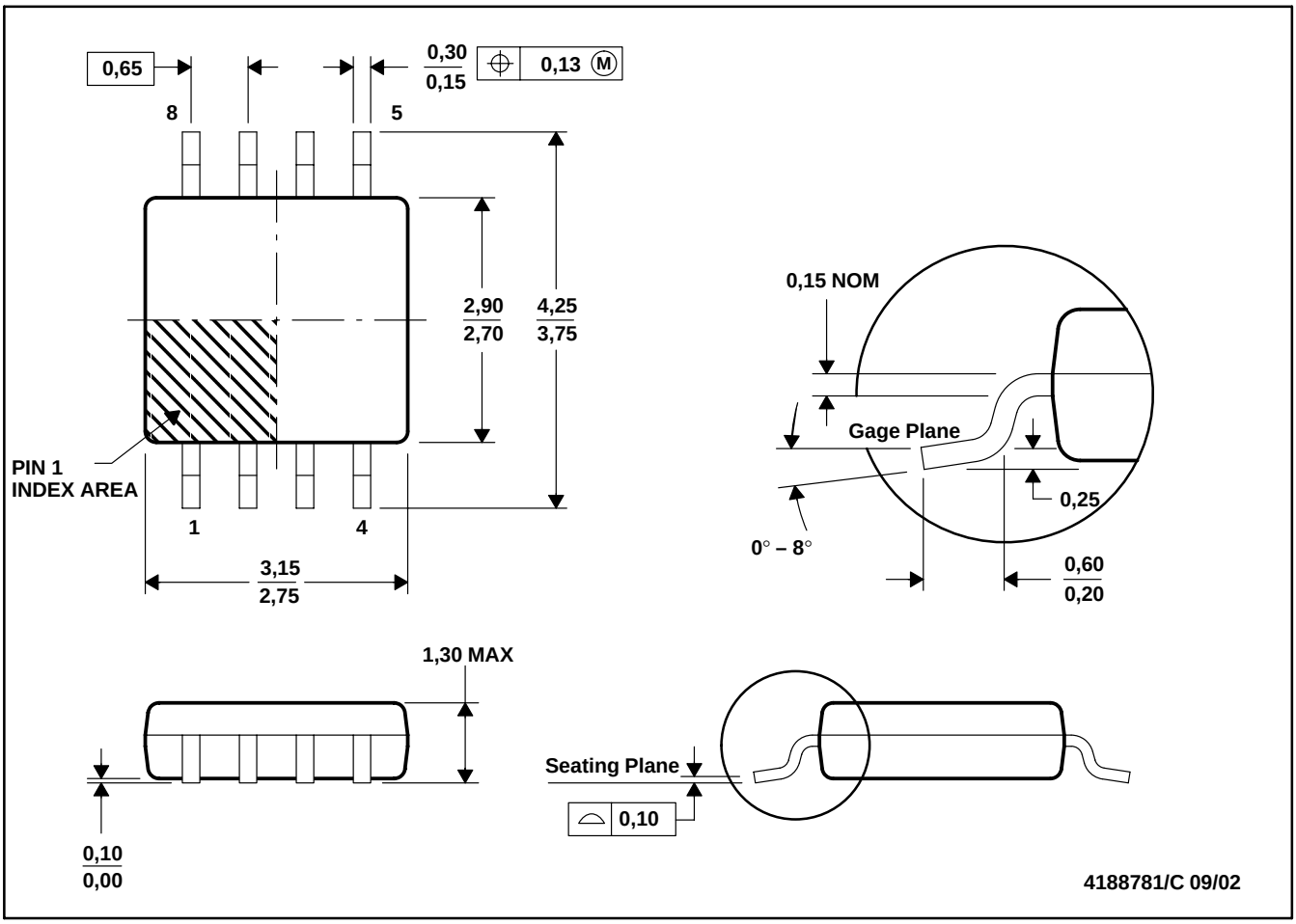


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9406DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
TCA9406DCUR	US8	DCU	8	3000	202.0	201.0	28.0
TCA9406YZPR	DSBGA	YZP	8	3000	210.0	185.0	35.0

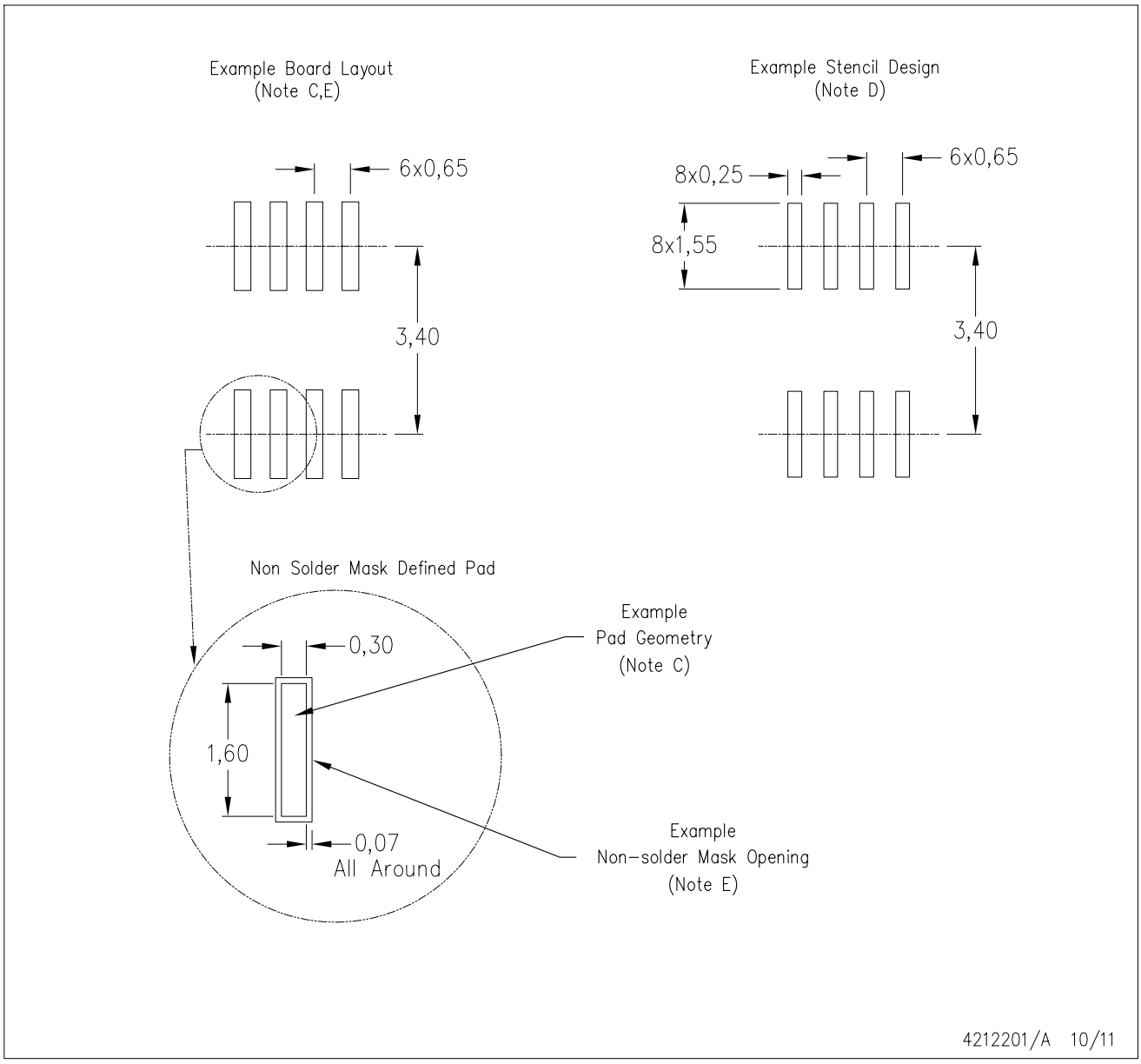
MPDS049B – MAY 1999 – REVISED OCTOBER 2002

DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



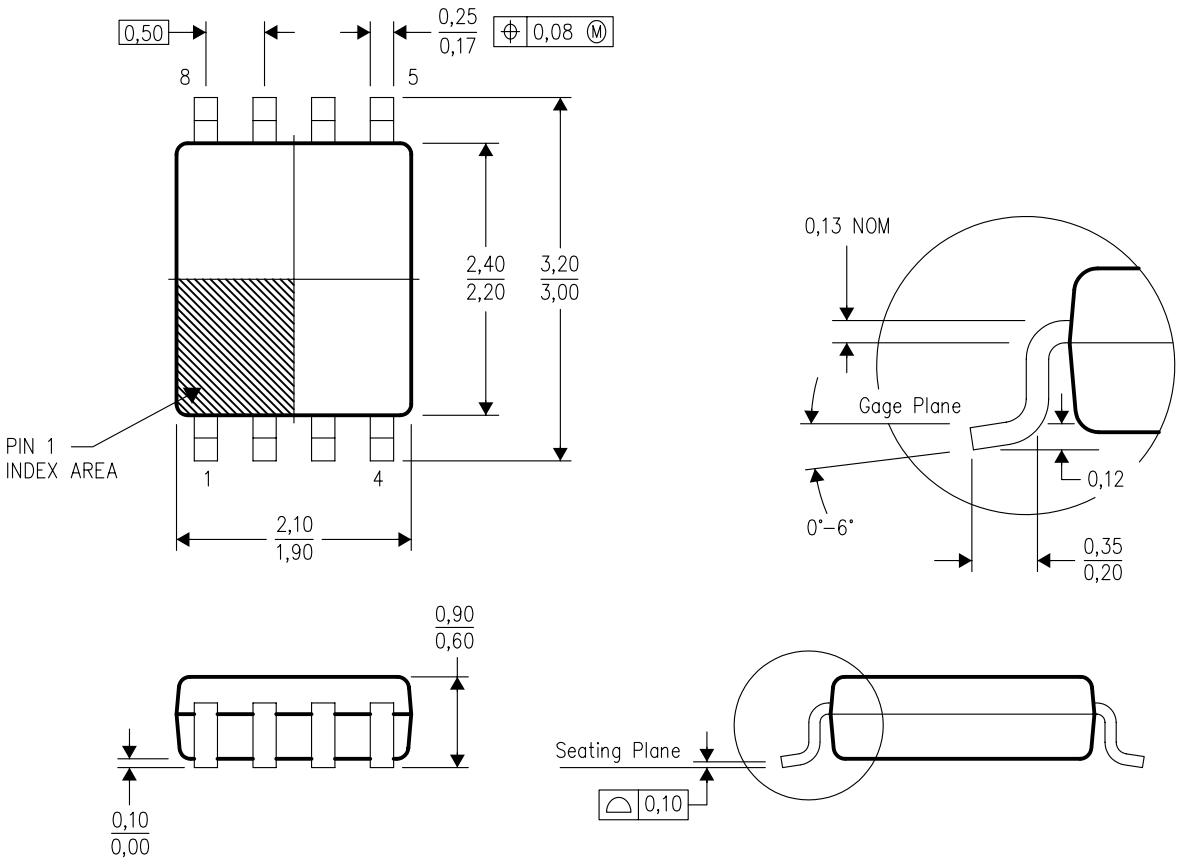
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Falls within JEDEC MO-187 variation DA.

DCT (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



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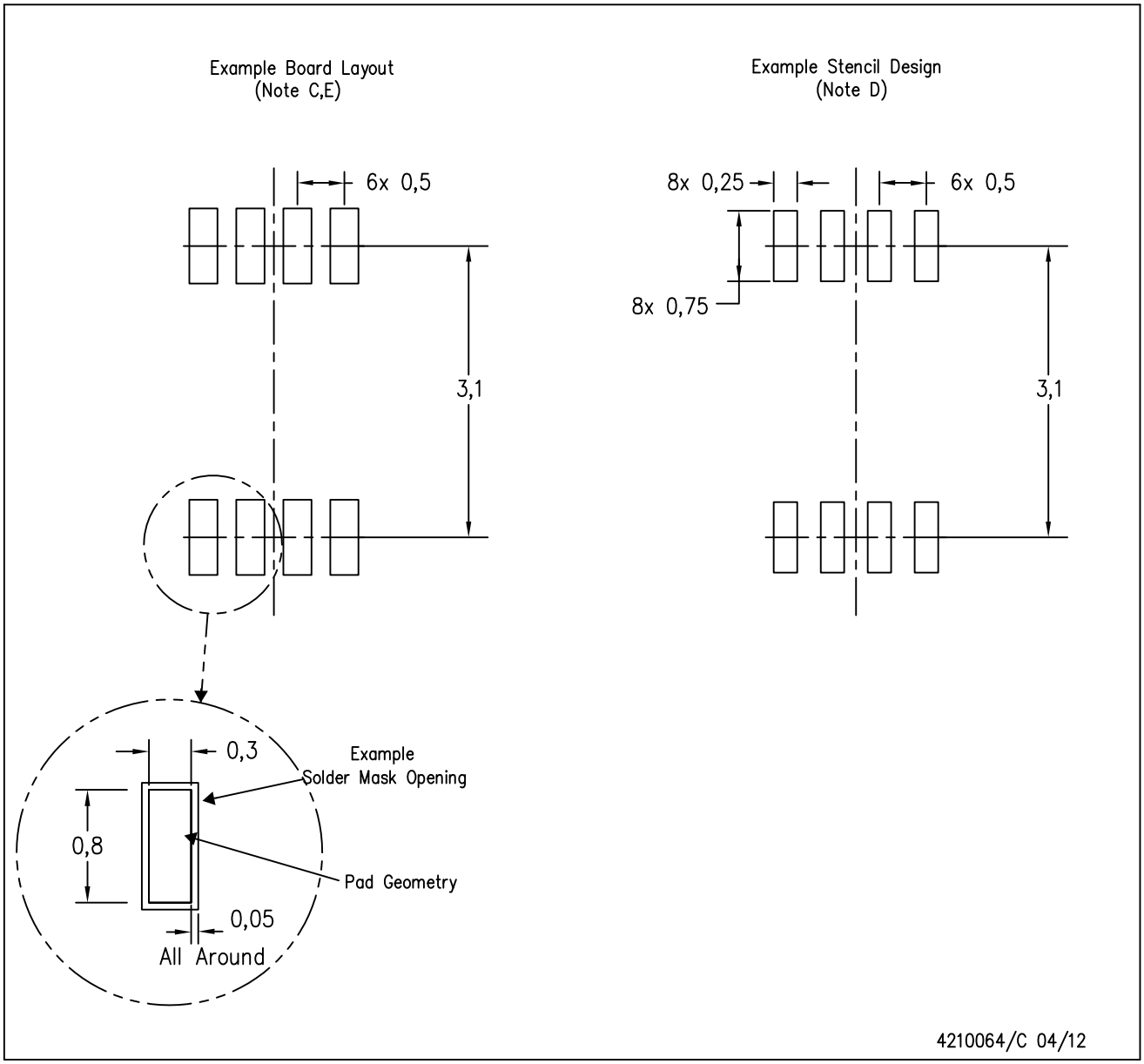
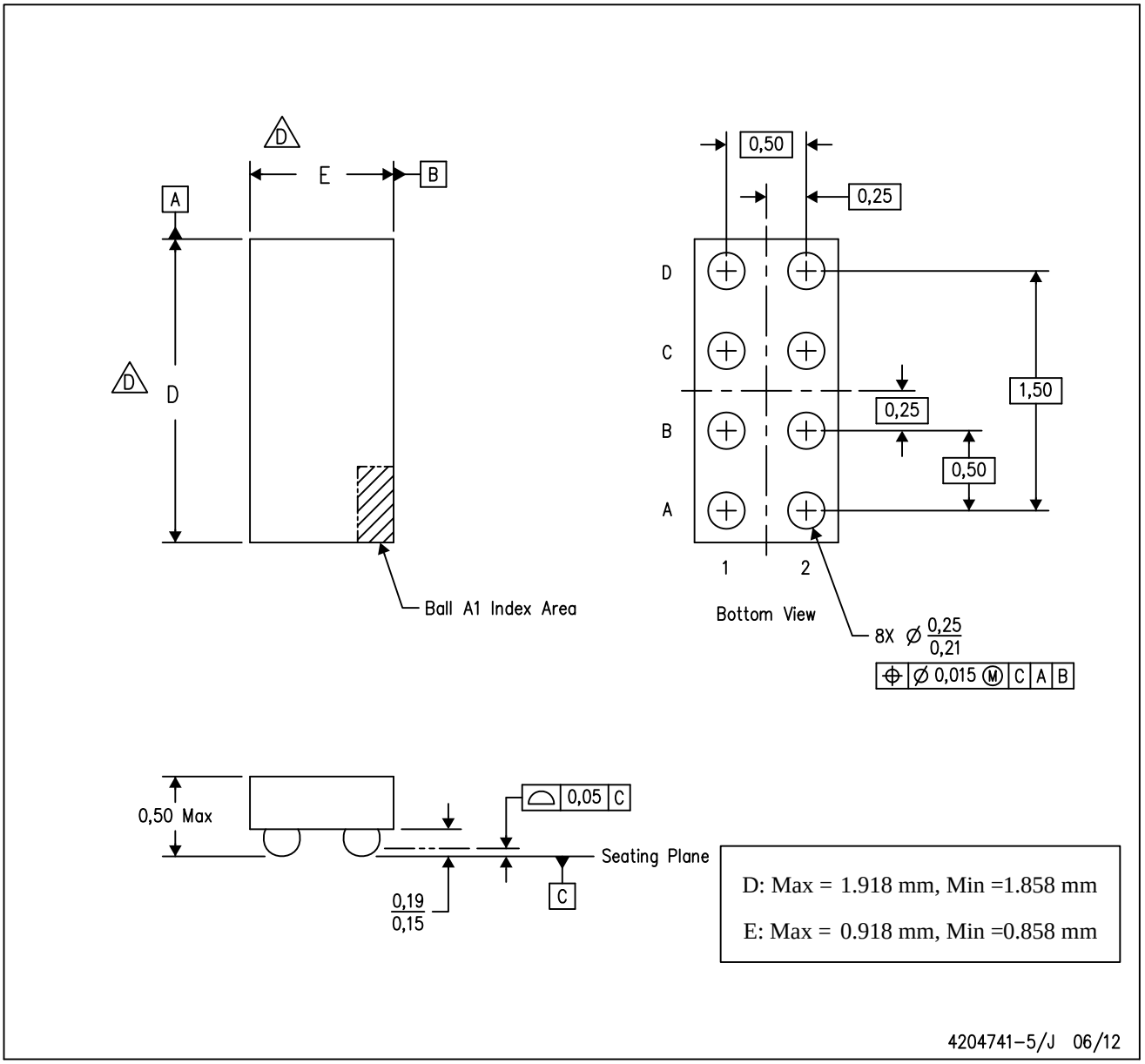
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. This package is a Pb–free solder ball design. Refer to the 8 YEP package (drawing 4204725) for tin–lead (SnPb).

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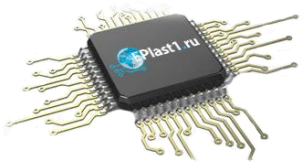

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