

## High-density power driver - high voltage full bridge with integrated gate driver

Datasheet - production data



### Features

- Power system-in-package integrating gate drivers and high-voltage power MOSFETs
  - Low  $R_{DS(on)}$  = 320 m $\Omega$
  - $BV_{DSS}$  = 600 V
- Suitable for operating as
  - Full bridge
  - Dual independent half bridges
- Wide driver supply voltage down to 6.5 V
- UVLO protection on supply voltage
- 3.3 V to 15 V compatible inputs with hysteresis and pull-down
- Interlocking function to prevent cross conduction
- Internal bootstrap diode
- Outputs in phase with inputs
- Very compact and simplified layout
- Flexible, easy and fast design

### Applications

- Motor drivers for industrial and home appliances
- Factory automation
- Fans and pumps
- HID, ballasts
- Power supply units
- DC-DC and DC-AC converters

### Description

The PWD13F60 is a high-density power driver integrating gate drivers and four N-channel power MOSFETs in dual half bridge configuration.

The integrated power MOSFETs have low  $R_{DS(on)}$  of 320 m $\Omega$  and 600 V drain-source breakdown voltage, while the embedded gate drivers high side can be easily supplied by the integrated bootstrap diode. The high integration of the device allows to efficiently drive loads in a tiny space.

The PWD13F60 device accepts a supply voltage ( $V_{CC}$ ) extending over a wide range and is protected by means of low-voltage UVLO detection on the supply voltage.

The input pins extended range allows an easy interfacing with microcontrollers, DSP units or Hall effect sensors.

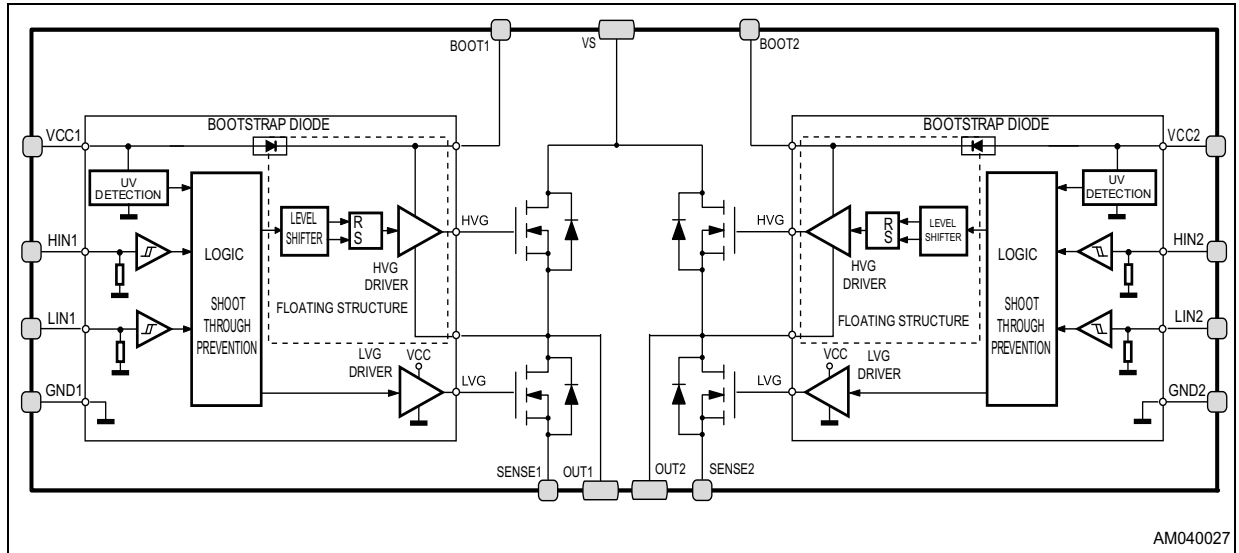
The device is available in a compact VFQFPN package.

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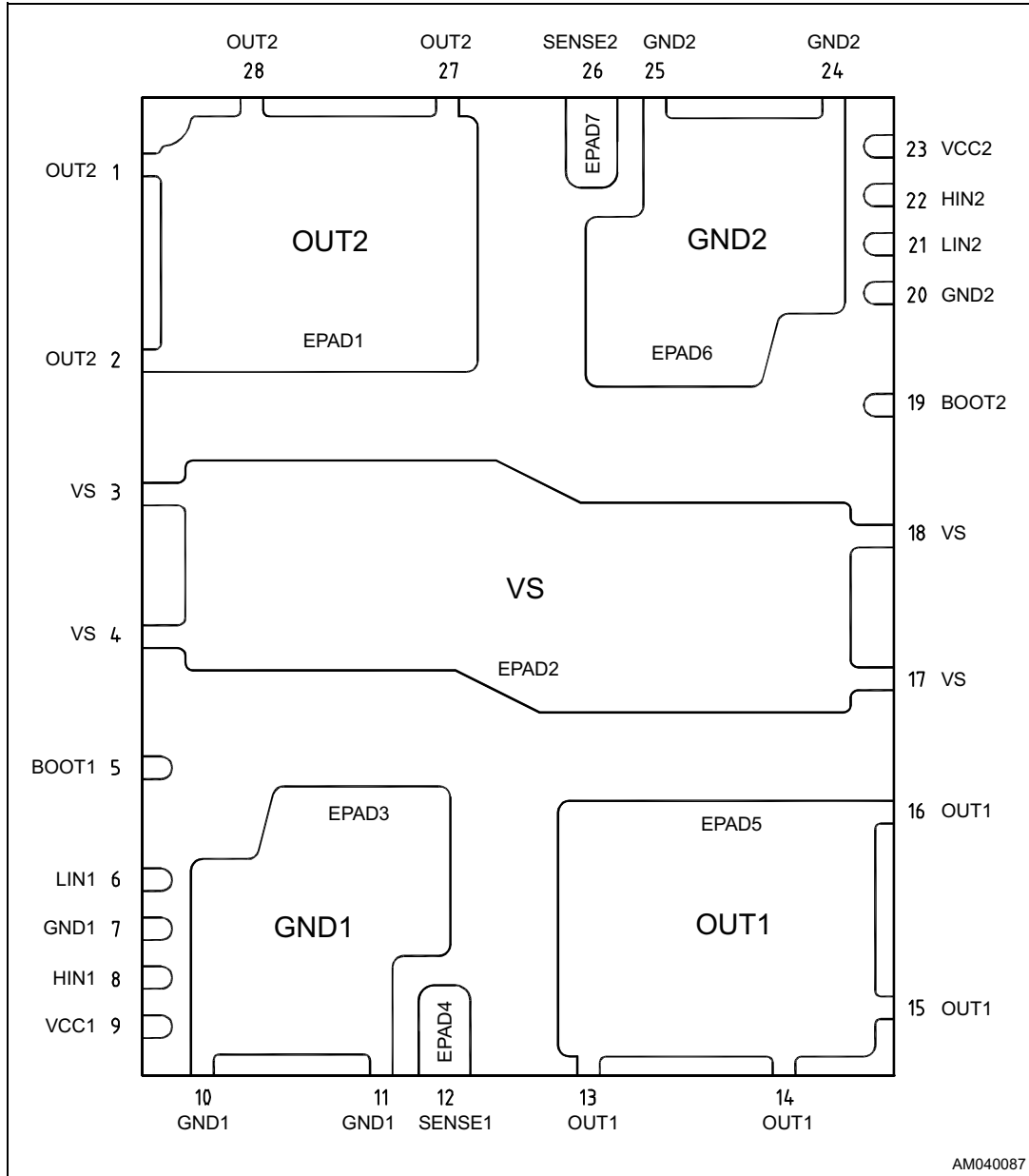
# 1 Block diagram

Figure 1. Block diagram



## 2 Pin connection diagram and description

Figure 2. Pin connection (top view)



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## Pin list

**Table 1. Pin description**

No.	Name	Type	Function
3, 4, 17, 18, EPAD2	VS	Power supply	High-voltage supply (high side MOSFET drains)
13, 14, 15, 16, EPAD5	OUT1	Power output	Half bridge 1 output
27, 28, 1, 2, EPAD1	OUT2	Power output	Half bridge 2 output
12, EPAD4	SENSE1	Power supply	Half bridge 1 sense (low side MOSFET source)
26, EPAD7	SENSE2	Power supply	Half bridge 2 sense (low side MOSFET source)
5	BOOT1	Power supply	Gate driver 1 high side supply voltage
19	BOOT2	Power supply	Gate driver 2 high side supply voltage
9	VCC1	Power supply	Gate driver 1 supply voltage
23	VCC2	Power supply	Gate driver 2 supply voltage
7, 10, 11, EPAD3	GND1	Power supply	Gate driver 1 ground
20, 24, 25, EPAD6	GND2	Power supply	Gate driver 2 ground
6	LIN1	Logic input	Logic input of low side MOSFET 1
8	HIN1	Logic input	Logic input of high side MOSFET 1
21	LIN2	Logic input	Logic input of low side MOSFET 2
22	HIN2	Logic input	Logic input of high side MOSFET 2

### 3 Electrical data

#### 3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
$V_{DS}$	MOSFET drain-to-source voltage	$T_J = 25\text{ °C}$	600	V
$V_{CC1}, V_{CC2}$	Drivers supply voltage	-	-0.3 to 19	V
$V_{CCx-SENSEx}$	VCC to SENSE pin voltage	-	-0.3 to 19	V
$V_{BOOTx}$	Bootstrap voltage	-	GNDx -0.3 to 600	V
$V_{BO1}, V_{BO2}$	BOOTx to OUTx pin voltage	-	-0.3 to 19	V
$I_D$	Drain current (per MOSFET)	DC at $T_{CB} = 25\text{ °C}^{(1)}$	8	A
		DC at $T_{CB} = 100\text{ °C}^{(1), (2)}$	6.9	A
		Peak at $T_{CB} = 25\text{ °C}^{(1), (2), (3)}$	32	A
$I_{SD}$	Source-drain diode current (per diode)	DC at $T_{CB} = 25\text{ °C}^{(1)}$	8	A
		Peak at $T_{CB} = 25\text{ °C}^{(1), (2), (3)}$	32	A
$SR_{out}$	Full bridge outputs slew rate (10% - 90%)	(2)	40	V/ns
$V_i$	Logic inputs voltage range	-	-0.3 to 15	V
$T_J$	Junction temperature	-	-40 to 150	°C
$T_s$	Storage temperature	-	-40 to 150	°C
$P_{tot}$	Total power dissipation <sup>(4)</sup>	$T_{CB} = 25\text{ °C}$ for each MOSFET	450	W
		$T_{amb} = 25\text{ °C}$ , JEDEC board <sup>(5), (6)</sup>	6.9	W

1.  $T_{CB}$  is temperature of case bottom pad.
2. Characterized, not tested in production.
3. The value specified by the design factor, pulse duration limited by max. junction temperature and SOA.
4. Value calculated basing on thermal resistance, power uniformly distributed over the four power MOSFETs, still air.
5. The device mounted on a FR4 2s2p board as JESD51-5/7.
6. Actual applicative board max. dissipation could be higher or lower depending on the layout and cooling techniques.

## 3.2 Recommended operating conditions

**Table 3. Recommended operating conditions**

Symbol	Parameter	Test condition	Min.	Max.	Unit
$V_{CC1}, V_{CC2}$	Driver supply voltage	-	6.5 <sup>(1)</sup>	-	V
$V_{BO1}, V_{BO2}$	BOOTx to OUTx pin voltage	-	6.5 <sup>(1)</sup>	-	V
VS	High-voltage supply	-	-	480	V
$T_J$	Junction temperature	-	-40	125	°C

1. The integrated gate driver can work with  $V_{CC}$  as low as  $V_{CC\_thON}$ . Higher supply voltage allows decreasing the MOSFETs  $R_{DS(on)}$ .

## 3.3 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Value	Unit
$R_{th(J-CB)}$	Thermal resistance junction to each MOSFET exposed pad, typ.	1.1	°C/W
$R_{th(J-A)}$	Thermal resistance junction to ambient <sup>(1)</sup>	18	°C/W

1. The junction to ambient thermal resistance is obtained simulating the device mounted on a FR4 2s2p board as the JESD51-5/7 with power dissipation uniformly distributed over the four power MOSFETs.

## 4 Electrical characteristics

### 4.1 Driver

V<sub>CCx</sub> = 15 V; T<sub>J</sub> = 25 °C, unless otherwise specified.

**Table 5. Driver section electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Low supply voltage section</b>						
V <sub>CC_hys</sub>	V <sub>CC</sub> UV hysteresis	-	0.2	0.4	0.6	V
V <sub>CC_thON</sub>	V <sub>CC</sub> UV turn ON threshold	-	5.7	6.1	6.5	V
V <sub>CC_thOFF</sub>	V <sub>CC</sub> UV turn OFF threshold	-	5.3	5.7	6.1	V
I <sub>qccu</sub>	Undervoltage quiescent supply current	V <sub>CC</sub> = 4.5 V	-	140	190	μA
I <sub>qcc</sub>	Quiescent current	HINx = GND; LINx = 5 V	-	270	350	μA
<b>Bootstrapped supply voltage section</b>						
I <sub>QBO</sub>	V <sub>BO</sub> quiescent current	V <sub>BO</sub> = 15 V LINx = GND; HINx = 5 V	-	60	97	μA
I <sub>LK</sub>	Bootstrap leakage current	V <sub>OUTx</sub> = V <sub>BOOTx</sub> = VS = 600 V; VCC = LINx = HINx = GND	-	-	1	μA
R <sub>BD(on)</sub>	Bootstrap driver on-resistance <sup>(1)</sup>	LIN = 5 V	-	120	-	Ω
<b>Logic inputs</b>						
V <sub>il</sub>	Logic level low threshold voltage	-	0.80	-	1.10	V
V <sub>ih</sub>	Logic level high threshold voltage	-	1.90	-	2.30	V
I <sub>ih</sub>	Logic '1' input bias current	LINx = HINx = 15 V	30	40	65	μA
I <sub>il</sub>	Logic '0' input bias current	LINx = HINx = GND	-	-	1	μA

1. R<sub>BD(on)</sub> is tested in the following way:

$$R_{BD(on)} = [(V_{CC} - V_{BOOTa}) - (V_{CC} - V_{BOOTb})] / [I_a - I_b]$$

Where: I<sub>a</sub> is the BOOT pin current when V<sub>BOOT</sub> = V<sub>BOOTa</sub>; I<sub>b</sub> is the BOOT pin current when V<sub>BOOT</sub> = V<sub>BOOTb</sub>.



## 4.2 Power MOSFET

$V_{CCx} = 15\text{ V}$ ;  $T_J = 25\text{ °C}$ , unless otherwise specified.

**Table 6. Power MOSFET electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>MOSFET on/off states</b>						
$V_{(BR)IDSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}^{(1)}$	600	-	-	V
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 600\text{ V}$	-	-	1	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}^{(1)}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$I_D = 3\text{ A}$ ; $V_{GS} = 10\text{ V}$	-	0.32	0.425	$\Omega$
<b>MOSFET avalanche</b>						
$I_{AS}$	Avalanche current, repetitive or not repetitive	Pulse width limited by $T_J\text{ max.}^{(1)}$	-	-	3	A
$E_{AS}$	Single pulse avalanche energy	Starting $T_J = 25\text{ °C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}^{(1)}$	-	-	162	mJ
<b>Source-drain diode</b>						
$V_{SD}$	Diode forward on voltage	LINx = GND; HINx = GND; $I_{SD} = 3\text{ A}$	-	0.8	1.25	V

1. Tested at the wafer level before packaging.

## 5 Device characterization values

Table 7, Table 8 and electrical characteristics curves (from Figure 4 to Figure 12) contained in this section represent typical values based on characterization and simulation results.

**Table 7. Power MOSFET**

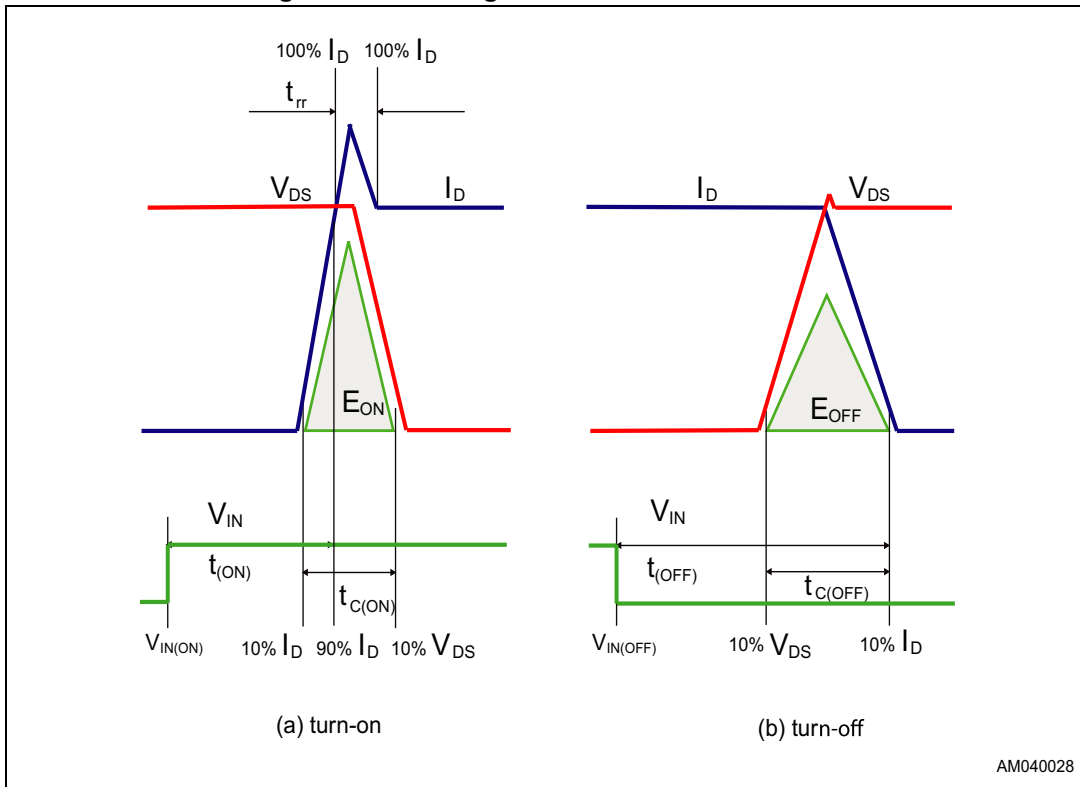
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>MOSFET dynamic</b>						
$Q_g$	Total gate charge	$V_{GS} = 10\text{ V}$ , $T_J = 25\text{ °C}$ $V_{DS} = 480\text{ V}$ , $I_D = 3\text{ A}$	-	26	-	nC
<b>Source-drain diode</b>						
$t_{rr}$	Diode reverse recovery time	$I_{SD} = 3\text{ A}$ , $V_S = 100\text{ V}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ °C}$	-	93	-	ns
$Q_{rr}$	Diode reverse recovery charge		-	376	-	nC
$I_{RRM}$	Diode reverse recovery current		-	8.1	-	A

**Table 8. Inductive load switching characteristics**

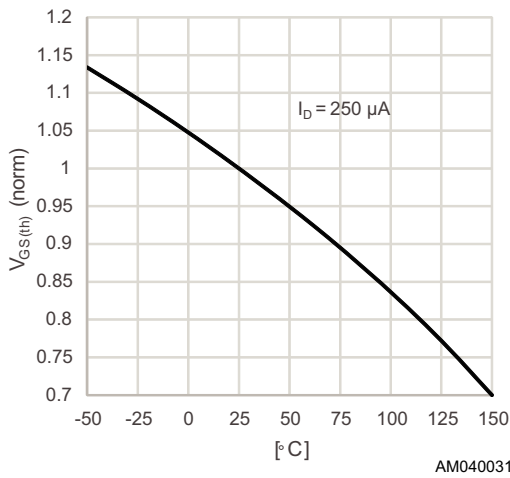
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{(on)}^{(1)}$	Turn-on time	$V_S = 300\text{ V}$ , $V_{CC} = V_{BO} = 15\text{ V}$ , $I_{OUT} = 3\text{ A}$ , $T_J = 25\text{ °C}$ , see Figure 3	-	280	-	ns
$t_{C(on)}^{(2)}$	Crossover time (on)		-	75	-	ns
$t_{(off)}^{(1)}$	Turn-off time		-	360	-	ns
$t_{C(off)}^{(2)}$	Crossover time (off)		-	105	-	ns
$E_{on}$	Turn-on switching losses		-	115	-	$\mu\text{J}$
$E_{off}$	Turn-off switching losses		-	35	-	$\mu\text{J}$
DT	Suggested minimum dead time		-	-	270	ns

- $t_{(on)}$  and  $t_{(off)}$  include the propagation delay time of the internal driver.
- $t_{C(on)}$  and  $t_{C(off)}$  are the switching times of the MOSFET itself under the internally given gate driving conditions.

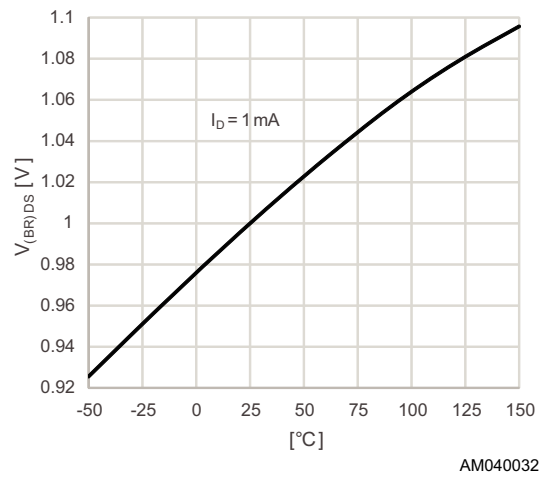
Figure 3. Switching time and losses definition



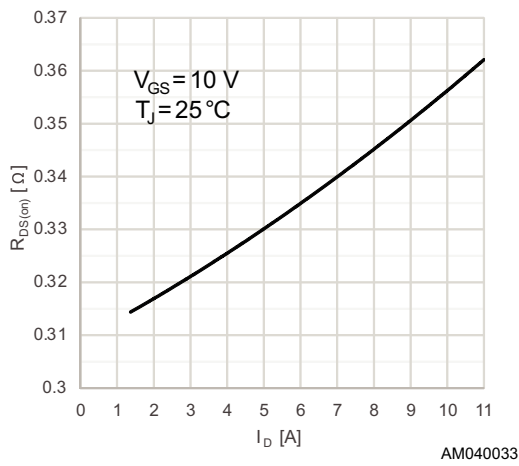
**Figure 4. Normalized gate threshold voltage vs. temperature**



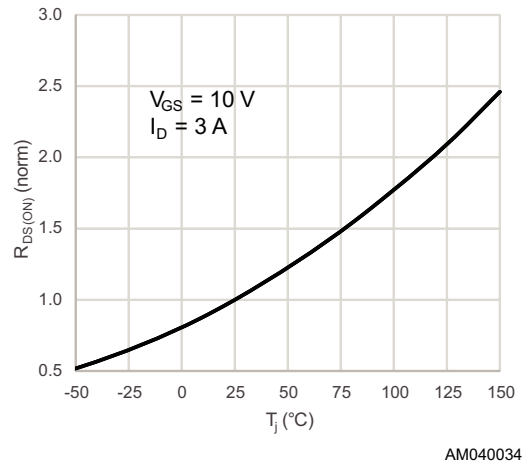
**Figure 5. Normalized drain-source breakdown voltage vs. temperature**



**Figure 6. Static drain-source on-resistance**



**Figure 7. Normalized on-resistance vs. temperature**



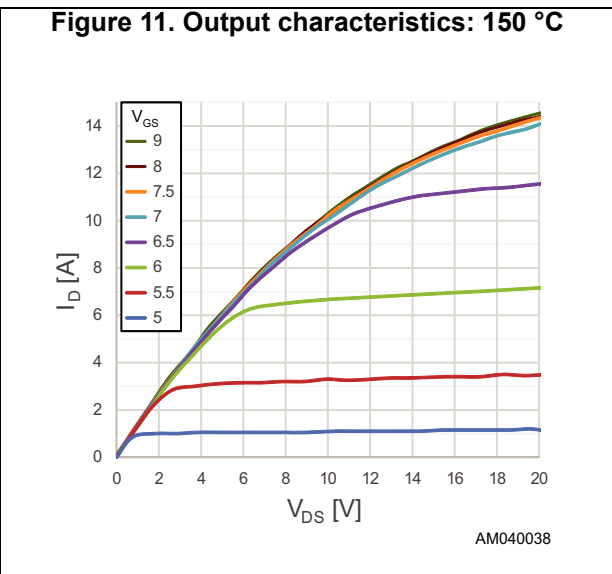
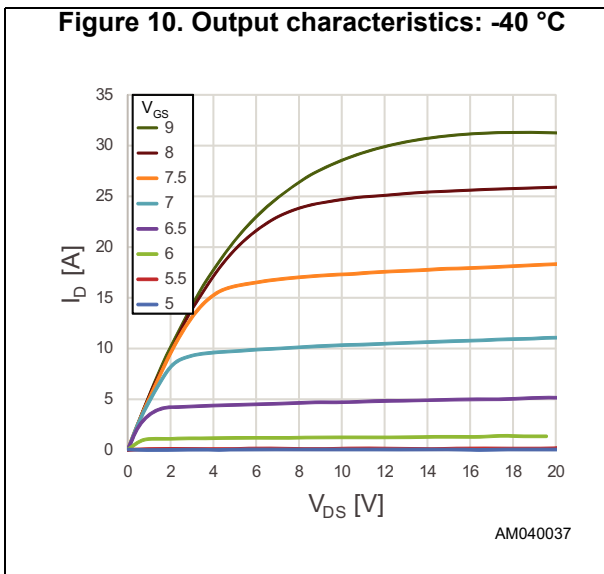
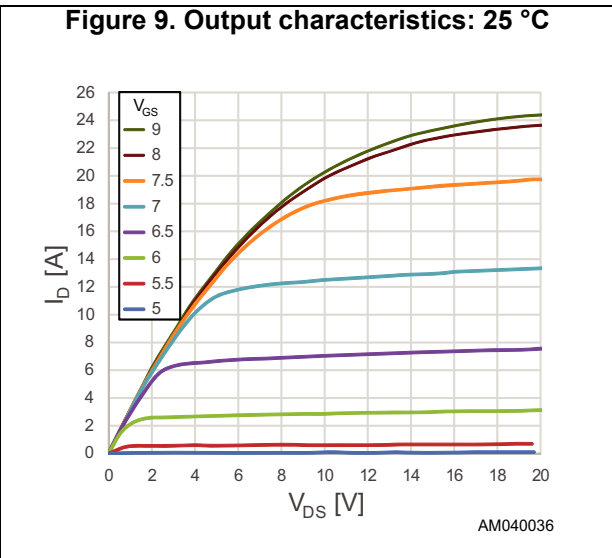
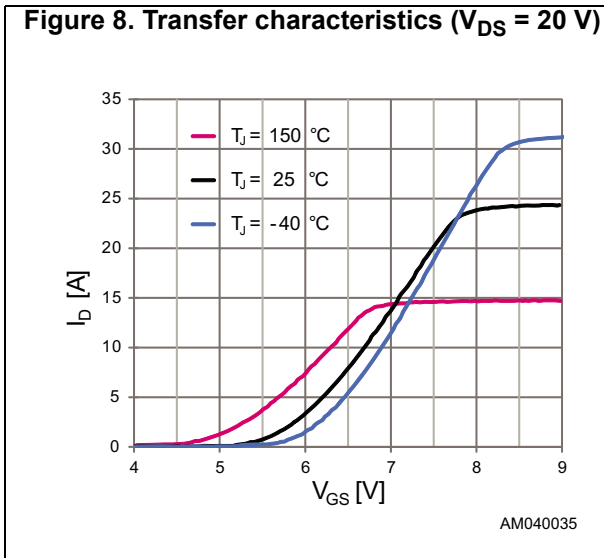
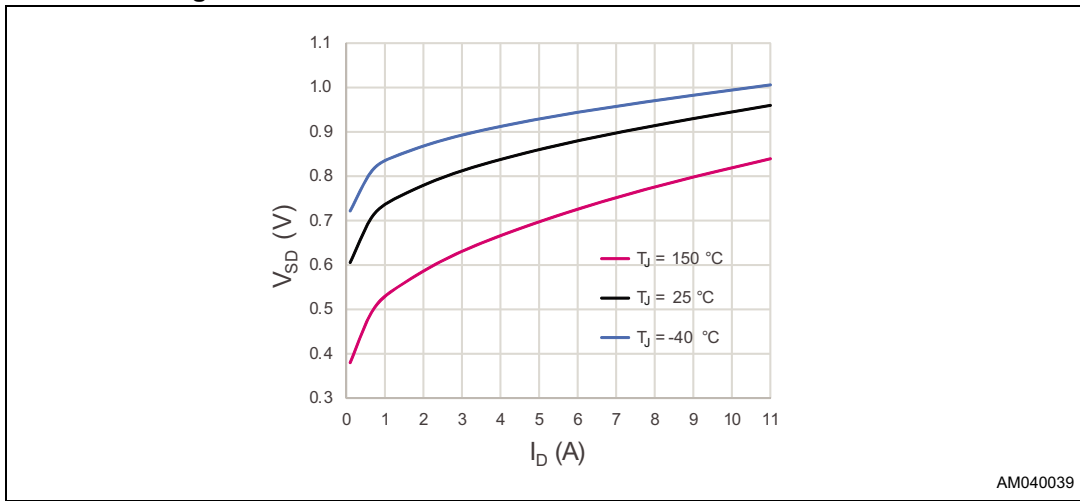


Figure 12. Static source-drain diode forward characteristics



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## 6 Functional description

### 6.1 Logic inputs

The PWD13F60 has four logic inputs to independently control the high side and low side internal MOSFETs.

An interlocking feature is offered to avoid undesired simultaneous turn on of both HS and LS MOSFETs within the same channel (see [Table 9](#)).

**Table 9. Truth table**

HINx	LINx	HSx	LSx
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	OFF	OFF

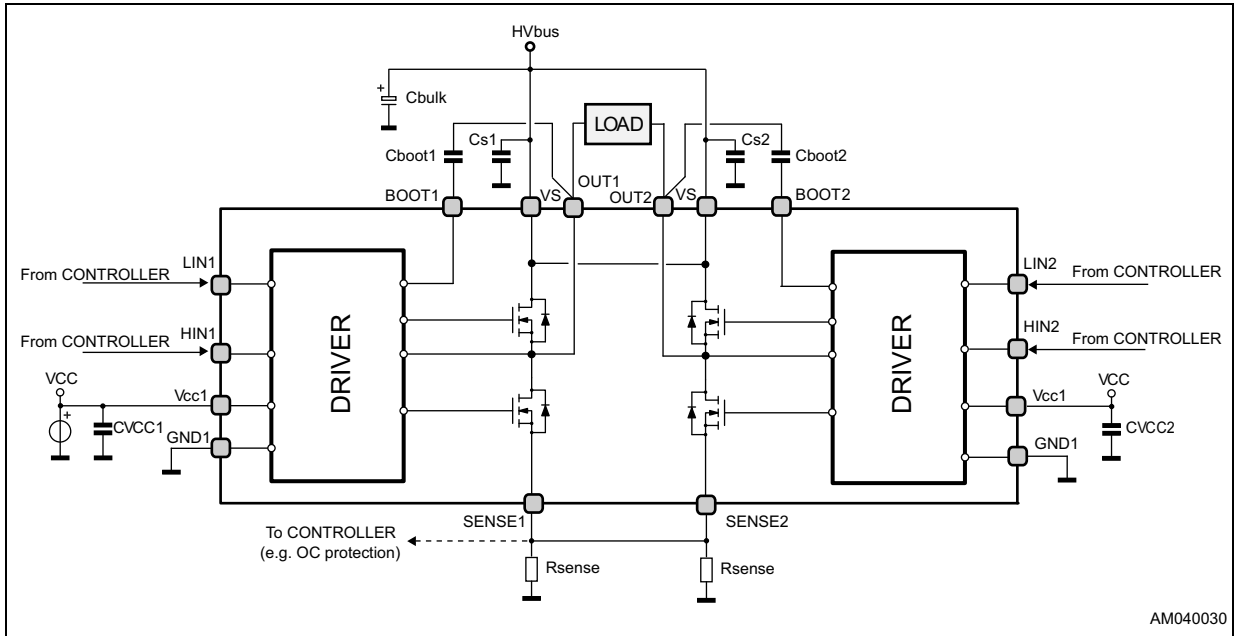
The logic inputs have internal pull-down resistors. The purpose of these resistors is to pull logic inputs low in case, for example, there is an interruption in the logic lines or the controller outputs are in tri-state condition. In this case the gate driver outputs are set to the low level and the corresponding MOSFETs are turned off.





# 7 Typical application diagram

Figure 14. Typical application



## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 8.1 VFQFPN 10 x 13 x 1.0 mm package information

The package outline CAD file is available upon request.

Figure 15. VFQFPN 10 x 13 x 1.0 mm package outline (drawing top and side view)

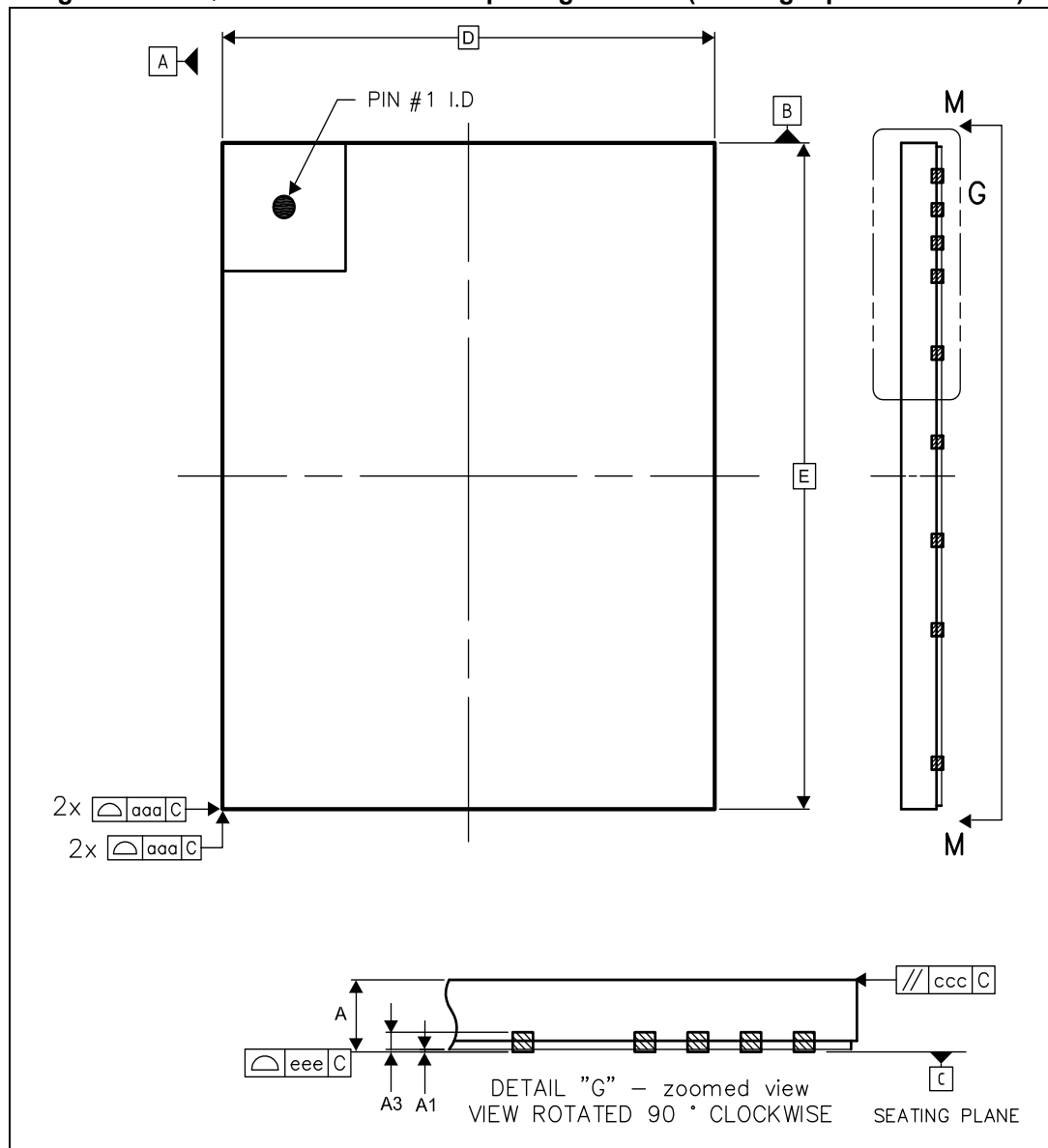




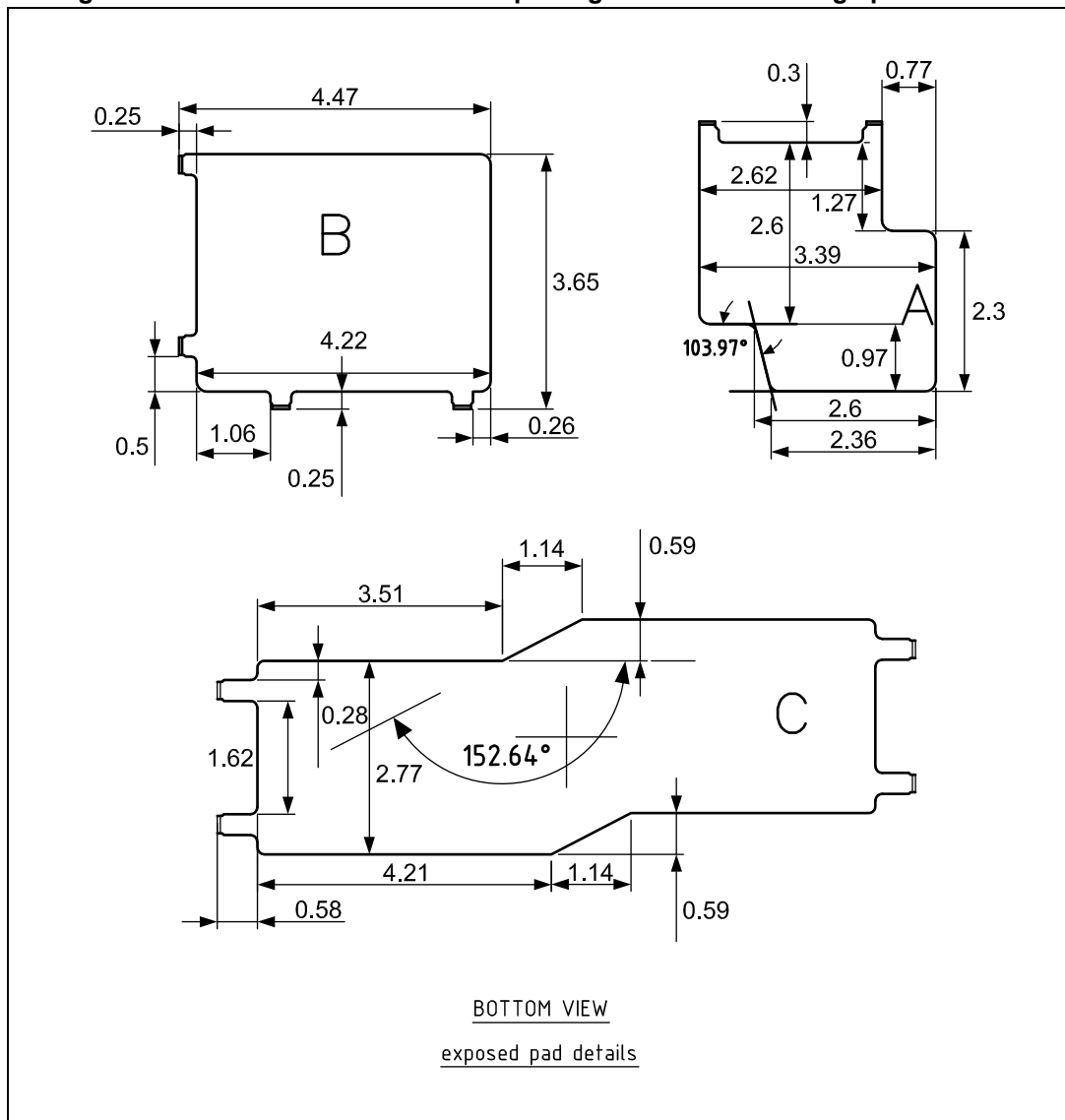
Table 10. VFQFPN 10 x 13 x 1.0 mm package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.00	-	0.05
A3	0.20		
b	0.15	0.25	0.35
b1	0.20	0.30	0.40
D	9.90	10.00	10.10
E	12.90	13.00	13.10
D1	0.70		
D2	2.52	2.62	2.72
D3	3.29	3.39	3.49
D4	0.25		
D5	4.12	4.22	4.32
D6	0.58		
D7	3.40	3.50	3.60
D8	3.59	3.69	3.79
D9	0.68		
E1	0.30		
E2	2.50	2.60	2.70
E3	3.47	3.57	3.67
E4	0.25		
E5	3.30	3.40	3.50
E6	2.67	2.77	2.87
E7	1.04	1.14	1.24
E8	0.005	-	0.09
L	0.35	0.40	0.45
e	0.65		
e1	3.45		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
N <sup>(1)</sup>	28		

1. N is the total number of terminals.



Figure 18. VFQFPN 10 x 13 x 1.0 mm package dimensions – large pads details



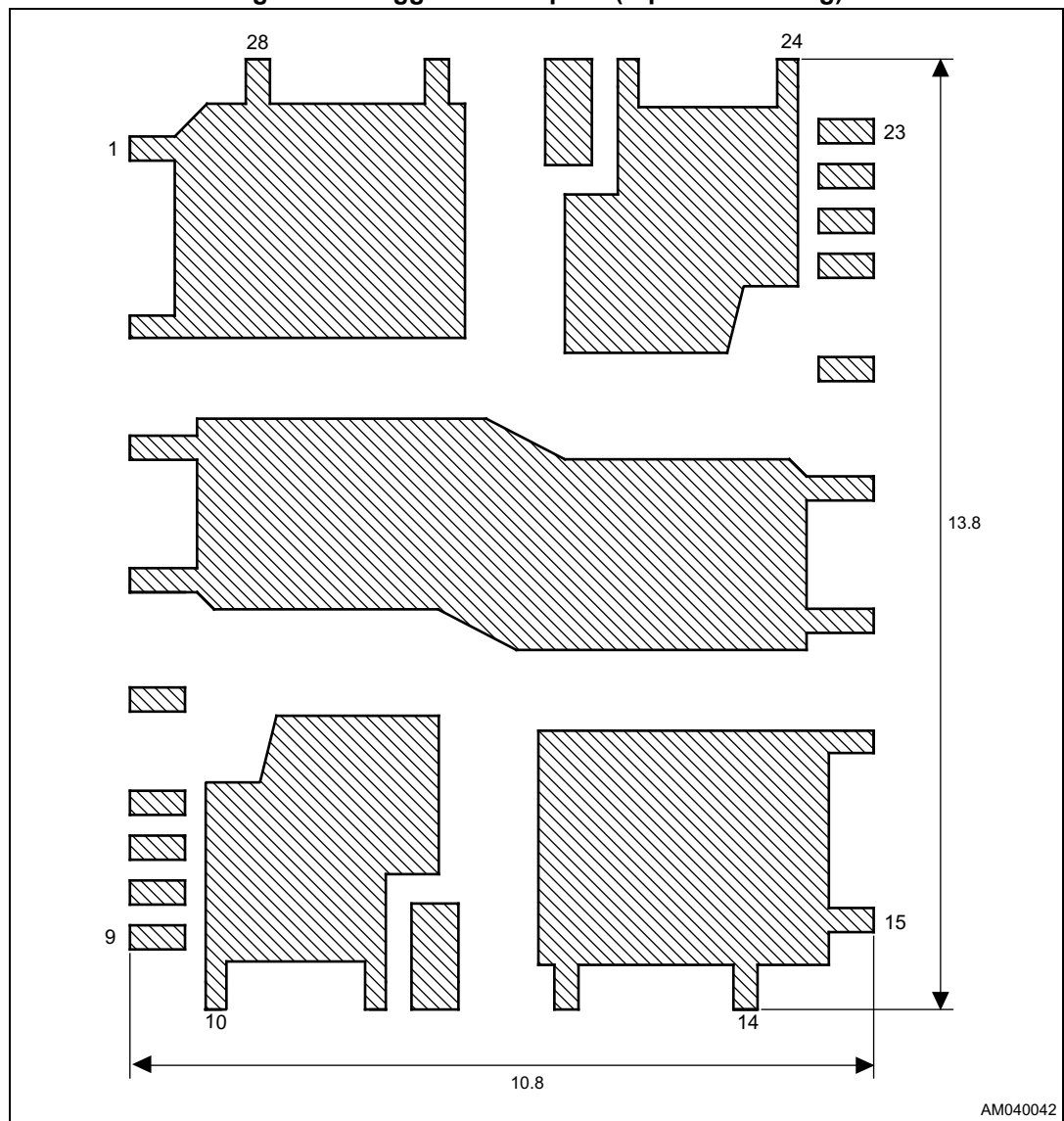
## 9 Suggested footprint

The PWD13F60 footprint for the PCB layout is usually defined based on several design factors as assembly plant technology capabilities and board component density. For easy device usage and evaluation, ST provides the following footprint design, which is suitable for the largest variety of PCBs.

The following footprint indicates the copper area which should be free from the solder mask, while the copper area shall extend beyond the indicated areas especially for the EPAD1, EPAD2, EPAD5. To aid thermal dissipation, it is recommended to add thermal vias under these EPADs to transfer and dissipate device heat to the other PCB copper layers. A PCB layout example is available with the PWD13F60 evaluation board.

As for the package outline, also the suggested footprint CAD file is available upon request.

Figure 19. Suggested footprint (top view drawing)







## 10 Ordering information

**Table 11. Device summary**

Order code	Package	Packaging
PWD13F60	VFQFPN 10 x 13 x 1.0 mm	Tray
PWD13F60TR	VFQFPN 10 x 13 x 1.0 mm	Tape and reel

## 11 Revision history

**Table 12. Document revision history**

Date	Revision	Changes
20-Jul-2017	1	Initial release.
02-Nov-2017	2	Updated document status to Datasheet - production data. Updated values and test conditions in <a href="#">Table 3 on page 7</a> , <a href="#">Table 5 on page 8</a> , and <a href="#">Table 6 on page 9</a> . Minor modifications throughout document.

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