



DAC7744

For most current data sheet and other product information, visit www.burr-brown.com

16-Bit, Quad Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **LOW POWER:** 200mW
- **UNIPOLAR OR BIPOLAR OPERATION**
- **SINGLE-SUPPLY OUTPUT RANGE:** +10V
- **DUAL SUPPLY OUTPUT RANGE:** $\pm 10V$
- **SETTLING TIME:** 10 μs to 0.003%
- **16-BIT MONOTONICITY:** $-40^{\circ}C$ to $+85^{\circ}C$
- **PROGRAMMABLE RESET TO MID-SCALE OR ZERO-SCALE**
- **DATA READBACK**
- **DOUBLE-BUFFERED DATA INPUTS**

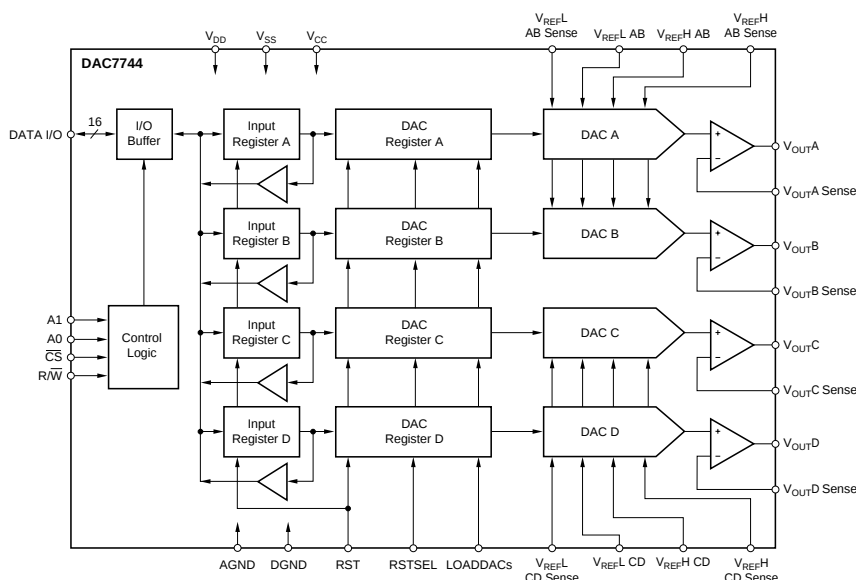
APPLICATIONS

- **PROCESS CONTROL**
- **ATE PIN ELECTRONICS**
- **CLOSED-LOOP SERVO-CONTROL**
- **MOTOR CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **DAC-PER-PIN PROGRAMMERS**

DESCRIPTION

The DAC7744 is a 16-bit, quad voltage output digital-to-analog converter with guaranteed 16-bit monotonic performance over the specified temperature range. It accepts 16-bit parallel input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a readback mode of the internal input registers. Programmable asynchronous reset clears all registers to a mid-scale code of 8000_H or to a zero-scale of 0000_H. The DAC7744 operates from either a single +15V supply or from a +15V, -15V, and +5V supply.

Low power and small size per DAC make the DAC7744 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7744 is available in a 48-lead SSOP package, and offers guaranteed specifications over the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: <http://www.burr-brown.com/> • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS (Dual Supply)

At $T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = +15V$, $V_{DD} = +5V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, and $V_{REFL} = -10V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7744E			DAC7744EB			DAC7744EC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY											
Linearity Error T_{MIN} to T_{MAX}	$T = 25^{\circ}C$			± 3 ± 4			*			± 2 ± 3	LSB LSB
Linearity Match			± 4			*			± 2		LSB
Differential Linearity Error T_{MIN} to T_{MAX}	$T = 25^{\circ}C$			± 3 ± 3			± 2 ± 2			± 1 ± 1	LSB LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			16			Bits
Bipolar Zero Error	$T = 25^{\circ}C$		± 0.01	± 0.025			*			*	% of FSR
Bipolar Zero Error, T_{MIN} to T_{MAX}				± 0.05			*			*	% of FSR
Full-Scale Error	$T = 25^{\circ}C$			± 0.025			*			*	% of FSR
Full-Scale Error, T_{MIN} to T_{MAX}				± 0.05			*			*	% of FSR
Bipolar Zero Matching	Channel-to-Channel Matching			± 0.024			*			*	% of FSR
Full-Scale Matching	Channel-to-Channel Matching			± 0.024			*			*	% of FSR
Power Supply Rejection Ratio (PSRR)	At Full Scale			25			*			*	ppm/V
ANALOG OUTPUT											
Voltage Output		V_{REFL}		V_{REFH}	*		*	*		*	V
Output Current		± 5			*			*			mA
Maximum Load Capacitance			500			*			*		pF
Short-Circuit Current			± 20			*			*		mA
Short-Circuit Duration	To V_{SS} , V_{DD} or GND		Indefinite			*			*		
REFERENCE INPUT											
Ref High Input Voltage Range		$V_{REFL} + 1.25$		+10	*		*	*		*	V
Ref Low Input Voltage Range		-10		$V_{REFH} - 1.25$	*		*	*		*	V
Ref High Input Current		-0.3		2.6		*			*		mA
Ref Low Input Current		-3.2		-0.3		*			*		mA
DYNAMIC PERFORMANCE											
Settling Time	To $\pm 0.003\%$, 20V Output Step		9	11		*	*		*	*	μs
Channel-to-Channel Crosstalk	See Figure 5		0.5			*			*		LSB
Digital Feedthrough			2			*			*		nV-s
Output Noise Voltage	$f = 10kHz$		60			*			*		$nV/\sqrt{Hz}$
DIGITAL INPUT											
V_{IH}		$0.7 \cdot V_{DD}$		V_{DD}	*			*			V
V_{IL}		0		$0.3 \cdot V_{DD}$			*				V
I_{IH}				± 10			*				μA
I_{IL}				± 10			*				μA
DIGITAL OUTPUT											
V_{OH}	$I_{OH} = -0.8mA$	3.6	4.5		*	*		*	*		V
V_{OL}	$I_{OL} = 1.6mA$		0.3	0.4		*	*		*	*	V
POWER SUPPLY											
V_{DD}		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
V_{CC}		+14.25	+15.0	+15.75	*	*	*	*	*	*	V
V_{SS}		-14.25	-15.0	-15.75	*	*	*	*	*	*	V
I_{DD}			50			*			*		μA
I_{CC}			6			*			*		mA
I_{SS}			-5			*			*		mA
Power			170	200		*			*		mW
TEMPERATURE RANGE											
Specified Performance		-40		+85	*		*	*		*	$^{\circ}C$

* Specifications same as grade to the left.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

SPECIFICATIONS (Single Supply)

At $T_A = T_{MIN}$ to T_{MAX} , $V_{CC} = +15V$, $V_{DD} = +5V$, $V_{SS} = GND$, $V_{REFH} = +10V$, and $V_{REFL} = +50mV$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7744E			DAC7744EB			DAC7744EC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY											
Linearity Error ⁽¹⁾	$T = 25^{\circ}C$			± 3			*			± 2	LSB
T_{MIN} to T_{MAX}				± 4			*			± 3	LSB
Linearity Match			± 4			*			± 2		LSB
Differential Linearity Error	$T = 25^{\circ}C$			± 3			± 2			± 1	LSB
T_{MIN} to T_{MAX}				± 3			± 2			± 1	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			16			Bits
Unipolar Zero	$T = 25^{\circ}C$		± 0.01	± 0.025			*			*	% of FSR
Unipolar Zero Error, T_{MIN} to T_{MAX}				± 0.05			*			*	% of FSR
Full-Scale Error	$T = 25^{\circ}C$			± 0.025			*			*	% of FSR
Full-Scale Error, T_{MIN} to T_{MAX}				± 0.05			*			*	% of FSR
Unipolar Zero Matching	Channel-to-Channel Matching			± 0.024			*			*	% of FSR
Full-Scale Matching	Channel-to-Channel Matching			± 0.024			*			*	% of FSR
Power Supply Rejection Ratio (PSRR)	At Full Scale			25			*			*	ppm/V
ANALOG OUTPUT											
Voltage Output	$V_{REFL} = 0V$, $V_{SS} = 0V$ $R = 10k\Omega$	0		V_{REFH}	*		*	*		*	V
Output Current		± 5			*			*			mA
Maximum Load Capacitance			500			*			*		pF
Short-Circuit Current			± 20			*			*		mA
Short-Circuit Duration	To V_{SS} , V_{CC} or GND		Indefinite			*			*		
REFERENCE INPUT											
Ref High Input Voltage Range		$V_{REFL} + 1.25$		+10	*		*	*		*	V
Ref Low Input Voltage Range		0		$V_{REFH} - 1.25$	*		*	*		*	V
Ref High Input Current		-0.3		1.0		*			*		mA
Ref Low Input Current		-1.5		-0.3		*			*		mA
DYNAMIC PERFORMANCE											
Settling Time	To $\pm 0.003\%$, 10V Output Step See Figure 6		8	10		*	*		*	*	μs
Channel-to-Channel Crosstalk			0.5			*			*		LSB
Digital Feedthrough			2			*			*		nV-s
Output Noise Voltage	$f = 10kHz$		60			*			*		$nV/\sqrt{Hz}$
DIGITAL INPUT											
V_{IH}		$0.7 \cdot V_{DD}$		V_{DD}	*			*			V
V_{IL}		0		$0.3 \cdot V_{DD}$			*				V
I_{IH}				± 10			*				μA
I_{IL}				± 10			*				μA
DIGITAL OUTPUT											
V_{OH}	$I_{OH} = -0.8mA$	3.6	4.5		*	*		*	*		V
V_{OL}	$I_{OL} = 1.6mA$		0.3	0.4		*	*		*	*	V
POWER SUPPLY											
V_{DD}		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
V_{CC}		+14.25	+15.0	+15.75	*	*	*	*	*	*	V
V_{SS}			0			*			*		V
I_{DD}			50			*			*		μA
I_{CC}			3.5			*			*		mA
Power			50	70		*			*		mW
TEMPERATURE RANGE											
Specified Performance		-40		+85	*		*	*		*	$^{\circ}C$

* Specifications same as grade to the left.

NOTE: (1) If $V_{SS} = 0V$, the specification applies at code 0021_H and above, due to possible negative zero scale error.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V_{CC} to V_{SS}	-0.3V to +32V
V_{CC} to AGND	-0.3V to +16V
V_{SS} to AGND	+0.3V to -16V
AGND to DGND	-0.3V to +0.3V
V_{REFH} to AGND	-9V to +11V
V_{REFL} to AGND	-11V to +9V
V_{DD} to GND	-0.3V to +6V
V_{REFH} to V_{REFL}	-1V to 22V
Digital Input Voltage to GND	-0.3V to $V_{DD} + 0.3V$
Digital Output Voltage to GND	-0.3V to $V_{DD} + 0.3V$
Maximum Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

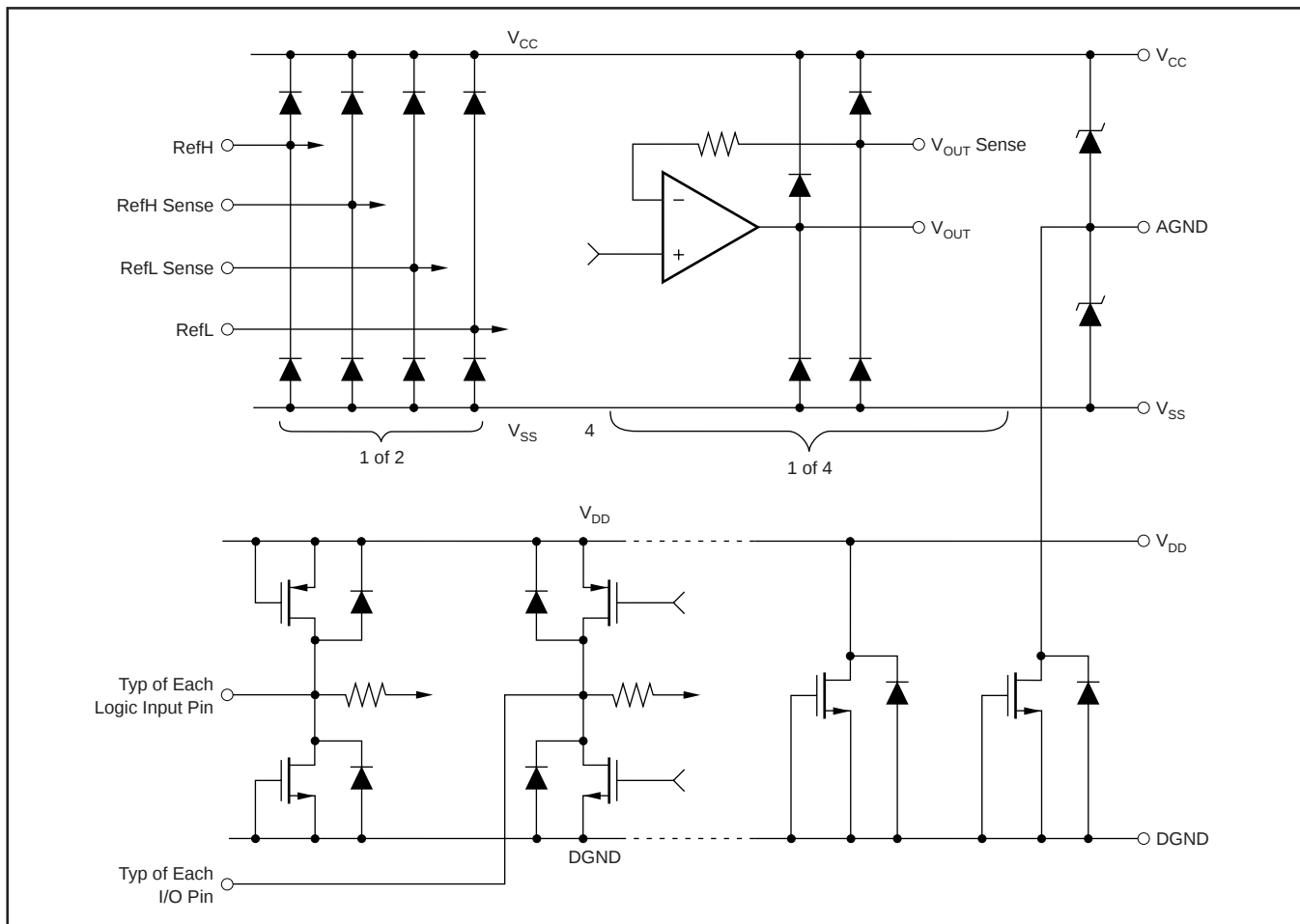
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

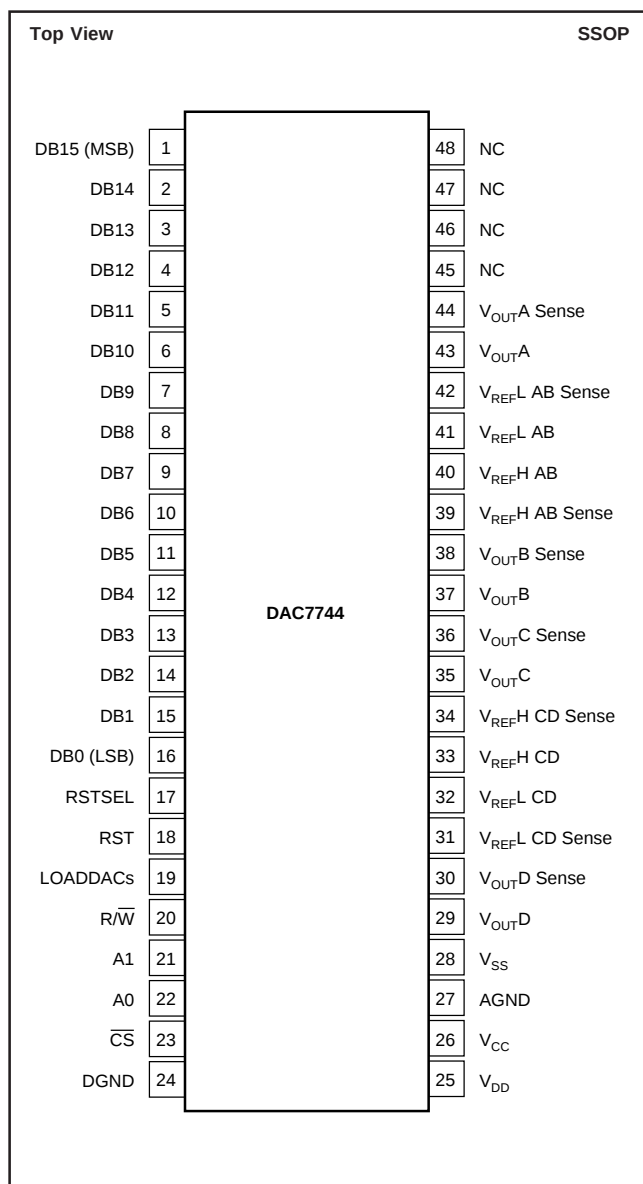
PRODUCT	LINEARITY ERROR (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER ⁽¹⁾	TRANSPORT MEDIA
DAC7744E "	±4 "	±3 "	48-Lead SSOP	333 "	-40°C to +85°C "	DAC7744E DAC7744E/1K	Rails Tape and Reel
DAC7744EB "	±4 "	±2 "	48-Lead SSOP	333 "	-40°C to +85°C "	DAC7744EB DAC7744EB/1K	Rails Tape and Reel
DAC7744EC "	±3 "	±1 "	48-Lead SSOP	333 "	-40°C to +85°C "	DAC7744EC DAC7744EC/1K	Rails Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "DAC7744E/1K" will get a single 1000-piece Tape and Reel.

ESD PROTECTION CIRCUITS



PIN CONFIGURATION



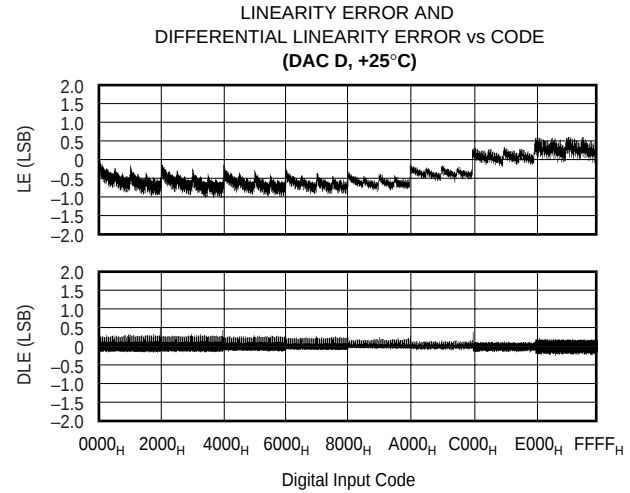
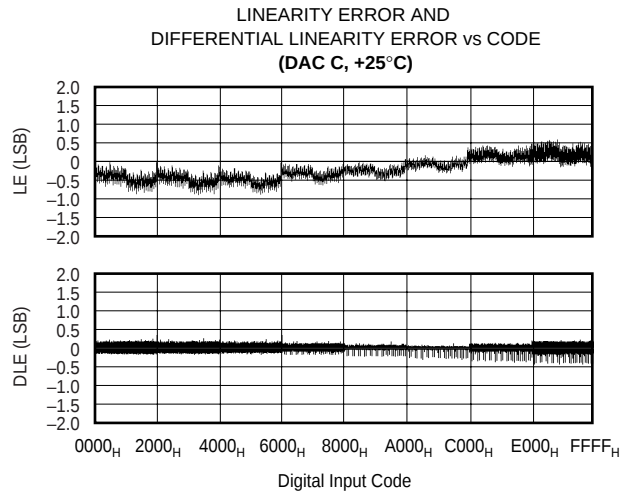
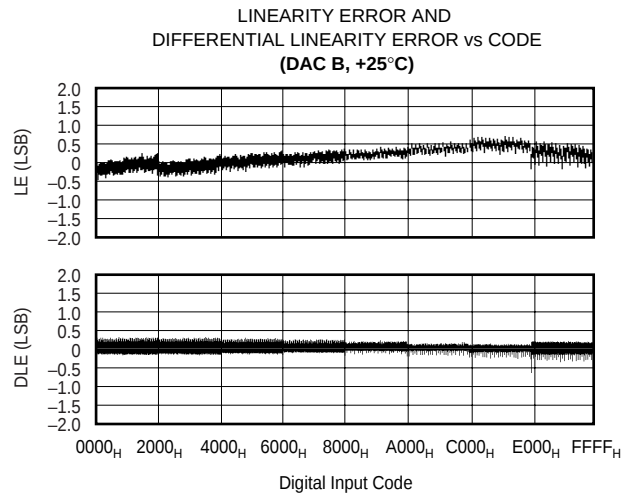
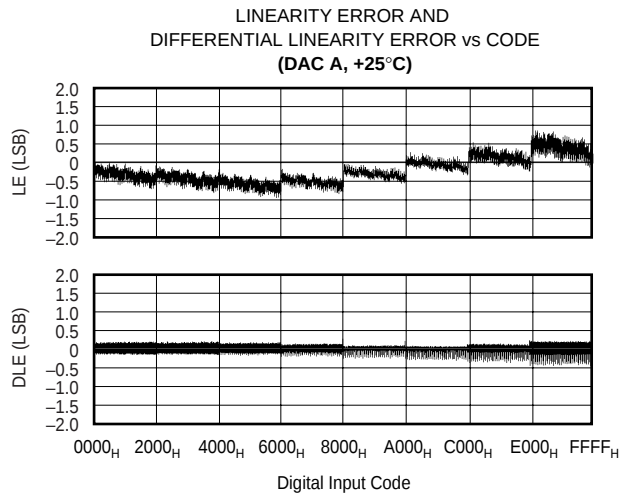
PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	DB15	Data Bit 15, MSB
2	DB14	Data Bit 14
3	DB13	Data Bit 13
4	DB12	Data Bit 12
5	DB11	Data Bit 11
6	DB10	Data Bit 10
7	DB9	Data Bit 9
8	DB8	Data Bit 8
9	DB7	Data Bit 7
10	DB6	Data Bit 6
11	DB5	Data Bit 5
12	DB4	Data Bit 4
13	DB3	Data Bit 3
14	DB2	Data Bit 2
15	DB1	Data Bit 1
16	DB0	Data Bit 0, LSB
17	RSTSEL	Reset Select. Determines the action of RST. If HIGH, a RST command will set the DAC registers to mid-scale. If LOW, a RST command will set the DAC registers to zero.
18	RST	Reset, Edge-Triggered. Depending on the state of RSTSEL, the DAC Input and Output registers are set to either mid-scale or zero.
19	LOADDACs	DAC Output Registers Load Control. Rising edge triggered.
20	R/W	Enabled by the $\overline{CS}$, controls data read and write from the input register.
21	A1	Enabled by the $\overline{CS}$, in combination with A0 selects the Individual DAC Input Registers.
22	A0	Enabled by the $\overline{CS}$, in combination with A1 selects the individual DAC input registers.
23	$\overline{CS}$	Chip Select, Active LOW.
24	DGND	Digital Ground
25	V _{DD}	Positive Power Supply
26	V _{CC}	Positive Power Supply
27	AGND	Analog Ground
28	V _{SS}	Negative Power Supply
29	V _{OUTD}	DAC D Voltage Output
30	V _{OUTD} Sense	DAC D's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
31	V _{REFL} CD Sense	DAC C and D Reference Low Sense Input
32	V _{REFL} CD	DAC C and D Reference Low Input
33	V _{REFH} CD	DAC C and D Reference High Input
34	V _{REFH} CD Sense	DAC C and D Reference High Sense Input
35	V _{OUTC}	DAC C Voltage Output
36	V _{OUTC} Sense	DAC C's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
37	V _{OUTB}	DAC B Voltage Output
38	V _{OUTB} Sense	DAC B's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
39	V _{REFH} AB Sense	DAC A and B Reference High Sense Input
40	V _{REFH} AB	DAC A and B Reference High Input
41	V _{REFL} AB	DAC A and B Reference Low Input
42	V _{REFL} AB Sense	DAC A and B Reference Low Sense Input
43	V _{OUTA}	DAC A Voltage Input
44	V _{OUTA} Sense	DAC A's Output Amplifier Inverting Input. Used to close the feedback loop at the load.
45	NC	No Connection
46	NC	No Connection
47	NC	No Connection
48	NC	No Connection

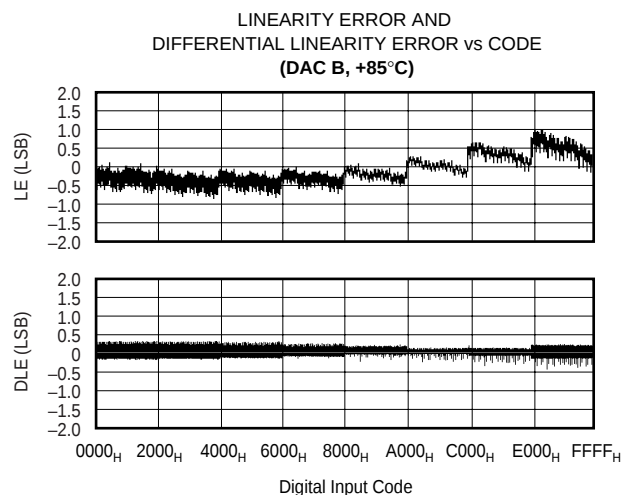
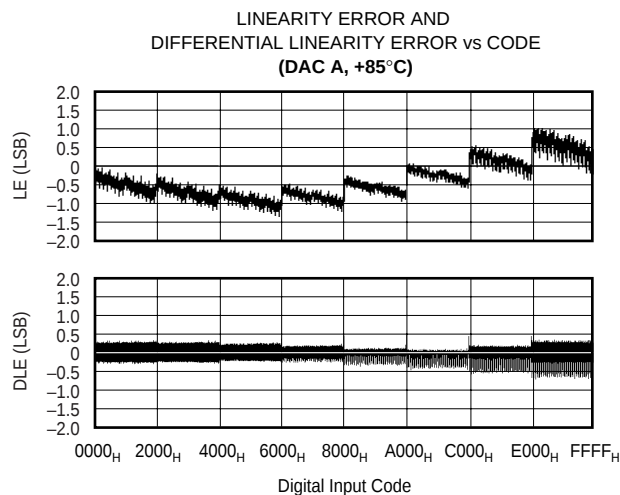
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = 0$, $V_{REFH} = +10V$, and $V_{REFL} = 0V$, representative unit, unless otherwise specified.

+25°C



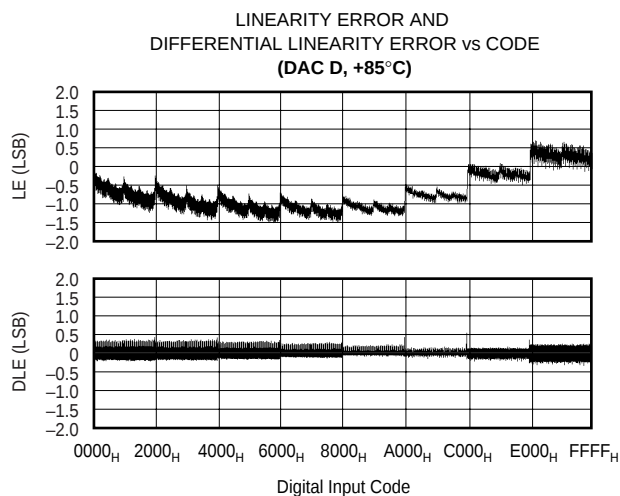
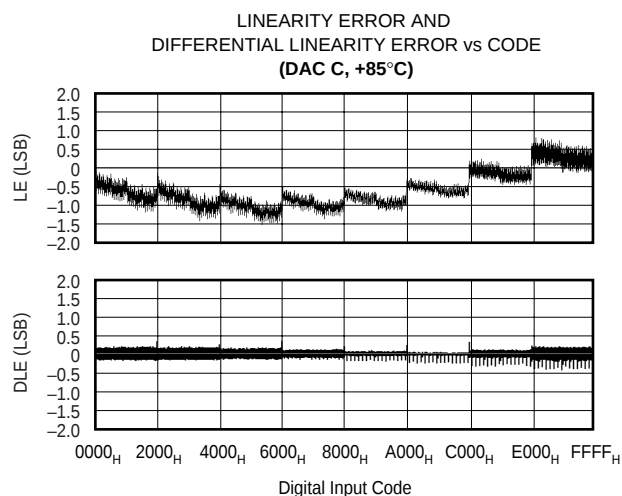
+85°C



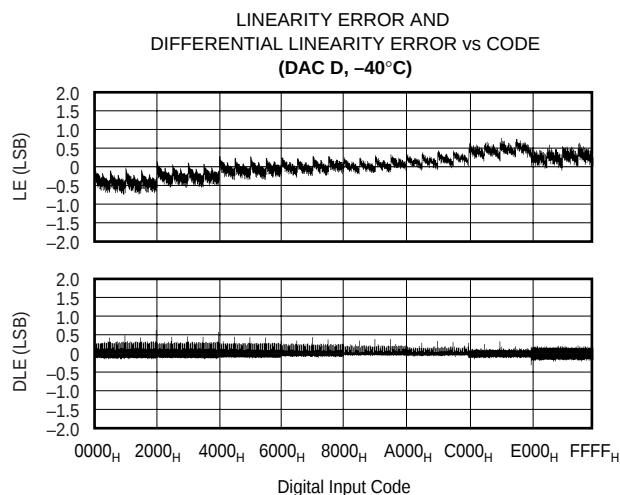
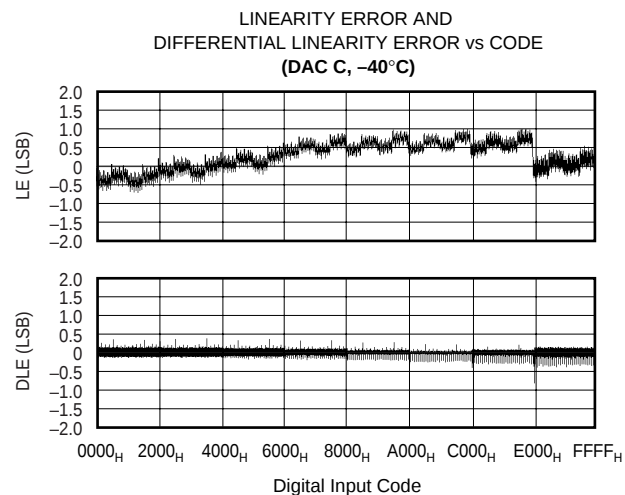
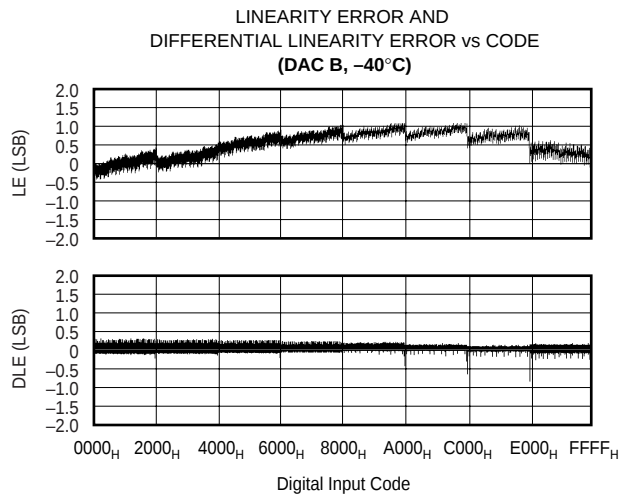
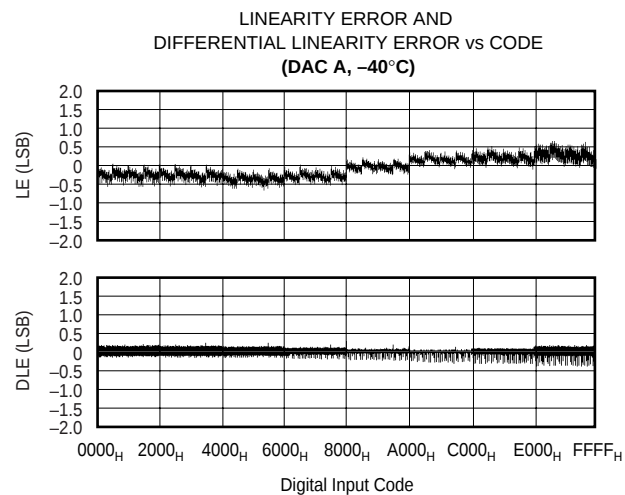
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = 0$, $V_{REFH} = +10V$, and $V_{REFL} = 0V$, representative unit, unless otherwise specified.

+85°C (cont.)

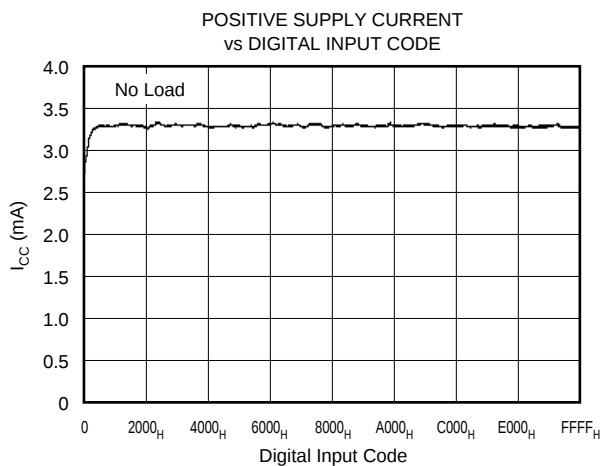
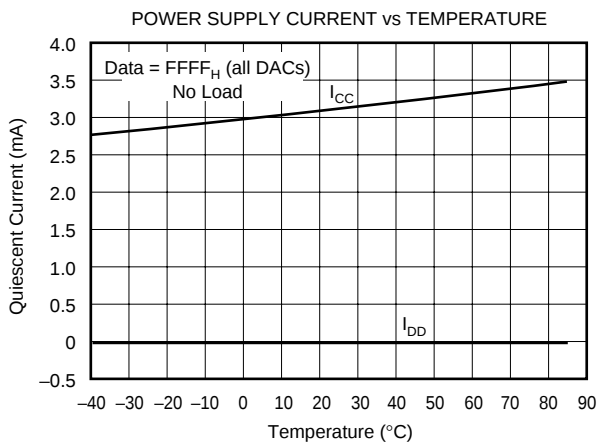
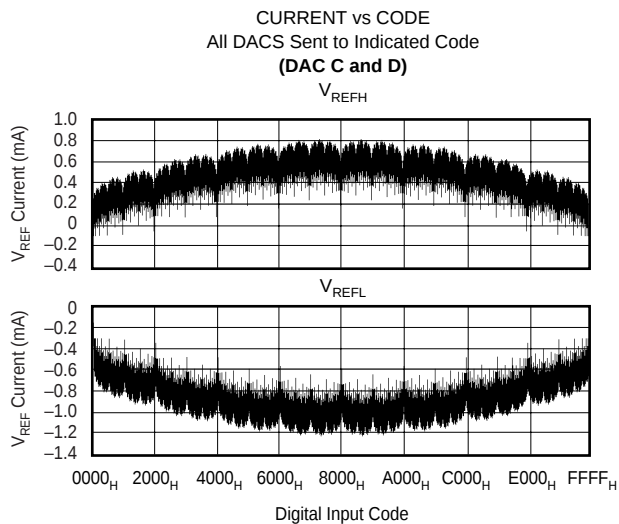
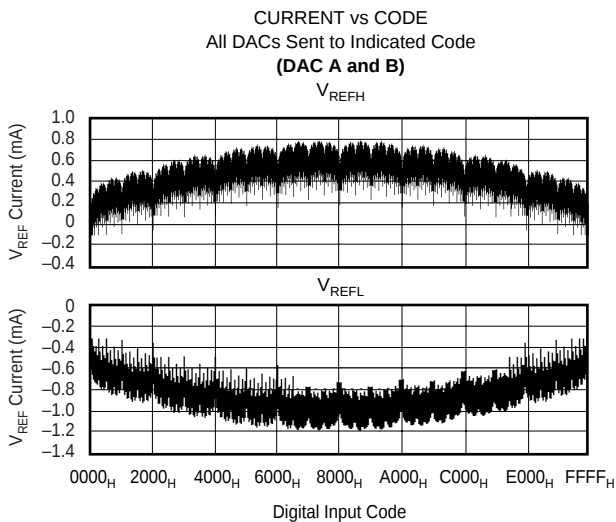
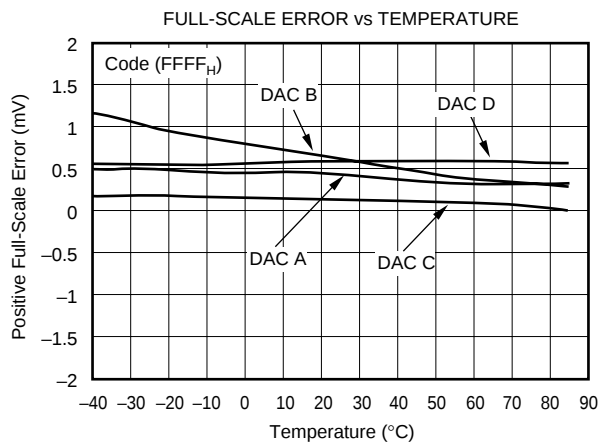
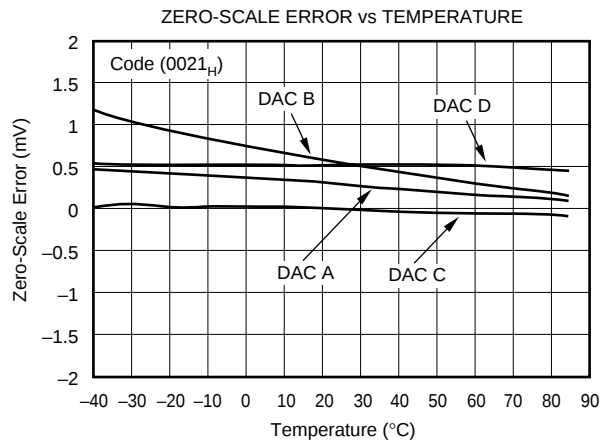


-40°C



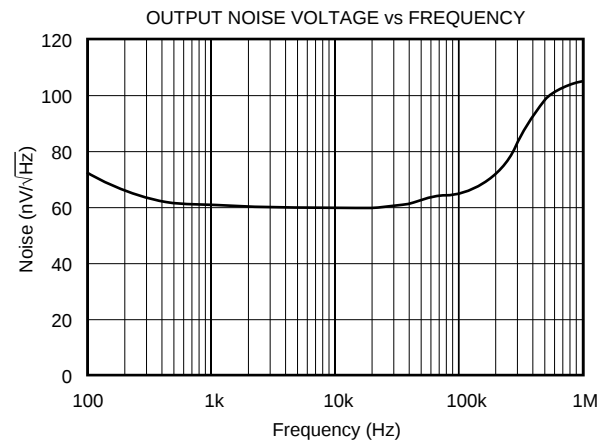
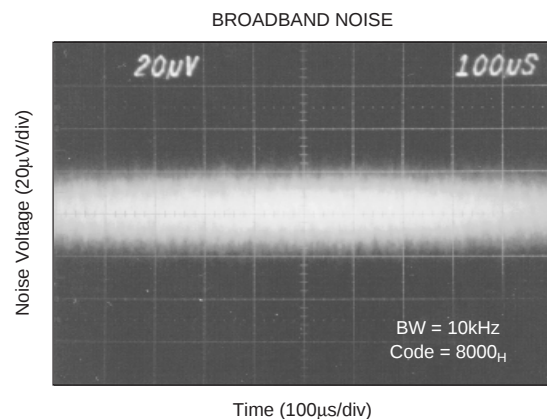
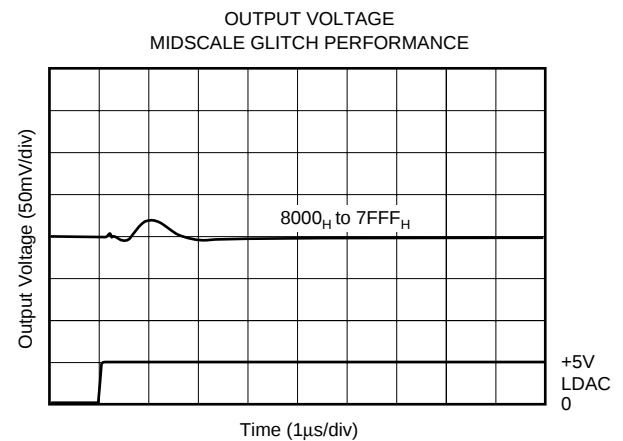
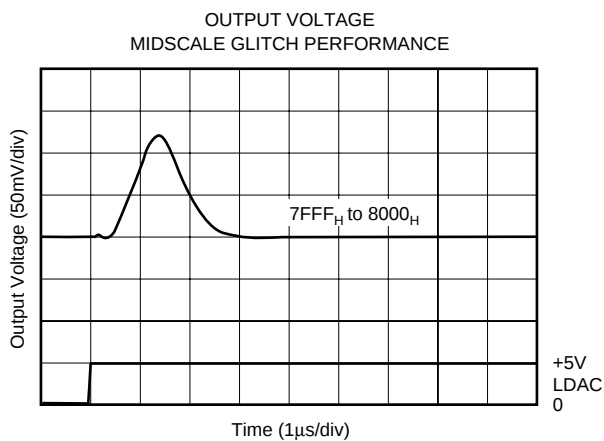
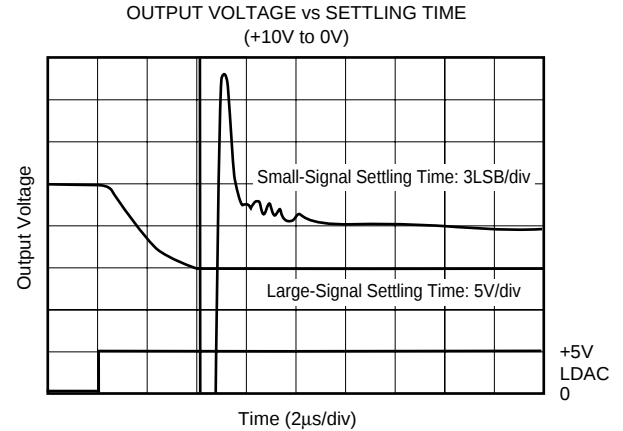
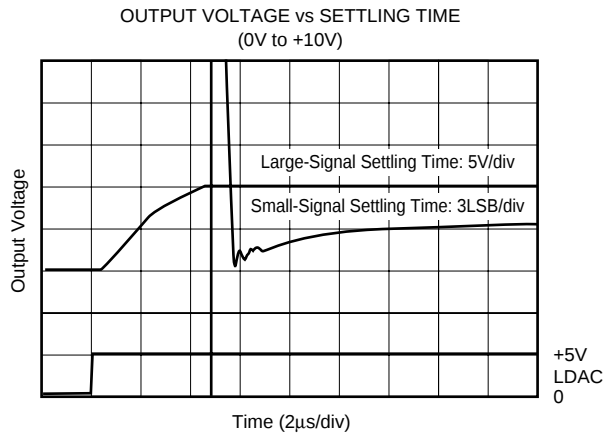
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = 0$, $V_{REFH} = +10V$, and $V_{REFL} = 0V$, representative unit, unless otherwise specified.



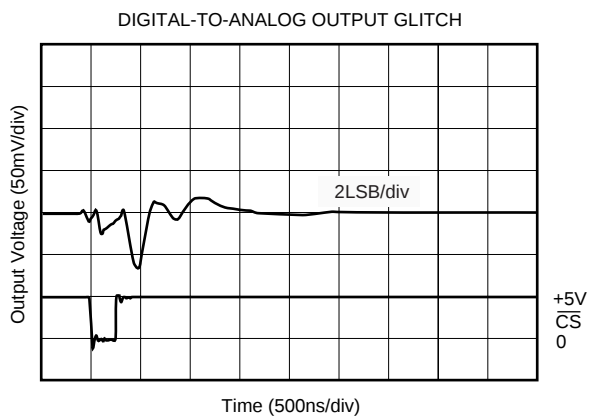
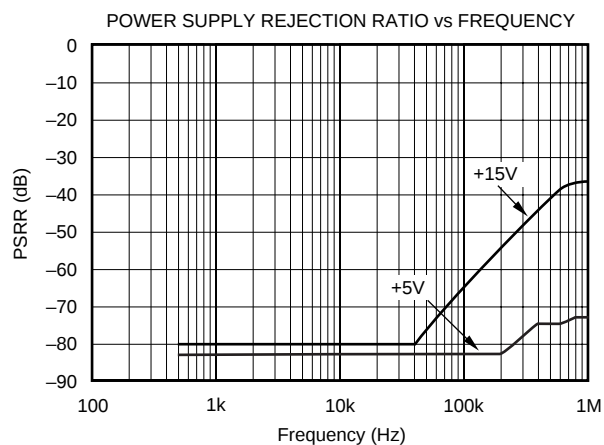
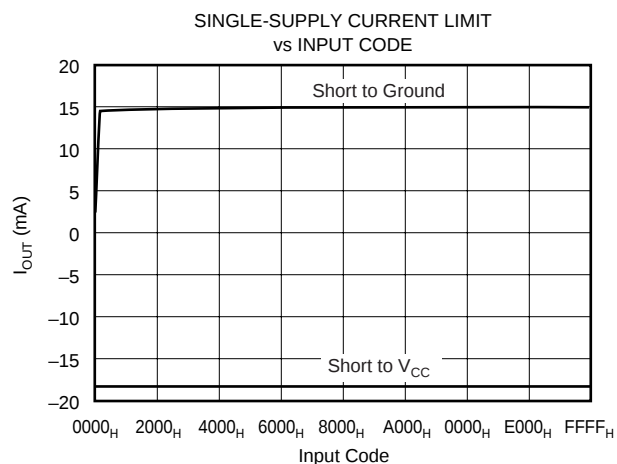
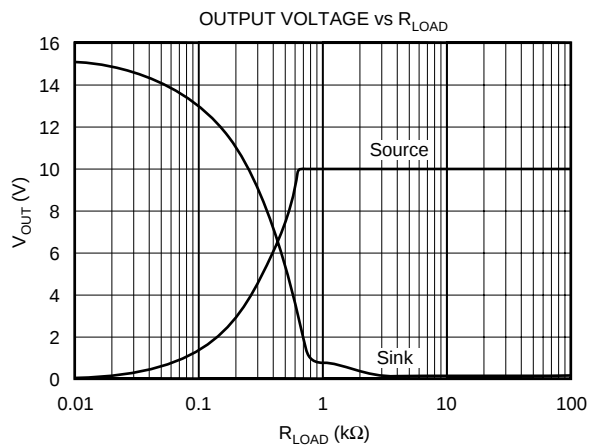
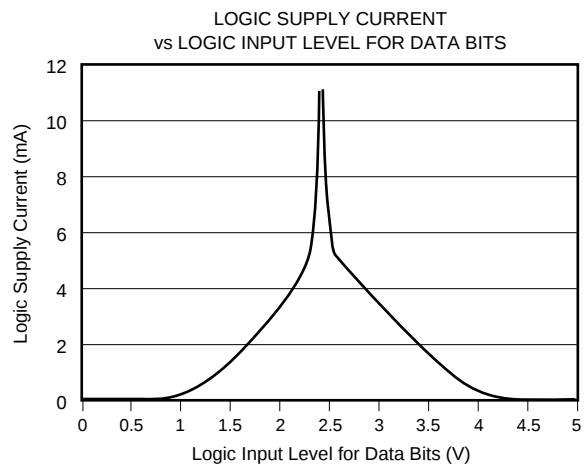
TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = 0$, $V_{REFH} = +10V$, and $V_{REFL} = 0V$, representative unit, unless otherwise specified.



TYPICAL PERFORMANCE CURVES: $V_{SS} = 0V$ (Cont.)

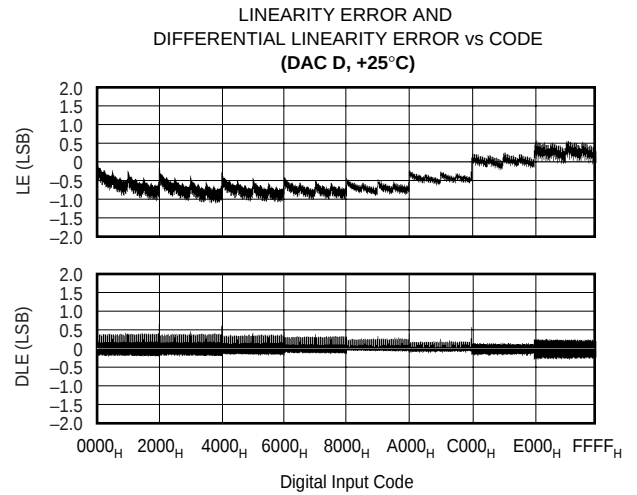
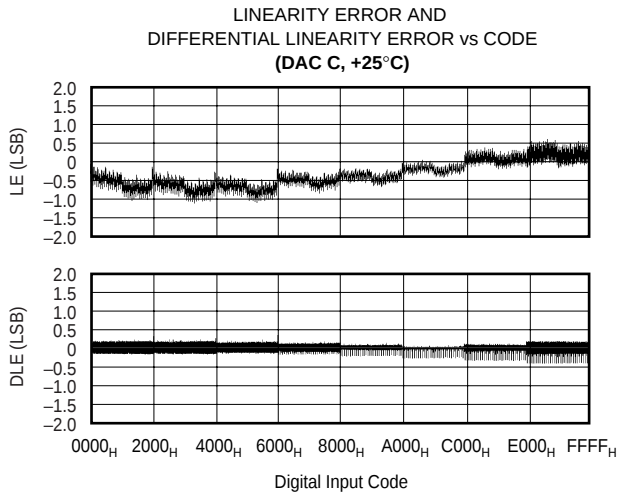
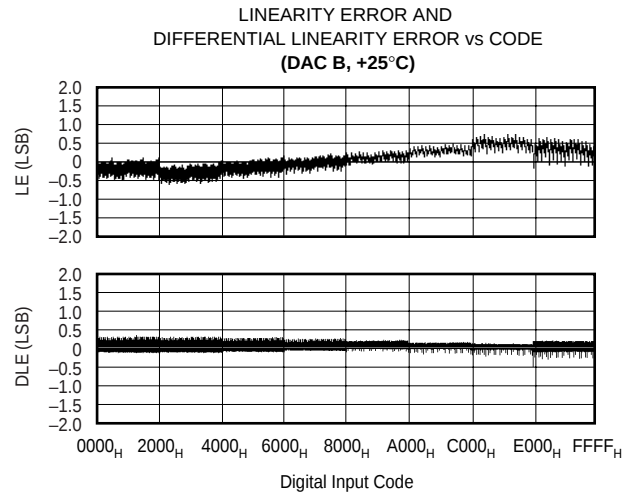
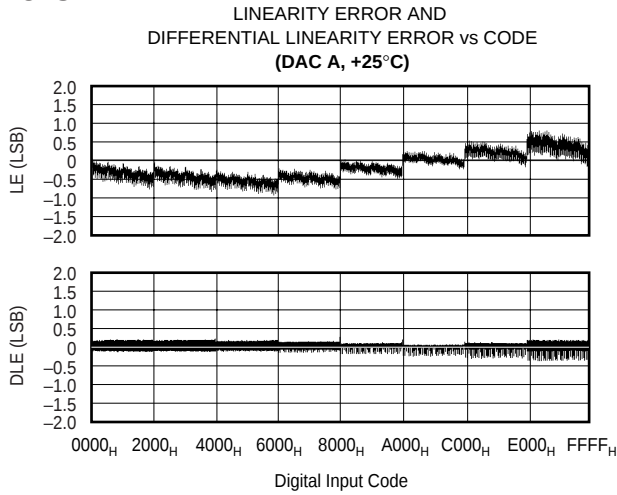
At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = 0$, $V_{REFH} = +10V$, and $V_{REFL} = 0V$, representative unit, unless otherwise specified.



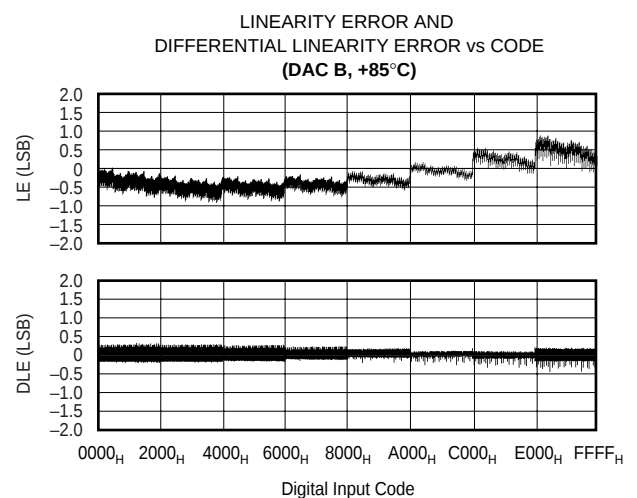
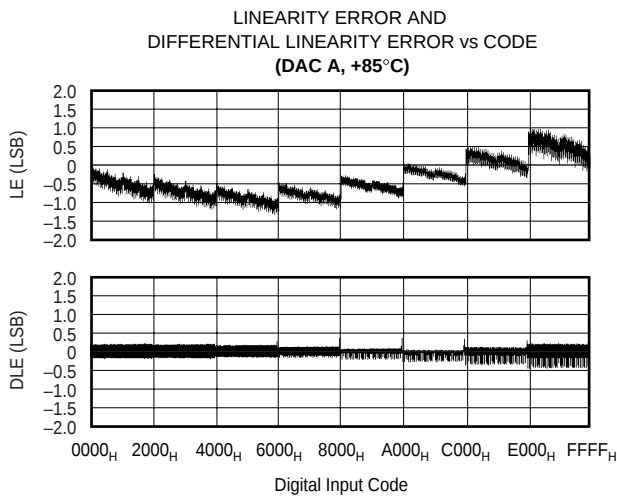
TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, and $V_{REFL} = -10V$, representative unit, unless otherwise specified.

+25°C



+85°C

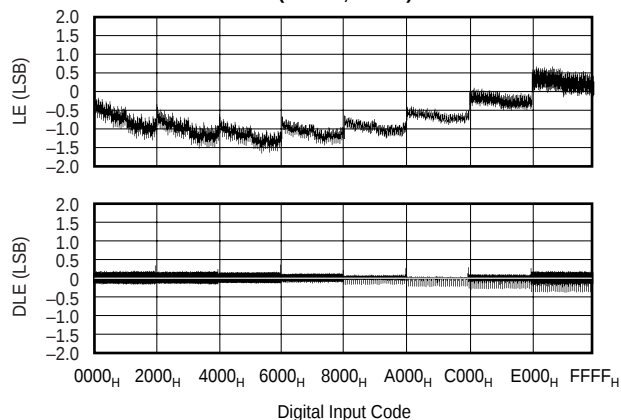


TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

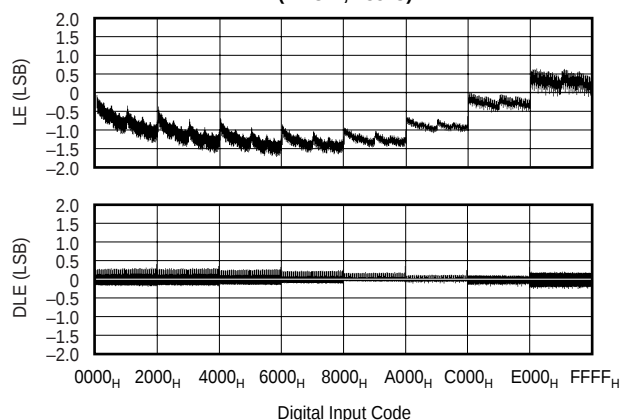
At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, and $V_{REFL} = -10V$, representative unit, unless otherwise specified.

+85°C (cont.)

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, +85°C)

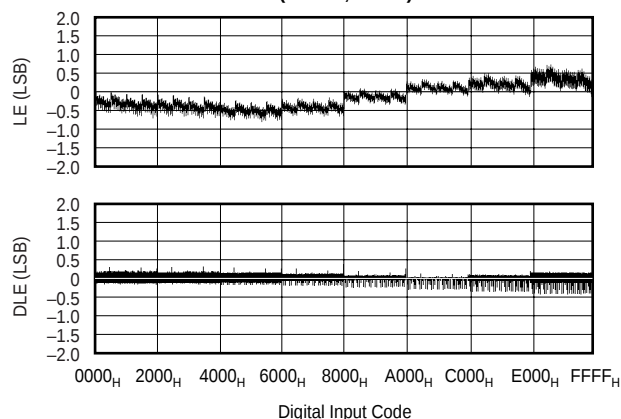


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, +85°C)

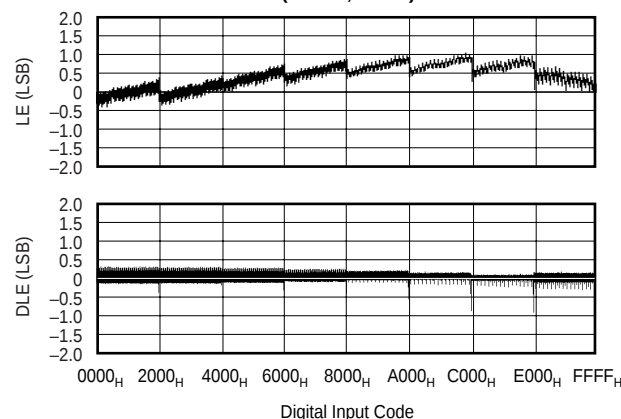


-40°C

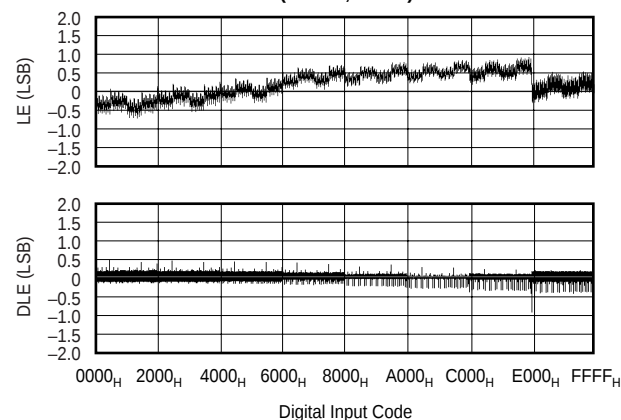
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, -40°C)



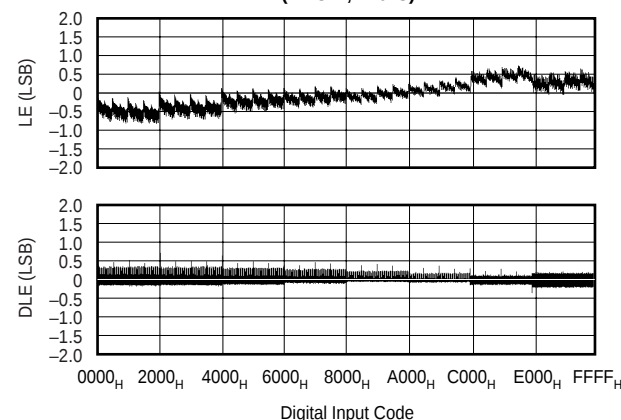
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, -40°C)



LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC C, -40°C)

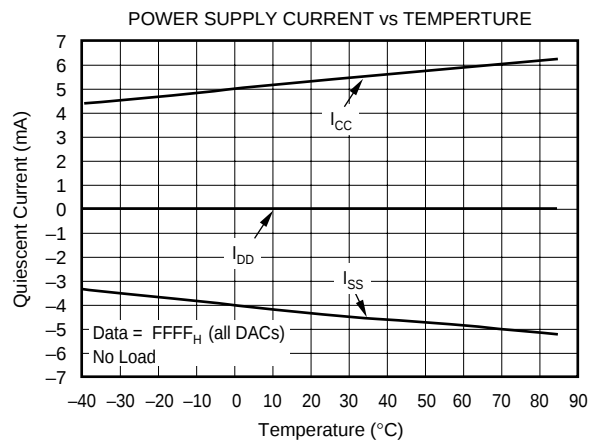
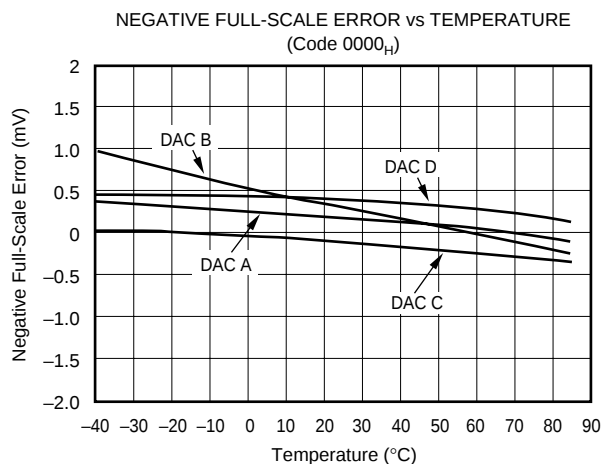
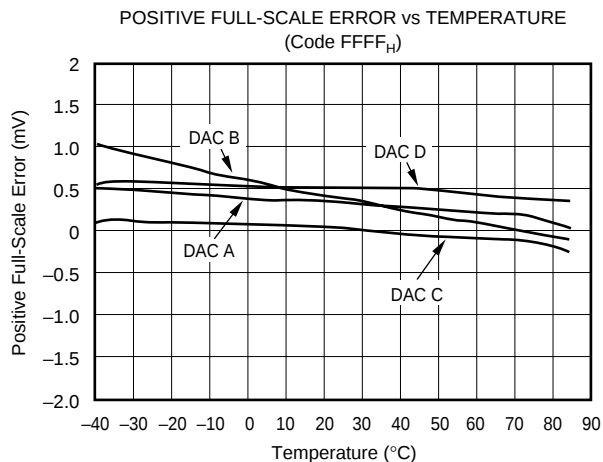
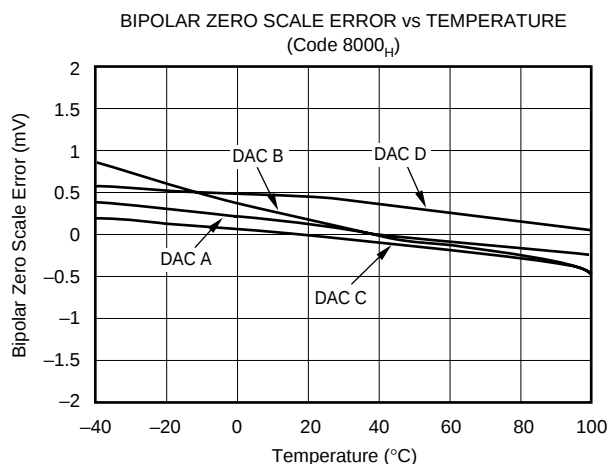
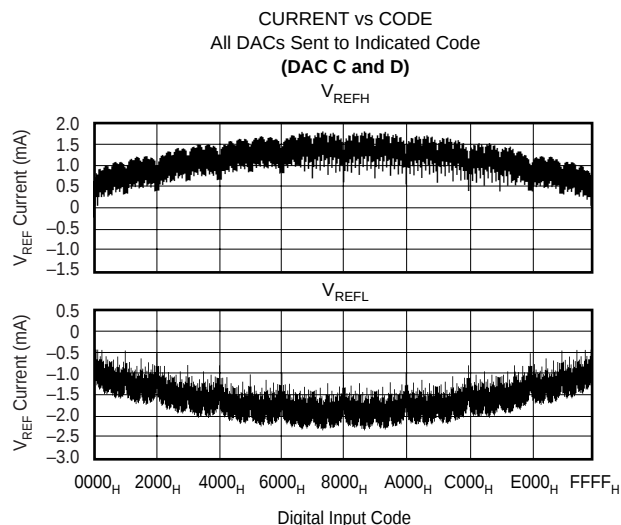
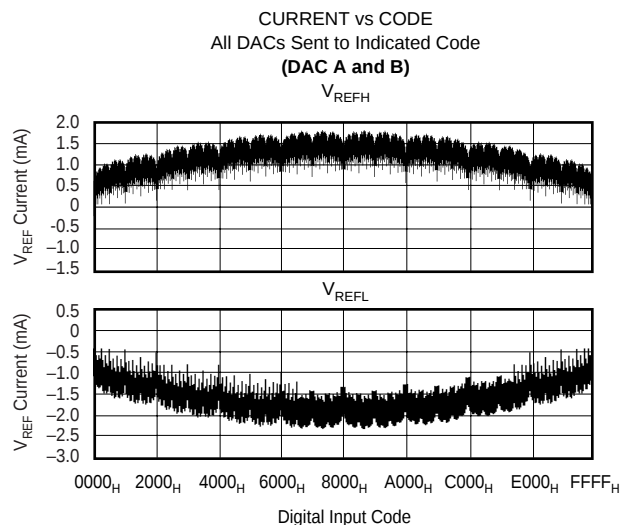


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC D, -40°C)



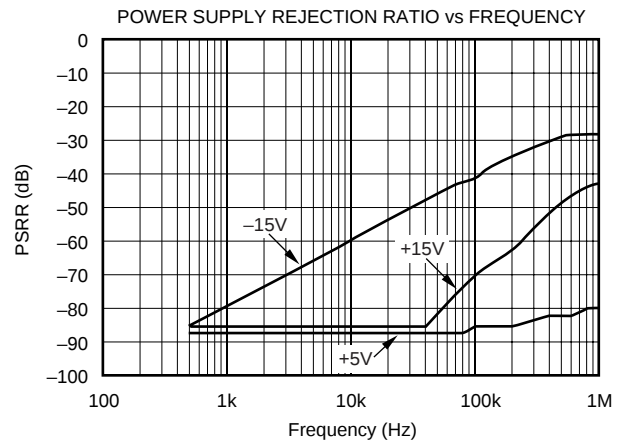
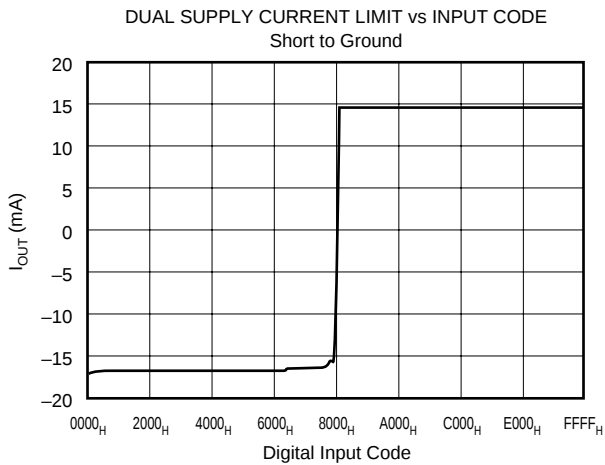
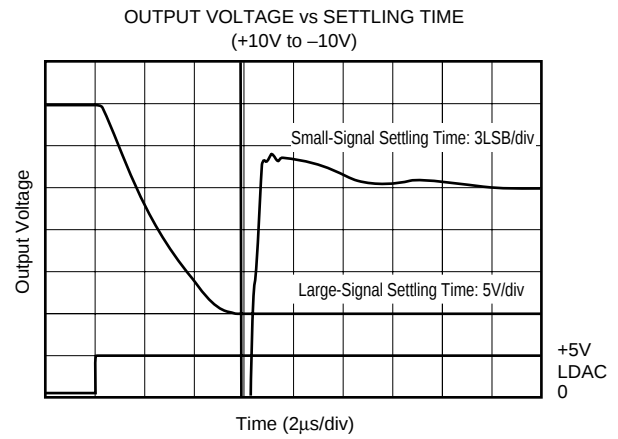
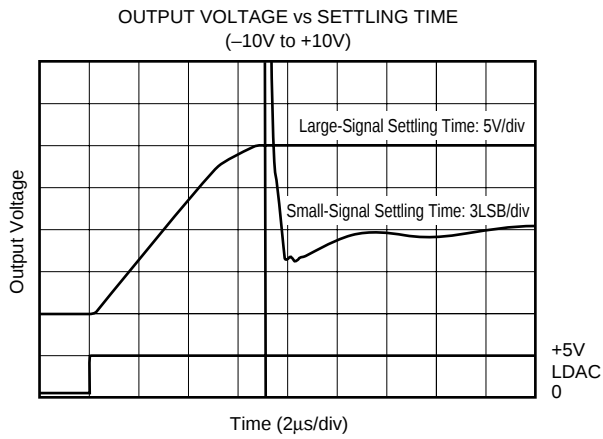
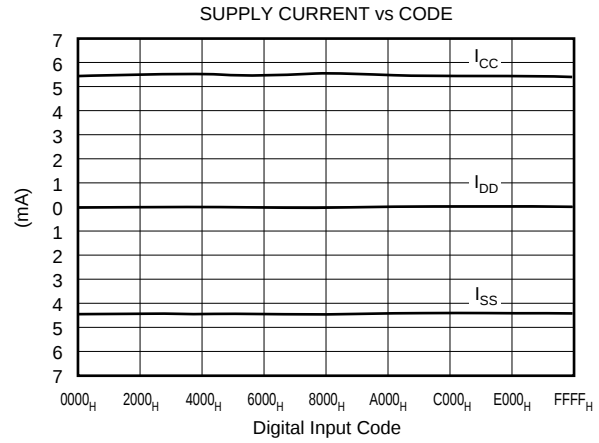
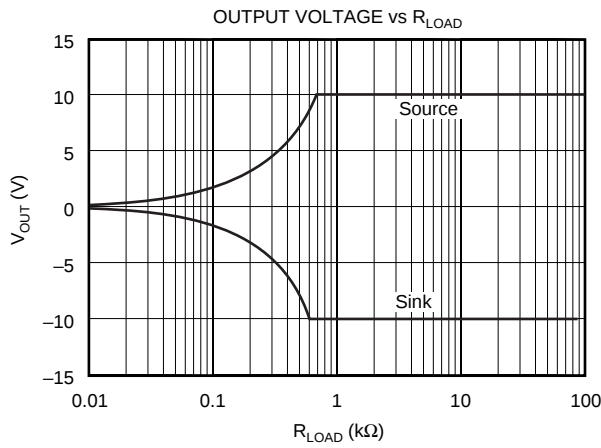
TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, and $V_{REFL} = -10V$, representative unit, unless otherwise specified.



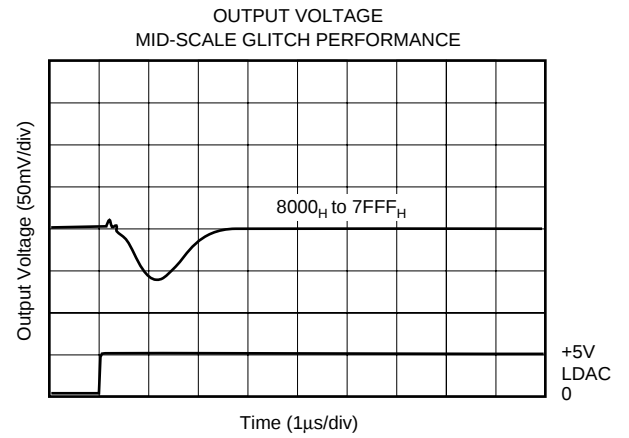
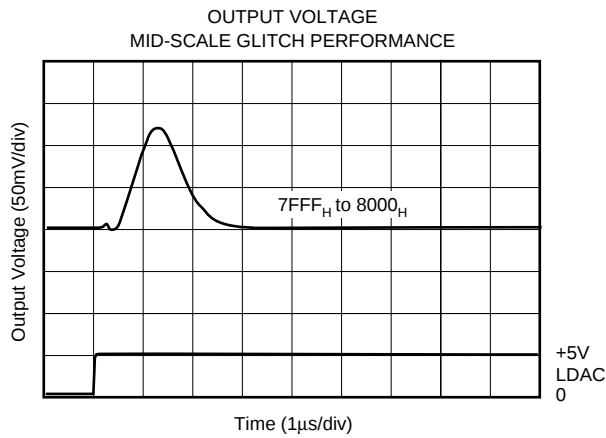
TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, and $V_{REFL} = -10V$, representative unit, unless otherwise specified.



TYPICAL PERFORMANCE CURVES: $V_{SS} = -15V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = +5V$, $V_{CC} = +15V$, $V_{SS} = -15V$, $V_{REFH} = +10V$, and $V_{REFL} = -10V$, representative unit, unless otherwise specified.



THEORY OF OPERATION

The DAC7744 is a quad voltage output, 16-bit digital-to-analog converter (DAC). The architecture is an R-2R ladder configuration with the three MSB's segmented followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network, segmented MSBs and output op amp (see Figure 1). The minimum voltage output (zero scale) and maximum voltage output (full scale) are set

by the external voltage references (V_{REFL} and V_{REFH} , respectively). The digital input is a 16-bit parallel word and the DAC input registers offer a readback capability. The converters can be powered from either a single +15V supply or a dual $\pm 15V$ supply. The device offers a reset function which immediately sets all DAC output voltages and DAC registers to mid-scale code 8000_H or to zero scale, code 0000_H. See Figures 2 and 3 for the basic operation of the DAC7744.

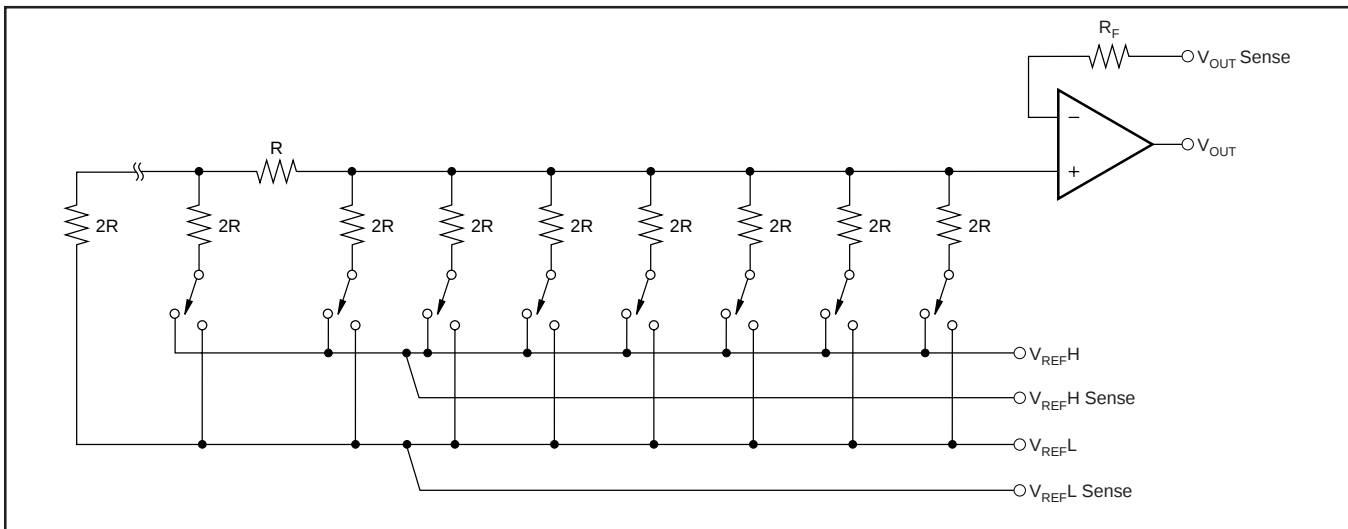


FIGURE 1. DAC7744 Architecture.

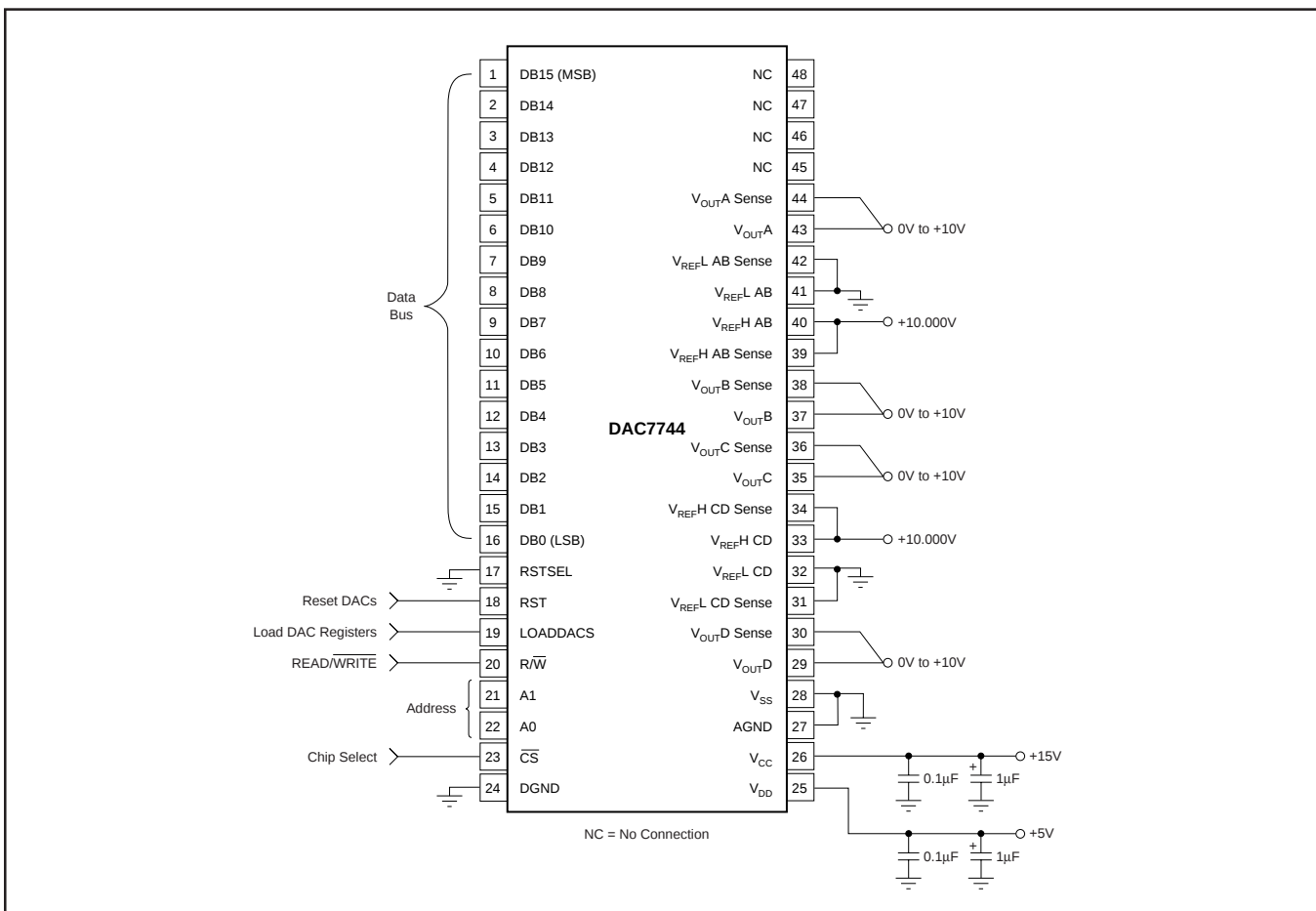


FIGURE 2. Basic Single-Supply Operation of the DAC7744.

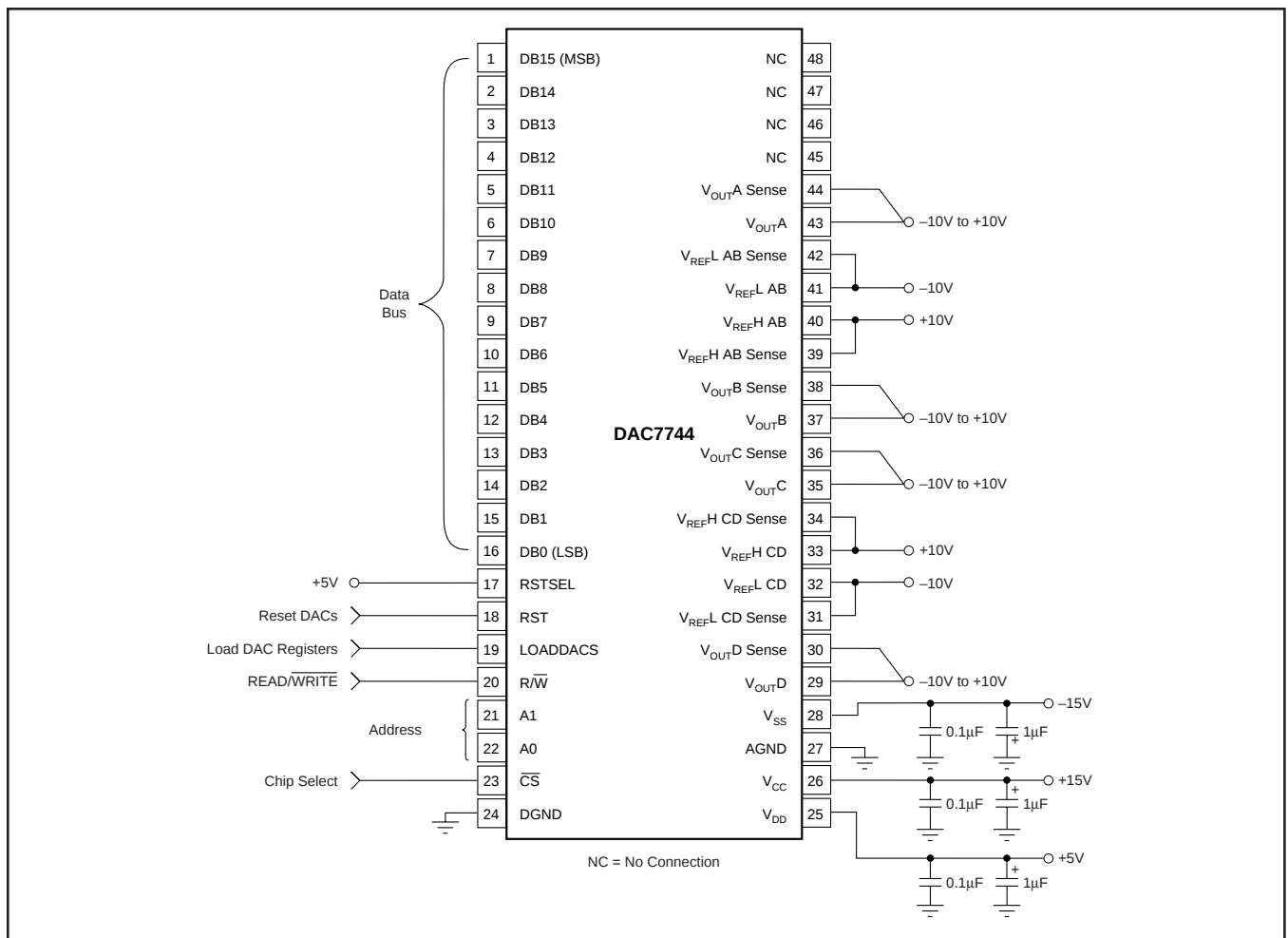


FIGURE 3. Basic Dual-Supply Operation of the DAC7744.

ANALOG OUTPUTS

When $V_{SS} = -15V$ (dual supply operation), the output amplifier can swing to within $4V$ of the supply rails, guaranteed over the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range. With $V_{SS} = 0V$ (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when $V_{SS} = 0V$. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000_H , 0001_H , 0002_H , etc.), if the output amplifier has a negative offset. At the negative limit of $-5mV$, the first specified output starts at code 0021_H .

Due to the high accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 10V full-scale range has a 1LSB value of $152\mu\text{V}$. With a load current of 1mA, series wiring and connector resistance of only $150\text{m}\Omega$ (R_{w2}) will cause a voltage drop of $150\mu\text{V}$, as shown in Figure 4. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is $1/2 \text{ m}\Omega$ per square. For a 1mA load, a 20 milli-inch wide printed circuit conductor 6 inches long will result in a voltage drop of $150\mu\text{V}$.

The DAC7744 offers a force and sense output configuration for the high open-loop gain output amplifiers. This feature

allows the loop around the output amplifier to be closed at the load, thus ensuring an accurate output voltage, as shown in Figure 4.

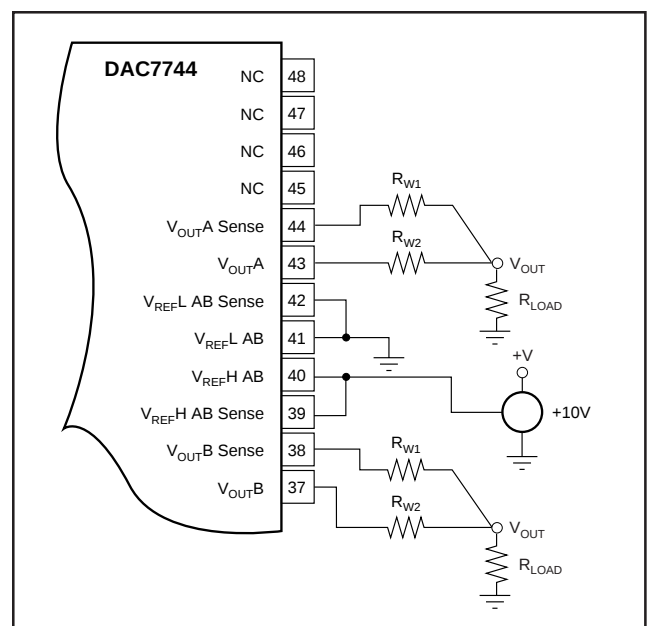


FIGURE 4. Analog Output Closed-Loop Configuration (1/2 DAC7744). R_W represents wiring resistances.

REFERENCE INPUTS

The reference inputs, V_{REFL} and V_{REFH} , can be any voltage between $V_{SS} + 4V$ and $V_{CC} - 4V$, provided that V_{REFH} is at least 1.25V greater than V_{REFL} . The minimum output of each DAC is equal to V_{REFL} plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of $-14.25V$ to $-15.75V$. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the V_{REFH} input and out of V_{REFL} depends on the DAC output voltages and can vary from a few

microamps to approximately 2.0mA. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. The DAC7744 features a reference drive and sense connection such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figures 5 through 12 show different reference configurations and the effect on the linearity and differential linearity.

The analog supplies (or the analog supplies and the reference power supplies) have to come up first. If the power supplies for the reference come up first, then the V_{CC} and V_{SS} supplies will be “powered from the reference via the ESD protection diode”, see page 4.

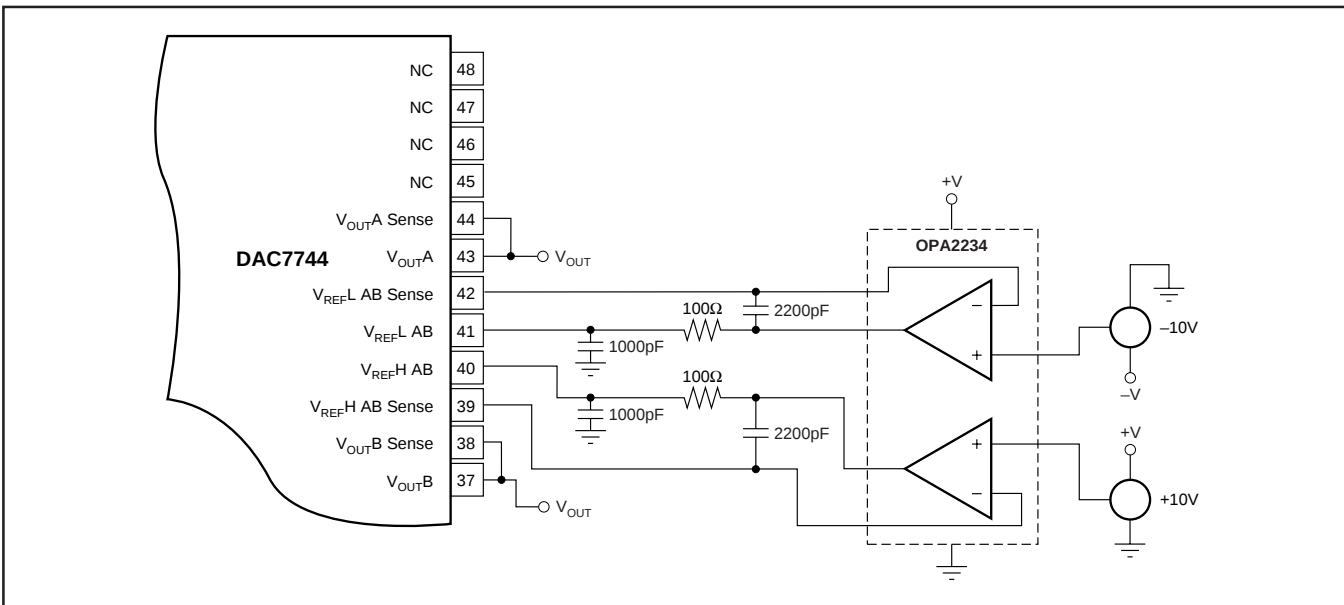


FIGURE 5. Dual Supply Configuration-Buffered References, used for Dual Supply Performance Curves (1/2 DAC7744).

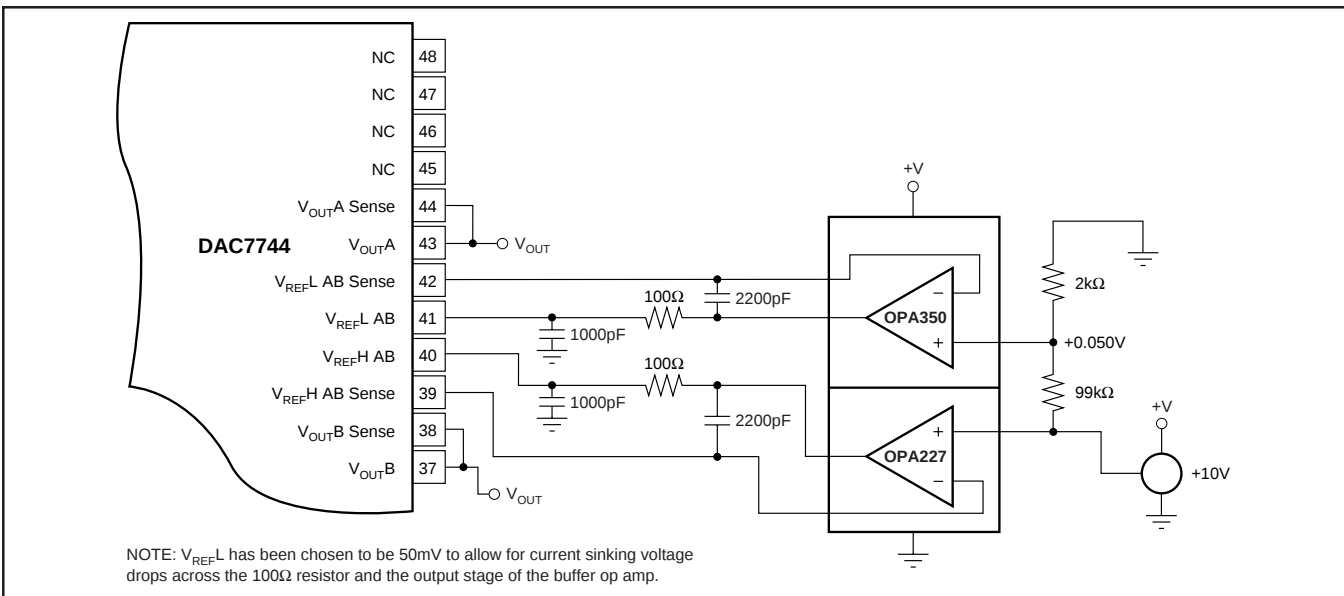


FIGURE 6. Single-Supply Buffered Reference with a Reference Low of 50mV Used for Single-Supply Performance Curves (1/2 DAC7744).

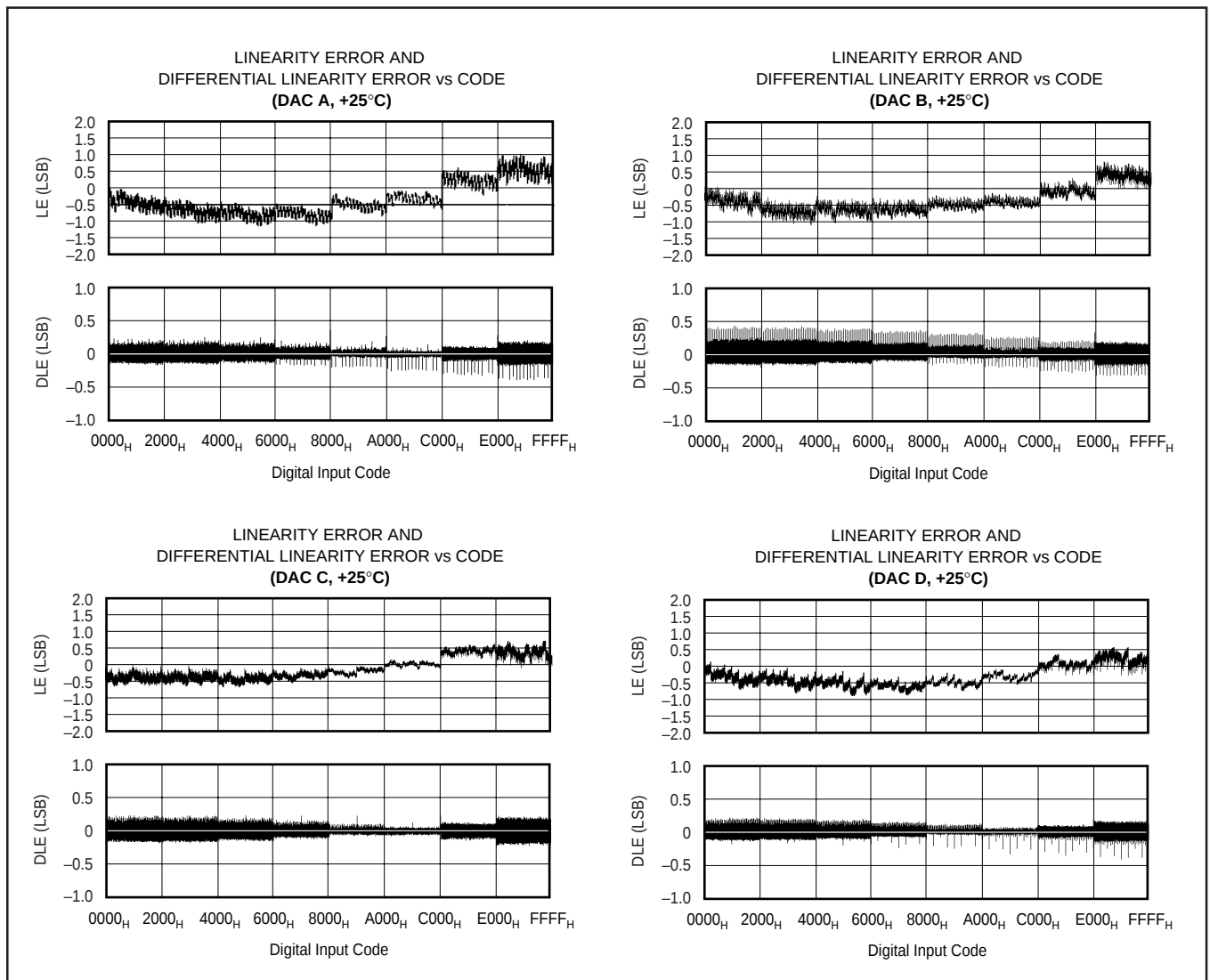


FIGURE 7. Integral Linearity and Differential Linearity Error Curves for Figure 8.

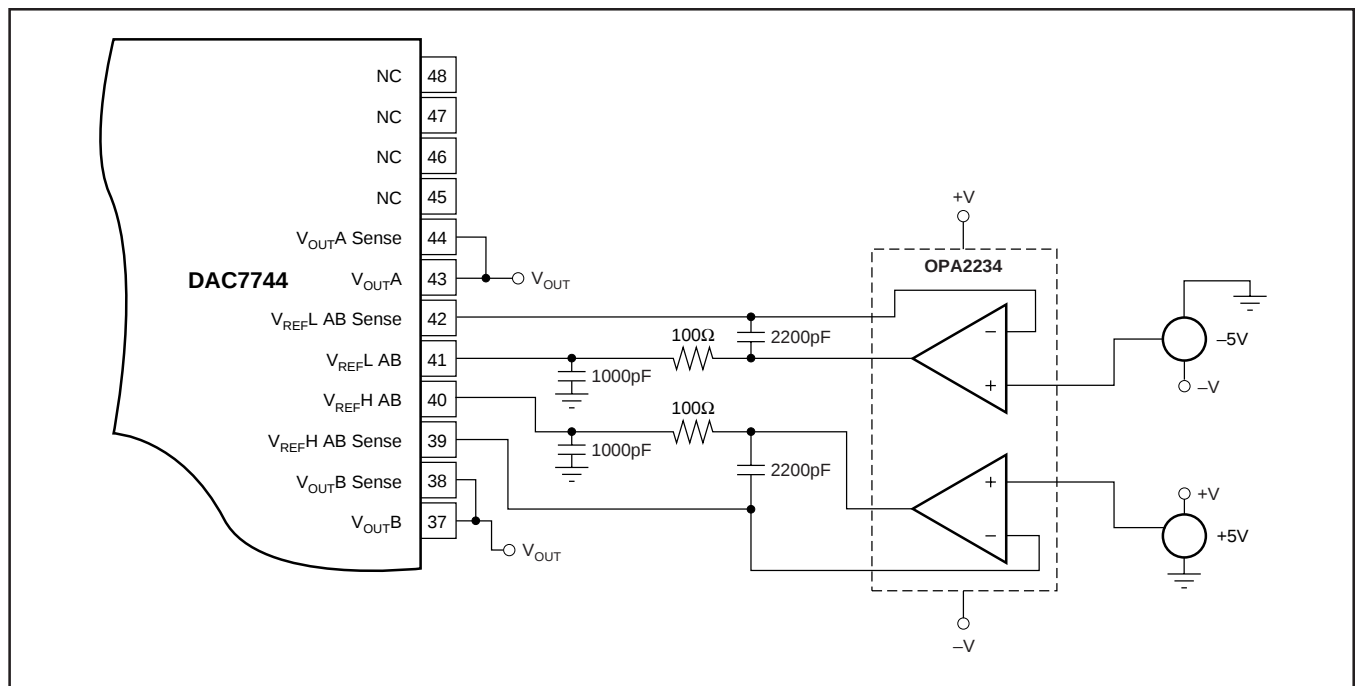


FIGURE 8. Dual-Supply Buffered Referenced with $V_{REFL} = -5V$ and $V_{REFH} = +5V$ (1/2 DAC7744).

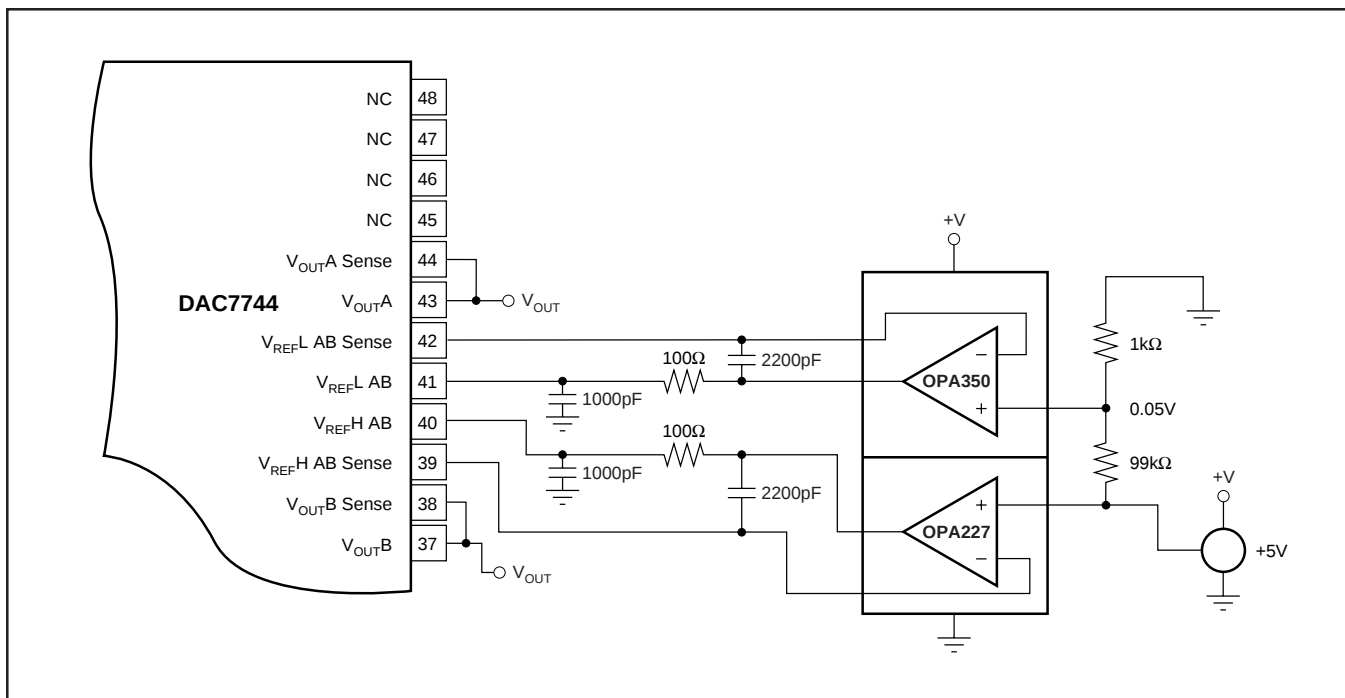


FIGURE 9. Single-Supply Buffered Reference with a Reference Low of 50mV and Reference High of +5V.

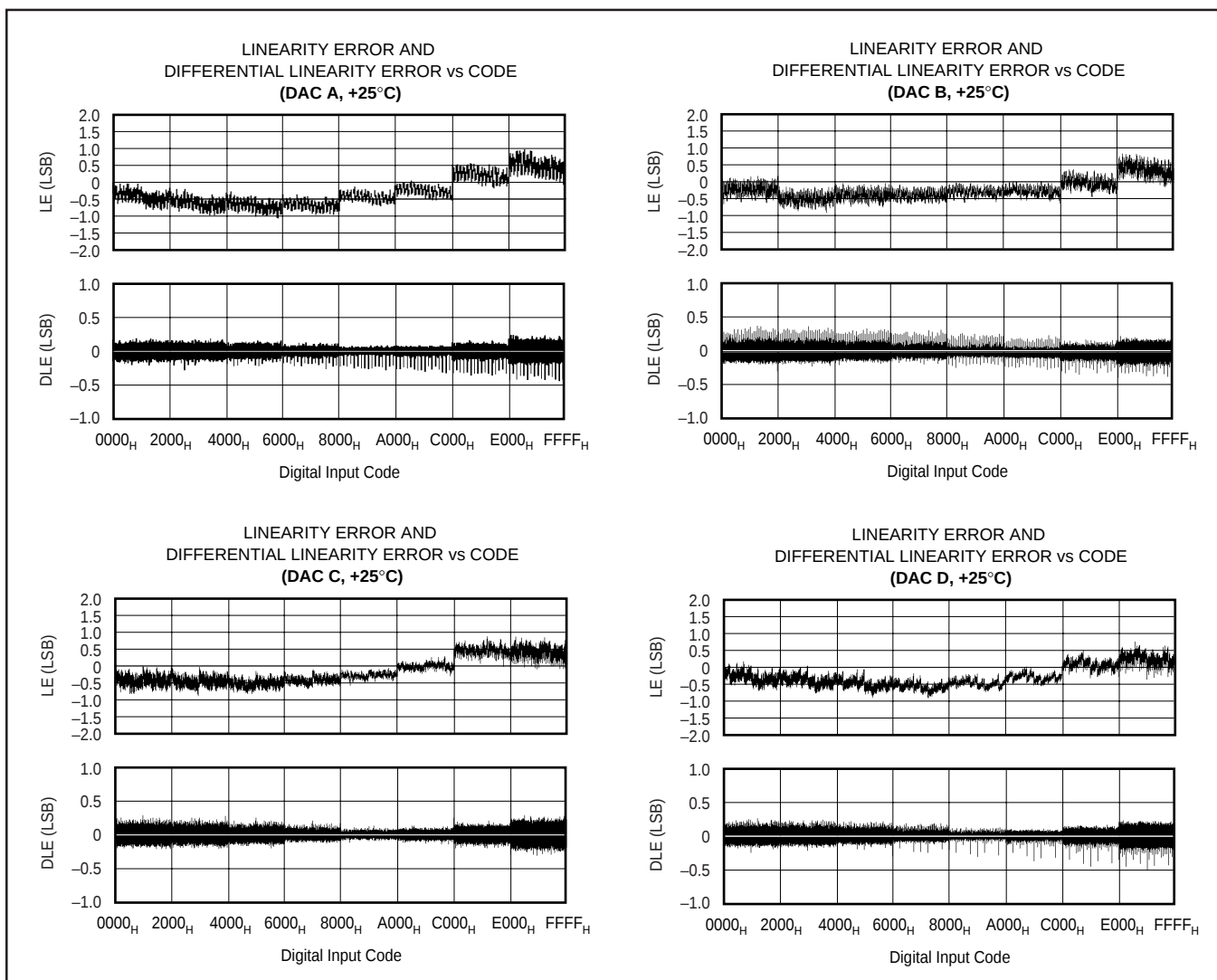


FIGURE 10. Integral Linearity and Differential Linearity Error Curves for Figure 9.

A1	A0	R/W	$\overline{CS}$	RST	RSTSEL	LOADDACS	INPUT REGISTER	DAC REGISTER	MODE	DAC
L	L	L	L	X	X	X	Write	Hold	Write Input	A
L	H	L	L	X	X	X	Write	Hold	Write Input	B
H	L	L	L	X	X	X	Write	Hold	Write Input	C
H	H	L	L	X	X	X	Write	Hold	Write Input	D
L	L	H	L	X	X	X	Read	Hold	Read Input	A
L	H	H	L	X	X	X	Read	Hold	Read Input	B
H	L	H	L	X	X	X	Read	Hold	Read Input	C
H	H	H	L	X	X	X	Read	Hold	Read Input	D
X	X	X	H	X	X	↑	Hold	Write	Update	All
X	X	X	H	X	X	H	Hold	Hold	Hold	All
X	X	X	X	↑	L	X		Reset to Zero	Reset to Zero	All
X	X	X	X	↑	H	X		Reset to Midscale	Reset to Midscale	All

TABLE I. DAC7744 Logic Truth Table.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7744. Note that each DAC register is edge triggered and not level triggered. When the LOADDACS signal is transitioned to HIGH, the digital word currently in the DAC register is latched. The first set of registers (the input registers) are triggered via the A0, A1, R/W, and $\overline{CS}$ inputs. Only one of these registers is transparent at any given time.

The double-buffered architecture is designed mainly so that each DAC input register can be written to at any time and then all DAC voltages updated simultaneously by the rising edge of LOADDACS. It also allows a DAC input register to be written to at any point then the DAC output voltages can be synchronously changed via a trigger signal connected to LOADDACS.

DIGITAL TIMING

Figure 11 and Table II provide detailed timing for the digital interface of the DAC7744.

DIGITAL INPUT CODING

The DAC7744 input data is in Straight Binary format. The output voltage is given by Equation 1.

$$V_{OUT} = V_{REF}L + \frac{(V_{REF}H - V_{REF}L) \cdot N}{65,536} \quad (1)$$

where N is the digital input code. This equation does not include the effects of offset (zero scale) or gain (full scale) errors.

DIGITALLY-PROGRAMMABLE CURRENT SOURCE

The DAC7744 offers a unique set of features that allows a wide range of flexibility in designing applications circuits such as programmable current sources. The DAC7744 offers both a differential reference input as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows transistor to be placed within the loop to implement a digitally-programmable, uni-directional current source. The availability of a differential reference also allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left(\left(\frac{V_{REF}H - V_{REF}L}{R_{SENSE}} \right) \cdot \left(\frac{N}{65,536} \right) \right) + (V_{REF}L / R_{SENSE}) \quad (2)$$

Figure 12 shows a DAC7744 in a 4-to-20mA current output configuration. The output current can be determined by Equation 3:

$$I_{OUT} = \left(\left(\frac{5V - 1V}{250\Omega} \right) \cdot \left(\frac{N}{65,536} \right) \right) + \left(\frac{1V}{250\Omega} \right) \quad (3)$$

At full scale, the output current is 16mA plus the 4mA for the zero current. At zero scale, the output current is the offset current of 4mA (1V/250Ω).

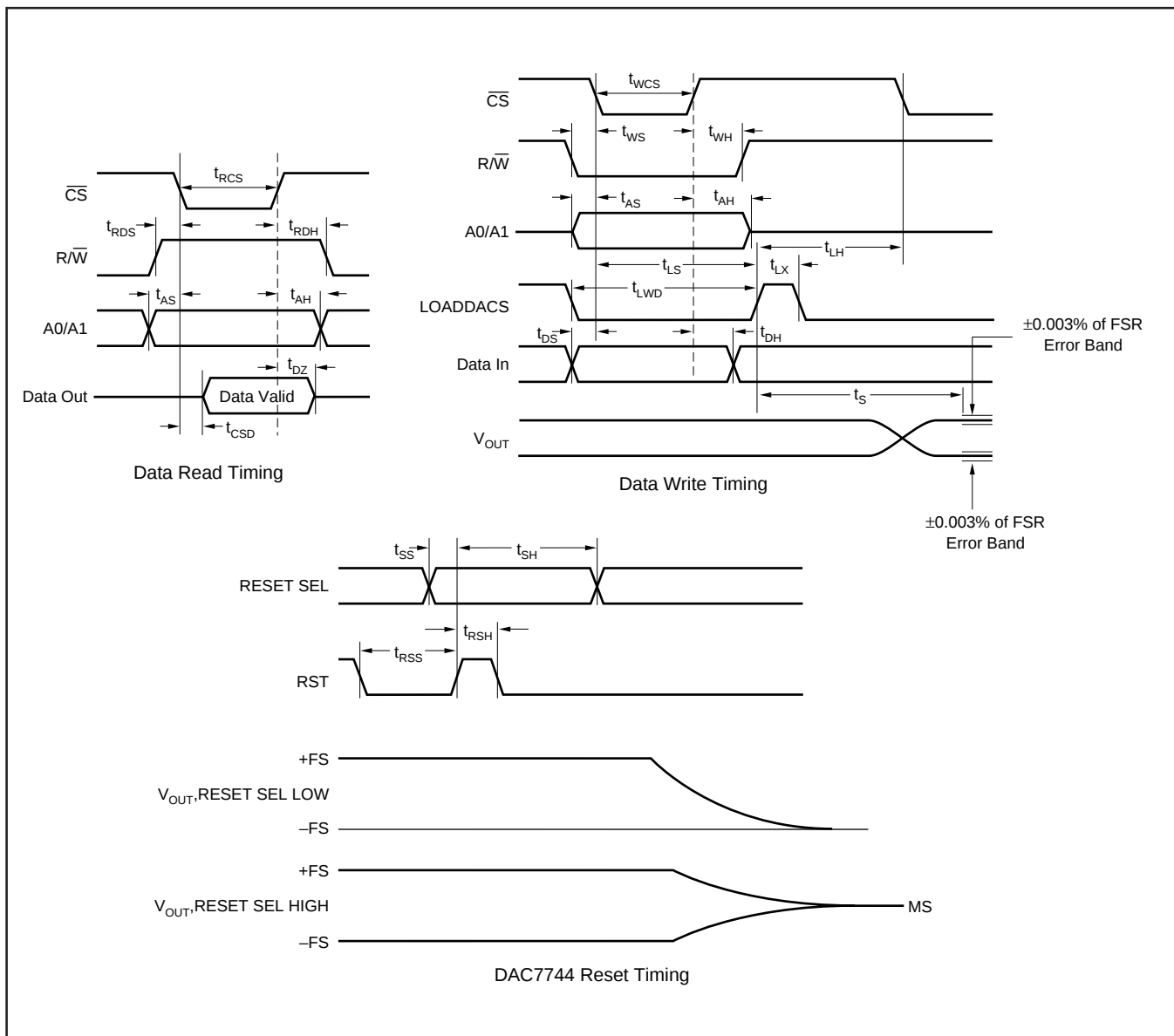


FIGURE 11. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RCS}	$\overline{CS}$ LOW for Read	100			ns
t_{RDS}	$R/\overline{W}$ HIGH to $\overline{CS}$ LOW	10			ns
t_{RDH}	$R/\overline{W}$ HIGH after $\overline{CS}$ HIGH	10			ns
t_{DZ}	$\overline{CS}$ HIGH to Data Bus in High Impedance	10			ns
t_{CSD}	$\overline{CS}$ LOW to Data Bus Valid		85	70	ns
t_{WCS}	$\overline{CS}$ LOW for Write	40		130	ns
t_{WS}	$R/\overline{W}$ LOW to $\overline{CS}$ LOW	0			ns
t_{WH}	$R/\overline{W}$ LOW after $\overline{CS}$ HIGH	10			ns
t_{AS}	Address Valid to $\overline{CS}$ LOW	0			ns
t_{AH}	Address Valid after $\overline{CS}$ HIGH	15			ns
t_{LS}	$\overline{CS}$ LOW to $LOADDACS$ HIGH	40			ns
t_{LH}	$\overline{CS}$ LOW after $LOADDACS$ HIGH	80			ns
t_{LX}	$LOADDACS$ HIGH	40			ns
t_{DS}	Data Valid to $\overline{CS}$ LOW	0			ns
t_{DH}	Data Valid after $\overline{CS}$ HIGH	15			ns
t_{LWD}	$LOADDACS$ LOW	40			ns
t_{SS}	RSTSEL Valid Before RESET HIGH	0			ns
t_{SH}	RSTSEL Valid After RESET HIGH	120			ns
t_{RSS}	RESET LOW Before RESET HIGH	10			ns
t_{RSH}	RESET LOW After RESET HIGH	10			ns
t_s	Settling Time			11	μ s

TABLE II. Timing Specifications ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$).



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
DAC7744E	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC7744E/1K	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC7744E/1KG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC7744EB	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC7744EB/1K	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC7744EB/1KG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC7744EBG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC7744EC	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC7744EC/1K	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC7744EC/1KG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC7744ECG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DAC7744EG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7744E/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
DAC7744EB/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
DAC7744EC/1K	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7744E/1K	SSOP	DL	48	1000	367.0	367.0	55.0
DAC7744EB/1K	SSOP	DL	48	1000	367.0	367.0	55.0
DAC7744EC/1K	SSOP	DL	48	1000	367.0	367.0	55.0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community e2e.ti.com



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.