2100 MHz to 2600 MHz Rx Mixer with Integrated Fractional-N PLL and VCO

ADRF6603

FEATURES

Rx mixer with integrated fractional-N PLL
RF input frequency range: 1100 MHz to 3200 MHz
Internal LO frequency range: 2100 MHz to 2600 MHz
Input P1dB: 14.8 dBm
Input IP3: 28.5 dBm
IIP3 optimization via external pin
SSB noise figure
- **IP3SET pin open: 14.3 dB**
- **IP3SET pin at 3.3 V: 15.6 dB**

Voltage conversion gain: 6.7 dB
Matched 200 Ω IF output impedance
IF 3 dB bandwidth: 500 MHz
Programmable via 3-wire SPI interface
40-lead, 6 mm × 6 mm LFCSP

APPLICATIONS

Cellular base stations

GENERAL DESCRIPTION

The ADRF6603 is a high dynamic range active mixer with integrated phase-locked loop (PLL) and voltage controlled oscillator (VCO). The PLL/synthesizer uses a fractional-N PLL to generate a f_{LO} input to the mixer. The reference input can be divided or multiplied and then applied to the PLL phase frequency detector (PFD).

The PLL can support input reference frequencies from 12 MHz to 160 MHz. The PFD output controls a charge pump whose output drives an off-chip loop filter.

The loop filter output is then applied to an integrated VCO. The VCO output at 2 × f_{LO} is applied to an LO divider, as well as to a programmable PLL divider. The programmable PLL divider is controlled by a sigma-delta (Σ-Δ) modulator (SDM). The modulus of the SDM can be programmed from 1 to 2047.

The active mixer converts the single-ended 50 Ω RF input to a 200 Ω differential IF output. The IF output can operate up to 500 MHz.

The ADRF6603 is fabricated using an advanced silicon-germanium BiCMOS process. It is available in a 40-lead, RoHS-compliant, 6 mm × 6 mm LFCSP with an exposed paddle. Performance is specified over the −40°C to +85°C temperature range.

Table 1.

Part No.	Internal LO Range	±3 dB RF_{IN} Balun Range	±1 dB RF_{IN} Balun Range
ADRF6601	750 MHz 1160 MHz	300 MHz 2500 MHz	450 MHz 1600 MHz
ADRF6602	1550 MHz 2150 MHz	1000 MHz 3100 MHz	1350 MHz 2750 MHz
ADRF6603	2100 MHz 2600 MHz	1100 MHz 3200 MHz	1450 MHz 2850 MHz
ADRF6604	2500 MHz 2900 MHz	1200 MHz 3600 MHz	1600 MHz 3200 MHz

FUNCTIONAL BLOCK DIAGRAM

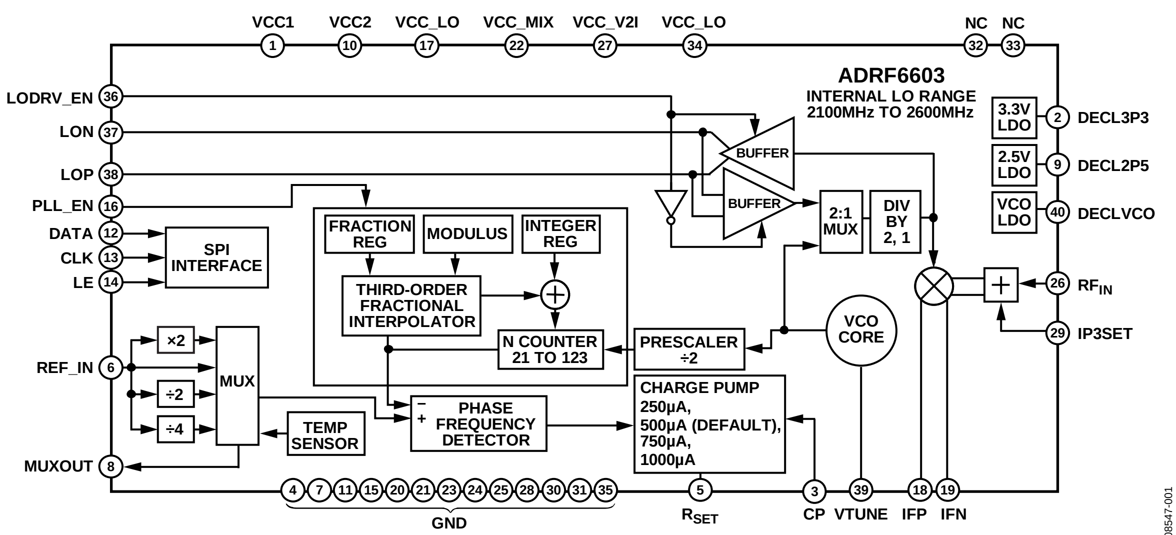

Figure 1.

Rev. A

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REVISION HISTORY

11/10—Rev. 0 to Rev. A

1/10—Revision 0: Initial Version

SPECIFICATIONS

RF SPECIFICATIONS

V_S = 5 V; ambient temperature (T_A) = 25°C; f_{REF} = 153.6 MHz; f_{PFD} = 38.4 MHz; high-side LO injection; f_{IF} = 140 MHz; IIP3 optimized using CDAC (0x1) and IP3SET (3.3 V), unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INTERNAL LO FREQUENCY RANGE		2100		2600	MHz
RF INPUT FREQUENCY RANGE	±3 dB RF input range	1100		3200	MHz
RF INPUT AT 2140 MHz					
Input Return Loss	Relative to 50 Ω (can be improved with external match)		<(−20)		dB
Input P1dB			14.9		dBm
Second-Order Intercept (IIP2)	−5 dBm each tone (10 MHz spacing between tones)		55.3		dBm
Third-Order Intercept (IIP3)	−5 dBm each tone (10 MHz spacing between tones)		29.3		dBm
Single-Side Band Noise Figure	IP3SET = 3.3 V		15.6		dB
	IP3SET = open		14.4		dB
LO-to-IF Leakage	At 1× LO frequency, 50 Ω termination at the RF port		−43		dBm
RF INPUT AT 2400 MHz					
Input Return Loss	Relative to 50 Ω (can be improved with external match)		−16		dB
Input P1dB			14.9		dBm
Second-Order Intercept (IIP2)	−5 dBm each tone (10 MHz spacing between tones)		55.1		dBm
Third-Order Intercept (IIP3)	−5 dBm each tone (10 MHz spacing between tones)		28.6		dBm
Single-Side Band Noise Figure	IP3SET = 3.3 V		15.8		dB
	IP3SET = open		14.2		dB
LO-to-IF Leakage	At 1× LO frequency, 50 Ω termination at the RF port		−43		dBm
RF INPUT AT 2650 MHz					
Input Return Loss	Relative to 50 Ω (can be improved with external match)		−11		dB
Input P1dB			14.7		dBm
Second-Order Intercept (IIP2)	−5 dBm each tone (10 MHz spacing between tones)		52.1		dBm
Third-Order Intercept (IIP3)	−5 dBm each tone (10 MHz spacing between tones)		28.1		dBm
Single-Side Band Noise Figure	IP3SET = 3.3 V		15.8		dB
	IP3SET = open		14.5		dB
LO-to-IF Leakage	At 1× LO frequency, 50 Ω termination at the RF port		−44		dBm
IF OUTPUT					
Voltage Conversion Gain	Differential 200 Ω load		6.7		dB
IF Bandwidth	Small signal 3 dB bandwidth		500		MHz
Output Common-Mode Voltage	External pull-up balun or inductors required		5		V
Gain Flatness	Over frequency range, any 5 MHz/50 MHz		0.2/1.0		dB
Gain Variation	Over full temperature range		1.2		dB
Output Swing	Differential 200 Ω load		2		V p-p
Differential Output Return Loss	Measured through 4:1 balun		−15		dB
LO INPUT/OUTPUT (LOP, LON)	Externally applied 1× LO input, internal PLL disabled				
Frequency Range		250		6000	MHz
Output Level (LO as Output)	1× LO into a 50 Ω load, LO output buffer enabled		−7		dBm
Input Level (LO as Input)		−6	0	+6	dBm
Input Impedance			50		Ω

SYNTHESIZER/PLL SPECIFICATIONS

V_S = 5 V; ambient temperature (T_A) = 25°C; f_{REF} = 153.6 MHz; f_{REF} power = 4 dBm; f_{PFD} = 38.4 MHz; high-side LO injection; f_{IF} = 140 MHz; IIP3 optimized using CDAC (0x1) and IP3SET (3.3 V), unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYNTHESIZER SPECIFICATIONS	Synthesizer specifications referenced to 1× LO				
Frequency Range	Internally generated LO	2100		2600	MHz
Figure of Merit[1]	P_{REF_IN} = 0 dBm		−222		dBc/Hz/Hz
Reference Spurs	f_{PFD} = 38.4 MHz				
	$f_{PFD}/4$		−107		dBc
	f_{PFD}		−82		dBc
	>f_{PFD}		−85		dBc
PHASE NOISE	f_{LO} = 2100 MHz to 2600 MHz, f_{PFD} = 38.4 MHz				
	1 kHz to 10 kHz offset		−88		dBc/Hz
	100 kHz offset		−99.5		dBc/Hz
	500 kHz offset		−120		dBc/Hz
	1 MHz offset		−128		dBc/Hz
	5 MHz offset		−142		dBc/Hz
	10 MHz offset		−148		dBc/Hz
	20 MHz offset		−150		dBc/Hz
Integrated Phase Noise	1 kHz to 40 MHz integration bandwidth		0.42		°rms
PFD Frequency		20		40	MHz
REFERENCE CHARACTERISTICS	REF_IN, MUXOUT pins				
REF_IN Input Frequency		12		160	MHz
REF_IN Input Capacitance			4		pF
MUXOUT Output Level	V_{OL} (lock detect output selected)			0.25	V
	V_{OH} (lock detect output selected)	2.7			V
MUXOUT Duty Cycle			50		%
CHARGE PUMP					
Pump Current	Programmable to 250 µA, 500 µA, 750 µA, 1 mA		500		µA
Output Compliance Range		1		2.8	V

[1] The figure of merit (FOM) is computed as phase noise (dBc/Hz) – 10Log10(f_{PFD}) – 20Log10(f_{LO}/f_{PFD}). The FOM was measured across the full LO range, with f_{REF} = 80 MHz, and f_{REF} power = 10 dBm (500 V/µs slew rate) with a 40 MHz f_{PFD}. The FOM was computed at 50 kHz offset.

LOGIC INPUT AND POWER SPECIFICATIONS

V_S = 5 V; ambient temperature (T_A) = 25°C; f_{REF} = 153.6 MHz; f_{PFD} = 38.4 MHz; high-side LO injection; f_{IF} = 140 MHz; IIP3 optimized using CDAC (0x1) and IP3SET (3.3 V), unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS	CLK, DATA, LE				
Input High Voltage, V_{INH}		1.4		3.3	V
Input Low Voltage, V_{INL}		0		0.7	V
Input Current, I_{INH}/I_{INL}			0.1		µA
Input Capacitance, C_{IN}			5		pF
POWER SUPPLIES	VCC1, VCC2, VCC_LO, VCC_MIX, and VCC_V2I pins				
Voltage Range		4.75	5	5.25	V
Supply Current	PLL only		97		mA
	External LO mode (internal PLL disabled, LO output buffer off, IP3SET pin = 3.3 V)		164		mA
	Internal LO mode (internal PLL enabled, IP3SET pin = 3.3 V, LO output buffer on)		274		mA
	Internal LO mode (internal PLL enabled, IP3SET pin = 3.3 V, LO output buffer off)		261		mA
	Power-down mode		30		mA

TIMING CHARACTERISTICS

VCC2 = 5 V ± 5%.

Table 5.

Parameter	Limit	Unit	Description
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA-to-CLK setup time
t_3	10	ns min	DATA-to-CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK-to-LE setup time
t_7	20	ns min	LE pulse width

Timing Diagram

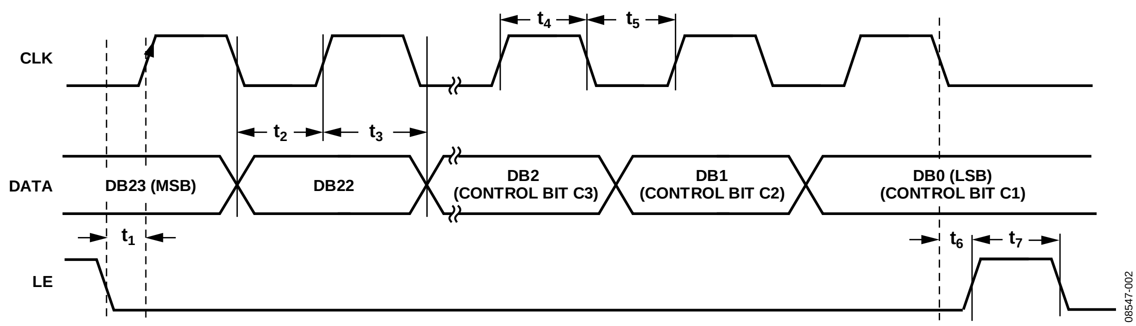


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

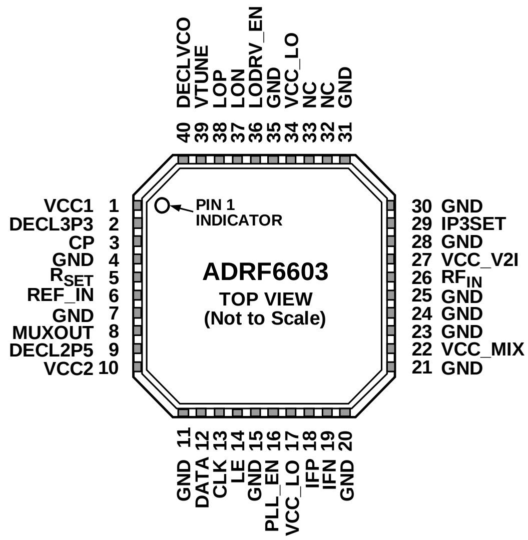
Parameter	Rating
Supply Voltage, VCC1, VCC2, VCC_LO, VCC_MIX, VCC_V2I	−0.5 V to +5.5 V
Digital I/O, CLK, DATA, LE, LODRV_EN, PLL_EN	−0.3 V to +3.6 V
VTUNE	0 V to 3.3 V
IFP, IFN	−0.3 V to VCC_V2I + 0.3 V
RF_{IN}	16 dBm
LOP, LON, REF_IN	13 dBm
$θ_{JA}$ (Exposed Paddle Soldered Down)	35°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PADDLE SHOULD BE SOLDERED TO A LOW IMPEDANCE GROUND PLANE.

08547-003

Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC1	Power Supply for the 3.3 V LDO. Power supply voltage range is 4.75 V to 5.25 V. Each power supply pin should be decoupled with a 100 pF capacitor and a 0.1 µF capacitor located close to the pin.
2	DECL3P3	Decoupling Node for 3.3 V LDO. Connect a 0.1 µF capacitor between this pin and ground.
3	CP	Charge Pump Output Pin. Connect to VTUNE through the loop filter.
4, 7, 11, 15, 20, 21, 23, 24, 25, 28, 30, 31, 35	GND	Ground. Connect these pins to a low impedance ground plane.
5	R_{SET}	Charge Pump Current. The nominal charge pump current can be set to 250 µA, 500 µA, 750 µA, or 1 mA using Bit DB11 and Bit DB10 in Register 4 and by setting Bit DB18 in Register 4 to 0 (internal reference current). In this mode, no external R_{SET} is required. If Bit DB18 is set to 1, the four nominal charge pump currents ($I_{NOMINAL}$) can be externally adjusted according to the following equation: $R_{SET} = \left(\frac{217.4 \times I_{CP}}{I_{NOMINAL}}\right) - 37.8\,\Omega$
6	REF_IN	Reference Input. Nominal input level is 1 V p-p. Input range is 12 MHz to 160 MHz. This pin is internally dc-biased and should be ac-coupled.
8	MUXOUT	Multiplexer Output. This output can be programmed to provide the reference output signal or the lock detect signal. The output is selected by programming the appropriate register.
9	DECL2P5	Decoupling Node for 2.5 V LDO. Connect a 0.1 µF capacitor between this pin and ground.
10	VCC2	Power Supply for the 2.5 V LDO. Power supply voltage range is 4.75 V to 5.25 V. Each power supply pin should be decoupled with a 100 pF capacitor and a 0.1 µF capacitor located close to the pin.
12	DATA	Serial Data Input. The serial data input is loaded MSB first; the three LSBs are the control bits.
13	CLK	Serial Clock Input. The serial clock input is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. Maximum clock frequency is 20 MHz.
14	LE	Load Enable. When the LE input pin goes high, the data stored in the shift registers is loaded into one of the eight registers. The relevant latch is selected by the three control bits of the 24-bit word.
16	PLL_EN	PLL Enable. Switch between internal PLL and external LO input. When this pin is logic high, the mixer LO is automatically switched to the internal PLL and the internal PLL is powered up. When this pin is logic low, the internal PLL is powered down and the external LO input is routed to the mixer LO inputs. The SPI can also be used to switch modes.

Pin No.	Mnemonic	Description
17, 34	VCC_LO	Power Supply. Power supply voltage range is 4.75 V to 5.25 V. Each power supply pin should be decoupled with a 100 pF capacitor and a 0.1 μF capacitor located close to the pin.
18, 19	IFP, IFN	Mixer IF Outputs. These outputs should be pulled to VCC with RF chokes.
22	VCC_MIX	Power Supply. Power supply voltage range is 4.75 V to 5.25 V. Each power supply pin should be decoupled with a 100 pF capacitor and a 0.1 μF capacitor located close to the pin.
26	RF_{IN}	RF Input (Single-Ended, 50 Ω).
27	VCC_V2I	Power Supply. Power supply voltage range is 4.75 V to 5.25 V. Each power supply pin should be decoupled with a 100 pF capacitor and a 0.1 μF capacitor located close to the pin.
29	IP3SET	Connect a resistor from this pin to a 5 V supply to adjust IIP3. Normally leave open.
32, 33	NC	No Connection.
36	LODRV_EN	LO Driver Enable. Together with Pin 16 (PLL_EN), this digital input pin determines whether the LOP and LON pins operate as inputs or outputs. LOP and LON become inputs if the PLL_EN pin is low or if the PLL_EN pin is set high with the PLEN bit (DB6 in Register 5) set to 0. LOP and LON become outputs if either the LODRV_EN pin or the LDRV bit (DB3 in Register 5) is set to 1 while the PLL_EN pin is set high. External LO drive frequency must be 1× LO. This pin has an internal 100 kΩ pull down resistor.
37, 38	LON, LOP	Local Oscillator Input/Output. The internally generated 1× LO is available on these pins. When internal LO generation is disabled, an external 1× LO can be applied to these pins.
39	VTUNE	VCO Control Voltage Input. This pin is driven by the output of the loop filter. Nominal input voltage range on this pin is 1.5 V to 2.5 V.
40	DECLVCO	Decoupling Node for VCO LDO. Connect a 100 pF capacitor and a 10 μF capacitor between this pin and ground.
	EPAD	Exposed Paddle. The exposed paddle should be soldered to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

RF FREQUENCY SWEEP

CDAC = 0x1, internally generated high-side LO, RF_{IN} = −5 dBm, f_{IF} = 140 MHz, unless otherwise noted.

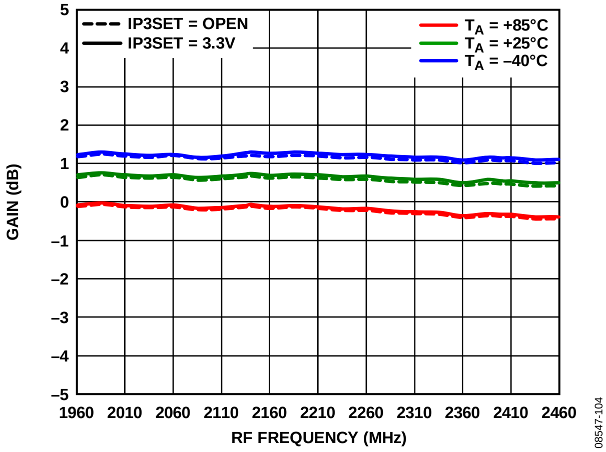


Figure 4. Gain vs. RF Frequency

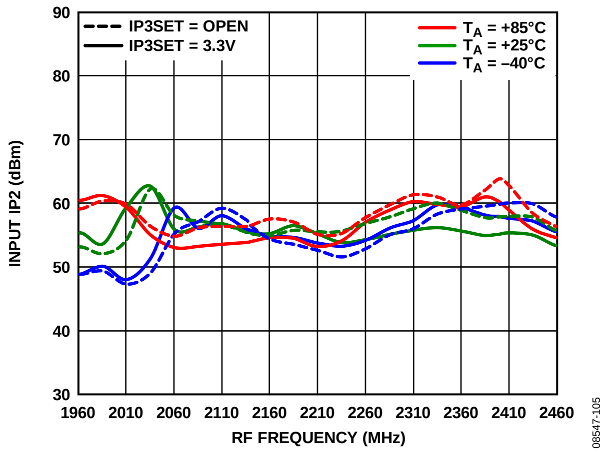


Figure 5. Input IP2 vs. RF Frequency

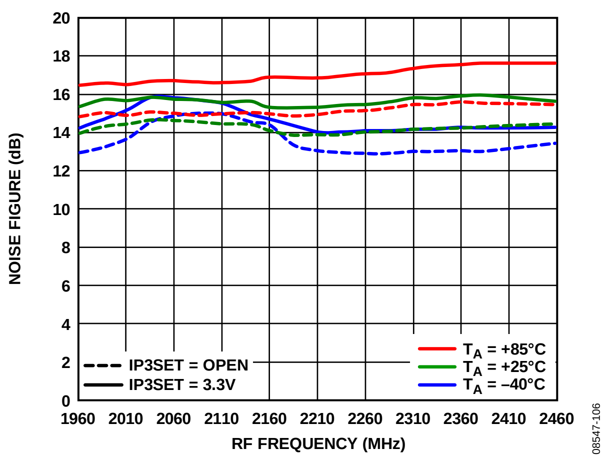


Figure 6. Noise Figure vs. RF Frequency

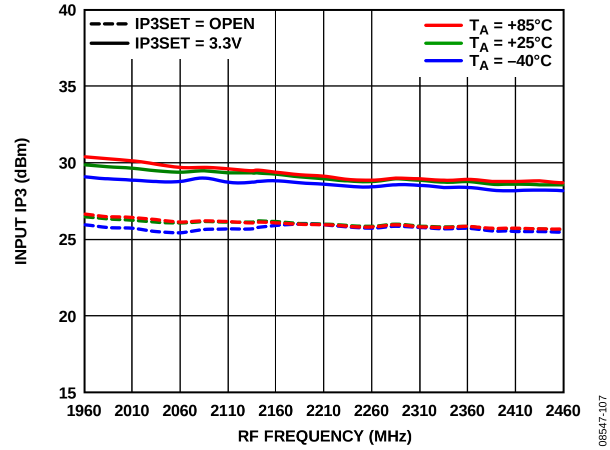


Figure 7. Input IP3 vs. RF Frequency

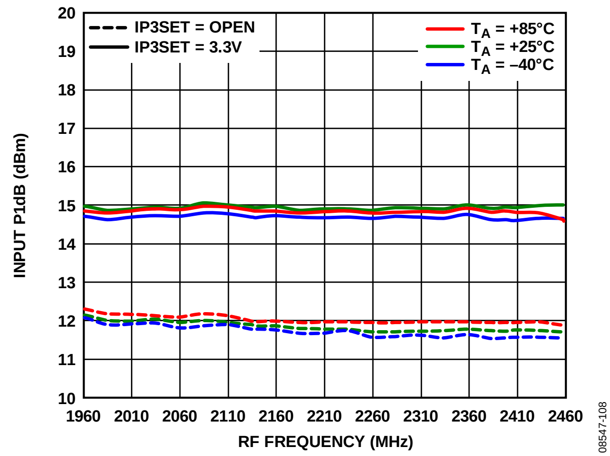


Figure 8. Input P1dB vs. RF Frequency

IF FREQUENCY SWEEP

CDAC = 0x1, internally generated swept low-side LO, f_{RF} = 1960 MHz, RF_{IN} = −5 dBm, unless otherwise noted.

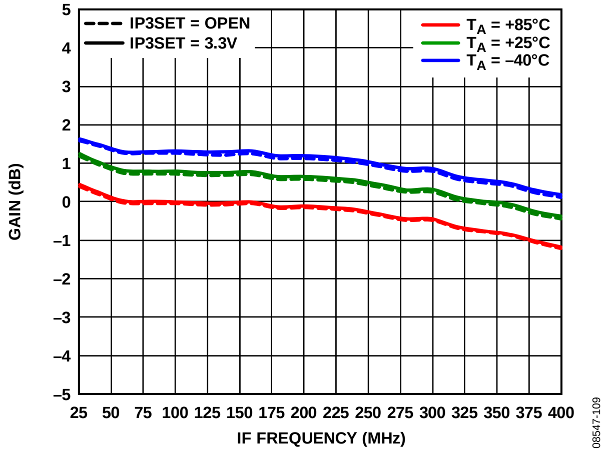


Figure 9. Gain vs. IF Frequency

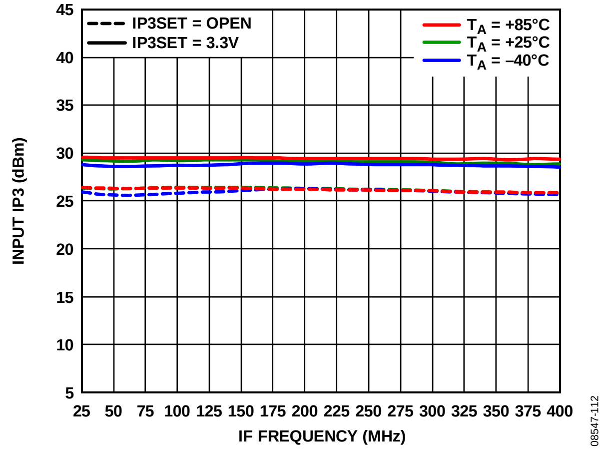


Figure 12. Input IP3 vs. IF Frequency, RF_{IN} = −5 dBm

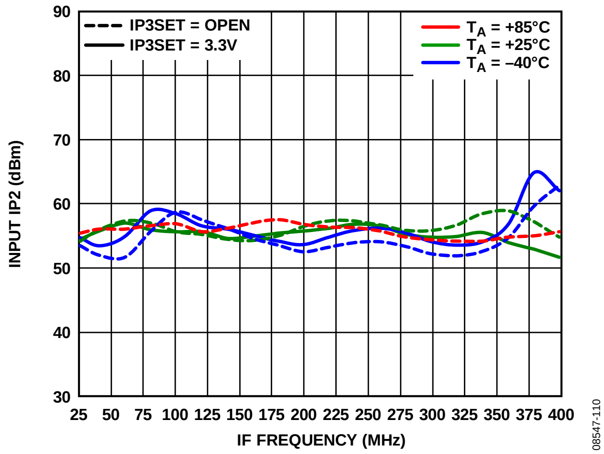


Figure 10. Input IP2 vs. IF Frequency, RF_{IN} = −5 dBm

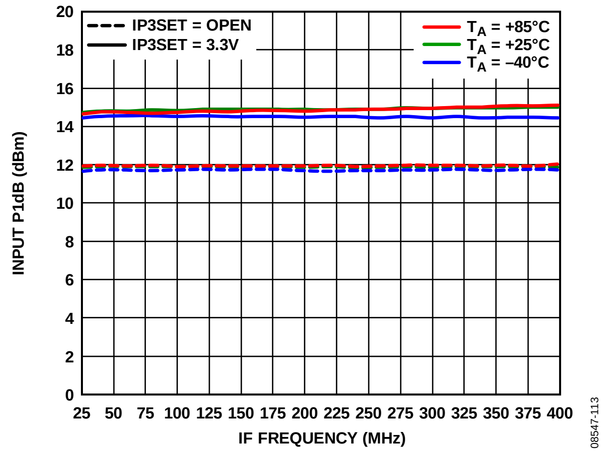


Figure 13. Input P1dB vs. IF Frequency

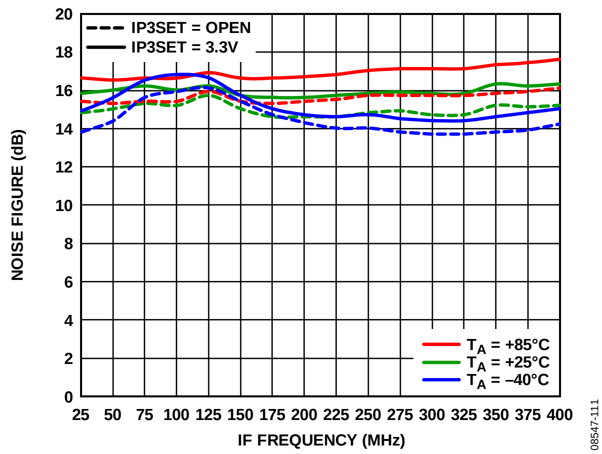


Figure 11. Noise Figure vs. IF Frequency

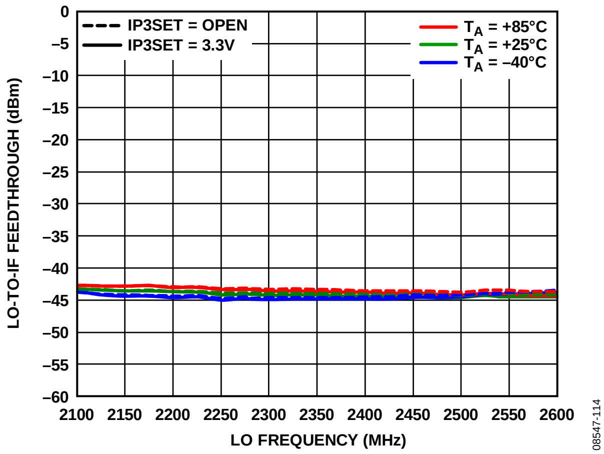


Figure 14. LO-to-IF Feedthrough vs. LO Frequency, LO Output Turned Off, CDAC = 0x0

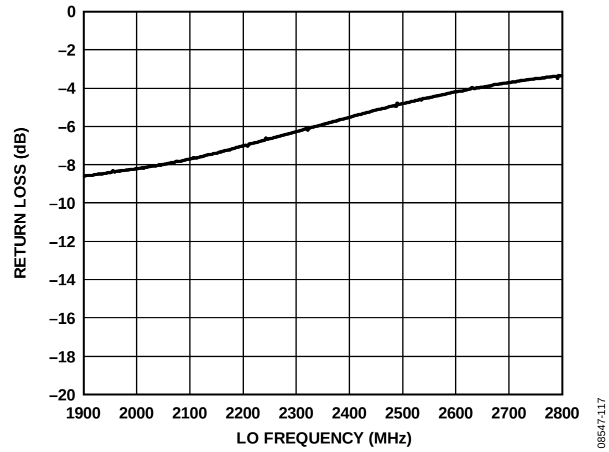


Figure 17. LO Input Return Loss vs. LO Frequency (Including TC1-1-13 Balun)

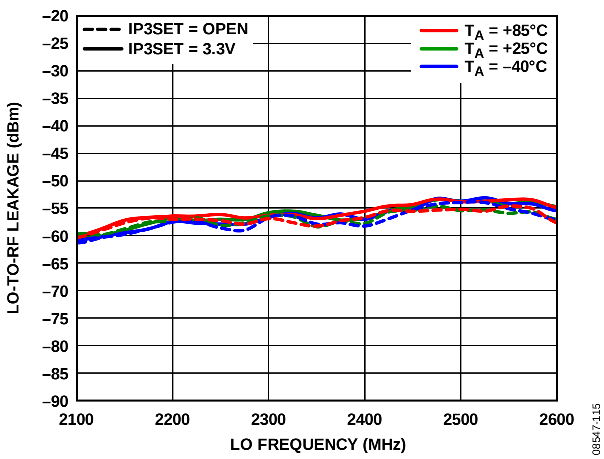


Figure 15. LO-to-RF Leakage vs. LO Frequency, LO Output Turned Off

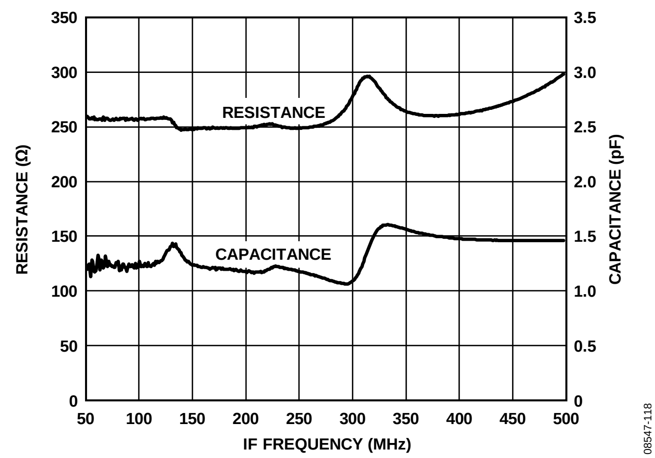


Figure 18. IF Differential Output Impedance (R Parallel C Equivalent)

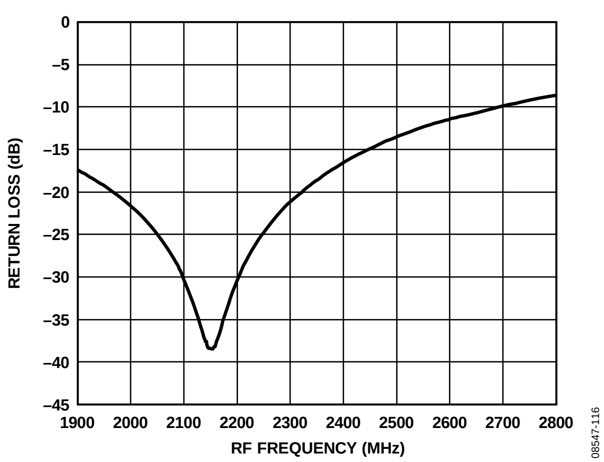


Figure 16. RF Input Return Loss vs. RF Frequency

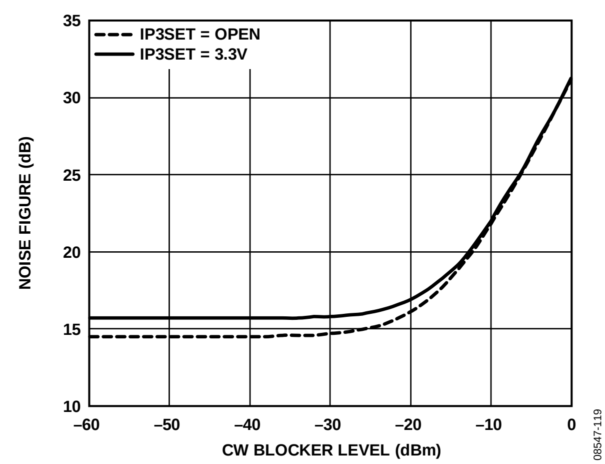


Figure 19. SSB Noise Figure vs. 5 MHz Offset Blocker Level, LO Frequency = 2105 MHz, RF Frequency = 1965 MHz

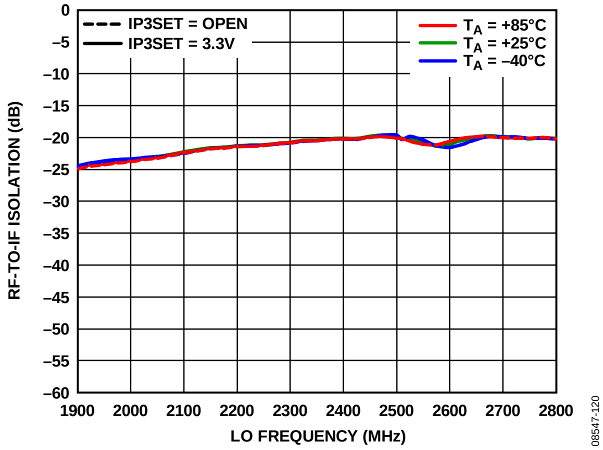


Figure 20. RF-to-IF Isolation vs. RF Frequency, High-Side LO, IF = 140 MHz, LO Output Turned Off

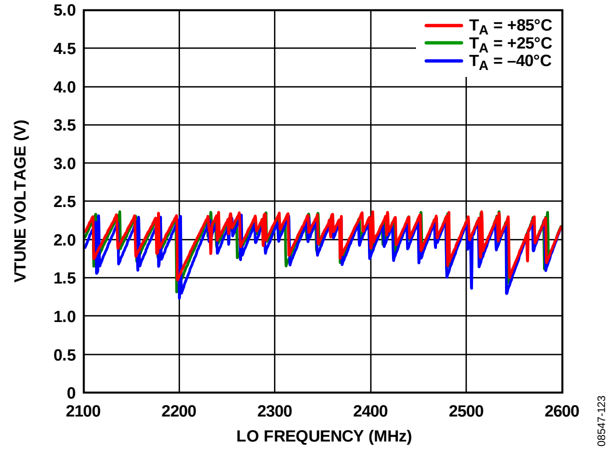


Figure 23. VTUNE vs. LO Frequency

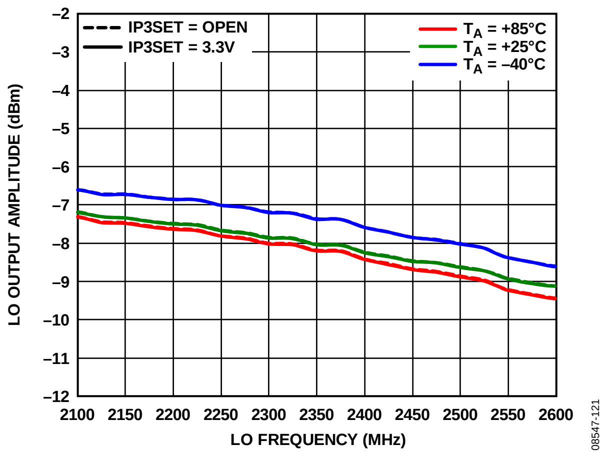


Figure 21. LO Output Amplitude vs. LO Frequency

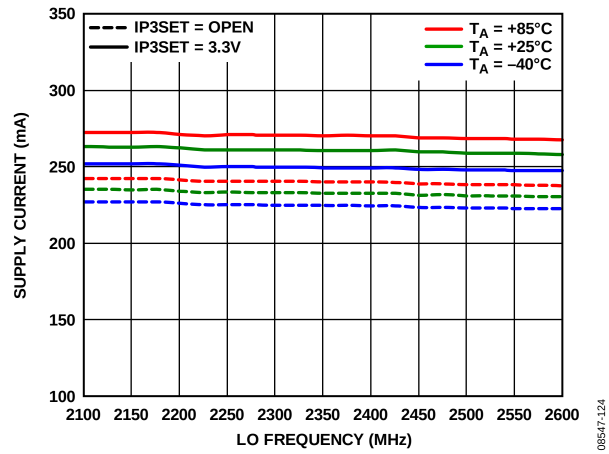


Figure 24. Supply Current vs. LO Frequency

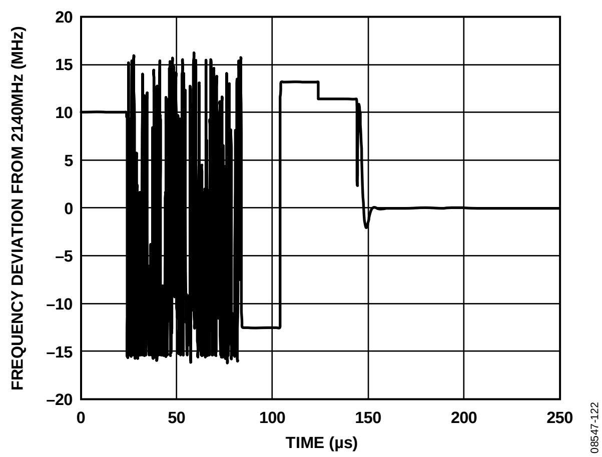


Figure 22. Frequency Deviation from 2140 MHz vs Time (Demonstrates LO Frequency Settling Time from 2150 MHz to 2140 MHz)

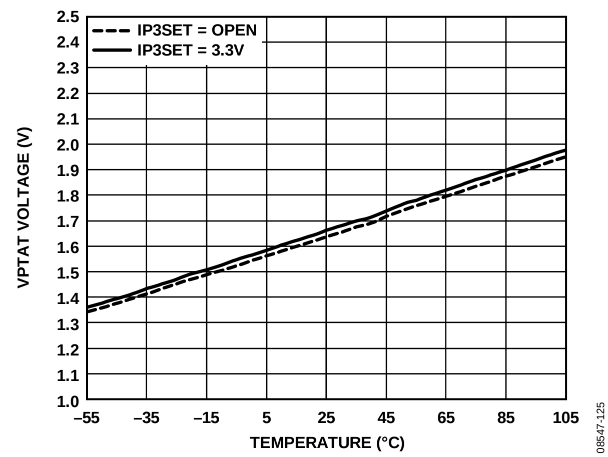


Figure 25. VPTAT Voltage vs. Temperature (IP3SET = Optimized, Open)

Complementary cumulative distribution function (CCDF), f_{RF} = 2140 MHz, f_{IF} = 140 MHz.

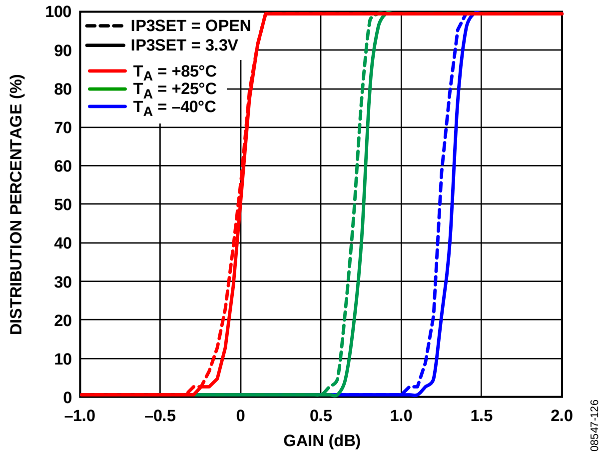


Figure 26. Gain

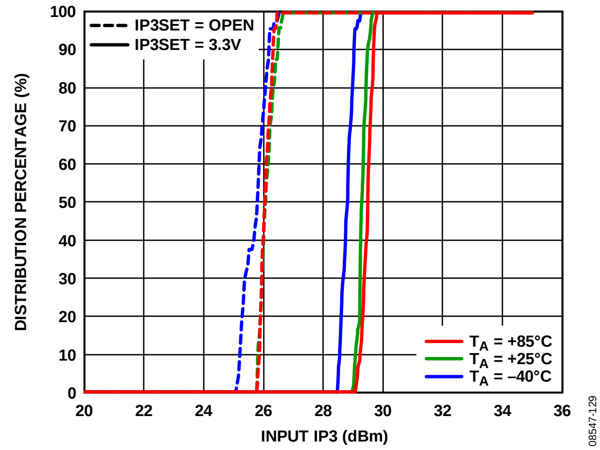


Figure 29. Input IP3

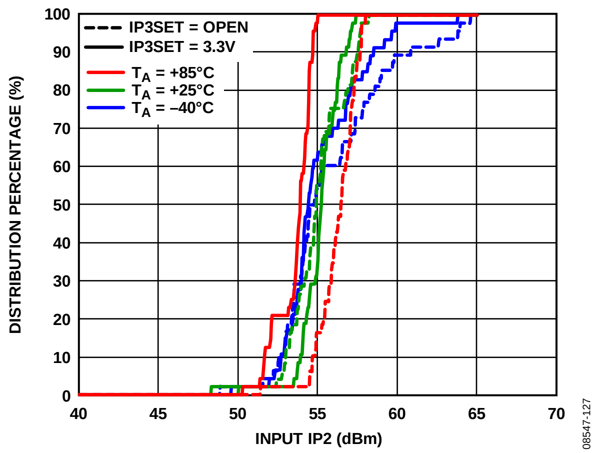


Figure 27. Input IP2

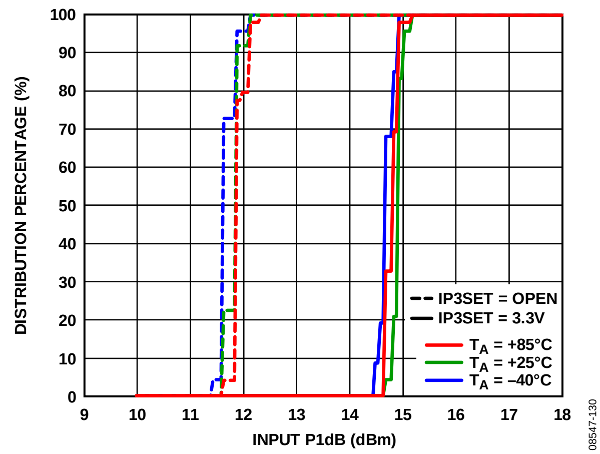


Figure 30. Input P1dB

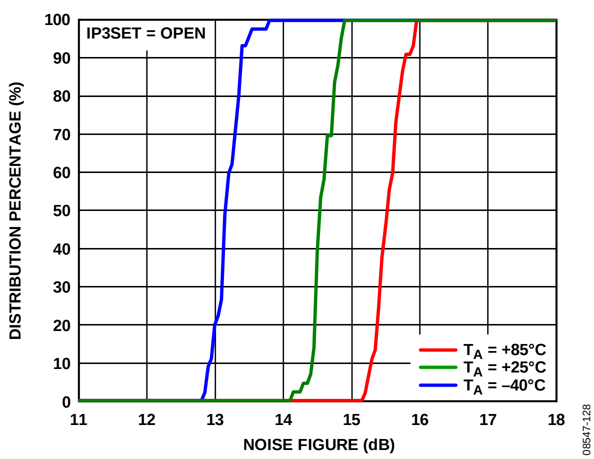


Figure 28. Noise Figure

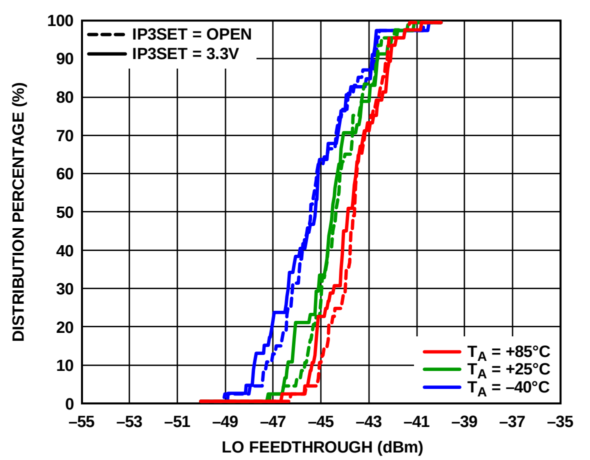


Figure 31. LO Feedthrough to IF, LO Output Turned Off

Measured at IF output, CDAC = 0x1, IP3SET = open, internally generated high-side LO, f_{REF} = 153.6 MHz, f_{PFD} = 38.4 MHz, RF_{IN} = −5 dBm, f_{IF} = 140 MHz, unless otherwise noted. Phase noise measurements made at LO output, unless otherwise noted.

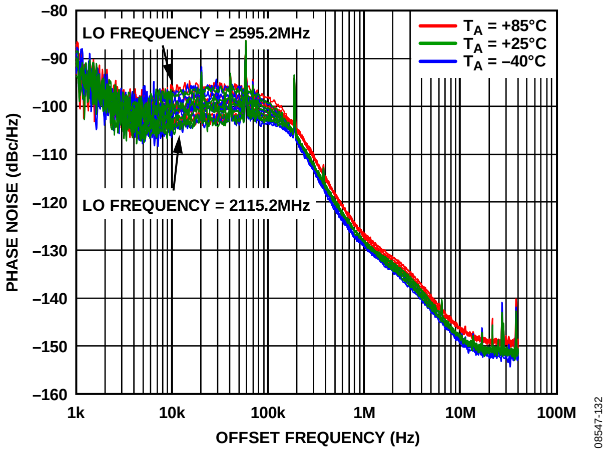


Figure 32. Phase Noise vs. Offset Frequency

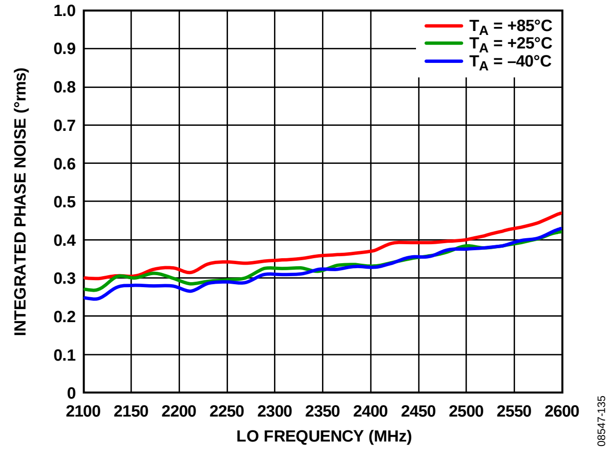


Figure 35. Integrated Phase Noise vs. LO Frequency

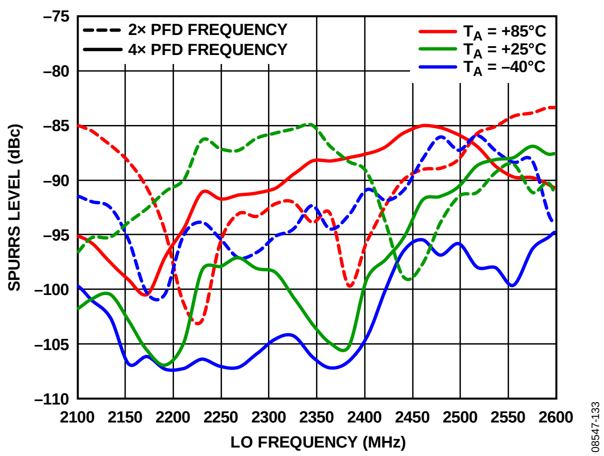


Figure 33. PLL Reference Spurs vs. LO Frequency (2× PFD and 4× PFD)

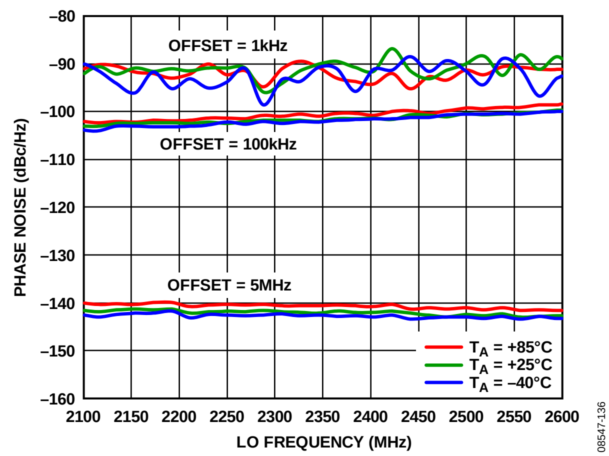


Figure 36. Phase Noise vs. LO Frequency (1 kHz, 100 kHz, and 5 MHz Steps)

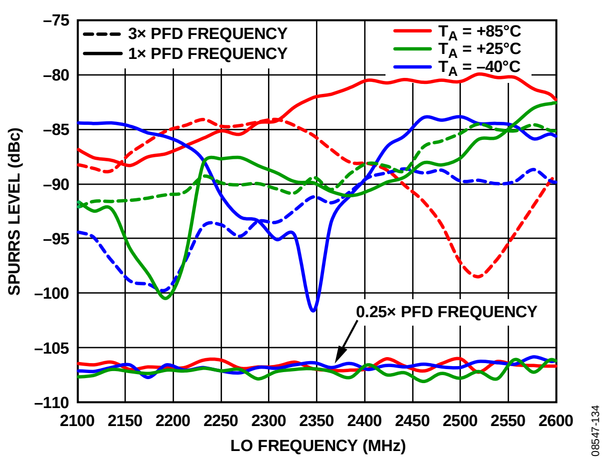


Figure 34. PLL Reference Spurs vs. LO Frequency (0.25× PFD, 1× PFD, and 3× PFD)

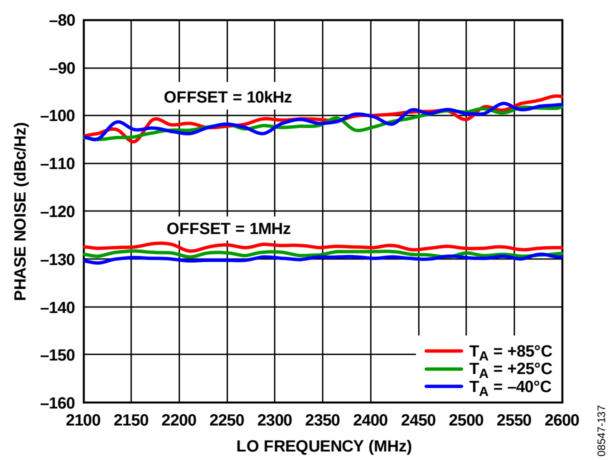


Figure 37. Phase Noise vs. LO Frequency (10 kHz, 1 MHz Steps)

SPURIOUS PERFORMANCE

$(N \times f_{RF}) - (M \times f_{LO})$ spur measurements were made using the standard evaluation board (see the Evaluation Board section). Mixer spurious products were measured in dB relative to the carrier (dBc) from the IF output power level. All spurious components greater than −125 dBc are shown.

LO = 2280 MHz, RF = 2140 MHz (horizontal axis is m, vertical axis is n), and RF_{IN} power = 0 dBm.

		M				
		0	1	2	3	4
N	0	−114.35	−45.19	−36.94		
	1	−20.79	0.0	−67.43	−52.11	
	2	−58.20	−61.95	−78.15	−85.93	−93.10
	3		−71.79	−91.89	−67.46	−105.88
	4			−107.79	−110.27	−107.87
	5				−107.88	−112.41
	6					−107.71
	7					−108.62

LO = 2540 MHz, RF = 2400 MHz (horizontal axis is m, vertical axis is n), and RF_{IN} power = 0 dBm.

		M				
		0	1	2	3	4
N	0	−113.65	−47.04	−36.36		
	1	−18.91	0.0	−65.01	−56.24	
	2	−59.08	−60.49	−69.27	−89.85	−94.25
	3		−77.54	−89.56	−68.39	−109.30
	4			−108.79	−110.65	−111.94
	5				−108.85	−111.54
	6					−108.89
	7					

LO = 2650 MHz, RF = 2510 MHz (horizontal axis is m, vertical axis is n), and RF_{IN} power = 0 dBm.

		M				
		0	1	2	3	4
N	0	−111.38	−46.57	−36.03		
	1	−17.70	0.0	−65.70	−54.37	
	2	−58.49	−75.49	−72.27	−71.05	−95.32
	3		−81.35	−89.18	−68.23	−103.38
	4			−106.13	−106.74	−112.72
	5				−107.26	−105.45
	6					−110.74
	7					

REGISTER STRUCTURE

This section provides the register maps for the ADRF6603. The three LSBs determine the register that is programmed.

REGISTER 0—INTEGER DIVIDE CONTROL (DEFAULT: 0x0001C0)

RESERVED													DIVIDE MODE	INTEGER DIVIDE RATIO							CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	DM	ID6	ID5	ID4	ID3	ID2	ID1	ID0	C3(0)	C2(0)	C1(0)

DM	DIVIDE MODE
0	FRACTIONAL (DEFAULT)
1	INTEGER

ID6	ID5	ID4	ID3	ID2	ID1	ID0	INTEGER DIVIDE RATIO
0	0	1	0	1	0	1	21 (INTEGER MODE ONLY)
0	0	1	0	1	1	0	22 (INTEGER MODE ONLY)
0	0	1	0	1	1	1	23 (INTEGER MODE ONLY)
0	0	1	1	0	0	0	24
...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...
0	1	1	1	0	0	0	56 (DEFAULT)
...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...
1	1	1	0	1	1	1	119
1	1	1	1	0	0	0	120 (INTEGER MODE ONLY)
1	1	1	1	0	0	1	121 (INTEGER MODE ONLY)
1	1	1	1	0	1	0	122 (INTEGER MODE ONLY)
1	1	1	1	0	1	1	123 (INTEGER MODE ONLY)

08547-004

Figure 38. Register 0—Integer Divide Control Register Map

REGISTER 1—MODULUS DIVIDE CONTROL (DEFAULT: 0x003001)

RESERVED										MODULUS VALUE											CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	C3(0)	C2(0)	C1(1)

MD10	MD9	MD8	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	MODULUS VALUE
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	1	0	2
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
1	1	0	0	0	0	0	0	0	0	0	1536 (DEFAULT)
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	1	1	1	1	1	2047

08547-005

Figure 39. Register 1—Modulus Divide Control Register Map

REGISTER 2—FRACTIONAL DIVIDE CONTROL (DEFAULT: 0x001802)

RESERVED										FRACTIONAL VALUE											CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	C3(0)	C2(1)	C1(0)

FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	FRACTIONAL VALUE
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
0	1	1	0	0	0	0	0	0	0	0	768 (DEFAULT)
...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...
FRACTIONAL VALUE MUST BE LESS THAN MODULUS											<MDR

08547-006

Figure 40. Register 2—Fractional Divide Control Register Map

REGISTER 3—Σ-Δ MODULATOR DITHER CONTROL (DEFAULT: 0x10000B)

	DITHER MAGNITUDE		DITHER ENABLE	DITHER RESTART VALUE																	CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	DITH1	DITH0	DEN	DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	C3(0)	C2(1)	C1(1)

DITH1	DITH0	DITHER MAGNITUDE
0	0	15 (DEFAULT)
0	1	7
1	0	3
1	1	1 (RECOMMENDED)

DEN	DITHER ENABLE
0	DISABLE
1	ENABLE (DEFAULT, RECOMMENDED)

DV16	DV15	DV14	DV13	DV12	DV11	DV10	DV9	DV8	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0	DITHER RESTART VALUE
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0x00001 (DEFAULT)
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0x1FFFF

08547-007

Figure 41. Register 3—Σ-Δ Modulator Dither Control Register Map

REGISTER 4—PLL CHARGE PUMP, PFD, AND REFERENCE PATH CONTROL (DEFAULT: 0x0AA7E4)

REF OUPUT MUX SELECT			INPUT REF PATH		CP CURRENT REF SOURCE	PFD POL	PFD PHASE OFFSET MULTIPLIER					CP CURRENT		CP SRC	CP CONTROL		PFD EDGE		PFD ANTI BACKLASH DELAY		CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
RMS2	RMS1	RMS0	RS1	RS0	CPM	CPBD	CPB4	CPB3	CPB2	CPB1	CPB0	CPP1	CPP0	CPS	CPC1	CPC0	PE1	PE0	PAB1	PAB0	C3(1)	C2(0)	C1(0)

PAB0	PAB1	PFD ANTI BACKLASH DELAY
0	0	0ns (DEFAULT)
0	1	0.5ns
1	0	0.75ns
1	1	0.9ns

PE0	REFERENCE PATH EDGE SENSITIVITY
0	FALLING EDGE
1	RISING EDGE (DEFAULT)

PE1	DIVIDER PATH EDGE SENSITIVITY
0	FALLING EDGE
1	RISING EDGE (DEFAULT)

CPC1	CPC0	CHARGE PUMP CONTROL
0	0	BOTH ON
0	1	PUMP DOWN
1	0	PUMP UP
1	1	TRISTATE (DEFAULT)

CPS	CHARGE PUMP CONTROL SOURCE
0	CONTROL BASED ON STATE OF DB7/DB8 (CP CONTROL)
1	CONTROL FROM PFD (DEFAULT)

CPP1	CPP0	CHARGE PUMP CURRENT
0	0	250µA
0	1	500µA (DEFAULT)
1	0	750µA
1	1	1000µA

CPB4	CPB3	CPB2	CPB1	CPB0	PFD PHASE OFFSET MULTIPLIER
0	0	0	0	0	$0 \times 22.5°/I_{CPMULT}$
0	0	0	0	1	$1 \times 22.5°/I_{CPMULT}$
0	0	1	1	0	$6 \times 22.5°/I_{CPMULT}$ (RECOMMENDED)
0	1	0	1	0	$10 \times 22.5°/I_{CPMULT}$ (DEFAULT)
1	0	0	0	0	$16 \times 22.5°/I_{CPMULT}$
1	1	1	1	1	$31 \times 22.5°/I_{CPMULT}$

CPBD	PFD PHASE OFFSET POLARITY
0	NEGATIVE
1	POSITIVE (DEFAULT)

CPM	CHARGE PUMP CURRENT REFERENCE SOURCE
0	INTERNAL (DEFAULT)
1	EXTERNAL

RS0	RS1	INPUT REFERENCE PATH SOURCE
0	0	2× REFIN
0	1	REFIN (DEFAULT)
1	0	0.5× REFIN
1	1	0.25× REFIN

RMS2	RMS1	RMS0	REF OUTPUT MUX SELECT
0	0	0	LOCK DETECT (DEFAULT)
0	0	1	VPTAT
0	1	0	REFIN (BUFFERED)
0	1	1	0.5× REFIN (BUFFERED)
1	0	0	2× REFIN (BUFFERED)
1	0	1	TRISTATE
1	1	0	RESERVED
1	1	1	RESERVED

08547-008

Figure 42. Register 4—PLL Charge Pump, PFD, and Reference Path Control Register Map

REGISTER 5—PLL ENABLE AND LO PATH CONTROL (DEFAULT: 0x0000E5)

RESERVED												CAP DAC				RES	PLL EN	LO DIV1	LO EXT	LO DRV	CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	CD3	CD2	CD1	CD0	LDV2	PLEN	LDV1	LXL	LDRV	C3(1)	C2(0)	C1(1)

CD3	CD2	CD1	CD0	CAPACITOR DAC CONTROL FOR IIP3 OPTIMIZATION
0	0	0	0	MIN
...	...	...	...	...
1	1	1	1	MAX

LDRV	LO OUTPUT DRIVER ENABLE
0	DRIVER OFF (DEFAULT)
1	DRIVER ON

LXL	EXTERNAL LO DRIVE ENABLE (PIN 37, PIN 38)
0	INTERNAL LO OUTPUT (DEFAULT)
1	EXTERNAL LO INPUT

LDV1	DIVIDE-BY-2 IN LO CHAIN ENABLE
0	DIVIDE BY 1
1	DIVIDE BY 2 (DEFAULT)

PLEN	PLL ENABLE
0	DISABLE
1	ENABLE (DEFAULT)

08547-009

Figure 43. Register 5—PLL Enable and LO Path Control Register Map

REGISTER 6—VCO CONTROL AND VCO ENABLE (DEFAULT: 0x1E2106)

RESERVED			CHARGE PUMP ENABLE	3.3V LDO ENABLE	VCO LDO ENABLE	VCO ENABLE	VCO SWITCH	VCO AMPLITUDE						VCO BW SW CTRL	VCO BAND SELECT FROM SPI						CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	CPEN	L3EN	LVEN	VCO EN	VCO SW	VC5	VC4	VC3	VC2	VC1	VC0	VBSRC	VBS5	VBS4	VBS3	VBS2	VBS1	VBS0	C3(1)	C2(1)	C1(0)

CPEN	CHARGE PUMP ENABLE
0	DISABLE
1	ENABLE (DEFAULT)

L3EN	3.3V LDO ENABLE
0	DISABLE
1	ENABLE (DEFAULT)

LVEN	VCO LDO ENABLE
0	DISABLE
1	ENABLE (DEFAULT)

VCO EN	VCO ENABLE
0	DISABLE
1	ENABLE (DEFAULT)

VCO SW	VCO SWITCH CONTROL FROM SPI
0	REGULAR (DEFAULT)
1	BAND CAL

VC[5:0]	VCO AMPLITUDE
0x00	0
….	….
0x18	24 (DEFAULT)
….	….
0x2B	43
….	….
0x3F	63 (RECOMMENDED)

VBSRC	VCO BW CAL AND SW SOURCE CONTROL
0	BAND CAL (DEFAULT)
1	SPI

VBS[5:0]	VCO BAND SELECT FROM SPI
0x00	DEFAULT 0x20
0x01	
….	
0x3F	

08547-010

Figure 44. Register 6—VCO Control and VCO Enable Register Map

REGISTER 7—MIXER BIAS ENABLE AND EXTERNAL VCO ENABLE (DEFAULT: 0x000007)

RES	XVCO	MIXER B_EN	RESERVED																		CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	XVCO	MBE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C3(1)	C2(1)	C1(1)

MBE	MIXER BIAS ENABLE
0	ENABLE (DEFAULT)
1	DISABLE

XVCO	EXTERNAL VCO
0	INTERNAL VCO (DEFAULT)
1	EXTERNAL VCO

08547-011

Figure 45. Register 7—Mixer Bias Enable and External VCO Enable Register Map

THEORY OF OPERATION

The ADRF6603 integrates a high performance downconverting mixer with a state-of-the-art fractional-N PLL. The PLL also integrates a low noise VCO. The SPI port allows the user to control the fractional-N PLL functions and the mixer optimization functions, as well as allowing for an externally applied LO or VCO.

The mixer core within the ADRF6603 is the next generation of an industry-leading family of mixers from Analog Devices, Inc. The RF input is converted to a current and then mixed down to IF using high performance NPN transistors. The mixer output currents are transformed to a differential output. The high performance active mixer core results in an exceptional IIP3 and IP1dB, with a very low output noise floor for excellent dynamic range. Over the specified frequency range, the ADRF6603 typically provides IF input P1dB of 14.6 dBm and IIP3 of 27 dBm.

Improved performance at specific frequencies can be achieved with the use of the internal capacitor DAC (CDAC), which is programmable via the SPI port, and by using a resistor to a 5 V supply from the IP3SET pin (Pin 29). Adjustment of the capacitor DAC allows increments in phase shift at internal nodes in the ADRF6603, thus allowing cancellation of third-order distortion with no change in supply current. Connecting a resistor to a 5 V supply from the IP3SET pin increases the internal mixer core current, thereby improving overall IIP2 and IIP3, as well as IP1dB. Using the IP3SET pin for this purpose increases the overall supply current.

The fractional divide function of the PLL allows the frequency multiplication value from REF_IN to LO output to be a fractional value rather than be restricted to an integer value as in traditional PLLs. In operation, this multiplication value is INT + (FRAC/MOD), where INT is the integer value, FRAC is the fractional value, and MOD is the modulus value, all programmable via the SPI port. In other fractional-N PLL designs, fractional multiplication is achieved by periodically changing the fractional value in a deterministic way. The disadvantage of this approach is often spurious components close to the fundamental signal. In the ADRF6603, a Σ-Δ modulator is used to distribute the fractional value randomly, thus significantly reducing the spurious content due to the fractional function.

PROGRAMMING THE ADRF6603

The ADRF6603 is programmed via a 3-pin SPI port. The timing requirements for the SPI port are shown in Figure 2. Eight programmable registers, each with 24 bits, control the operation of the device. The register functions are listed in Table 8.

Table 8. ADRF6603 Register Functions

Register	Function
Register 0	Integer divide control for the PLL
Register 1	Modulus divide control for the PLL
Register 2	Fractional divide control for the PLL
Register 3	Σ-Δ modulator dither control
Register 4	PLL charge pump, PFD, reference path control
Register 5	PLL enable and LO path control
Register 6	VCO control and VCO enable
Register 7	Mixer bias enable and external VCO enable

Note that internal calibration for the PLL must be run when the ADRF6603 is initialized at a given frequency. This calibration is run automatically whenever Register 0, Register 1, or Register 2 is programmed. Because the other registers affect PLL performance, Register 0, Register 1, and Register 2 should always be programmed last and in this order: Register 0, Register 1, Register 2.

To program the frequency of the ADRF6603, the user typically programs only Register 0, Register 1, and Register 2. However, if registers other than these are programmed first, a short delay should be inserted before programming Register 0. This delay ensures that the VCO band calibration has sufficient time to complete before the final band calibration for Register 0 is initiated.

Software is available on the ADRF6603 product page under the Evaluation Boards & Development Kits section that allows easy programming from a PC running Windows XP or Vista.

INITIALIZATION SEQUENCE

To ensure proper power-up of the ADRF6603, it is important to reset the PLL circuitry after the VCC supply rail settles to 5 V ± 0.25 V. Resetting the PLL ensures that the internal bias cells are properly configured, even under poor supply start-up conditions.

To ensure that the PLL is reset after power-up, follow this procedure:

1. Disable the PLL by setting the PLEN bit to 0 (Register 5, Bit DB6).
2. After a delay of >100 ms, set the PLEN bit to 1 (Register 5, Bit DB6).

After this procedure is followed, the other registers should be programmed in this order: Register 7, Register 6, Register 4, Register 3, Register 2, Register 1. Then, after a delay of >100 ms, Register 0 should be programmed.

LO SELECTION LOGIC

The downconverting mixer in the ADRF6603 can be used without the internal PLL by applying an external differential LO to Pin 37 and Pin 38 (LON and LOP). In addition, when using an LO generated by the internal PLL, the LO signal can be accessed directly at these same pins. This function can be used for debugging purposes, or the internally generated LO can be used as the LO for a separate mixer.

The operation of the LO generation and whether LOP and LON are inputs or outputs are determined by the logic levels applied at Pin 16 (PLL_EN) and Pin 36 (LODRV_EN), as well as Bit DB3 (LDRV) and Bit DB6 (PLEN) in Register 5. The combination of externally applied logic and internal bits required for particular LO functions is given in Table 9.

Table 9. LO Selection Logic

Pins[1]		Register 5 Bits[1]		Outputs	
Pin 16 (PLL_EN)	**Pin 36 (LODRV_EN)**	**Bit DB6 (PLEN)**	**Bit DB3 (LDRV)**	**Output Buffer**	**LO**
0	X	0	X	Disabled	External
0	X	1	X	Disabled	External
1	X	0	X	Disabled	External
1	0	1	0	Disabled	Internal
1	X	1	1	Enabled	Internal
1	1	1	X	Enabled	Internal

[1] X = don't care.

APPLICATIONS INFORMATION

BASIC CONNECTIONS FOR OPERATION

Figure 46 shows the schematic for the ADRF6603 evaluation board. The six power supply pins should be individually decoupled using 100 pF and 0.1 µF capacitors located as close as possible to the device. In addition, the internal decoupling nodes (DECL3P3, DECL2P5, and DECLVCO) should be decoupled with the capacitor values shown in Figure 46.

The RF input is internally ac-coupled and needs no external bias. The IF outputs are open collector, and a bias inductor is required from these outputs to VCC.

A peak-to-peak differential swing on RF_{IN} of 1 V (0.353 V rms for a sine wave input) results in an IF output power of 4.7 dBm.

The reference frequency for the PLL should be from 12 MHz to 160 MHz and should be applied to the REF_IN pin, which should be ac-coupled and terminated with a 50 Ω resistor as shown in Figure 46. The reference signal, or a divided-down version of the reference signal, can be brought back off chip at the multiplexer output pin (MUXOUT). A lock detect signal and a voltage proportional to the ambient temperature can also be selected on the multiplexer output pin.

The loop filter is connected between the CP and VTUNE pins. When connected in this way, the internal VCO is operational. For information about the loop filter components, see the Evaluation Board Configuration Options section.

Operation with an external VCO is also possible. In this case, the loop filter components should be referred to ground. The output of the loop filter is connected to the input voltage pin of the external VCO. The output of the VCO is brought back into the device on the LOP and LON pins, using a balun if necessary.

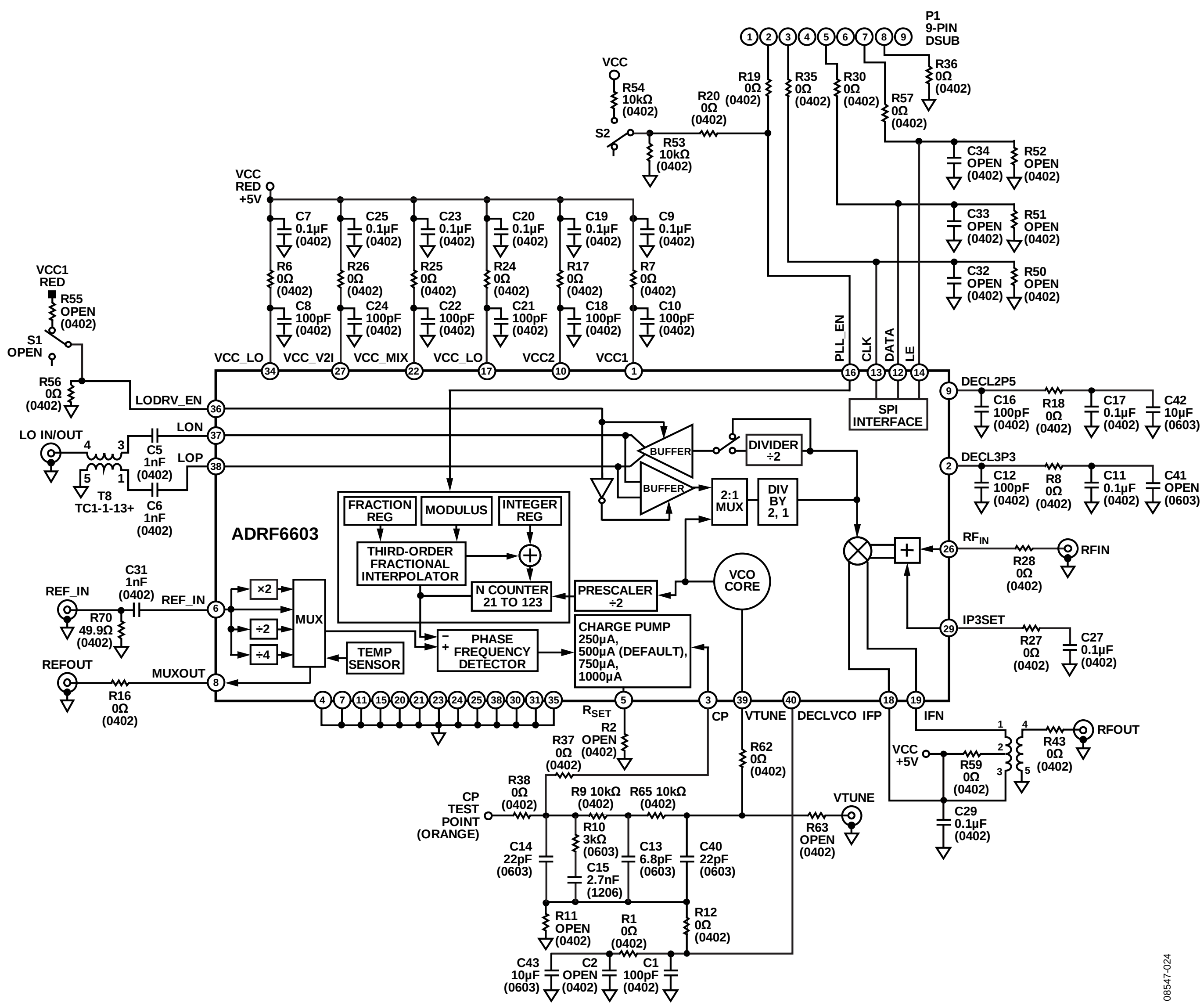


Figure 46. Basic Connections for Operation of the ADRF6603

AC TEST FIXTURE

Characterization data for the ADRF6603 was taken under very strict test conditions. All possible techniques were used to achieve optimum accuracy and to remove degrading effects of the signal generation and measurement equipment. Figure 47 shows the typical AC test set up used in the characterization of the ADRF6603.

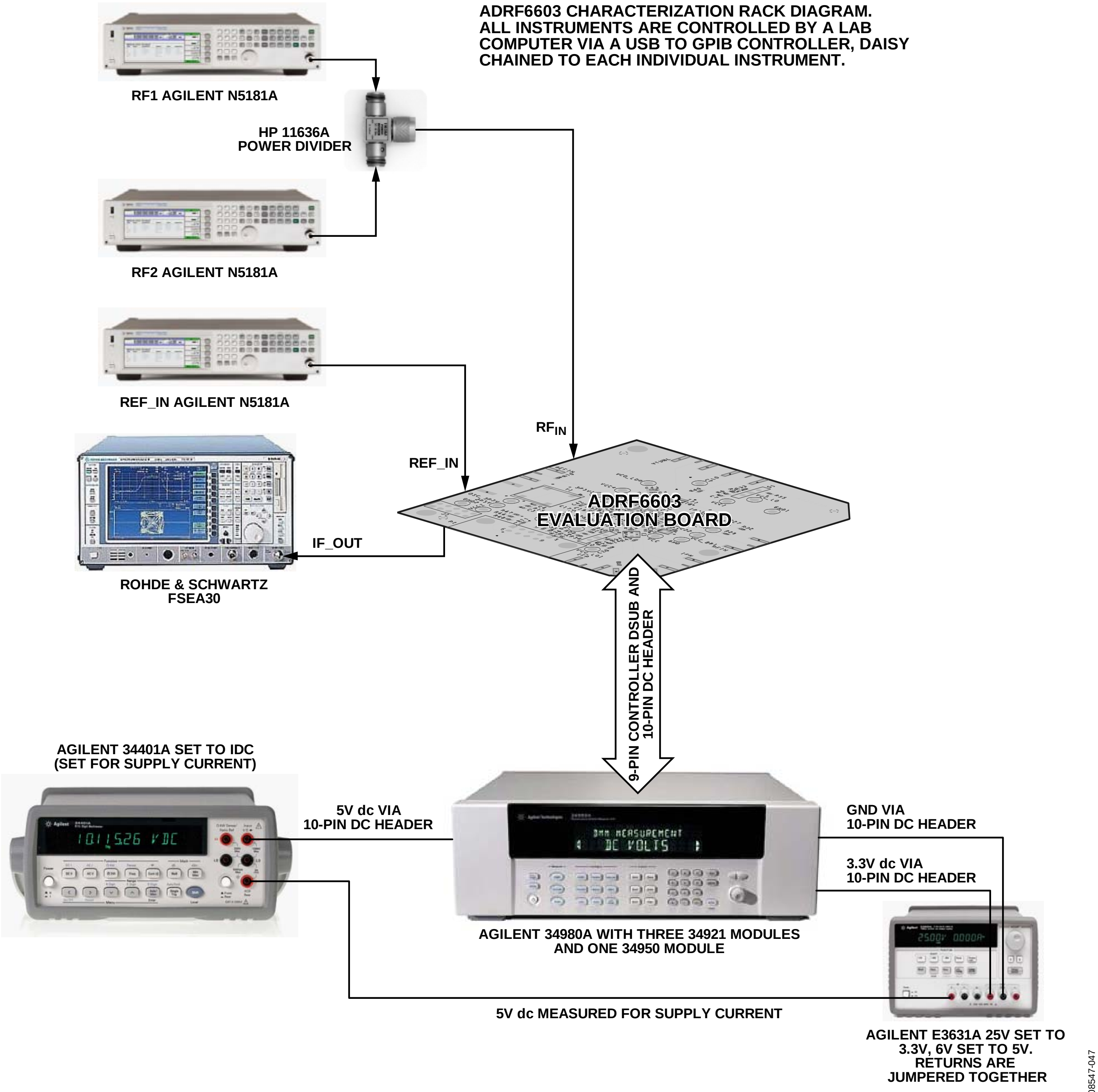


Figure 47. ADRF6603 AC Test Setup

EVALUATION BOARD

Figure 50 shows the schematic of the RoHS-compliant evaluation board for the ADRF6603. This board has four layers and was designed using Rogers 4350 hybrid material to minimize high frequency losses. FR4 material is also adequate if the design can accept the slightly higher trace loss of this material.

The evaluation board is designed to operate using the internal VCO of the device (the default configuration) or with an external VCO. To use an external VCO, R62 and R12 should be removed. Place 0 Ω resistors in R63 and R11. The input of the external VCO should be connected to the VTUNE SMA connector, and the external VCO output should be connected to the LO IN/OUT SMA connector. In addition to these hardware changes, internal register settings must also be changed to enable operation with an external VCO (see the Register 6—VCO Control and VCO Enable (Default: 0x1E2106) section).

Additional configuration options for the evaluation board are described in Table 10.

EVALUATION BOARD CONTROL SOFTWARE

Software to program the ADRF6603 is available for download on the ADRF6603 product page under the Evaluation Boards & Development Kits section. To install the software

1. Download and extract the zip file: ADRF6x0x_3p0p0_XP_install.exe file.
2. Follow the instructions in the read me file.

The evaluation board can be connected to the PC using a PC parallel port or a USB port. These options are selectable from the opening menu of the software interface (see Figure 48). The evaluation board is shipped with a 25-pin parallel port cable for connection to the PC parallel port.

To connect the evaluation board to a USB port, a USB adapter board (EVAL-ADF4XXXZ-USB) must be purchased from Analog Devices. This board connects to the PC using a standard USB cable with a USB mini-connector at one end. An additional 25-pin male to 9-pin female adapter is required to mate the ADF4XXXZ-USB board to the 9-pin D-Sub connector on the ADRF6603 evaluation board.

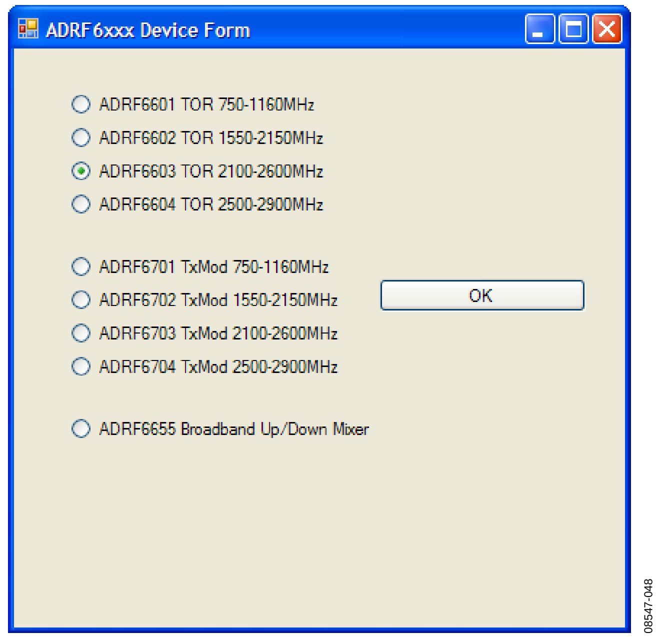


Figure 48. Control Software Opening Menu

Figure 49 shows the main menu of the control software with the default settings displayed.

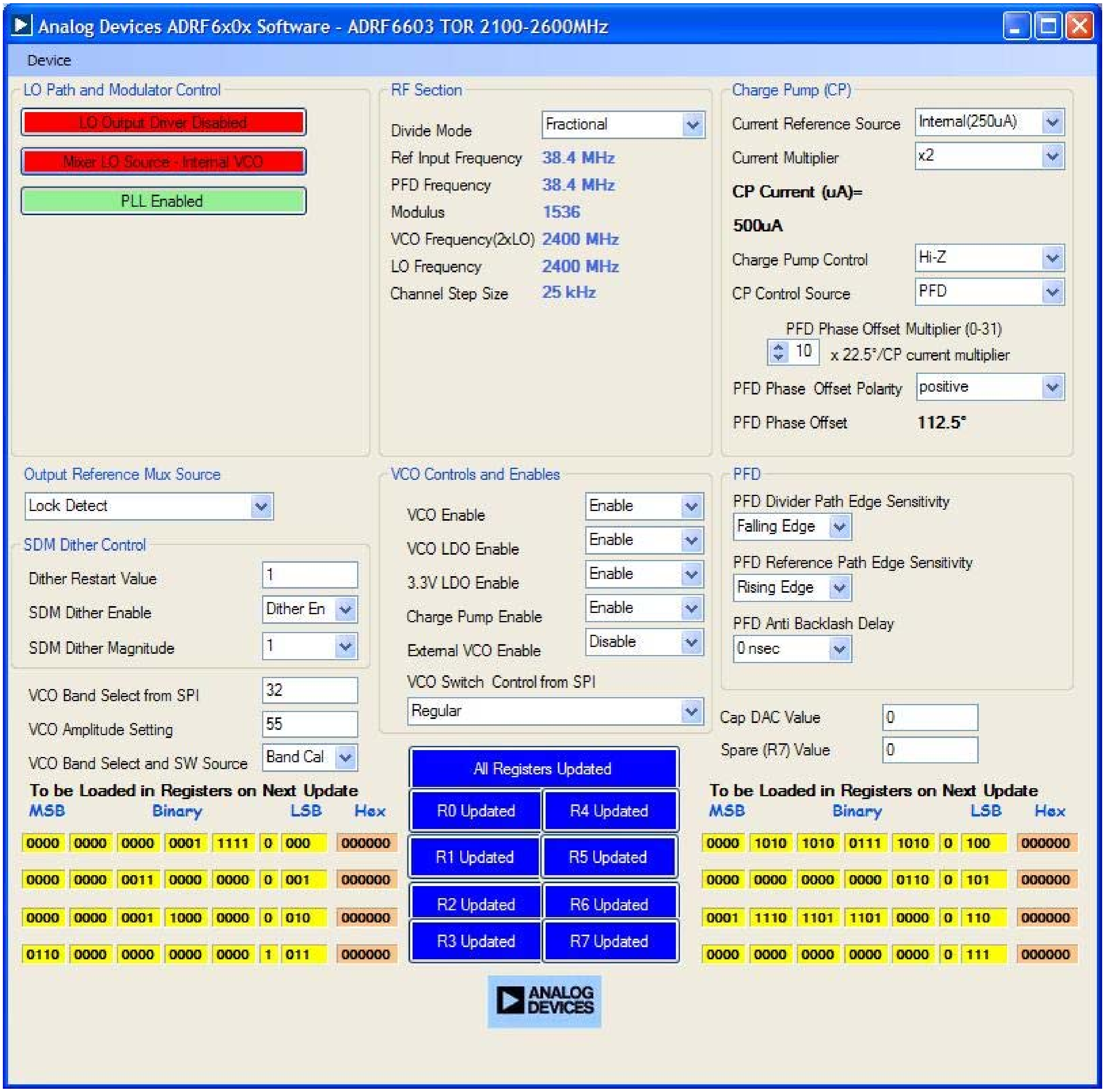


Figure 49. Main Screen of the ADRF6603 Evaluation Board Software

SCHEMATIC AND ARTWORK

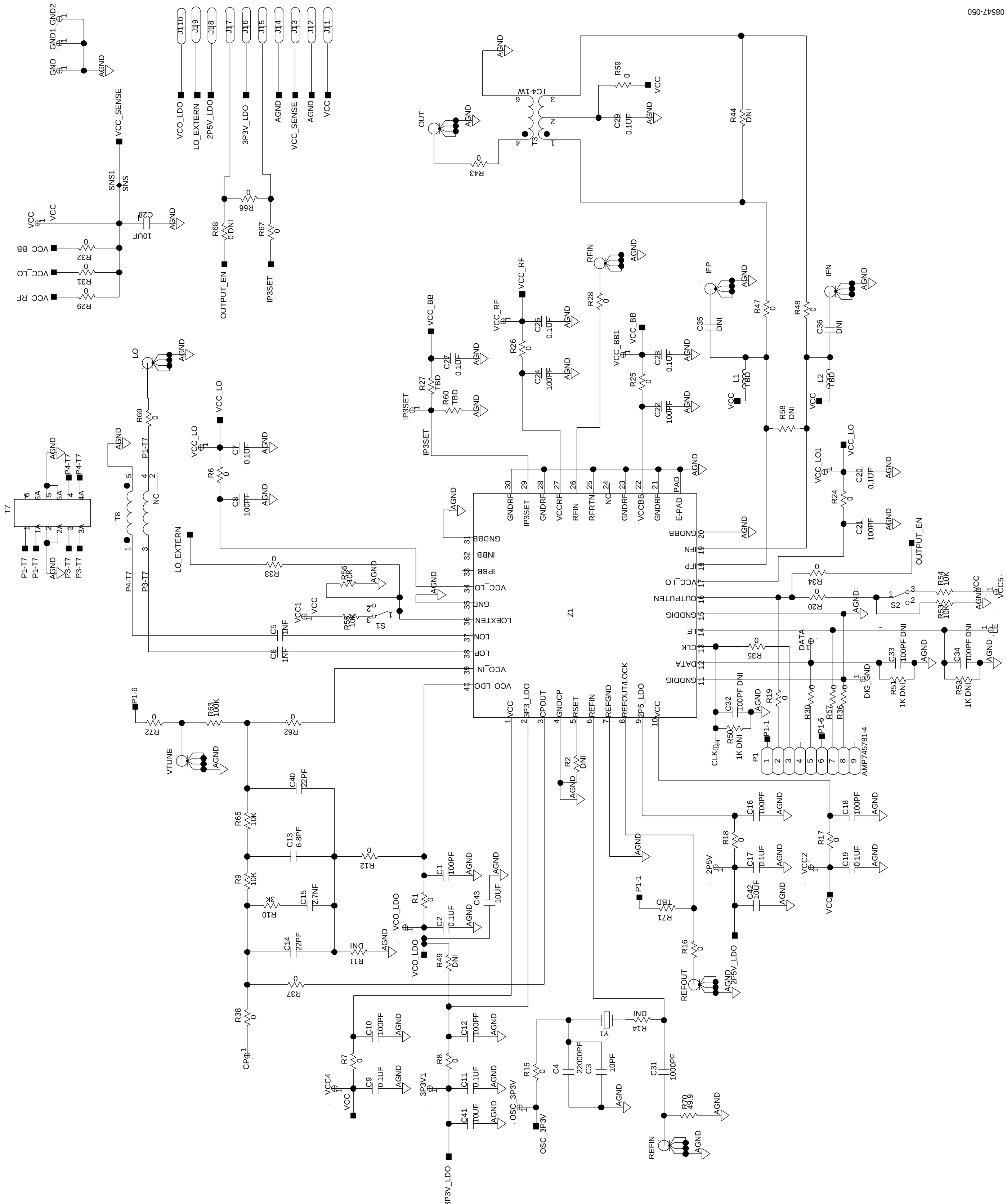


Figure 50. Evaluation Board Schematic

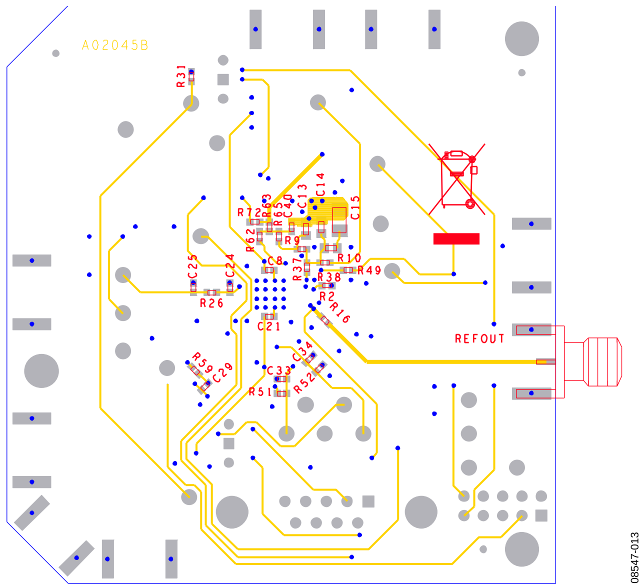


Figure 51. Evaluation Board Layout (Bottom)

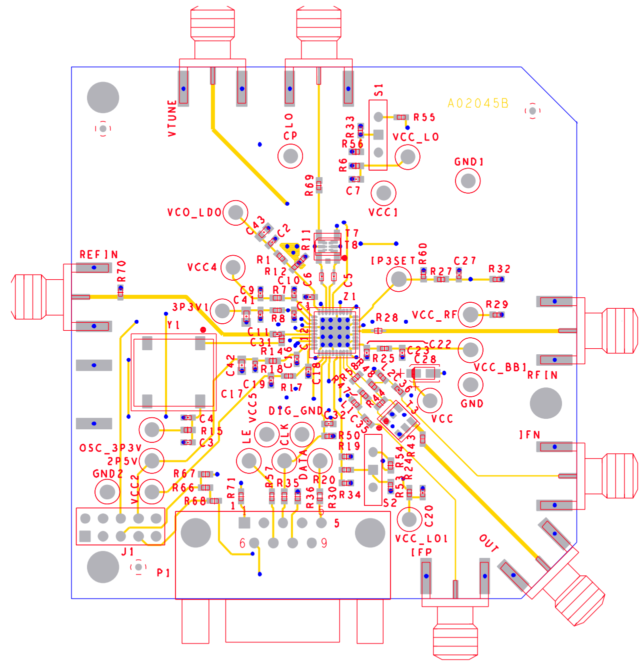


Figure 52. Evaluation Board Layout (Top)

EVALUATION BOARD CONFIGURATION OPTIONS

Table 10.

Component	Description	Default Condition/ Option Settings
S1, R55, R56, R33	LO select. Switch and resistors to ground the LODRV_EN pin. The LODRV_EN pin setting, in combination with internal register settings, determines whether the LOP and LON pins function as inputs or outputs (see the LO Selection Logic section for more information).	S1 = R55 = open (not installed), R56 = R33 = 0 Ω, LODRV_EN = 0 V
LO IN/OUT SMA Connector	LO input/output. An external 1× LO or 2× LO can be applied to this single-ended input connector.	LO input
REFIN SMA Connector	Reference input. The input reference frequency for the PLL is applied to this connector. Input impedance is 50 Ω.	
REFOUT SMA Connector	Multiplexer output. The REFOUT connector connects directly to the MUXOUT pin. The on-board multiplexer can be programmed to bring out the following signals: REFIN, 2× REFIN, REFIN/2, and REFIN/4; temperature sensor output voltage; and lock detect indicator.	Lock detect
CP Test Point	Charge pump test point. The unfiltered charge pump signal can be probed at this test point. Note that the CP pin should not be probed during critical measurements such as phase noise.	
R37, C14, R9, R10, C15, C13, R65, C40	Loop filter. Loop filter components.	
R11, R12	Loop filter return. When the internal VCO is used, the loop filter components should be returned to Pin 40 (DECLVCO) by installing a 0 Ω resistor in R12. When an external VCO is used, the loop filter components can be returned to ground by installing a 0 Ω resistor in R11.	R12 = 0 Ω (0402), R11 = open (0402)
R62, R63, VTUNE SMA Connector	Internal vs. external VCO. When the internal VCO is enabled, the loop filter components are connected directly to the VTUNE pin (Pin 39) by installing a 0 Ω resistor in R62. To use an external VCO, R62 should be left open. A 0 Ω resistor should be installed in R63, and the voltage input of the VCO should be connected to the VTUNE SMA connector. The output of the VCO is brought back into the PLL via the LO IN/OUT SMA connector.	R62 = 0 Ω (0402), R63 = open (0402)
R2	R_{SET} pin. This pin is unused and should be left open.	R2 = open (0402)
RFIN SMA Connector	RF input. The RF input signal should be applied to the RFIN SMA connector. The RF input of the ADRF6603 is ac-coupled, so no bias is necessary.	R3 = R23 = open (0402)
T3	IF output. The differential IF output signals from the ADRF6603 (IFP and IFN) are converted to a single-ended signal by T3.	

OUTLINE DIMENSIONS

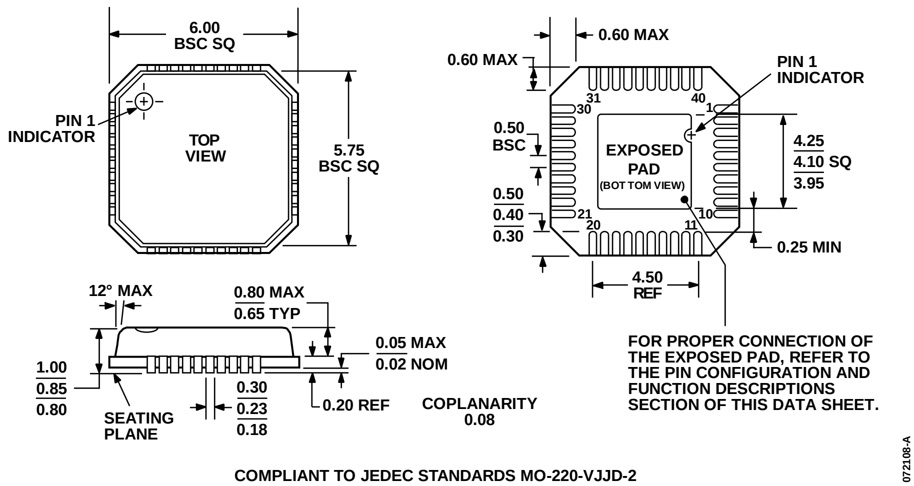


Figure 53. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(CP-40-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF6603ACPZ-R7	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-40-1
ADRF6603-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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NOTES

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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