

# MC74HCU04A

## Hex Unbuffered Inverter

### High-Performance Silicon-Gate CMOS

The MC74HCU04A is identical in pinout to the LS04 and the MC14069UB. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device consists of six single-stage inverters. These inverters are well suited for use as oscillators, pulse shapers, and in many other applications requiring a high-input impedance amplifier. For digital applications, the HC04A is recommended.

#### Features

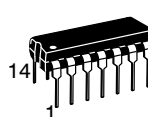
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V; 2.5 to 6.0 V in Oscillator Configurations
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 12 FETs or 3 Equivalent Gates
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



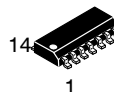
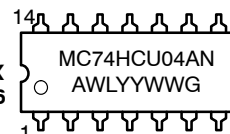
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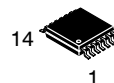
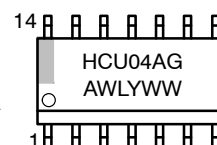
#### MARKING DIAGRAMS



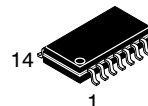
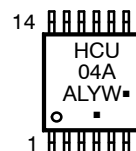
PDIP-14  
N SUFFIX  
CASE 646



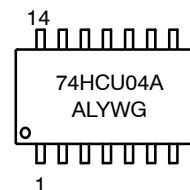
SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



SOEIAJ-14  
F SUFFIX  
CASE 965



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G or ▪ = Pb-Free Package

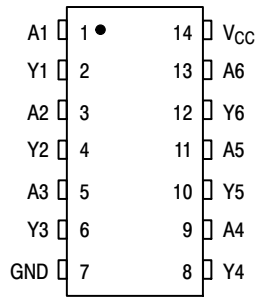
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# MC74HCU04A

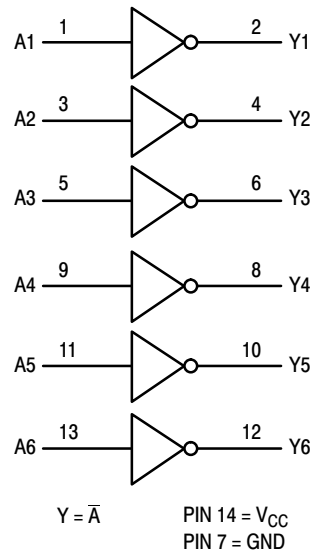
## PIN ASSIGNMENT



## FUNCTION TABLE

Inputs A	Outputs Y
L	H
H	L

## LOGIC DIAGRAM



## ORDERING INFORMATION

Device	Package	Shipping†
MC74HCU04ANG	PDIP-14 (Pb-Free)	25 Units / Rail
MC74HCU04ADG	SOIC-14 (Pb-Free)	55 Units / Rail
MC74HCU04ADR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
MC74HCU04ADTR2G	TSSOP-14*	2500 / Tape & Reel
MC74HCU04AFELG	SOEIAJ-14 (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	- 0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air	Plastic DIP† 750 SOIC Package† 500 TSSOP Package† 450	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — Plastic DIP: -10mW/°C from 65° to 125°C  
SOIC Package: -7mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	- 55	+ 125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	-	No Limit	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	$V_{CC}$ V	Guaranteed Limit			Unit
				- 55 to 25°C	$\leq 85^\circ\text{C}$	$\leq 125^\circ\text{C}$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.5 V^*$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.7	1.7	1.7	V
			3.0	2.5	2.5	2.5	
			4.5	3.6	3.6	3.6	
			6.0	4.8	4.8	4.8	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.5 V^*$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.3	0.3	0.3	V
			3.0	0.5	0.5	0.5	
			4.5	0.8	0.8	0.8	
			6.0	1.1	1.1	1.1	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = GND$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	1.8	1.8	1.8	V
			4.5	4.0	4.0	4.0	
			6.0	5.5	5.5	5.5	
		$V_{in} = GND$ $ I_{out}  \leq 2.4 \text{ mA}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	3.0	2.36	2.26	2.20	
			4.5	3.86	3.76	3.70	
			6.0	5.36	5.26	5.20	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{CC}$ $ I_{out}  \leq 20 \mu\text{A}$	2.0	0.2	0.2	0.2	V
			4.5	0.5	0.5	0.5	
			6.0	0.5	0.5	0.5	
		$V_{in} = V_{CC}$ $ I_{out}  \leq 2.4 \text{ mA}$ $ I_{out}  \leq 4.0 \text{ mA}$ $ I_{out}  \leq 5.2 \text{ mA}$	3.0	0.32	0.32	0.32	
			4.5	0.32	0.37	0.40	
			6.0	0.32	0.37	0.40	

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				- 55 to 25°C	≤ 85°C	≤ 125°C	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	1	10	40	μA

1. For V<sub>CC</sub> = 2.0 V, V<sub>out</sub> = 0.2 V or V<sub>CC</sub> - 0.2 V.

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			- 55 to 25°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	70 40 14 12	90 45 18 15	105 50 21 18	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 27 15 13	95 32 19 16	110 36 22 19	ns
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Inverter)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V		pF
		15		

2. Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

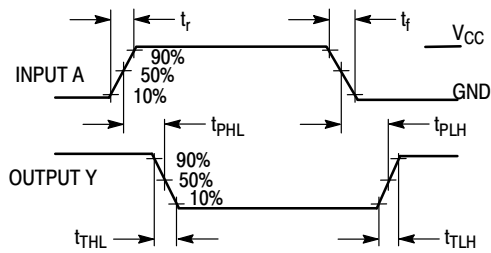
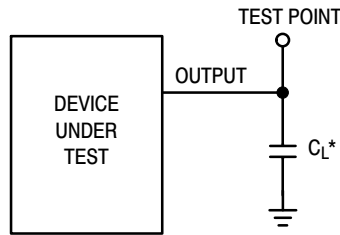


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit

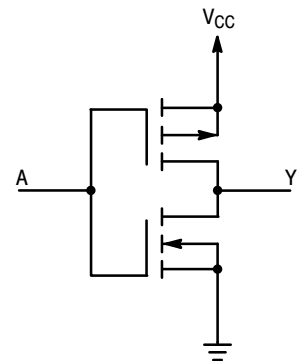


Figure 3. Logic Detail  
(1/6 of Device Shown)

# MC74HCU04A

## TYPICAL APPLICATIONS

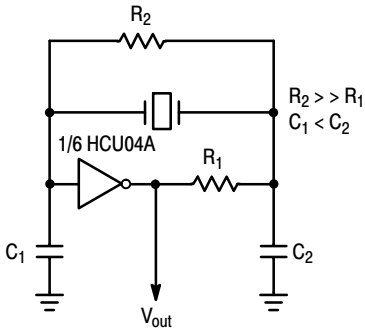


Figure 4. Crystal Oscillator

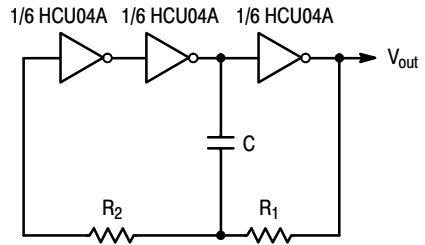


Figure 5. Stable RC Oscillator

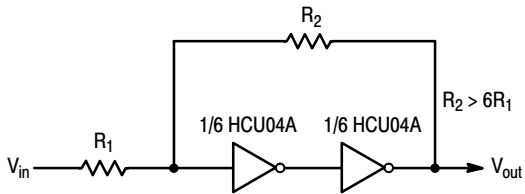


Figure 6. Schmitt Trigger

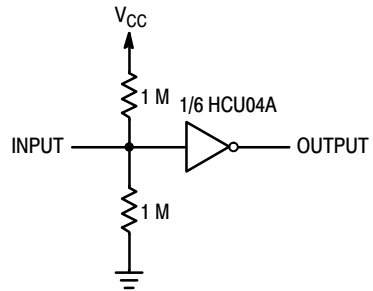


Figure 7. High Input Impedance Single-Stage Amplifier with a 2 to 6 V Supply Range

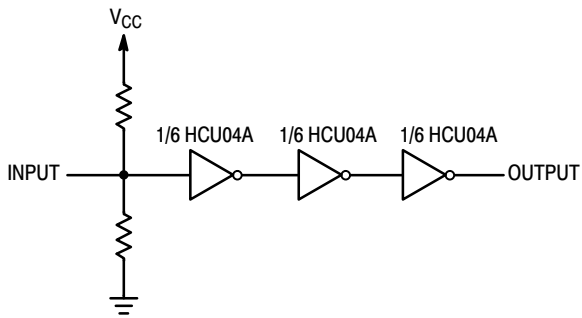
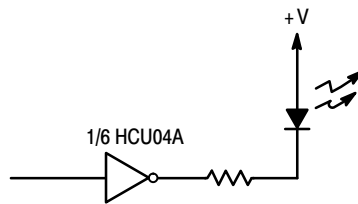


Figure 8. Multi-Stage Amplifier



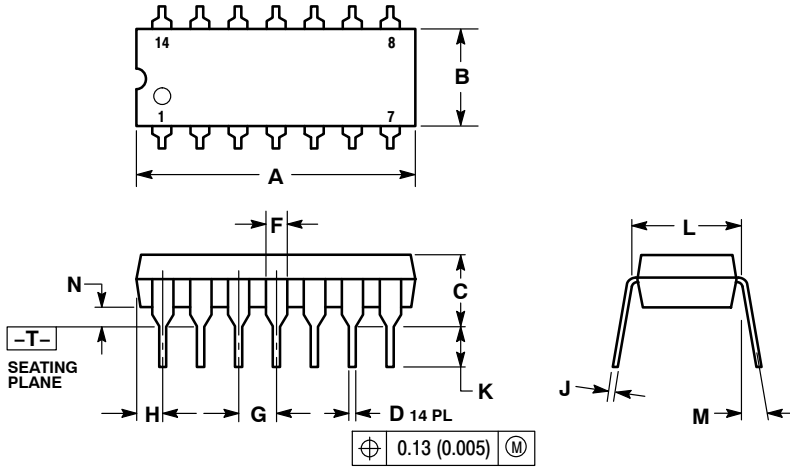
For reduced power supply current, use high-efficiency LEDs such as the Hewlett-Packard HLMP series or equivalent.

Figure 9. LED Driver

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## PACKAGE DIMENSIONS

PDIP-14  
N SUFFIX  
CASE 646-06  
ISSUE P



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

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## PACKAGE DIMENSIONS

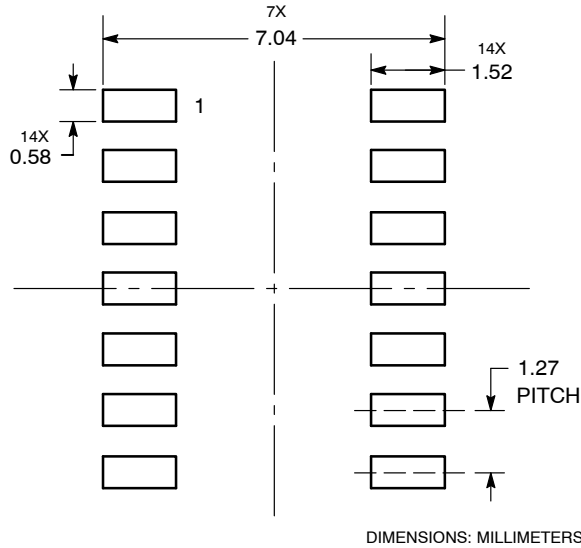
SOIC-14  
D SUFFIX  
CASE 751A-03  
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

## SOLDERING FOOTPRINT



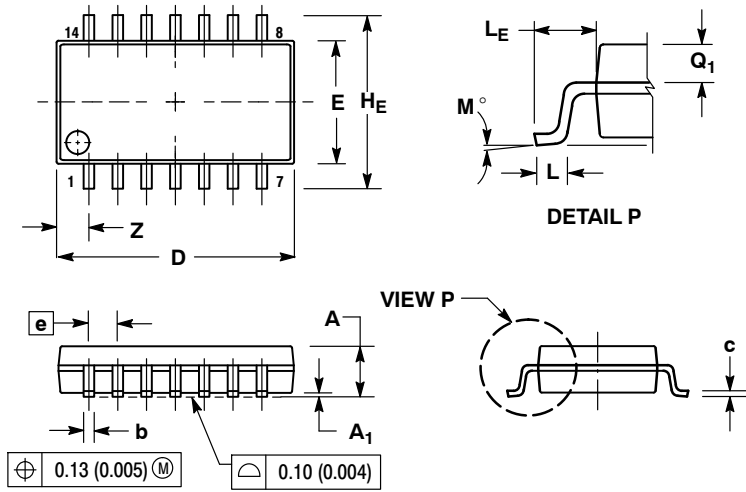




# MC74HCU04A

## PACKAGE DIMENSIONS

SOEIAJ-14  
F SUFFIX  
CASE 965-01  
ISSUE B



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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