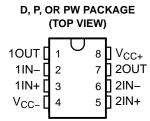
SLOS477A-JUNE 2005-REVISED JULY 2005

FEATURES

- Operating Voltage...±2 V to ±18 V
- Low Offset Voltage...1 mV Max at 25°C, TL5580A
- Wide GBW...12 MHz Typ
- Slew Rate...5 V/μs Typ
- Low THD...0.0005% Typ
- Low-Noise Voltage...7 nV/√Hz at 1 kHz Typ

APPLICATIONS

- Audio
- Test Equipment
- Industrial Process Controls
- Data-Acquisition Systems
- Active Filters
- Power-Supply Regulation



DESCRIPTION/ORDERING INFORMATION

The TL5580 is a dual bipolar operational amplifier that combines both high dc and ac performance with its low offset voltage, high-gain bandwidth, low harmonic distortion, and low-noise characteristics. In addition, its output is capable of driving $600-\Omega$ loads. All these characteristics make the device ideally suited for use in audio, active filtering, and industrial measurement applications.

ORDERING INFORMATION

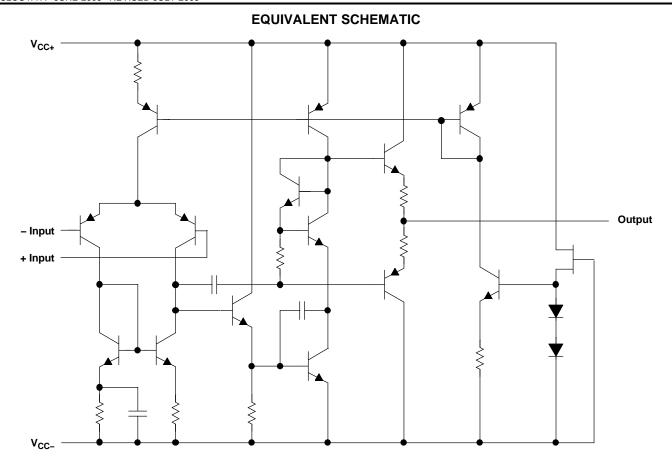
T _A	V _{IO} (25°C, MAX)	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
		PDIP – P	Tube of 50	TL5580IP	TL5580IP
		SOIC - D	Tube of 75	TL5580ID	75500
	Standard grade 1.5 mV	30IC - D	Reel of 2500	TL5580IDR	Z5580
		TSSOP – PW	Tube of 150	TL5580IPW	Z5580
–40°C to 85°C		1330P – PW	Reel of 2000	TL5580IPWR	25560
-40 C to 65 C		PDIP – P	Tube of 50	TL5580AIP	TL5580AIP
		SOIC - D	Tube of 75	TL5580AID	755004
	A grade 1 mV	30IC - D	Reel of 2500	TL5580AIDR	Z5580A
		TSSOP – PW	Tube of 150	TL5580AIPW	Z5580A
		1330P - FW	Reel of 2000	TL5580AIPWR	2000A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.







TL5580, TL5580A **DUAL LOW-NOISE WIDE-BANDWIDTH PRECISION AMPLIFIER**

SLOS477A-JUNE 2005-REVISED JULY 2005

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage			±18	V
VI	Input voltage (any input)			±15	V
V_{ID}	Differential input voltage		±30	V	
Io	Output current		±50	mA	
		D package		97	
θ_{JA}	Package thermal impedance (2)(3)	P package		85	°C/W
		PW package		149	
T _J	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		-60	125	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating" conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CC+}	Constructions		16	\/
V _{CC} -	Supply voltage	-2	-16	V
T _A	Operating free-air temperature	-40	85	°C

Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability. The package thermal impedance is calculated in accordance with JESD 51-7.

TL5580, TL5580A DUAL LOW-NOISE WIDE-BANDWIDTH PRECISION AMPLIFIER

SLOS477A-JUNE 2005-REVISED JULY 2005



Electrical Characteristics

 $V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT	
		TI FEROA		25°C		0.3	1		
.,	land offert college	TL5580A	D <4010	-40°C to 85°C			1.35	\/	
V _{IO}	V _{IO} Input offset voltage	TI 5500	$R_{S} \le 10 \text{ k}\Omega$	25°C		0.3	1.5	mV	
		TL5580		-40°C to 85°C			2		
αV_{IO}	Average temperature coeff offset voltage	icient of input		-40°C to 85°C		1.8	5	μV/°C	
-	land offers and an armount			25°C		5	75	A	
I _{IO} Input offset current				-40°C to 85°C			100	nA	
	lament bing assument			25°C		100	500	A	
I _{IB}	I _{IB} Input bias current			-40°C to 85°C			800	nA	
۸	A _{VD} Large-signal differential-voltage amplification		D > 2 kO V 140 V	25°C	90	110		dB	
A _{VD}			$R_L \ge 2 \text{ k}\Omega, V_O = \pm 10 \text{ V}$	-40°C to 85°C	87			uБ	
	Outrout valta na avvia a		D > 0 lo	25°C	12.75 - 12.25	±13.5		V	
V _{OM}	Output voltage swing		$R_L \ge 2 k\Omega$	-40°C to 85°C	12.5 –12			V	
.,	Common model innut valte			25°C ±13 ±13		±13.5		.,	
V_{ICR}	Common-mode input voltage	ge range		-40°C to 85°C	±12			V	
OMPD	0		$R_S \le 10 \text{ k}\Omega$,	25°C	90	110		-ID	
CMRR	CMRR Common-mode rejection ratio		$V_{ICR} = -12 \text{ V to } 12 \text{ V}$	-40°C to 85°C	85			dB	
1. (1)	k _{SVR} ⁽¹⁾ Supply-voltage rejection ratio		D <4010	25°C	85	110		٩D	
K _{SVR} (1)			$R_{S} \le 10 \text{ k}\Omega$	-40°C to 85°C	83			dB	
	Cumply gurrent (all generalities	" "		25°C		6	9	m A	
ICC	I _{CC} Supply current (all amplifiers)			-40°C to 85°C			12	mA	

⁽¹⁾ Measured with $V_{CC\pm}$ varied simultaneously

Operating Characteristics

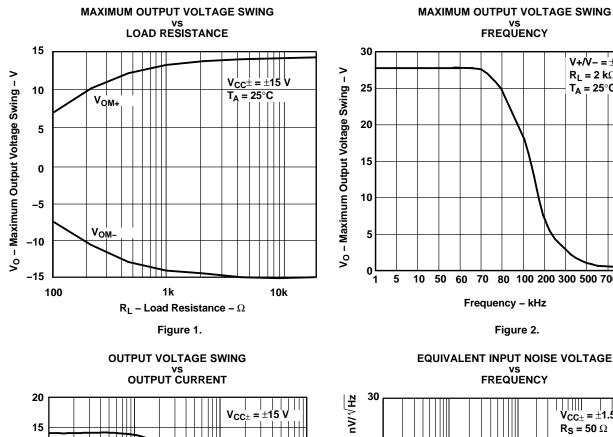
 $V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

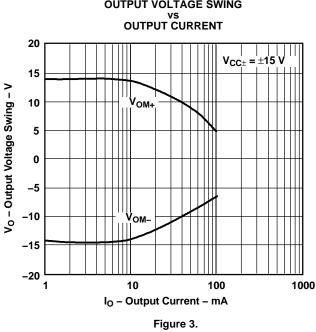
	PARAMETER	TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	$R_L \ge 2 \text{ k}\Omega$	5	V/μs
GBW	Gain bandwidth product	f = 10 kHz	12	MHz
THD	Total harmonic distortion	$V_O = 5 \text{ V}, R_L = 2 \text{ k}\Omega, f = 1 \text{ kHz}, A_{VD} = 20 \text{ dB}$	0.0005	%
V _n	Equivalent input noise voltage	f = 1 kHz	7	nV/√ Hz

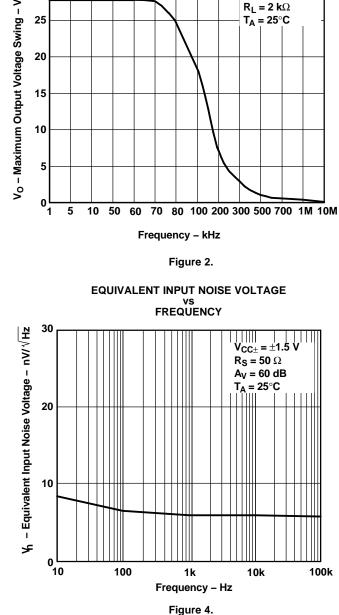
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V+/V-=±15 V

TYPICAL CHARACTERISTICS

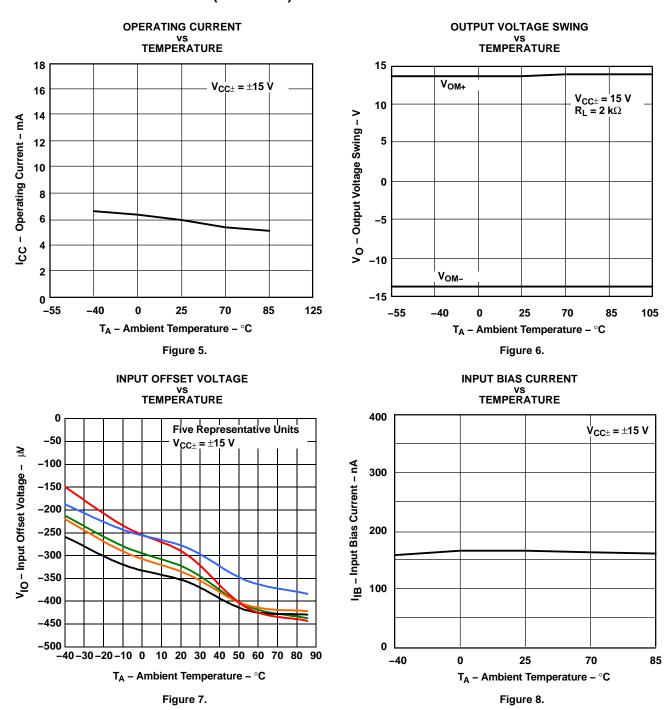








TYPICAL CHARACTERISTICS (continued)

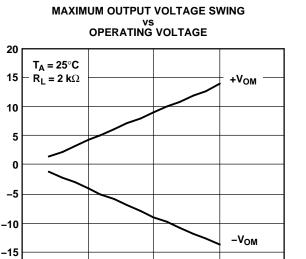




V_O- Maximum Output Voltage Swing - V

-20 L

TYPICAL CHARACTERISTICS (continued)



V_{CC+}/V_{CC-} – Operating Voltage – V Figure 9.

±10

±20

±15

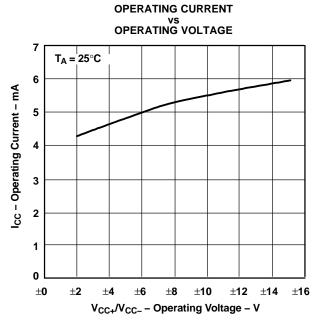


Figure 10.

TOTAL HARMONIC DISTORTION VS OUTPUT VOLTAGE

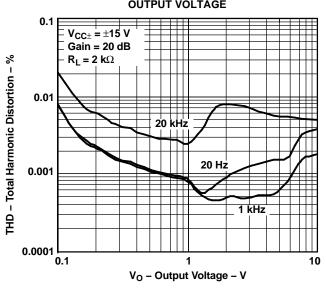


Figure 11.

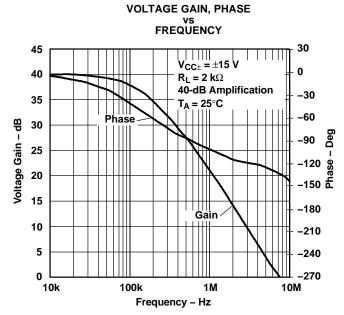


Figure 12.



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL5580AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL5580AIPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL5580AIPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580AIPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL5580IPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL5580IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM



PACKAGE OPTION ADDENDUM

24-May-2007

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins F	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL5580IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL5580IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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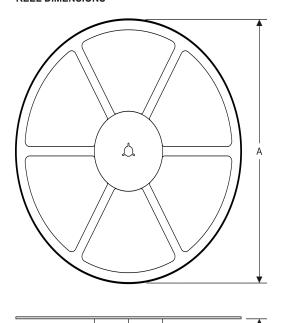
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PACKAGE MATERIALS INFORMATION

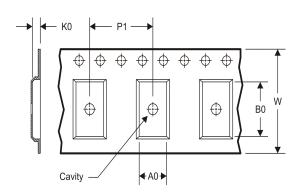
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL5580AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5580AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL5580IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL5580IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

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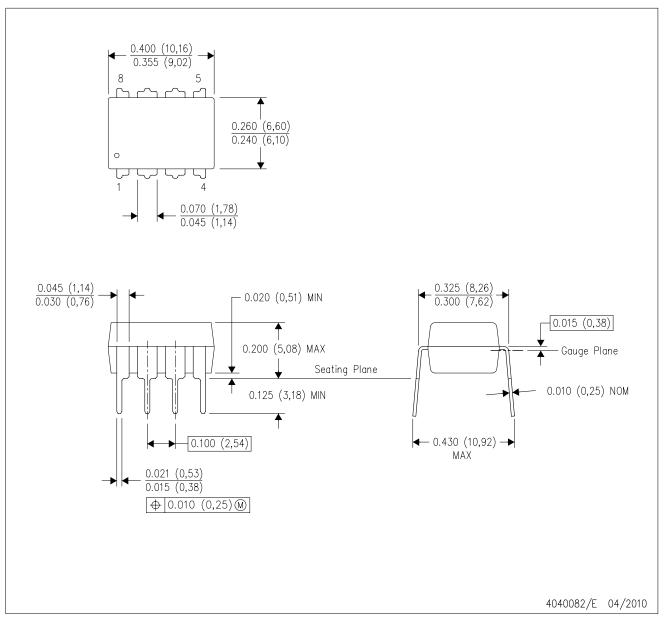


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL5580AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5580AIPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL5580IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL5580IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

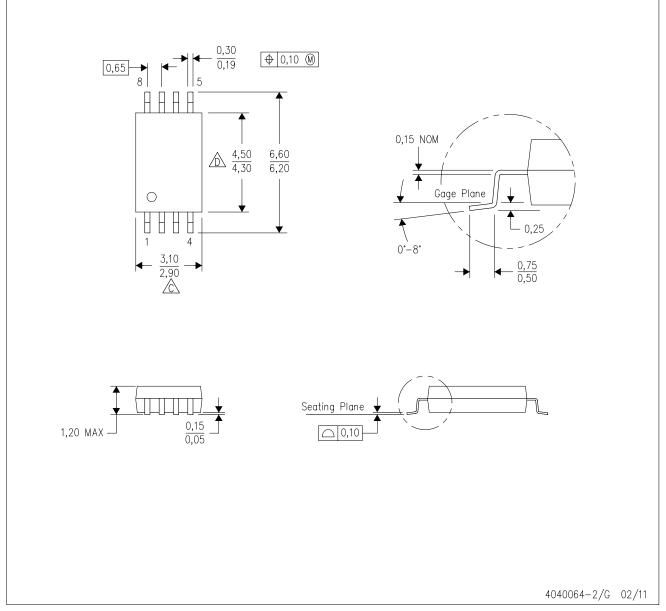


- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



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Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов:
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
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Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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