3 MSPS,10-/12-Bit ADCs in 8-Lead TSOT

AD7273/AD7274

FEATURES

Throughput rate: 3 MSPS
Specified for V_{DD} of 2.35 V to 3.6 V
Power consumption
11.4 mW at 3 MSPS with 3 V supplies
Wide input bandwidth
70 dB SNR at 1 MHz input frequency
Flexible power/serial clock speed management
No pipeline delays
High speed serial interface
SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible
Temperature range: −40°C to +125°C
Power-down mode: 0.1 µA typ
8-lead TSOT package
8-lead MSOP package

FUNCTIONAL BLOCK DIAGRAM

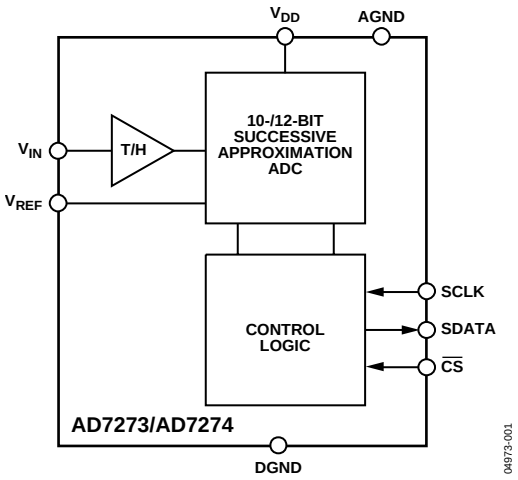

Figure 1.

GENERAL DESCRIPTION

The AD7273/AD7274 are 10-/12-bit, high speed, low power, successive approximation ADCs, respectively. The parts operate from a single 2.35 V to 3.6 V power supply and feature throughput rates of up to 3 MSPS. Each part contains a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 55 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$, and the conversion is also initiated at this point. The conversion rate is determined by the SCLK. There are no pipeline delays associated with these parts.

The AD7273/AD7274 use advanced design techniques to achieve very low power dissipation at high throughput rates.

The reference for the parts is applied externally and can be in the range of 1.4 V to V_{DD}. This allows the widest dynamic input range to the ADC.

Table 1.

Part Number	Resolution	Package	
AD7273[1]	10	8-lead MSOP	8-Lead TSOT
AD7274[1]	12	8-lead MSOP	8-Lead TSOT
AD7276	12	8-lead MSOP	6-Lead TSOT
AD7277	10	8-lead MSOP	6-Lead TSOT
AD7278	8	8-lead MSOP	6-Lead TSOT

[1] Parts contain external reference pin.

PRODUCT HIGHLIGHTS

1. 3 MSPS ADCs in an 8-lead TSOT package.
2. High throughput with low power consumption.
3. Flexible power/serial clock speed management. Allows maximum power efficiency at low throughput rates.
4. Reference can be driven up to the power supply.
5. No pipeline delay.
6. The parts feature a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

9/05—Revision 0: Initial Version

SPECIFICATIONS

AD7274 SPECIFICATIONS

V_{DD} = 2.35 V to 3.6 V, V_{REF} = 2.35 V to V_{DD}, f_{SCLK} = 48 MHz, f_{SAMPLE} = 3 MSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	B Grade[1]	Unit[2]	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 1 MHz sine wave
Signal-to-Noise + Distortion (SINAD)[3]	68	dB min	
Signal-to-Noise Ratio (SNR)	69.5	dB min	
Total Harmonic Distortion (THD)[3]	−73	dB max	
	−78	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[3]	−80	dB typ	
Intermodulation Distortion (IMD)			
Second-Order Terms	−82	dB typ	fa = 1 MHz, fb = 0.97 MHz
Third-Order Terms	−82	dB typ	fa = 1 MHz, fb = 0.97 MHz
Aperture Delay	5	ns typ	
Aperture Jitter	18	ps typ	
Full Power Bandwidth	55	MHz typ	@ 3 dB
	8	MHz typ	@ 0.1 dB
Power Supply Rejection Ratio (PSRR)	82	dB typ	
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity[3]	±1	LSB max	
Differential Nonlinearity[3]	±1	LSB max	Guaranteed no missed codes to 12 bits
Offset Error[3]	±3	LSB max	
Gain Error[3]	±3.5	LSB max	
Total Unadjusted Error (TUE)[3]	±3.5	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to V_{REF}	V	
DC Leakage Current	±1	µA max	−40°C to +85°C
	±5.5	µA max	85°C to 125°C
Input Capacitance	42	pF typ	When in track
	10	pF typ	When in hold
REFERENCE INPUT			
V_{REF} Input Voltage Range	1.4 to V_{DD}	V min/V max	
DC leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
Input Impedance	32	Ω typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	1.7	V min	2.35 V ≤ V_{DD} ≤ 2.7 V
	2	V min	2.7 V < V_{DD} ≤ 3.6 V
Input Low Voltage, V_{INL}	0.7	V max	2.35 V ≤ V_{DD} < 2.7 V
	0.8	V max	2.7 V ≤ V_{DD} ≤ 3.6 V
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	2	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA, V_{DD} = 2.35 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±2.5	µA max	
Floating-State Output Capacitance[4]	4.5	pF max	
Output Coding	Straight (natural) binary		

Parameter	B Grade[1]	Unit[2]	Test Conditions/Comments
CONVERSION RATE			
Conversion Time	291	ns max	14 SCLK cycles with SCLK at 48 MHz
Track-and-Hold Acquisition Time[3]	60	ns max	
Throughput Rate	3	MSPS max	See the Serial Interface section
POWER RQUIREMENTS			
V_{DD}	2.35/3.6	V min/V max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	1	mA typ	V_{DD} = 3 V, SCLK on or off
Normal Mode (Operational)	5	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 3 MSPS
	3.8	mA typ	V_{DD} = 3 V
Partial Power-Down Mode (Static)	34	µA typ	
Full Power-Down Mode (Static)	2	µA max	−40°C to +85°C, typically 0.1 µA
	10	µA max	85°C to 125°C
Power Dissipation[5]			
Normal Mode (Operational)	18	mW max	V_{DD} = 3.6 V , f_{SAMPLE} = 3 MSPS
	11.4	mW typ	V_{DD} = 3 V
Partial Power-Down	102	µW max	V_{DD} = 3 V
Full Power-Down	7.2	µW max	V_{DD} = 3.6 V, −40°C to +85°C

[1] Temperature range from −40°C to +125°C.
[2] Typical specifications are tested with V_{DD} = 3 V and V_{REF} = 3 V at 25°C.
[3] See the Terminology section.
[4] Guaranteed by characterization.
[5] See the Power vs. Throughput Rate section.

AD7273 SPECIFICATIONS

V_{DD} = 2.35 V to 3.6 V, V_{REF} = 2.35 V to V_{DD}, f_{SCLK} = 48 MHz, f_{SAMPLE} = 3 MSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	B Grade[1]	Unit[2]	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 1 MHz sine wave
Signal-to-Noise + Distortion (SINAD)[3]	61	dB min	
Total Harmonic Distortion (THD)[3]	−72	dB max	
	−77	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[3]	−80	dB typ	
Intermodulation Distortion (IMD)			
Second-Order Terms	−81	dB typ	fa = 1 MHz, fb = 0.97 MHz
Third-Order Terms	−81	dB typ	fa = 1 MHz, fb = 0.97 MHz
Aperture Delay	5	ns typ	
Aperture Jitter	18	ps typ	
Full Power Bandwidth	74	MHz typ	@ 3 dB
	10	MHz typ	@ 0.1 dB
Power Supply Rejection Ratio (PSRR)	82	dB typ	
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity[3]	±0.5	LSB max	
Differential Nonlinearity[3]	±0.5	LSB max	Guaranteed no missed codes to 10 bits
Offset Error[3]	±1	LSB max	
Gain Error[3]	±1.5	LSB max	
Total Unadjusted Error (TUE)[3]	±2.5	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to V_{REF}	V	
DC Leakage Current	±1	µA max	−40°C to +85°C
	±5.5	µA max	85°C to 125°C
Input Capacitance	42	pF typ	When in track
	10	pF typ	When in hold
REFERENCE INPUT			
V_{REF} Input Voltage Range	1.4 to V_{DD}	V min/V max	
DC leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
Input Impedance	32	Ω typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	1.7	V min	2.35 V ≤ V_{DD} ≤ 2.7 V
	2	V min	2.7 V < V_{DD} ≤ 3.6 V
Input Low Voltage, V_{IN}	0.7	V max	2.35 V ≤ V_{DD}< 2.7 V
	0.8	V max	2.7 V ≤ V_{DD} ≤ 3.6 V
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	2	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} − 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.35 V to 3.6 V
Output Low Voltage, V_{OL}	0.2	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±2.5	µA max	
Floating-State Output Capacitance[4]	4.5	pF max	
Output Coding	Straight (natural) binary		
CONVERSION RATE			
Conversion Time	250	ns max	12 SCLK cycles with SCLK at 48 MHz
Track-and-Hold Acquisition Time[3]	60	ns max	
Throughput Rate	3.45	MSPS max	See the Serial Interface section

Parameter	B Grade[1]	Unit[2]	Test Conditions/Comments
POWER RQUIREMENTS			
V_{DD}	2.35/3.6	V min/V max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	0.6	mA typ	V_{DD} = 3 V, SCLK on or off
Normal Mode (Operational)	5	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 3 MSPS
	3.2	mA typ	V_{DD} = 3 V
Partial Power-Down Mode (Static)	34	µA typ	
Full Power-Down Mode (Static)	2	µA max	−40°C to +85°C, typically 0.1 µA
	10	µA max	85°C to 125°C
Power Dissipation[5]			
Normal Mode (Operational)	18	mW max	V_{DD} = 3.6 V , f_{SAMPLE} = 3 MSPS
	9.6	mW typ	V_{DD} = 3 V
Partial Power-Down	102	µW max	V_{DD} = 3 V
Full Power-Down	7.2	µW max	V_{DD} = 3.6 V, −40°C to +85°C

[1] Temperature range from −40°C to +125°C.
[2] Typical specifications are tested with V_{DD} = 3 V and V_{REF} = 3 V at 25°C.
[3] See the Terminology section.
[4] Guaranteed by characterization.
[5] See the Power vs. Throughput Rate section.

TIMING SPECIFICATIONS

V_{DD} = 2.35 V to 3.6 V; V_{REF} = 2.35 to V_{DD}; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.[1] Guaranteed by characterization. All input signals are specified with tr = tf = 2 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX} AD7273/AD7274	Unit	Description
f_{SCLK}[2]	500	kHz min[3]	
	48	MHz max	
$t_{CONVERT}$	14 × t_{SCLK}		AD7274
	12 × t_{SCLK}		AD7273
t_{QUIET}	4	ns min	Minimum quiet time required between bus relinquish and start of next conversion
t_1	3	ns min	Minimum $\overline{CS}$ pulse width
t_2	6	ns min	$\overline{CS}$ to SCLK setup time
t_3[4]	4	ns max	Delay from $\overline{CS}$ until SDATA three-state disabled
t_4[4]	15	ns max	Data access time after SCLK falling edge
t_5	0.4 t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 t_{SCLK}	ns min	SCLK high pulse width
t_7[4]	5	ns min	SCLK to data valid hold time
t_8	14	ns max	SCLK falling edge to SDATA three-state
	5	ns min	SCLK falling edge to SDATA three-state
t_9	4.2	ns max	$\overline{CS}$ rising edge to SDATA three-state
$t_{POWER-UP}$[5]	1	µs max	Power-up time from full power-down

[1] Sample tested during initial release to ensure compliance. All timing specifications given are with a 10 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Minimum f_{SCLK} at which specifications are guaranteed.
[4] The time required for the output to cross the V_{IH} or V_{IL} voltage.
[5] See the Power-Up Times section

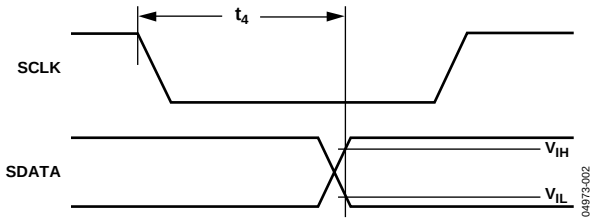


Figure 2. Access Time After SCLK Falling Edge

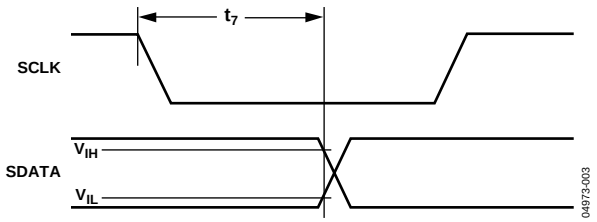


Figure 3. Hold Time After SCLK Falling Edge

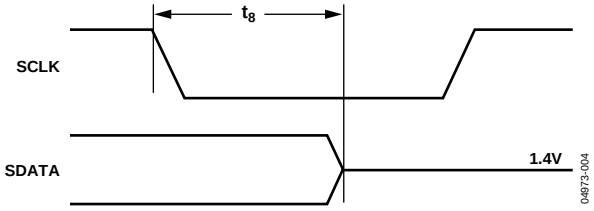


Figure 4. SCLK Falling Edge SDATA Three-State

TIMING EXAMPLES

For the AD7274, if $\overline{CS}$ is brought high during the 14th SCLK rising edge after the two leading zeros and 12 bits of the conversion are provided, the part can achieve the fastest throughput rate, 3 MSPS. If $\overline{CS}$ is brought high during the 16th SCLK rising edge after the two leading zeros, 12 bits of the conversion, and two trailing zeros are provided, a throughput rate of 2.97 MSPS is achievable. This is illustrated in the following two timing examples.

Timing Example 1

In Figure 6, using a 14 SCLK cycle, f_{SCLK} = 48 MHz, and the throughput is 3 MSPS. This produces a cycle time of $t_2 + 12.5(1/f_{SCLK}) + t_{ACQ}$ = 333 ns, where t_2 = 6 ns min and t_{ACQ} = 67 ns. This satisfies the requirement of 60 ns for t_{ACQ}. Figure 6 also shows that t_{ACQ} comprises $0.5(1/f_{SCLK}) + t_9 + t_{QUIET}$, where t_9 = 4.2 ns max. This allows a value of 52.8 ns for t_{QUIET}, satisfying the minimum requirement of 4 ns.

Timing Example 2

The example in Figure 7 uses a 16 SCLK cycle, f_{SCLK} = 48 MHz, and the throughput is 2.97 MSPS. This produces a cycle time of $t_2 + 12.5(1/f_{SCLK}) + t_{ACQ}$ = 336 ns, where t_2 = 6 ns min and t_{ACQ} = 70 ns. Figure 7 shows that t_{ACQ} comprises $2.5(1/f_{SCLK}) + t_8 + t_{QUIET}$, where t_8 = 14 ns max. This satisfies the minimum requirement of 4 ns for t_{QUIET}.

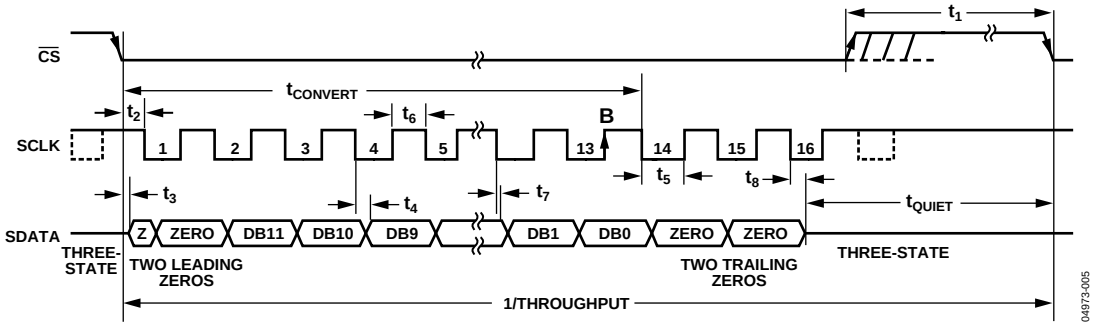


Figure 5. AD7274 Serial Interface Timing 16 SCLK Cycle

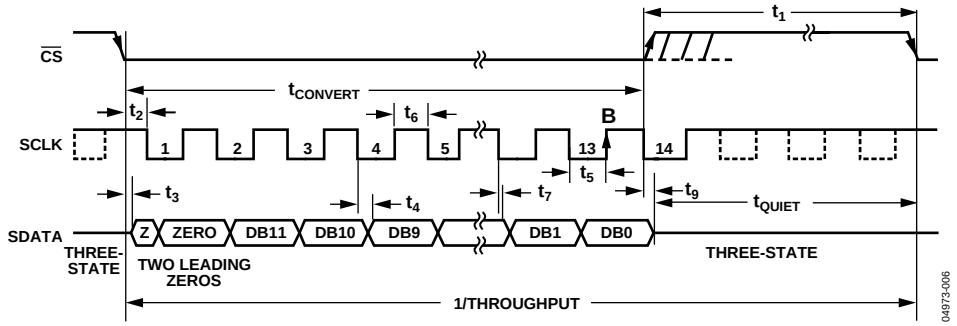


Figure 6.AD7274 Serial Interface Timing 14 SCLK Cycle

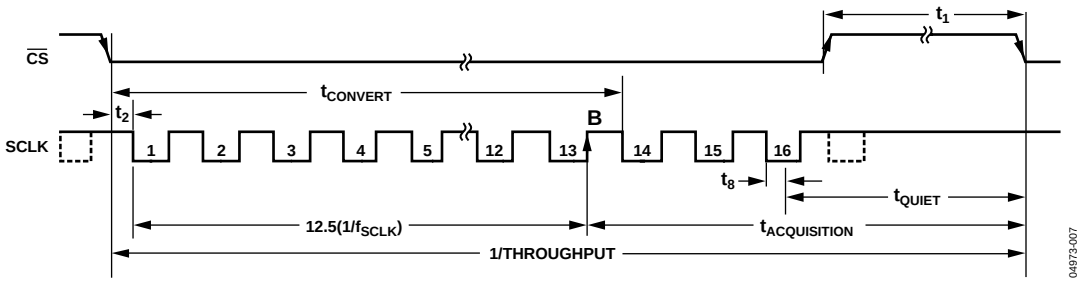


Figure 7. Serial Interface Timing 16 SCLK Cycle

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameters	Ratings
V_{DD} to AGND/DGND	−0.3 V to +6 V
Analog Input Voltage to AGND	−0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to +6 V
Digital Output Voltage to DGND	−0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	
Commercial (B Grade)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
6-Lead TSOT Package	
θ_{JA} Thermal Impedance	230°C/W
θ_{JC} Thermal Impedance	92°C/W
8-Lead MSOP Package	
θ_{JA} Thermal Impedance	205.9°C/W
θ_{JC} Thermal Impedance	43.74°C/W
Lead Temperature Soldering	
Reflow (10 to 30 sec)	255°C
Lead Temperature Soldering	
Reflow (10 to 30 sec)	260°C
ESD	1.5 kV

[1] Transient currents of up to 100 mA cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

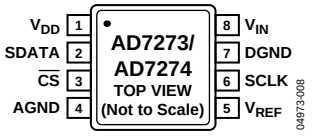


Figure 8. 8-Lead MSOP Pin Configuration

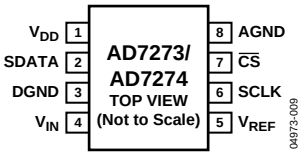


Figure 9. 8-Lead TSOT Pin Configuration

Table 6. Pin Function Descriptions

Pin No.			
MSOP	**TSOT**	**Mnemonic**	**Description**
1	1	V_{DD}	Power Supply Input. The V_{DD} range for the AD7273/AD7274 is from 2.35 V to 3.6 V.
2	2	SDATA	Data Out. Logic output. The conversion result from the AD7273/AD7274 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7274 consists of two leading zeros followed by the 12 bits of conversion data and two trailing zeros, provided MSB first. The data stream from the AD7273 consists of two leading zeros followed by the 10 bits of conversion data and four trailing zeros, provided MSB first.
3	7	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversion on the AD7273/AD7274 and framing the serial data transfer.
4	8	AGND	Analog Ground. Ground reference point for all circuitry on the AD7273/AD7274. All analog signals and any external reference signal should be referred to this AGND voltage.
5	5	V_{REF}	Voltage Reference Input. This pin becomes the reference voltage input. An external reference should be applied at this pin. The external reference input range is 1.4 V to V_{DD}. A 10 µF capacitor should be tied between this pin and AGND.
6	6	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the conversion process of AD7273/AD7274.
7	3	DGND	Digital Ground. Ground reference point for all digital circuitry on the AD7273/AD7274. The DGND and AGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
8	4	V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 to V_{REF}.

TYPICAL PERFORMANCE CHARACTERISTICS

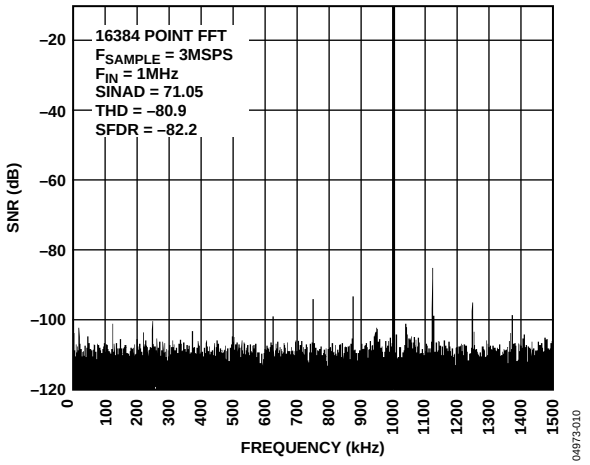


Figure 10. AD7274 Dynamic Performance at 3 MSPS, Input Tone = 1 MHz

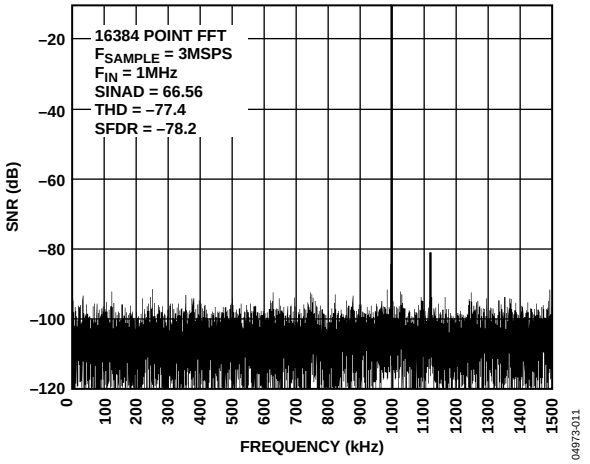


Figure 11. AD7273 Dynamic Performance at 3 MSP, Input Tone = 1 MHz

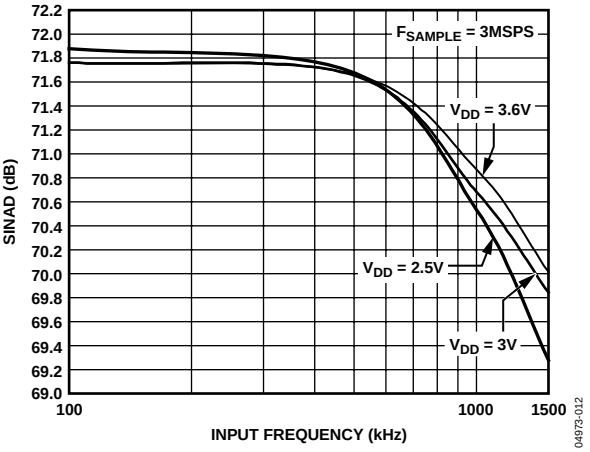


Figure 12. AD7274 SINAD vs. Analog Input Frequency at 3 MSPS for Various Supply Voltages, SCLK Frequency = 48 MHz

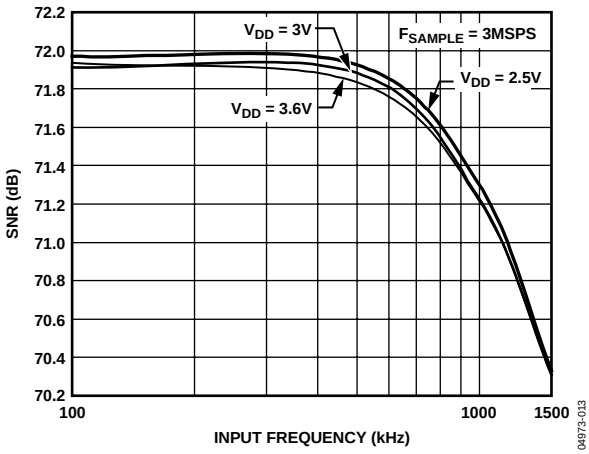


Figure 13. AD7274 SNR vs. Analog Input Frequency at 3 MSPS for Various Supply Voltages, SCLK Frequency = 48 MHz

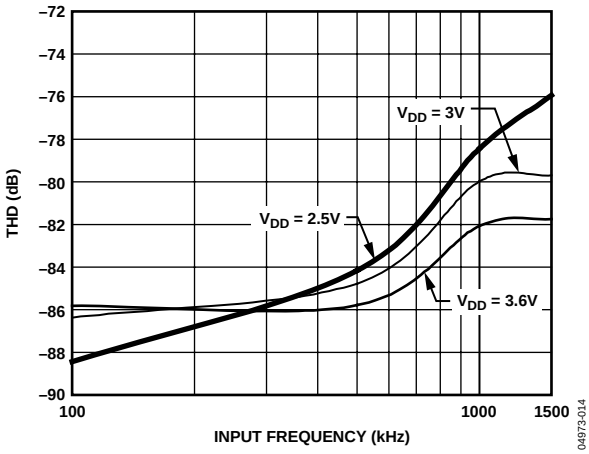


Figure 14. THD vs. Analog Input Frequency at 3 MSPS for Various Supply Voltages, SCLK Frequency = 48 MHz

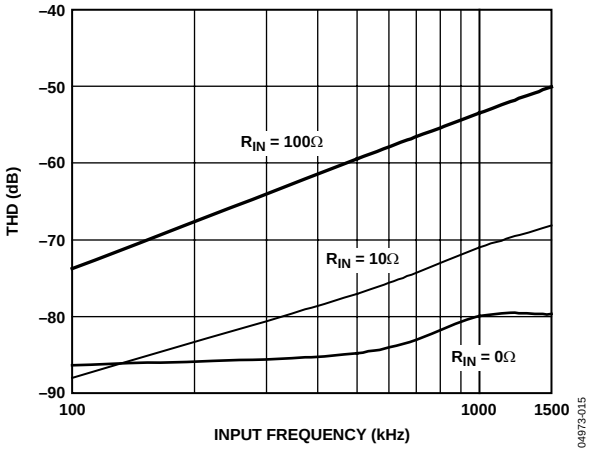


Figure 15. THD vs. Analog Input Frequency at 3 MSPS for Various Source Impedance, SCLK Frequency = 48 MHz, Supply Voltage = 3 V

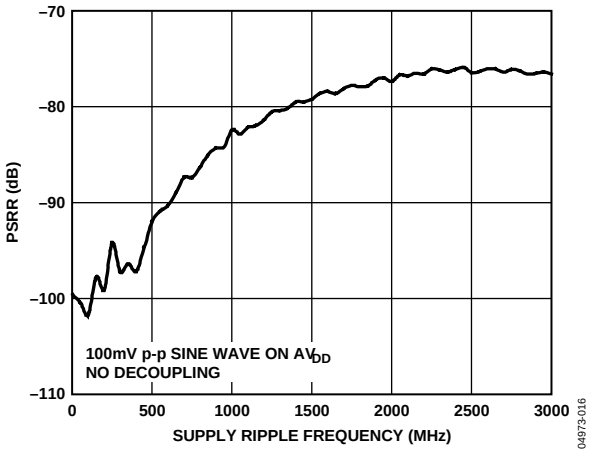


Figure 16. Power Supply Rejection Ratio (PSRR) vs. Supply Ripple Frequency Without Decoupling

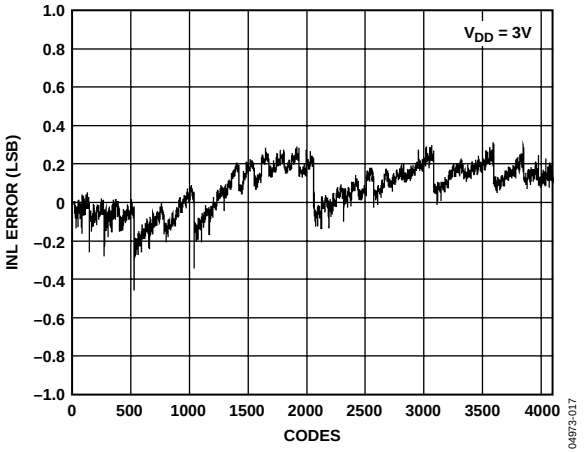


Figure 17. AD7274 INL Performance

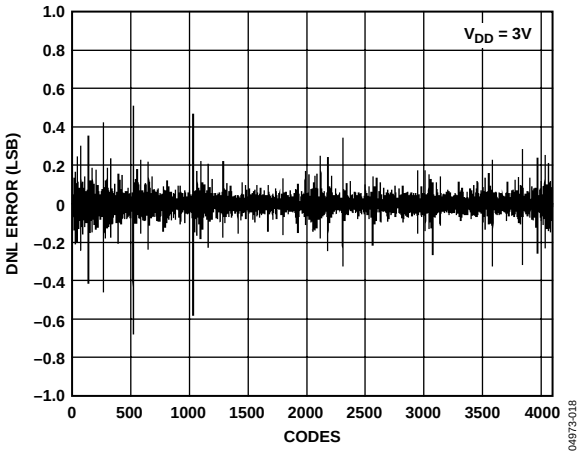


Figure 18. AD7274 DNL Performance

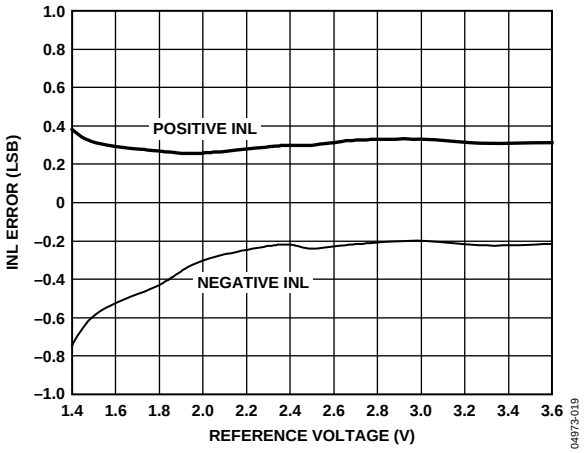


Figure 19. Change in INL vs. Reference Voltage, 3 V Supply

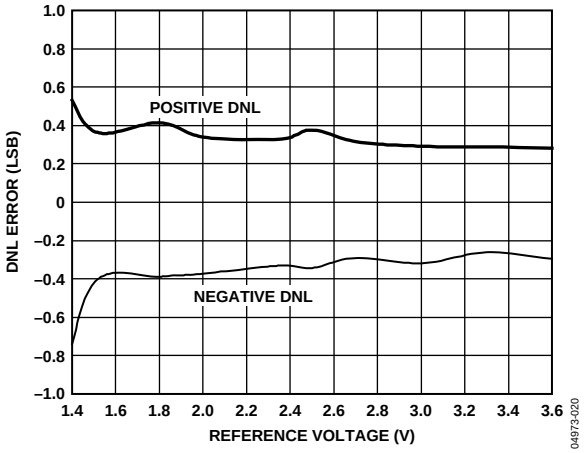


Figure 20. Change in DNL vs. Reference Voltage, 3 V Supply

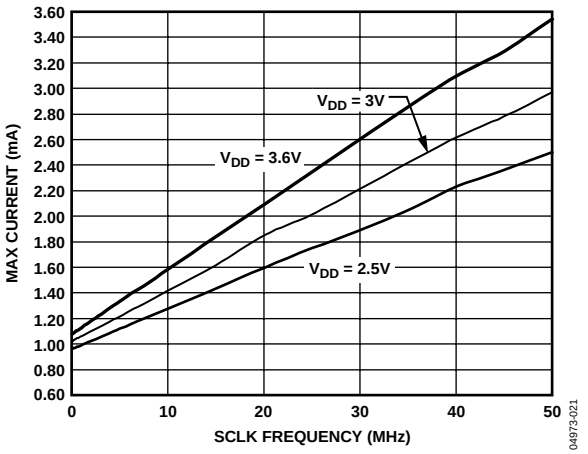


Figure 21. Maximum Current vs. Supply Voltage for Different SCLK Frequencies

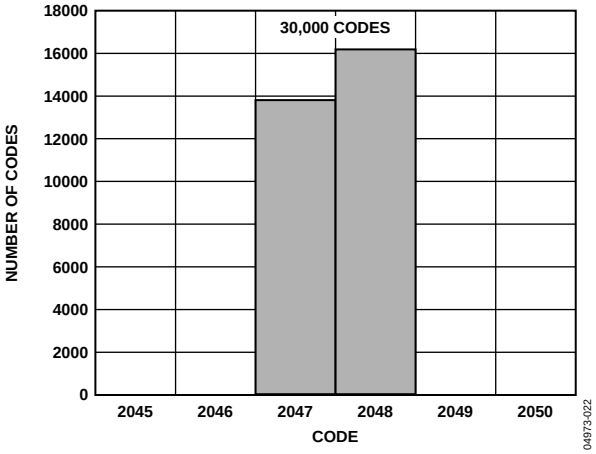


Figure 22. Histogram of Codes for 30,000 Samples

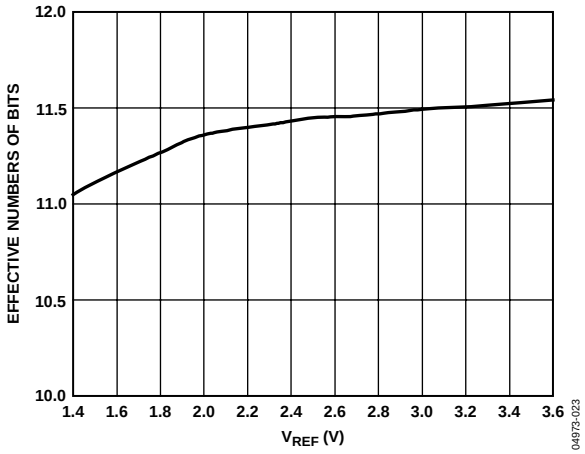


Figure 23. ENOB/SINAD vs. Reference Voltage

TERMINOLOGY

Integral Nonlinearity (INL)
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7273/AD7274, the endpoints of the transfer function are zero scale at 0.5 LSB below the first code transition and full scale at 0.5 LSB above the last code transition.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, that is, AGND + 0.5 LSB.

Gain Error
The deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal, that is, VREF – 1.5 LSB, after adjusting for the offset error.

Total Unadjusted Error (TUE)
A comprehensive specification that includes gain, linearity, and offset errors.

Track-and-Hold Acquisition Time
The time required for the output of the track-and-hold amplifier to reach its final value, within ±0.5 LSB, after the end of the conversion. See the Serial Interface section for more details.

Signal-to-Noise + Distortion Ratio (SINAD)
The measured ratio of signal to noise plus distortion at the output of the ADC. The signal is the rms amplitude of the fundamental, and noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), including harmonics but excluding dc. The ratio is dependent on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. For an ideal N-bit converter, the SINAD is

$$SINAD = 6.02\,N + 1.76\ \text{dB}$$

According to this equation, the SINAD is 74 dB for a 12-bit converter and 62 dB for a 10-bit converter. However, various error sources in the ADC, including integral and differential nonlinearities and internal ac noise sources, cause the measured SINAD to be less than its theoretical value.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. It is defined as:

$$THD\,(\text{dB}) = 20 \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental, and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise (SFDR)
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum; however, for ADCs with harmonics buried in the noise floor, it is determined by a noise peak.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, …. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7273/AD7274 are tested using the CCIF standard in which two input frequencies are used (see fa and fb in the Specifications section). In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Power Supply Rejection Ratio (PSRR)
The ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the ADC V_{DD} supply of frequency f_S.

$$PSRR\,(\text{dB}) = 10 \log \left(Pf / Pf_S\right)$$

where Pf is the power at frequency f in the ADC output; Pf_S is the power at frequency f_S coupled onto the ADC V_{DD} supply.

Aperture Delay
The measured interval between the leading edge of the sampling clock and the point at which the ADC actually takes the sample.

Aperture Jitter
The sample-to-sample variation in the effective point in time at which the sample is taken.

CIRCUIT INFORMATION

The AD7273/AD7274 are high speed, low power, 10-/12-bit, single supply ADCs, respectively. The parts can be operated from a 2.35 V to 3.6 V supply. When operated from any supply voltage within this range, the AD7273/AD7274 are capable of throughput rates of 3 MSPS when provided with a 48 MHz clock.

The AD7273/AD7274 provide the user with an on-chip track-and-hold ADC and a serial interface housed in an 8-lead TSOT or an 8-lead MSOP package, which offers the user considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the part and provides the clock source for the successive approximation ADC. The analog input range is 0 to V_{REF}. An external reference in the range of 1.4 V to V_{DD} is required by the ADC.

The AD7273/AD7274 also feature a power-down option to save power between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7273/AD7274 are successive approximation ADCs based on a charge redistribution DAC. Figure 24 and Figure 25 show simplified schematics of the ADC. Figure 24 shows the ADC during its acquisition phase, where SW2 is closed, SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{IN}.

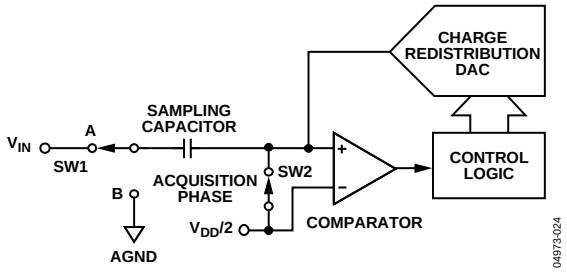


Figure 24. ADC Acquisition Phase

When the ADC starts a conversion, SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced (see Figure 25). The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 26 shows the ADC transfer function.

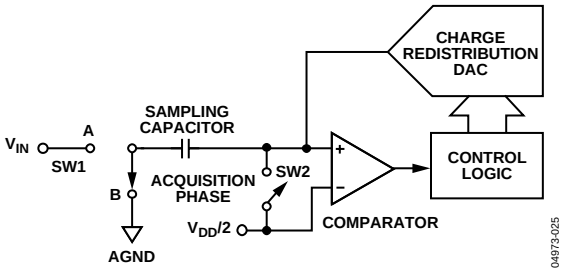


Figure 25. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7273/AD7274 is straight binary. The designed code transitions occur midway between successive integer LSB values, such as 0.5 LSB and 1.5 LSB. The LSB size is V_{REF}/4,096 for the AD7274 and V_{REF}/1,024 for the AD7273. The ideal transfer characteristic for the AD7273/AD7274 is shown in Figure 26.

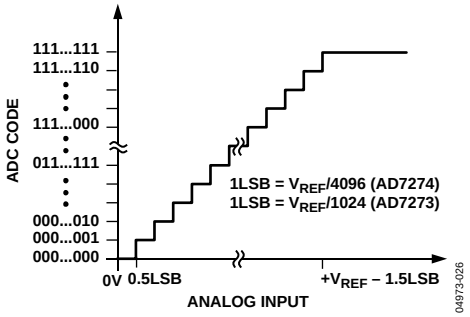


Figure 26. AD7273/AD7274 Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 27 shows a typical connection diagram for the AD7273/AD7274. An external reference must be applied to the ADC. This reference can be in the range of 1.4 V to V_{DD}. A precision reference, such as the REF19x family or the ADR421, can be used to supply the reference voltage to the AD7273/AD7274.

The conversion result is output in a 16-bit word with two leading zeros followed by the 12-bit or 10-bit result. The 12-bit result from the AD7274 is followed by two trailing zeros, and the 10-bit result from the AD7273 is followed by four trailing zeros.

Table 7 provides some typical performance data with various references under the same setup conditions for the AD7274.

Table 7. AD7274 Performance (Various Voltage Reference IC)

Voltage Reference	AD7274 SNR Performance 1 MHz Input
AD780 @ 2.5 V	71.3 dB
AD780 @ 3 V	70.1 dB
REF195	70.9 dB

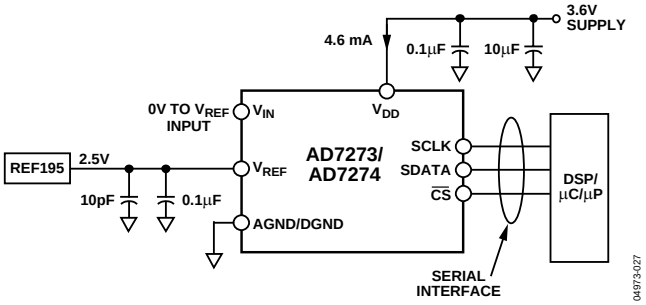


Figure 27. AD7273/AD7274 Typical Connection Diagram

ANALOG INPUT

Figure 28 shows an equivalent circuit of the analog input structure of the AD7273/AD7274. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300 mV. Signals exceeding this value cause these diodes to become forward biased and to start conducting current into the substrate. These diodes can conduct a maximum current of 10 mA without causing irreversible damage to the part. Capacitor C1 in Figure 28 is typically about 4 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 75 Ω. Capacitor C2 is the ADC sampling capacitor and has a capacitance of 32 pF typically. For ac applications, removing high frequency components from the analog input signal is recommended by using a band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADCs. This may necessitate the use of an input buffer amplifier. The AD8021 op amp is compatible with this device; however, the choice of the op amp is a function of the particular application.

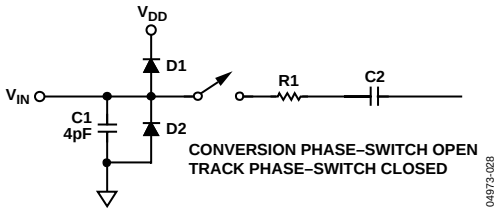


Figure 28. Equivalent Analog Input Circuit

When no amplifier is used to drive the analog input, the source impedance should be limited to a low value. The maximum source impedance depends on the amount of THD that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 14 shows a graph of the THD vs. the analog input frequency for different source impedances when using a supply voltage of 3 V and sampling at a rate of 3 MSPS.

DIGITAL INPUTS

The digital inputs applied to the AD7273/AD7274 are not limited by the maximum ratings that limit the analog inputs. Instead, the digital inputs can be applied at up to 6 V and are not restricted by the V_{DD} + 0.3 V limit of the analog inputs. For example, if the AD7273/AD7274 were operated with a V_{DD} of 3 V, then 5 V logic levels could be used on the digital inputs. However, it is important to note that the data output on SDATA still has 3 V logic levels when V_{DD} = 3 V. Another advantage of SCLK and $\overline{CS}$ not being restricted by the V_{DD} + 0.3 V limit is that power supply sequencing issues are avoided. For example, unlike with the analog inputs, with the digital inputs, if $\overline{CS}$ or SCLK are applied before V_{DD}, there is no risk of latch-up.

MODES OF OPERATION

The mode of operation of the AD7273/AD7274 is selected by controlling the logic state of the $\overline{CS}$ signal during a conversion. There are three possible modes of operation: normal mode, partial power-down mode, and full power-down mode. The point at which $\overline{CS}$ is pulled high after the conversion is initiated determines which power-down mode, if any, the device enters. Similarly, if the device is already in power-down mode, $\overline{CS}$ can control whether the device returns to normal operation or remains in power-down mode. These modes of operation are designed to provide flexible power management options, which can be chosen to optimize the power dissipation/throughput rate ratio for different application requirements.

NORMAL MODE

This mode is intended for fastest throughput rate performance because the AD7273/AD7274 remain fully powered at all times, eliminating worry about power-up times. Figure 29 shows the general diagram of the operation of the AD7273/AD7274 in this mode.

The conversion is initiated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure that the part remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 SCLK falling edges elapse after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling, but before the 16th SCLK falling edge, the part remains powered up, but the conversion is terminated, and SDATA goes back into three-state.

For the AD7274, a minimum of 14 serial clock cycles are required to complete the conversion and access the complete conversion result. For the AD7273, a minimum of 12 serial clock cycles are required to complete the conversion and access the complete conversion result.

$\overline{CS}$ can idle high until the next conversion or low until $\overline{CS}$ returns high before the next conversion (effectively idling $\overline{CS}$ low). Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

PARTIAL POWER-DOWN MODE

This mode is intended for use in applications where slower throughput rates are required. An example of this is when either the ADC is powered down between each conversion or a series of conversions is performed at a high throughput rate and then the ADC is powered down for a relatively long duration between these bursts of several conversions.

When the AD7273/AD7274 are in partial power-down mode, all analog circuitry is powered down except the bias generation circuit.

To enter partial power-down mode, interrupt the conversion process by bringing $\overline{CS}$ high between the second and 10th falling edges of SCLK, as shown in Figure 30. Once $\overline{CS}$ is brought high in this window of SCLKs, the part enters partial power-down mode, the conversion that was initiated by the falling edge of $\overline{CS}$ is terminated, and SDATA goes back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This prevents accidental power-down due to glitches on the $\overline{CS}$ line.

To exit this mode of operation and power up the AD7274/AD7273, perform a dummy conversion. On the falling edge of $\overline{CS}$, the device begins to power up and continues to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device is fully powered up once 16 SCLKs elapse; valid data results from the next conversion, as shown in Figure 31. If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, the AD7274/AD7273 goes into full power-down mode. Therefore, although the device may begin to power up on the falling edge of $\overline{CS}$, it powers down on the rising edge of $\overline{CS}$ as long as this occurs before the 10th SCLK falling edge.

If the AD7273/AD7274 is already in partial power-down mode and $\overline{CS}$ is brought high before the 10th falling edges of SCLK, the device enters full power-down mode. For more information on the power-up times associated with partial power-down mode in various configurations, see the Power-Up Times section.

FULL POWER-DOWN MODE

This mode is intended for use in applications where throughput rates slower than those in the partial power-down mode are required, because power-up from a full power-down takes substantially longer than that from a partial power-down. This mode is suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and thus power-down.

When the AD7273/AD7274 are in full power-down mode, all analog circuitry is powered down. To enter full power-down mode put the device into partial power-down mode by bringing $\overline{CS}$ high between the second and 10th falling edges of SCLK. In the next conversion cycle, interrupt the conversion process in the way shown in Figure 32 by bringing $\overline{CS}$ high before the 10th SCLK falling edge. Once $\overline{CS}$ is brought high in this window of SCLKs, the part powers down completely. Note that it is not necessary to complete 16 SCLKs once $\overline{CS}$ is brought high to enter either of the power-down modes. Glitch protection is not available when entering full power-down mode.

To exit full power-down mode and power up the AD7273/AD7274 again, perform a dummy conversion, similar to when powering up from partial power-down mode. On the falling

edge of $\overline{CS}$, the device begins to power up and continues to power up until after the falling edge of the 10th SCLK as long as $\overline{CS}$ is held low. The power-up time required must elapse before a conversion can be initiated, as shown in Figure 33. See the Power-Up Times section for the power-up times associated with the AD7273/AD7274.

POWER-UP TIMES

The AD7273/AD7274 has two power-down modes, partial power-down and full power-down, which are described in detail in the Modes of Operation section. This section deals with the power-up time required when coming out of either of these modes.

To power up from partial power-down mode, one cycle is required. Therefore, with a SCLK frequency of up to 48 MHz, one dummy cycle is sufficient to allow the device to power up from partial power-down mode. Once the dummy cycle is complete, the ADC is fully powered up and the input signal is acquired properly. The quiet time, t_{QUIET}, must be allowed from the point where the bus goes back into three-state after the dummy conversion to the next falling edge of $\overline{CS}$.

To power up from full power-down, approximately 1 μs should be allowed from the falling edge of $\overline{CS}$, shown in Figure 33 as $t_{POWER-UP}$. Note that during power-up from partial power-down mode, the track-and-hold, which is in hold mode while the part is powered down, returns to track mode after the first SCLK edge is received after the falling edge of $\overline{CS}$. This is shown as Point A in Figure 31.

When power supplies are first applied to the AD7273/AD7274, the ADC can power up in either of the power-down modes or in normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure that the part is fully powered up before attempting a valid conversion. Likewise, if the part is to be kept in partial power-down mode immediately after the supplies are applied, two dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th SCLK falling edge (see Figure 29). In the second cycle, $\overline{CS}$ must be brought high between the second and 10th SCLK falling edges (see Figure 30).

Alternatively, if the part is to be placed into full power-down mode after the supplies are applied, three dummy cycles must be initiated. The first dummy cycle must hold $\overline{CS}$ low until after the 10th SCLK falling edge (see Figure 29); the second and third dummy cycles place the part into full power-down mode (see Figure 32). See also the Modes of Operation section.

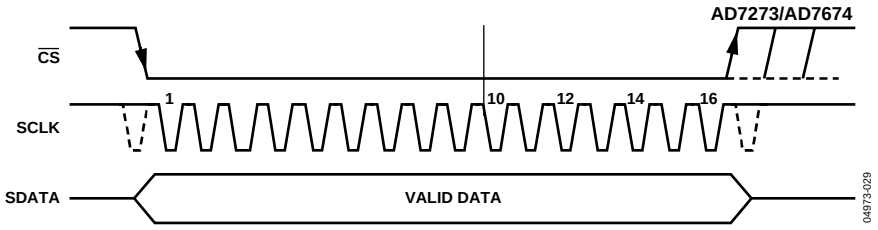


Figure 29. Normal Mode Operation

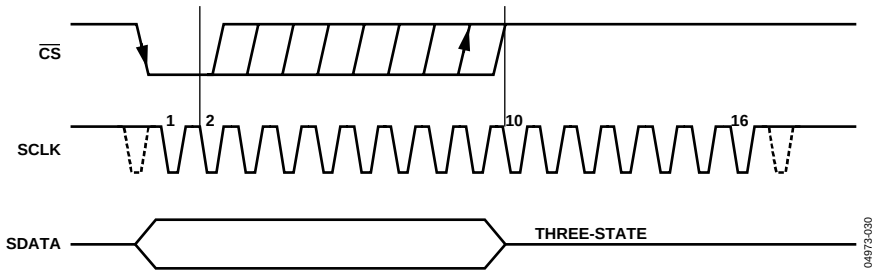


Figure 30. Entering Partial Power-Down Mode

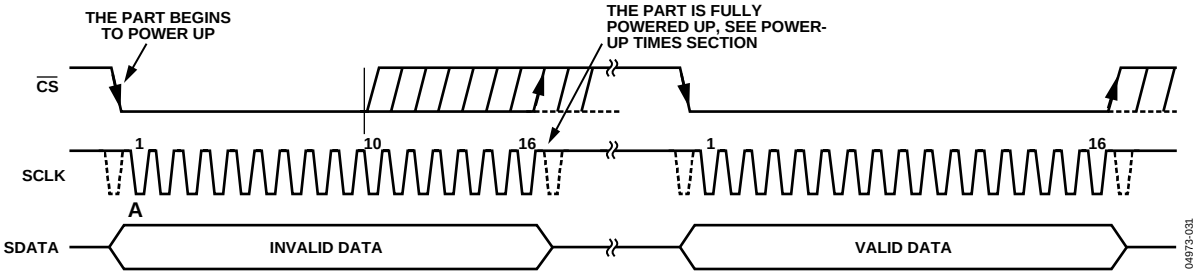


Figure 31. Exiting Partial Power-Down Mode

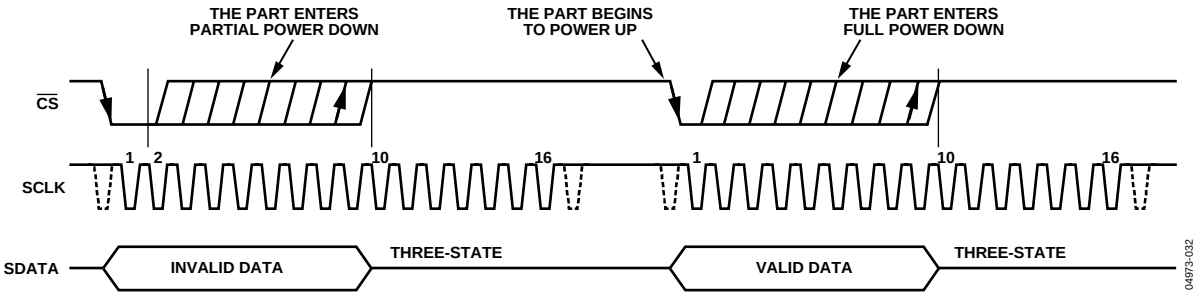


Figure 32. Entering Full Power-Down Mode

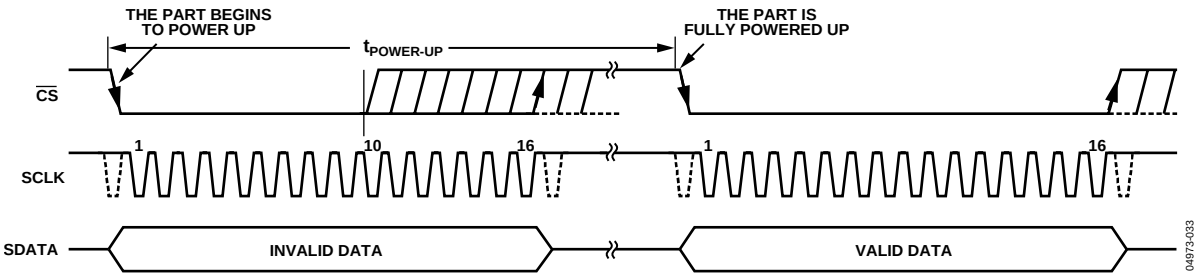


Figure 33. Exiting Full Power-Down Mode

POWER VS. THROUGHPUT RATE

Figure 34 shows the power consumption of the device in normal mode, in which the part is never powered down. By using the power-down mode of the AD7273/AD7274 when not performing a conversion, the average power consumption of the ADC decreases as the throughput rate decreases.

Figure 35 shows that as the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption over time drops accordingly. For example, if the AD7273/AD7274 are operated in continuous sampling mode with a throughput rate of 200 kSPS and a SCLK of 48 MHz (V_{DD} = 3 V) and the devices are placed into power-down mode between conversions, the power consumption is calculated as follows. The power dissipation during normal operation is 11.6 mW (V_{DD} = 3 V). If the power-up time is one dummy cycle, that is, 333 ns, and the remaining conversion time is 290 ns, the AD7273/AD7274 can be said to dissipate 11.6 mW for 623 ns during each conversion cycle. If the throughput rate is 200 kSPS, the cycle time is 5 µs and the average power dissipated during each cycle is 623/5,000 × 9.6 mW = 1.42 mW. Figure 35 shows the power vs. throughput rate when using the partial power-down mode between conversions at 3 V. The power-down mode is intended for use with throughput rates of less than 600 kSPS, because at higher sampling rates there is no power saving achieved by using the power-down mode.

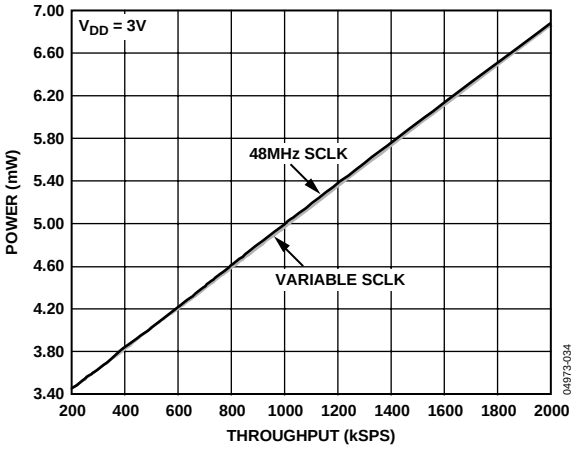


Figure 34. Power vs. Throughput, Normal Mode

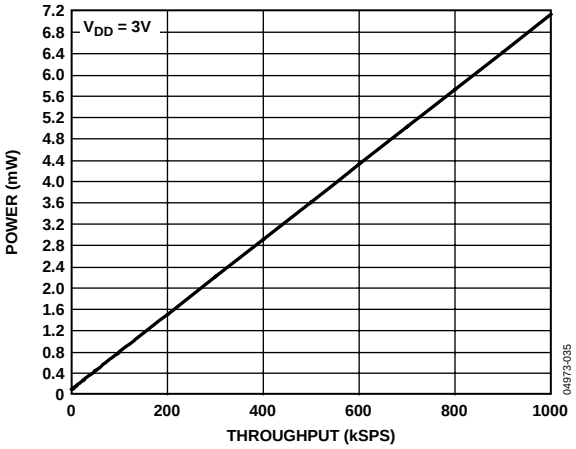


Figure 35. Power vs. Throughput, Partial Power-Down Mode

SERIAL INTERFACE

Figure 36 through Figure 38 show the detailed timing diagrams for serial interfacing to the AD7274 and AD7273, respectively. The serial clock provides the conversion clock and controls the transfer of information from the AD7273/AD7274 during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode and takes the bus out of three-state. The analog input is sampled and the conversion is initiated at this point.

For the AD7274, the conversion requires completing 14 SCLK cycles. Once 13 SCLK falling edges have elapsed, the track-and-hold goes back into track mode on the next SCLK rising edge, as shown in Figure 36 at Point B. If the rising edge of $\overline{CS}$ occurs before 14 SCLKs have elapsed, the conversion is terminated and the SDATA line goes back into three-state. If 16 SCLKs are considered in the cycle, the last two bits are zeros and SDATA returns to three-state on the 16th SCLK falling edge, as shown in Figure 37.

For the AD7273, the conversion requires completing 12 SCLK cycles. Once 11 SCLK falling edges elapse, the track-and-hold goes back into track mode on the next SCLK rising edge, as shown in Figure 38 at Point B. If the rising edge of $\overline{CS}$ occurs before 12 SCLKs elapse, the conversion is terminated and the SDATA line goes back into three-state. If 16 SCLKs are considered in the cycle, the AD7273 clocks out four trailing zeros for the last four bits and SDATA returns to three-state on the 16th SCLK falling edge, as shown in Figure 38.

If the user considers a 14-SCLK cycle serial interface for the AD7273/AD7274, $\overline{CS}$ must be brought high after the 14th SCLK falling edge. Then the last two trailing zeros are ignored, and SDATA goes back into three-state. In this case, the 3 MSPS throughput can be achieved by using a 48 MHz clock frequency.

$\overline{CS}$ going low clocks out the first leading zero to be read by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with the second leading zero. Therefore, the first falling clock edge on the serial clock provides the first leading zero and clocks out the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, because it is clocked out on the previous (15th) falling edge.

In applications with a slower SCLK, it is possible to read data on each SCLK rising edge. In such cases, the first falling edge of SCLK clocks out the second leading zero and can be read on the first rising edge. However, the first leading zero clocked out when $\overline{CS}$ goes low is missed if read within the first falling edge. The 15th falling edge of SCLK clocks out the last bit and can be read on the 15th rising SCLK edge.

If $\overline{CS}$ goes low just after one SCLK falling edge elapses, $\overline{CS}$ clocks out the first leading zero and can be read on the SCLK rising edge. The next SCLK falling edge clocks out the second leading zero and can be read on the following rising edge.

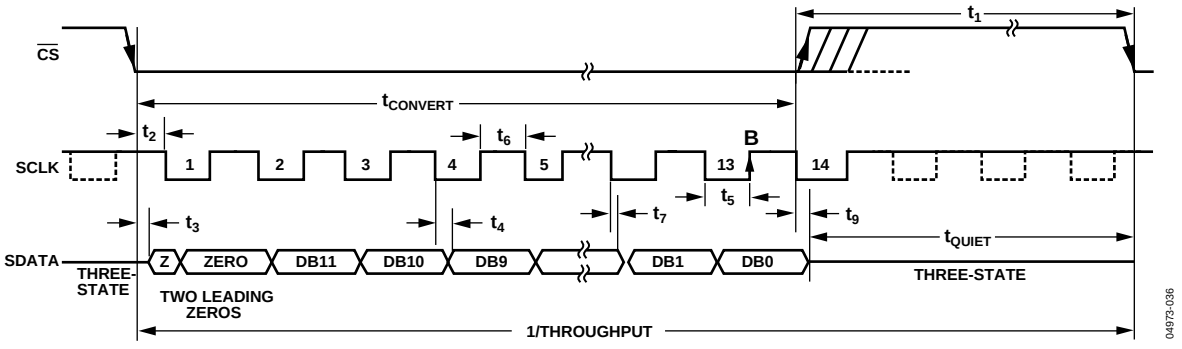


Figure 36. AD7274 Serial Interface Timing Diagram 14 SCLK Cycle

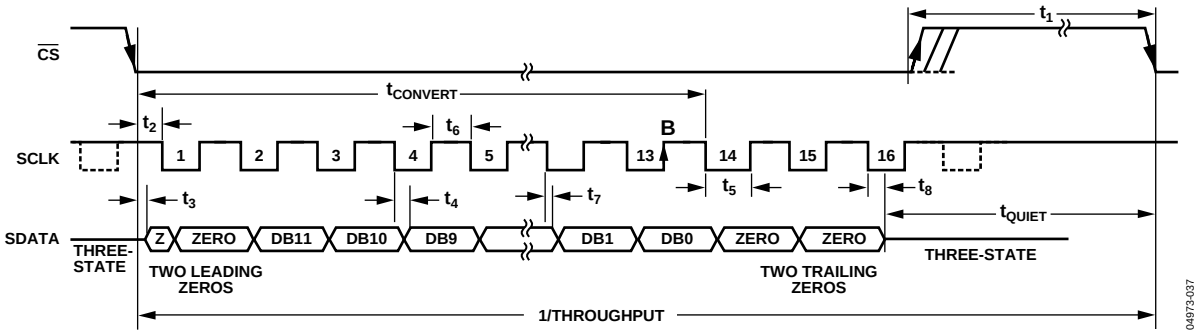


Figure 37. AD7274 Serial Interface Timing Diagram 16 SCLK Cycle

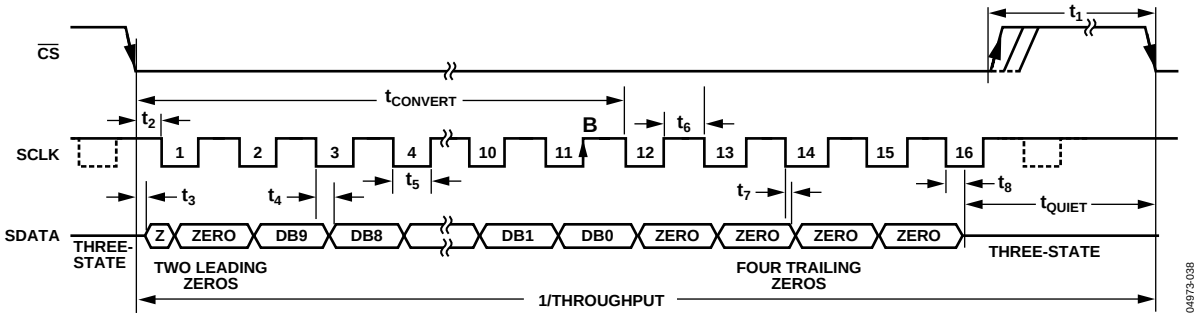


Figure 38. AD7273 Serial Interface Timing Diagram

MICROPROCESSOR INTERFACING

AD7273/AD7274 to ADSP-BF53x

The ADSP-BF53x family of DSPs interfaces directly to the AD7273/AD7274 without requiring glue logic. The SPORT0 Receive Configuration 1 register should be set up as outlined in Table 8.

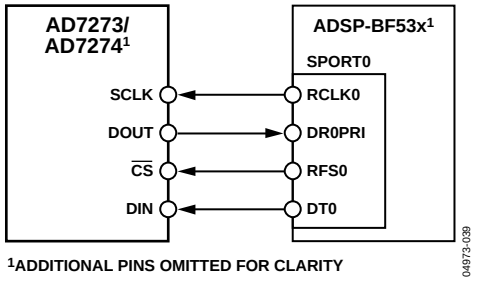


Figure 39. Interfacing to the ADSP-BF53x

Table 8. The SPORT0 Receive Configuration 1 Register (SPORT0_RCR1)

Setting	Description
RCKFE = 1	Sample data with falling edge of RSCLK
LRFS = 1	Active low frame signal
RFSR = 1	Frame every word
IRFS = 1	Internal RFS used
RLSBIT = 0	Receive MSB first
RDTYPE = 00	Zero fill
IRCLK = 1	Internal receive clock
RSPEN = 1	Receive enabled
SLEN = 1111	16-bit data-word (or can be set to 1101 for a 14-bit data-word)
TFSR = RFSR = 1	

To implement the power-down modes, set SLEN to 1001 to issue an 8-bit SCLK burst.

APPLICATION HINTS

GROUNDING AND LAYOUT

The printed circuit board that houses the AD7273/AD7274 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates using ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All AGND pins of the AD7273/AD7274 should be sunk into the AGND plane. Digital and analog ground planes should be joined in only one place. If the AD7273/AD7274 are in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at only one point, a star ground point, established as close as possible to the ground pin on the AD7273/AD7274.

Avoid running digital lines under the device, because this couples noise onto the die. However, the analog ground plane should be allowed to run under the AD7273/AD7274 to avoid noise coupling. The power supply lines to the AD7273/AD7274 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, components with fast-switching signals, such as clocks, should be shielded with digital ground, and they should never be run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feedthrough within the board, traces on opposite sides of the board should run at right angles to each other. A microstrip technique is by far the best method, but it is not always possible to use this approach with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the solder side.

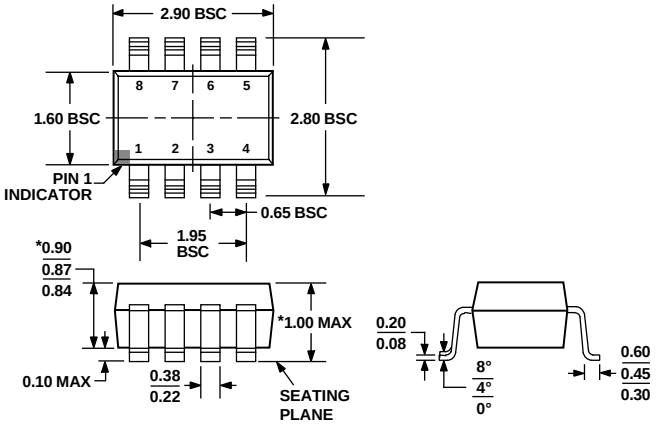
Good decoupling is also important. All analog supplies should be decoupled with 10 μF ceramic capacitors in parallel with 0.1 μF capacitors to AGND/DGND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 μF capacitors should have low effective series resistance (ESR) and low effective series inductance (ESI), such as is typical of common ceramic or surface-mount types of capacitors. Capacitors with low ESR and low ESI provide a low impedance path to ground at high frequencies, which allows them to handle transient currents due to internal logic switching.

EVALUATING THE AD7273/AD7274 PERFORMANCE

The recommended layout for the AD7273/AD7274 is outlined in the evaluation board documentation. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the evaluation board controller. The evaluation board controller can be used in conjunction with the AD7273/AD7274 evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7273/AD7274.

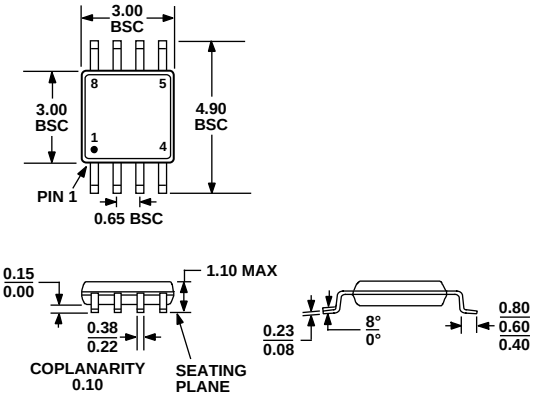
The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7273/AD7274. The software and documentation are on a CD shipped with the evaluation board.

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-193-BA WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 40. 8-Lead Thin Small Outline Transistor Package [TSOT] (UJ-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 41. 8-Lead Mini Small Outline Package [MSOP] (RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Description	Package Option	Branding
AD7274BRM	−40°C to +125°C	±1 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C1V
AD7274BRMZ[2]	−40°C to +125°C	±1 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C34
AD7274BRMZ-REEL[2]	−40°C to +125°C	±1 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C34
AD7274BUJ-500RL7	−40°C to +125°C	±1 max	8-Lead Mini Small Outline Package (MSOP)	UJ-8	C1V
AD7274BUJZ-500RL7[2]	−40°C to +125°C	±1 max	8-Lead Thin Small Outline Transistor Package (TSOT)	UJ-8	C34
AD7274BUJZ-REEL7[2]	−40°C to +125°C	±1 max	8-Lead Thin Small Outline Transistor Package (TSOT)	UJ-8	C34
AD7273BRMZ[2]	−40°C to +125°C	±0.5 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C33
AD7273BRMZ-REEL[2]	−40°C to +125°C	±0.5 max	8-Lead Mini Small Outline Package (MSOP)	RM-8	C33
AD7273BUJ-REEL7	−40°C to +125°C	±0.5 max	8-Lead Thin Small Outline Transistor Package (TSOT)	UJ-8	C1U
AD7273BUJZ-500RL7[2]	−40°C to +125°C	±0.5 max	8-Lead Thin Small Outline Transistor Package (TSOT)	UJ-8	C33
EVAL-AD7274CB[3]			Evaluation Board		
EVAL-AD7273CB[3]			Evaluation Board		
EVAL-CONTROL BRD2[4]			Control Board		

[1] Linearity error refers to integral nonlinearity.
[2] Z = Pb-free part.
[3] This can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL board for evaluation/demonstration purposes.
[4] This board is a complete unit that allows a PC to control and communicate with all Analog Devices evaluation boards that end in a CB designator. To order a complete evaluation kit, the particular ADC evaluation board (such as EVAL-AD7273CB/AD7274CB), the EVAL-CONTROL BRD2, and a 12 V transformer must be ordered. See the relevant evaluation board technical note for more information.

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D04973–0–9/05(0)

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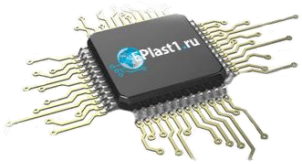
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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