# Three Channel, Three Level, High Speed Ultrasound Driver IC

## Features

- Advanced CMOS technology
- 4.5 to 12.5V power supply voltage
- 2.0A output source and sink current
- 6.5ns rise and fall time with 1.0nF load
- 10ns propagation delay
- ±2ns matched delay times
- 12 matched channels
- 1.8 to 3.3V CMOS logic interface
- Smart logic threshold
- Low inductance package

## Applications

- Medical ultrasound imaging
- Piezoelectric transducer drivers
- Metal flaw detection
- Non-Destructive Testing (NDT)

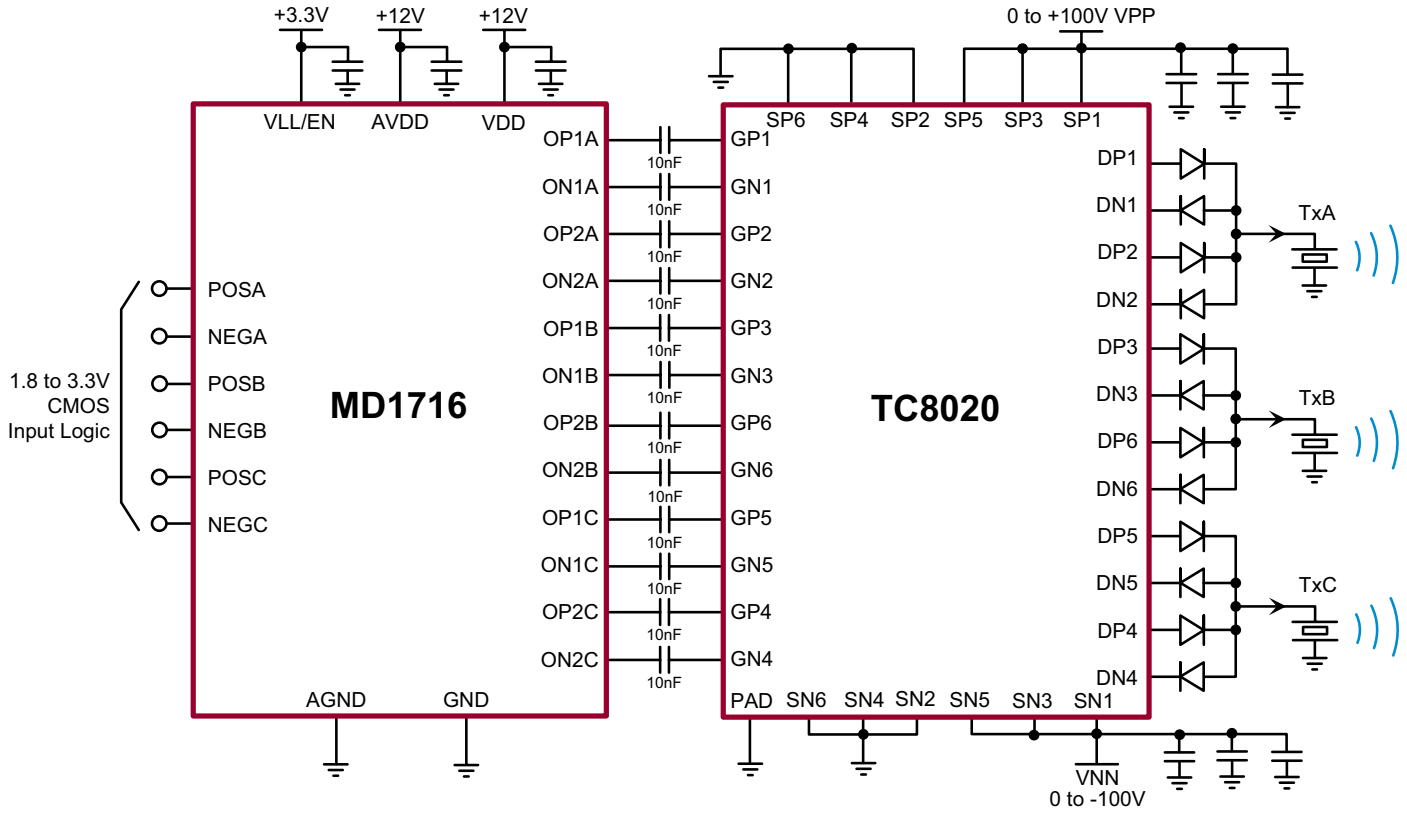
## General Description

The Supertex MD1716, paired with the Supertex TC8020, forms a three channel, three level, high voltage, high speed, transmit pulser chip set. The chip set is designed for medical ultrasound imaging applications but can also be used for metal flaw detection, Non-Destructive Testing (NDT), and piezoelectric transducer drivers.

The MD1716 is a three channel logic controller circuit with 12 low impedance MOSFET gate drivers. There are three sets of control logic inputs, one each for channels A, B and C. Each channel consists of two pairs of MOSFET gate drivers. These drivers are designed to match the gate driving requirements of the Supertex TC8020.

The TC8020 is the high voltage output stage of the pulser. It consists of six pairs of MOSFETs. Each pair has both an N- and P-channel MOSFET. They are designed to have the same impedance and can provide typical peak currents of ±3.5 amps.

## Typical Application Circuit



## Ordering Information

| Device | Package Option |
|---|---|
| | **40-Lead QFN**<br>***6.00x6.00mm body***<br>***1.00mm height (max)***<br>***0.50mm pitch*** |
| MD1716 | MD1716K6-G |

*-G indicates package is RoHS compliant ('Green')*

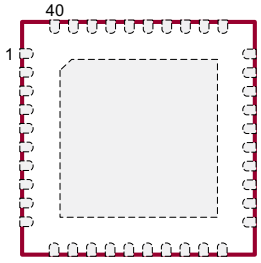
## Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| GND and AGND, Ground | 0V |
| $V_{LL}$ logic input pin | -0.5V to +5.5V |
| $AV_{DD}1$, $V_{DD}1$, positive gate drive supply | -0.5V to +14.5V |
| $V_{DD}2$, positive gate drive supply | -0.5V to +14.5V |
| Storage temperature | -65°C to 150°C |
| Power dissipation | 1.3W |

*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

** 1.0oz 4-layer 3x4" PCB*

## Pin Configuration




**40-Lead QFN (K6)**
***(top view)***

## Package Marking


L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
____ = "Green" Packaging

*Package may or may not include the following marks: Si or*

**40-Lead QFN (K6)**

## Operating Supply Voltages

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{LL}$ | Logic supply | 1.8 | 3.3 | 3.6 | V | --- |
| $AV_{DD}$ | Positive analog supply | 4.75 | - | 12.9 | V | $AV_{DD} \geq V_{DD}$ |
| $V_{DD}$ | Positive gate drive supply | 4.75 | - | 12.9 | V | --- |

## Operating Supply Current

*(Over operating conditions unless otherwise specified, $V_{LL}$ = 3.3V, $AV_{DD}$ = $V_{DD}$ = +12V, $T_A$ = 25°C)*

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_{VLL}$ | Logic reference current | - | 10 | - | µA | $V_{LL}$ = 3.3V |
| $I_{AVDDQ}$ | $AV_{DD}$ power down current | - | 400 | - | µA | EN = 0, all inputs Low. |
| $I_{VDDQ}$ | $V_{DD}$ power down current | - | 50 | 100 | | |
| $I_{AVDDEN}$ | $AV_{DD}$ power up current | - | 2.0 | 3.0 | mA | EN = 1, all inputs Low. |
| $I_{VDDEN}$ | $V_{DD}$ power up current | - | 0.7 | 1.0 | mA | |
| $I_{AVDDCW}$ | $AV_{DD}$ CW 5.0MHz current | - | 10 | - | mA | All channels on at 5.0MHz, No load.<br>$V_{DD}$ = 5.0V |
| $I_{VDDCW}$ | $V_{DD}$ CW 5.0MHz current | - | 33 | - | | |

## AC Electrical Characteristics

*(Over operating conditions unless otherwise specified, $V_{LL}$ = 3.3V, $AV_{DD}$ = $V_{DD}$ = +12V, $T_A$ = 25°C)*

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $t_{irf}$ | Input rise & fall time | - | - | 10 | ns | Logic input edge speed requirement |
| $t_r$ | Output rise time | - | 6.5 | - | ns | 1.0nF load, see timing diagram, input signal rise/fall time 2.0ns |
| $t_f$ | Output fall time | - | 6.5 | - | ns | |
| $t_{dr}$ | Output rise delay | - | 10 | - | ns | 1.0nF load, see timing diagram, input signal rise/fall time 2.0ns |
| $t_{df}$ | Output fall delay | - | 10 | - | ns | |
| $\|t_r - t_f\|$ | Rise and fall time matching | - | 1.0 | - | - | For each channel |
| $\|t_{dr} - t_{df}\|$ | Propagation delay matching | - | 1.0 | - | - | |
| $t_{dm}$ | Delay time matching | - | ±2.0 | - | ns | Channel to Channel and Device to Device |
| $\Delta t_j$ | Output jitter | - | 20 | - | ps | $V_{DD}$ = 10V |
| $t_{EN\_ON}$ | IC enable time | - | - | 50 | µs | --- |
| $t_{EN\_OFF}$ | IC disable time | - | - | 2.0 | µs | --- |

## P-Channel Gate Driver Outputs

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $R_{SINK}$ | Output sink resistance | - | - | 6.0 | Ω | $I_{SINK}$ = 100mA |
| $R_{SOURCE}$ | Output source resistance | - | - | 6.0 | Ω | $I_{SOURCE}$ = 100mA |
| $I_{SINK}$ | Peak output sink current | 1.7 | 2.0 | - | A | --- |
| $I_{SOURCE}$ | Peak output source current | 1.7 | 2.0 | - | A | --- |

## N-Channel Gate Driver Outputs

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $R_{SINK}$ | Output sink resistance | - | 3.0 | 6.0 | Ω | $I_{SINK}$ = 100mA |
| $R_{SOURCE}$ | Output source resistance | - | 4.0 | 6.0 | Ω | $I_{SOURCE}$ = 100mA |
| $I_{SINK}$ | Peak output sink current | 1.7 | 2.0 | - | A | --- |
| $I_{SOURCE}$ | Peak output source current | 1.7 | 2.0 | - | A | --- |

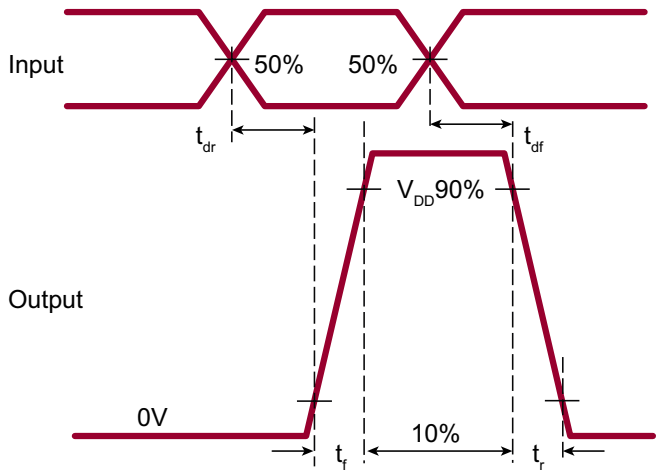
## Logic Inputs

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{ENL}$ | Chip disable low voltage | 0 | - | 0.3 | V | VLL/EN is a dual function pin |
| $V_{IH}$ | Input logic high voltage | $0.8V_{LL}$ | - | $V_{LL}$ | V | --- |
| $V_{IL}$ | Input logic low voltage | 0 | - | $0.2V_{LL}$ | V | --- |
| $I_{IH}$ | Input logic high current | - | - | 1.0 | µA | --- |
| $I_{IL}$ | Input logic low current | -1.0 | - | - | µA | --- |

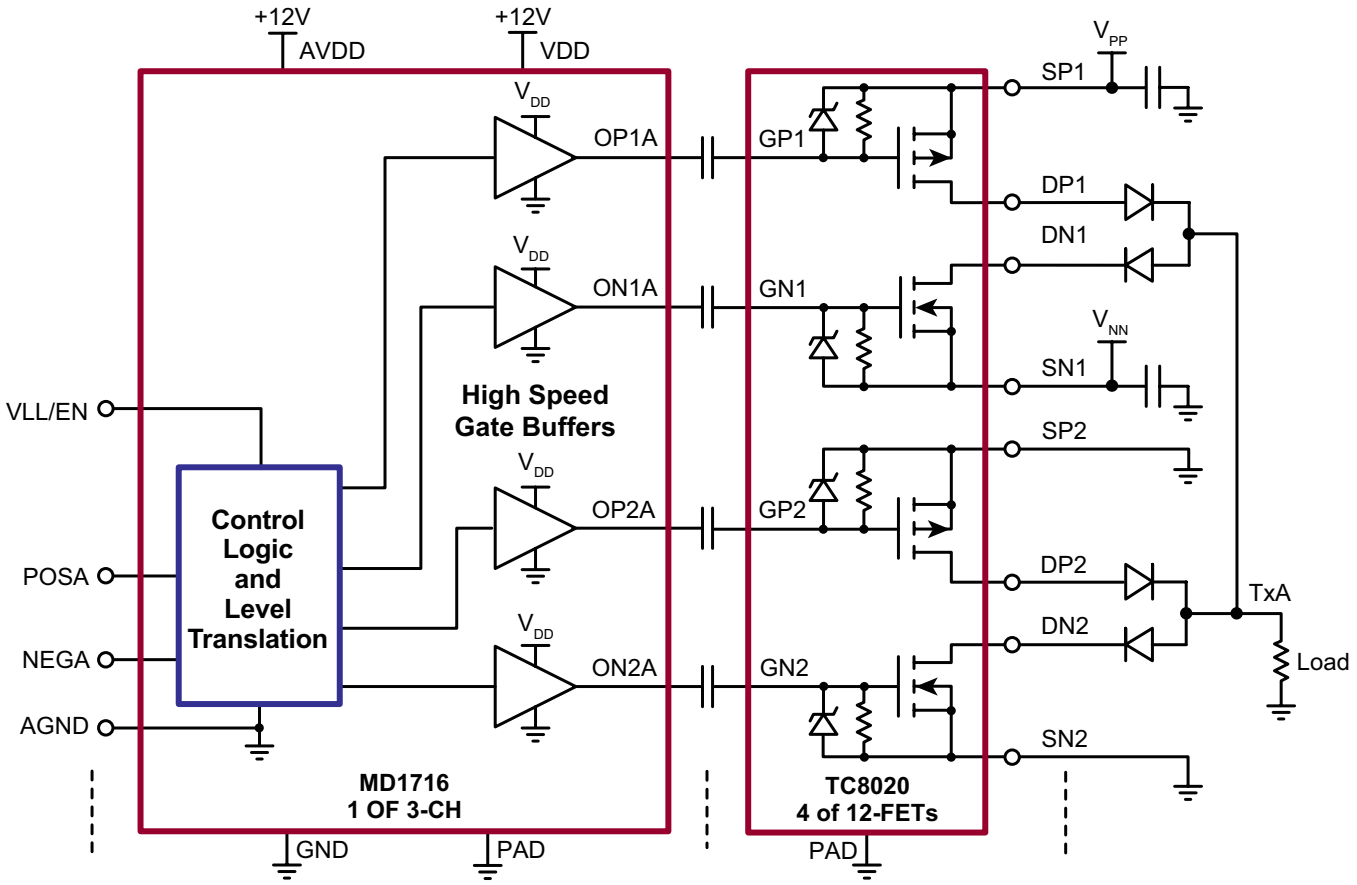
## Truth Table

| EN | Logic Inputs A | | SP1 to DP1 | SN1 to DN1 | SP2 to DP2 | SN2 to DN2 |
|---|---|---|---|---|---|---|
| | POSA | NEGA | | | | |
| 1 | 0 | 0 | OFF | OFF | **ON** | **ON** |
| 1 | 0 | 1 | OFF | **ON** | OFF | OFF |
| 1 | 1 | 0 | **ON** | OFF | OFF | OFF |
| 1 | 1 | 1 | OFF | OFF | OFF | OFF |
| **EN** | **Logic Inputs B** | | **SP3 to DP3** | **SN3 to DN3** | **SP6 to DP6** | **SN6 to DN6** |
| | **POSB** | **NEGB** | | | | |
| 1 | 0 | 0 | OFF | OFF | **ON** | **ON** |
| 1 | 0 | 1 | OFF | **ON** | OFF | OFF |
| 1 | 1 | 0 | **ON** | OFF | OFF | OFF |
| 1 | 1 | 1 | OFF | OFF | OFF | OFF |
| **EN** | **Logic Inputs C** | | **SP5 to DP5** | **SN5 to DN5** | **SP4 to DP4** | **SN4 to DN4** |
| | **POSC** | **NEGC** | | | | |
| 1 | 0 | 0 | OFF | OFF | **ON** | **ON** |
| 1 | 0 | 1 | OFF | **ON** | OFF | OFF |
| 1 | 1 | 0 | **ON** | OFF | OFF | OFF |
| 1 | 1 | 1 | OFF | OFF | OFF | OFF |
| 0 | X | X | OFF | OFF | OFF | OFF |
| 0→1 | 0 | 0 | EN transitions from low to high or high to low should occur at all logic inputs low. | | | |
| 1→0 | 0 | 0 | | | | |

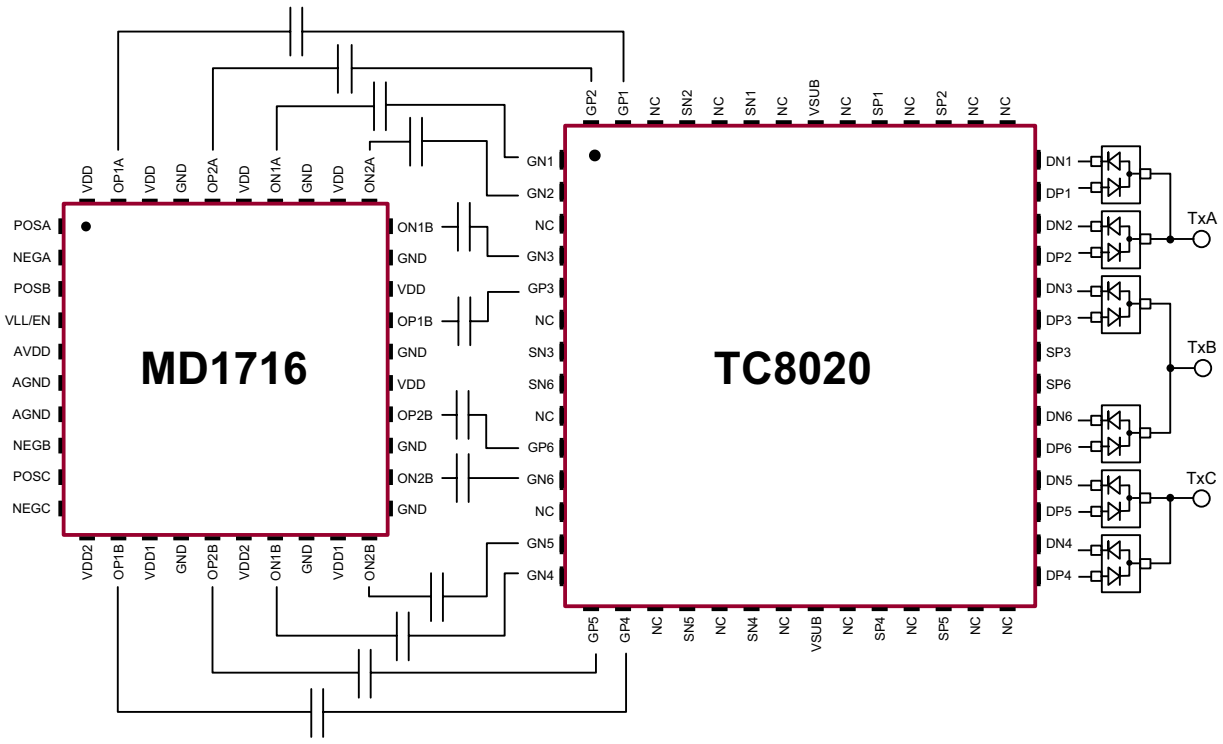
## Timing Diagram



## Detail Circuit




## Circuit Pin Layout



## Pin Description

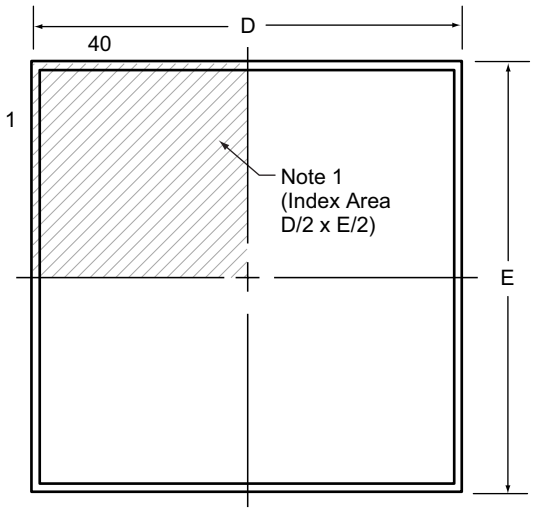
| Pin # | Name | Description |
|---|---|---|
| 1 | POSA | POS input logic control for channel A. See logic truth table for details. |
| 2 | NEGA | NEG input logic control for channel A. See logic truth table for details. |
| 3 | POSB | POS input logic control for channel B. See logic truth table for details. |
| 4 | VLL/EN | Logic Hi reference voltage and chip enable input. |
| 5 | AVDD | Positive supply voltage of analog circuitry. AVDD should be same or higher potential than the VDD. |
| 6 | AGND | Digital ground, and connection of IC substrate. |
| 7 | AGND | |
| 8 | NEGB | NEG input logic control for channel B. See logic truth table for details. |
| 9 | POSC | POS input logic control for channel C. See logic truth table for details. |
| 10 | NEGC | NEG input logic control for channel C. See logic truth table for details. |
| 11 | VDD | Positive supply voltage of the gate drivers for the output stage in A, B and C channels. |
| 12 | OP2C | Damping P-Channel gate drivers for channel C. |
| 13 | VDD | Positive supply voltage of the gate drivers for the output stage in A, B and C channels. |
| 14 | GND | Power Ground. |
| 15 | OP1C | High Voltage Output P-Channel gate drivers for channel C. |
| 16 | VDD | Positive supply voltage of the gate drivers for the output stage in A, B and C channels. |
| 17 | ON2C | Damping N-Channel gate drivers for channel C. |
| 18 | GND | Power Ground. |
| 19 | VDD | Positive supply voltage of the gate drivers for the output stage in A, B and C channels. |
| 20 | ON1C | High Voltage Output N-Channel gate drivers for channel C. |
| 21 | GND | Power Ground. |
| 22 | ON2B | Damping N-Channel gate drivers for channel B. |
| 23 | GND | Power Ground. |
| 24 | OP2B | Damping P-Channel gate drivers for channel B. |
| 25 | VDD | Positive supply voltage of the gate drivers for the output stage in A, B and C channels. |
| 26 | GND | Power Ground. |
| 27 | OP1B | High Voltage Output P-Channel gate drivers for channel B. |
| 28 | VDD | Positive supply voltage of the gate drivers for the output stage in A, B and C channels. |
| 29 | GND | Power Ground. |
| 30 | ON1B | High Voltage Output N-Channel gate drivers for channel B. |
| 31 | ON2A | Damping N-Channel gate drivers for channel A. |
| 32 | VDD | Positive supply voltage of the gate drivers for the output stage in A, B and C channels. |
| 33 | GND | Power Ground. |

## Pin Description *(cont.)*

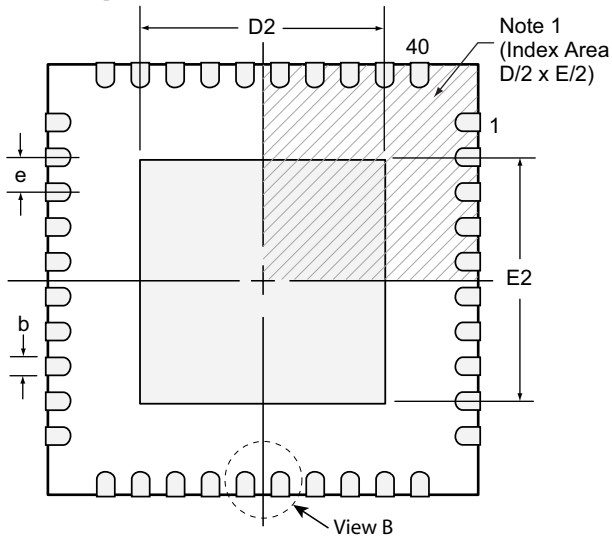
| Pin # | Name | Description |
|---|---|---|
| 34 | ON1A | High Voltage Output N-Channel gate drivers for channel A. |
| 35 | VDD | Positive supply voltage of the gate drivers for the output stage in A, B and C channels. |
| 36 | OP2A | Damping P-Channel gate drivers for channel A. |
| 37 | GND | Power Ground. |
| 38 | VDD | Positive supply voltage of the gate drivers for the output stage in A, B and C channels. |
| 39 | OP1A | High Voltage Output P-Channel gate drivers for channel A. |
| 40 | VDD | Positive supply voltage of the gate drivers for the output stage in A, B and C channels. |
| Center Pad | Thermal pad | IC substrate, must connect to GND externally. |

# 40-Lead QFN Package Outline (K6)

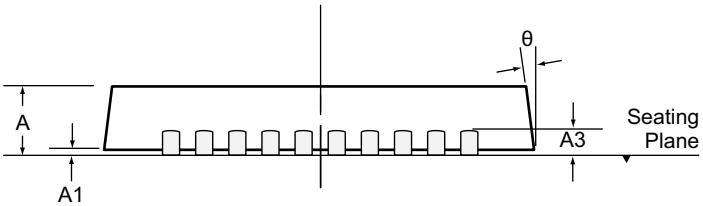
***6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch***



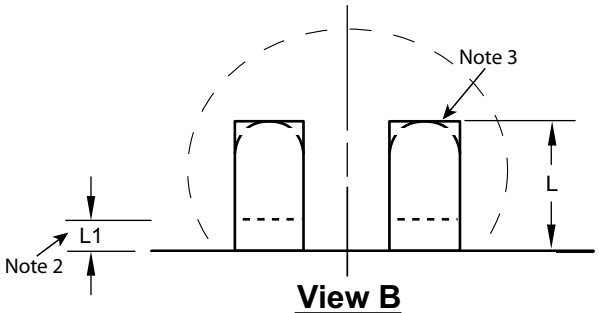

**Top View**




**Bottom View**




**Side View**




**View B**

***Notes:***

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

| Symbol | | A | A1 | A3 | b | D | D2 | E | E2 | e | L | L1 | θ° |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (mm) | MIN | 0.80 | 0.00 | 0.20 REF | 0.18 | 5.85* | 1.05 | 5.85* | 1.05 | 0.50 BSC | 0.30† | 0.00 | 0 |
| | NOM | 0.90 | 0.02 | | 0.25 | 6.00 | - | 6.00 | - | | 0.40† | - | - |
| | MAX | 1.00 | 0.05 | | 0.30 | 6.15* | 4.45 | 6.15* | 4.45 | | 0.50† | 0.15 | 14 |

*JEDEC Registration MO-220, Variation VJJD-6, Issue K, June 2006.*
** This dimension is not specified in the JEDEC drawing.*
*† This dimension differs from the JEDEC drawing.*
***Drawings not to scale.***
***Supertex Doc. #:*** *DSPD-40QFNK66X6P050, Version C041009.*

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)*



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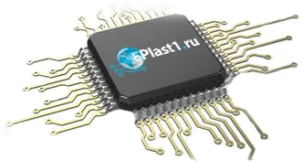
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.




**Как с нами связаться**

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