LTC2107 and LTC6409 16-Bit, 210Msps ADC with DC-Coupled Driver

DESCRIPTION

Demonstration circuit 2266A features the LTC®2107, 210Msps ADC, and the LTC6409 low noise amplifier. DC2266A supports the LTC2107 DDR LVDS output mode.

The circuitry on the analog inputs is optimized for analog input frequencies from DC to 100MHz. When driven with a 50Ω source, the gain will be 6dB. To modify the input for other input ranges or gains refer to the LTC6409 data sheet.

Design files for this circuit board are available at http://www.linear.com/demo/DC2266A

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage – LTC2107 (V_{IN})	This Supply Must Provide Up to 800mA	3.3		5.0	V
Supply Voltage – LTC6409 ($AMPV_{CC}$)	This Supply Must Provide Up to 75mA	3.3		5.0	V
Analog Input Range	Depending on PGA Setting	1.6		2.4	V_{P-P}
Maximum Input Level at J1 and J2	$2.4V_{P-P}$ Input Range			1.2	V_{P-P}
	$1.6V_{P-P}$ Input Range			0.8	V_{P-P}
Logic Input Voltages	Minimum Logic High	1.2			V
	Maximum Logic Low			0.6	V
Logic Output Voltages (Differential)	Nominal Logic Levels (100Ω Load, 3.5mA Mode, 1.25V Common Mode)		0.350		V
	Minimum Logic Levels (100Ω Load, 3.5mA Mode, 1.25V Common Mode)	0.247			V
Sampling Frequency (Encode Clock Frequency)		10		210	MHz
Convert Clock Level (Single ended)	Minimum Logic Levels (ENC^- Tied to GND)	0		2.5	V
Convert Clock Level (Differential)	Minimum Logic Levels (ENC^- Not Tied to GND, 1.2V Common Mode)	0.2			V

QUICK START PROCEDURE

The DC2266A is easy to set up to evaluate the performance of the LTC2107 A/D converter. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below.

The DC1371 Data Acquisition and Collection System was supplied with the DC2266A board. Follow the DC1371 Quick Start Guide to install the required software and for connecting the DC1371 to the DC2266A and to a PC.

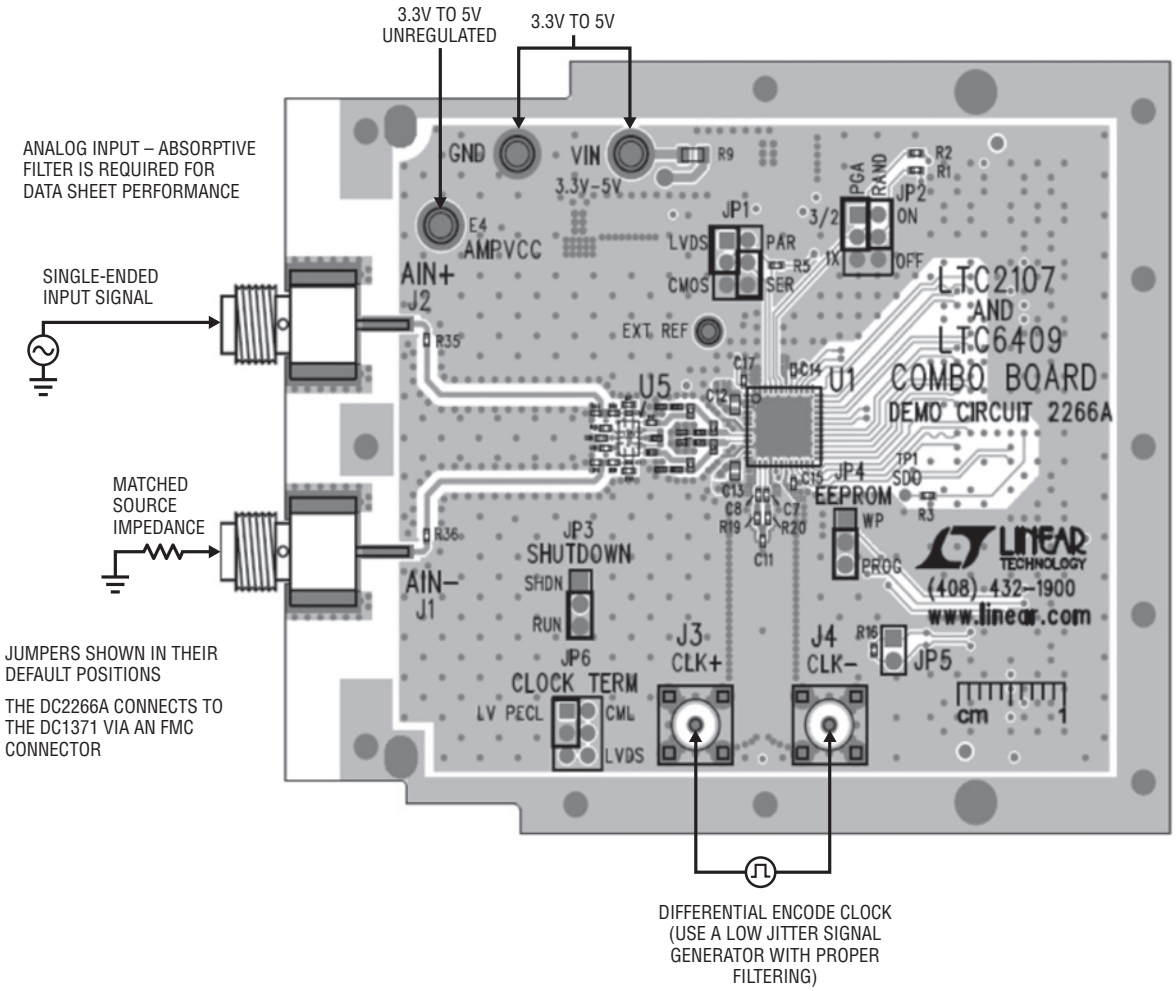


Figure 1. DC2266A Setup (Zoom for Detail)

HARDWARE SETUP

SMAS

J1 AIN–: Negative Analog Input. Apply a signal to J1 from a 50Ω driver. Absorptive filters are required for optimum performance. Terminate this channel to an impedance that matches J2 when using a single-ended input on J2. If J1 is being driven single-ended, a matching impedance should be connected on the input J2 for proper balance.

J2 AIN+: Positive Analog Input. Apply a signal to J2 from a 50Ω driver. Absorptive filters are required for optimum performance. For a single-ended signal, a matching impedance should be connected on the input J1 for proper balance. Use this channel when using a single-ended input.

J3 and J4: Encode Clock Input for Differential Signals. By default, the DC2266A is designed to be driven with a differential clock source connected to J3 and J4. The jumper position on JP6 can be changed to provide termination for various signaling standards.

TURRETS

VIN: Positive Input Voltage for the ADC and Digital Buffers. This voltage feeds a regulator that supplies the proper voltages for the ADC and buffers. The voltage range for this turret is 3.3V to 5V.

AMPVCC: Positive Input Voltage for the LTC6409. This voltage is unregulated and powers the amplifier directly. The voltage range for this turret is 3.3V to 5V.

EXT REF: Optional Reference Voltage. This pin is connected directly to the SENSE pin of the ADC. Connect EXT REF to a 1.25V external reference and the external reference mode is automatically selected. The external reference must be 1.25V ± 25mV for proper operation. If no external voltage is supplied, this pin will be pulled up to 2.5V through a weak pull-up resistor.

GND: Ground Connection. This demo board only has a single ground plane. This turret should be tied to the GND terminal of the power supply being used.

JUMPERS

The DC2266A demonstration circuit should have the following jumper settings as default positions (see Figure 1) which configure the ADC in Serial programming mode. In the default configuration, JP1-JP2 should be left in the default locations. This will pull PAR/SER low, and the required pins high through weak pull-up resistors so the SPI commands can be sent from the PC. If JP1 is set to PAR then jumpers JP1-JP2 can be configured manually.

JP1: PAR/SER: Selects Parallel or Serial programming mode (Default: Serial).

CMOS/LVDS: In Serial programming mode (SER), this pin should be in the LVDS position to allow serial data transfer (Default: LVDS or up). In the Parallel programming mode (PAR), this pin controls the digital output mode. When this pin is in the CMOS position, the full-rate CMOS output mode is enabled. When this pin is in the LVDS position, the double data rate LVDS output mode (with 3.5mA output current) is enabled. Note: when using the DC1371, Parallel mode DDR LVDS must be selected.

JP2: PGA: In Serial programming mode (SER), this pin is pulled high through a weak pull-up resistor to allow serial data transfer. In the Parallel programming mode (PAR), this pin controls the programmable gain amplifier front-end (PGA). In the 1x jumper position, a front-end gain of 1x is selected, ADC input range of $2.4V_{P-P}$. This allows $1.2V_{P-P}$ to be presented at the input of the amplifier. In the 3/2 jumper position, a front-end gain of 1.5x is selected, ADC input range of $1.6V_{P-P}$ which allows $0.8V_{P-P}$ to be presented at the input of the amplifier (Default: 3/2 or up).

RAND: In Serial programming mode (SER), this pin is pulled high through a weak pull-up resistor to allow serial data transfer. In the Parallel programming mode (PAR), this pin becomes the digital output randomization control bit. When this pin is in the OFF position, digital output randomization is disabled. When this pin is in the ON position, digital output randomization is enabled. To decode the randomized data, exclusive-OR each bit with the least significant bit. This is done for you in PScope™ when the randomizer option is enabled (Default: ON or up).

HARDWARE SETUP

JP3: Shutdown: In the RUN position, this results in normal operation of the ADC. In the SHDN position, the ADC is powered down and the digital outputs are set in a high impedance state (Default: RUN or down).

JP4: EEPROM: EEPROM Write Protect. For factory use only. Should be left in the enable (PROG) position.

JP5: Overflow Test Point: This is a test point for the differential overflow signal. This jumper can be installed to provide a convenient way to probe the overflow signal (Default: removed).

JP6: Clock Term: This jumper provides termination voltages for various signaling standards. LVPECL, CML, and LVDS termination voltages can be selected. The selected voltage is then used to terminate the clock input through 50Ω resistors. By removing the jumper completely, an external voltage can be applied directly to pin 5 of JP6 so an arbitrary signaling scheme can be used (Default: LVPECL).

APPLYING POWER AND SIGNALS TO THE DC2266A

If a DC1371 is used to acquire data from the DC2266A, the DC1371 must FIRST be connected to a powered USB port and provided an external 5V BEFORE applying +3.3V to +5.0V across the pins marked VIN, AMPVCC and GND on the DC2266A. Regulators on the board produce the voltages required for the ADC. The LTC6409 is powered directly. The DC2266A demonstration circuit requires up to 800mA from the VIN supply, and 75mA from the AMPVCC supply. The DC2266A should not be removed or connected to the DC1371 while power is applied.

ANALOG INPUT NETWORK

The input network of the DC2266A can be modified to accommodate various applications. In the default setup, both of the inputs are brought out to SMA connectors so the demo board can be driven with a differential source. To drive the demo board with a single-ended source simply drive J2 and terminate J1 with the matched source impedance of the signal source.

As a default, the DC2266A is populated with no filtering between the input SMAs and the LTC6409. This allows a custom filter to be designed and used between the signal source and amplifier.

In almost all cases, an off-board absorptive filter will be required on the analog input of the DC2266A to produce optimum SNR.

The off-board filter should be located close to the input of the demo board to avoid reflections from impedance discontinuities at the driven end of a long transmission line. Most filters do not present 50Ω outside the passband. In some cases, 3dB to 10dB pads may be required to make the filter look more absorptive to obtain low distortion.

The gain of the amplifier can also be changed by varying the feedforward and feedback resistors. For optimal distortion and noise performance, there is an absorptive filter (diplexer) network populated after the LTC6409. This reduces the sampling artifacts seen by the amplifier and reduces the reflections of these products that return to the ADC.

Be sure not to overdrive the ADC by setting the gain too high; refer to the LTC6409 data sheet for resistor value considerations.

APPLYING POWER AND SIGNALS TO THE DC2266A

ENCODE CLOCK

Apply a differential encode clock to the SMA connectors on the DC2266A marked J3 and J4. These SMA connectors are 0.5" apart to accommodate LTC differential clock boards.

For the best noise performance, the encode input must be driven with a very low jitter, signal generator source. The amplitude should be as large as possible up to $2V_{P-P}$ or 10dBm.

The DC2266A demo board is designed to accept various differential signaling standards. Changing the position of JP6 to CML, LVDS, or LVPECL selects the proper termination for your input signal.

SOFTWARE

The DC1371 is controlled by the PScope system software which can be downloaded from the Linear Technology website at: www.linear.com/software/

If a DC1371 was provided, follow the DC1371 Quick Start Guide and the instructions below.

To start the data collection software if "PScope.exe" is installed (by default) in \Program~Files\LTC\PScope\, double click the PScope icon or bring up the run window under the start menu and browse to the PScope directory and select PScope.

If the DC2266A demonstration circuit is properly connected to the DC1371, PScope should automatically detect the DC2266A, and configure itself accordingly. If necessary, the procedure below explains how to manually configure PScope.

Under the "Configure" menu, go to "ADC Configuration..." Check the "Config Manually" box and use the following configuration options, see Figure 2.

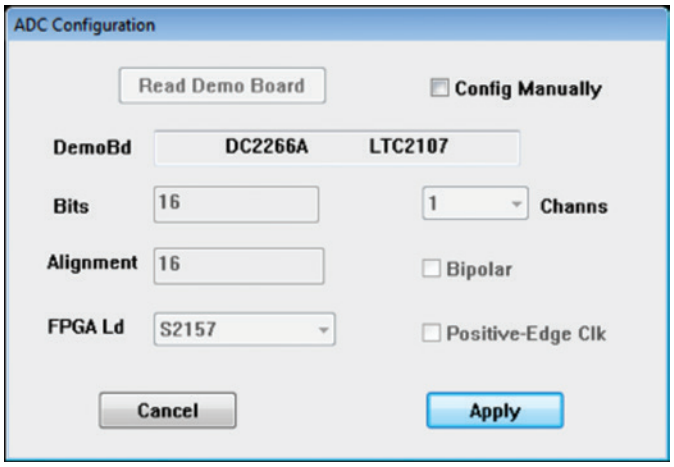


Figure 2: ADC Configuration

Manual Configuration Settings:

Bits: 16

Alignment: 16

FPGA Ld: S2157

Channs: 1

Bipolar: Unchecked

Positive-Edge Clk: Unchecked

If everything is hooked up properly, powered and a suitable, convert clock is present, clicking the "Collect" button should result in time and frequency plots displayed in the PScope window. Additional information and help for PScope is available in the DC1371 Quick Start Guide and in the online help available within the PScope program itself.

SERIAL PROGRAMMING

PScope has the ability to program the DC2266A board serially through the DC1371. There are several options available for the LTC2107 that are only available through serially programming. PScope allows all of these features to be tested.

APPLYING POWER AND SIGNALS TO THE DC2266A

These options are available by first clicking on the "Set Demo Bd Options" icon on the PScope toolbar (Figure 3).

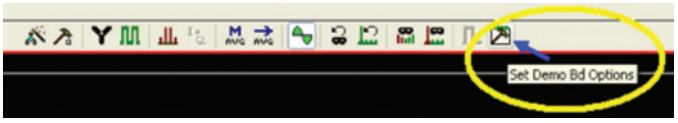


Figure 3: PScope Toolbar

This will bring up the menu shown in Figure 4.

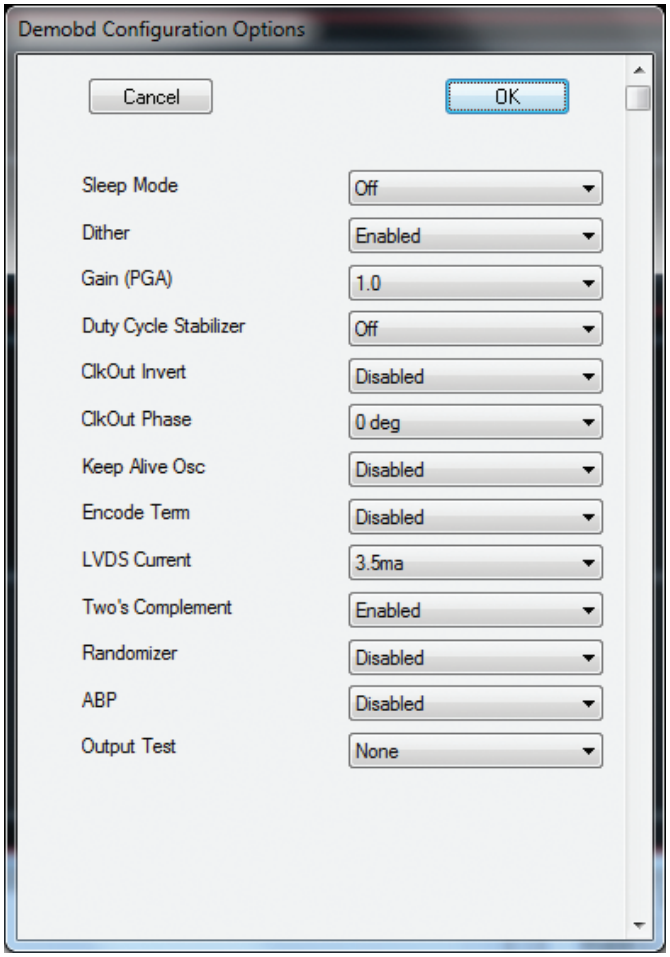


Figure 4: Demo Board Configuration Options

This menu allows any of the options available for the LTC2107 to be programmed serially. The LTC2107 family has the following options:

Sleep Mode – Selects Between Normal Operation and Sleep Mode:

- Off (Default) – Entire ADC is Powered and Active
- On – The Entire ADC is Powered Down

Dither – Selects Between Internal Dither Being Enabled or Disabled:

- Enabled (Default) – Internal Dither Enabled
- Disabled – Internal Dither Disabled

Gain (PGA) – Selects Input Range of the ADC:

- 1.0 (Default) – Selects the 2.4V Input Range
- 1.5 – Selects the 1.6V Input Range

Duty Cycle Stabilizer – Enables or Disables Duty Cycle Stabilizer:

- Stabilizer Off (Default) – Duty Cycle Stabilizer Disabled
- Stabilizer On – Duty Cycle Stabilizer Enabled

ClkOut Invert – Selects the Polarity of the CLKOUT Signal:

- Disabled (Default) – Normal CLKOUT Polarity
- Enabled – CLKOUT Polarity is Inverted

ClkOut Phase – Selects the Phase Delay of the CLKOUT Signal:

- 0 deg (Default) – No CLKOUT Delay
- 45 deg – CLKOUT Delayed by 45 Degrees
- 90 deg – CLKOUT Delayed by 90 Degrees
- 135 deg – CLKOUT Delayed by 135 Degrees

APPLYING POWER AND SIGNALS TO THE DC2266A

Keep Alive Osc – Enables or Disables the Internal Keep Alive Oscillator:

- Disabled (Default) – Keep Alive Oscillator is Disabled
- Enabled – Keep Alive Oscillator is Enabled

Encode Term – Enables or Disables LVDS Internal Termination:

- Disabled (Default) – Disables Internal Termination
- Enabled – Enables Internal Termination

LVDS Current – Selects the LVDS Output Drive Current:

- 1.75mA – LVDS Output Driver Current
- 2.1mA – LVDS Output Driver Current
- 2.5mA – LVDS Output Driver Current
- 3.0mA – LVDS Output Driver Current
- 3.5mA (Default) – LVDS Output Driver Current
- 4.0mA – LVDS Output Driver Current
- 4.5mA – LVDS Output Driver Current

Two's Complement – Enables or Disables Two's Complement Mode:

- Enabled (Default) – Selects Two's Complement Mode
- Disabled – Selects Offset Binary Mode

Randomizer – Enables Data Output Randomizer:

- Disabled (Default) – Disables Data Output Randomizer
- Enabled – Enables Data Output Randomizer

ABP – Enables or Disables Alternate Bit Polarity (ABP) Mode:

- Disabled (Default) – Disables Alternate Bit Polarity
- Enabled – Enables Alternate Bit Polarity (Before Enabling ABP, Be Sure the Part is in Offset Binary Mode)

Output Test – Selects Digital Output Test Patterns:

- None (Default) – ADC Data Presented at Output
- All Out = 1 – All Digital Outputs Are 1
- All Out = 0 – All Digital Outputs Are 0
- Checkerboard – OF and D15-D0 Alternate Between 1 0101 0101 1010 0101 and 0 1010 1010 0101 1010 on Alternating Samples
- Alternating – Digital Outputs Alternate Between All 1s and All 0s on Alternating Samples

Once the desired settings are selected hit OK and PScope will automatically update the register of the device on the DC2266A demo board.

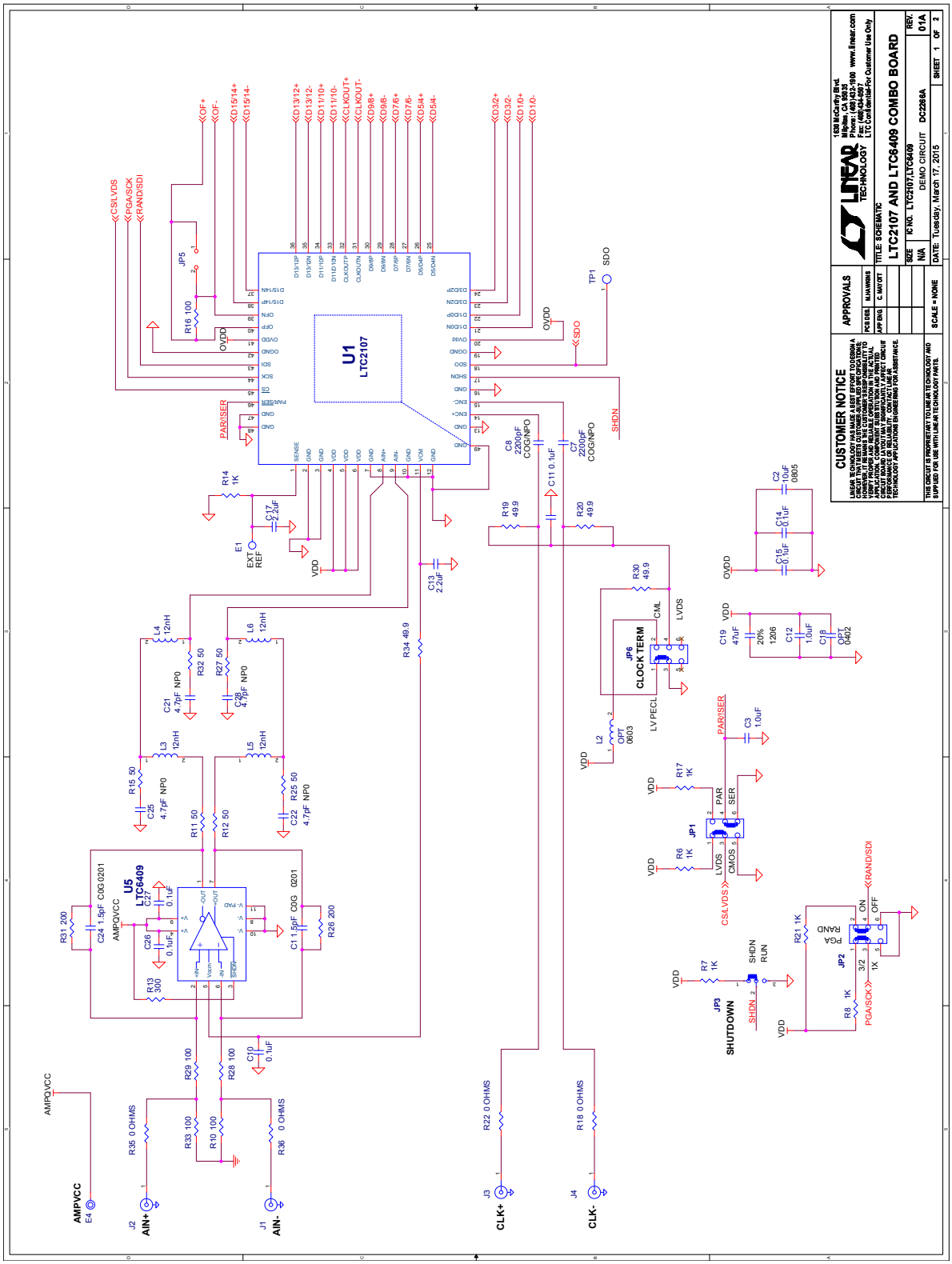
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	2	C1, C24	CAP.,1.5pF, C0G, 50V ±0.25pF, 0201	MURATA, GRM0335C1H1R5CA01D
2	1	C2	CAP., 10µF, X7R, 16V, 10%, 0805	SAMSUNG, CL21B106KOQNNNE
3	2	C3, C12	CAP., 1µF, X5R, 25V, 10%, 0603	TDK, C1608X5R1E105K080AC
4	4	C4, C9, C16, C20	CAP., 10µF, X5R, 16V, 20%, 1206	TDK, C3216X5R1C106M
5	2	C5, C6	CAP., 100µF, X5R, 16V, 20%, 1210	TAIYO YUDEN, EMK325ABJ107MM-T
6	2	C7, C8	CAP., 2200pF, C0G, 25V, 5%, 0402	KEMET, C0402C222J3GACTU
7	3	C10, C26, C27	CAP., 0.1µF, X7R, 50V, 10%, 0402	TDK, C1005X7R1H104K
8	4	C11, C14, C15, C23	CAP., 0.1µF, X5R, 16V, 10%, 0402	AVX, 0402YD104KAT2A
9	1	C13	CAP., 2.2µF, X5R, 16V, 20%, 0603	AVX, 0603YD225MAT2A
10	1	C17	CAP., 2.2µF, X5R, 16V, 20%, 0402	TDK, C1005X5R1C225M050BC
11	0	C18	CAP., OPTION, 0402	OPTION
12	1	C19	CAP., 47µF, X5R, 16V, 20%, 1206	TDK, C3216X5R1C476M160AB
13	4	C21, C22, C25, C28	CAP., 4.7pF, NP0, 50V, ±0.25pF, 0402	TDK, C1005C0G1H4R7C
14	1	E1	TEST POINT, TURRET, 0.064" MTG. HOLE	MILL-MAX, 2308-2-00-80-00-00-07-0
15	3	E2, E3, E4	TEST POINT, TURRET, 0.094" MTG.HOLE	MILL-MAX, 2501-2-00-80-00-00-07-0
16	3	JP1, JP2, JP6	CONN., HEADER, 2 × 3, 2mm, THRU-HOLE, VERTICAL	SAMTEC, TMM-103-02-L-D
17	2	JP3, JP4	CONN., HEADER, 1 × 3, 2mm, THRU-HOLE, VERTICAL	SAMTEC, TMM-103-02-L-S
18	1	JP5	CONN., HEADER, 1 × 2, 2mm, THRU-HOLE, VERTICAL	SAMTEC, TMM102-02-L-S
19	2	J1, J2	CONN., SMA 50Ω EDGE-LAUNCH	AMPHENOL CONNEX, 132372
20	2	J3, J4	CONN., SMA JACK, STRAIGHT, THRU-HOLE	AMPHENOL CONNEX, 132134
21	1	L1	IND., FERRITE BEAD, 47Ω @ 100MHz, 0603	MURATA, BLM18BB470SN1D
22	0	L2	IND., OPTION, 0603	OPTION
23	4	L3, L4, L5, L6	IND., CER. CHIP, 12nH, 2%, 0402	COILCRAFT, 0402CS-12NXGLU
24	1	P1	CONN., HIGH DENSITY ARRAY, MALE, 400 PINS	SAMTEC, SEAM-40-02.0-S-10-2-A-K-TR
25	4	R1, R2, R3, R5	RES., 33Ω, 1/16W, 5%, 0402	YAGEO, RC0402JR-0733RL
26	3	R4, R23, R24	RES., 4.99k, 1/16W, 1%, 0402	YAGEO, RC0402FR-074K99L
27	6	R6, R7, R8, R14, R17, R21	RES., 1k, 1/16W, 5%, 0402	YAGEO, RC0402JR-071KL
28	0	R9	RES., OPTION, 0805	OPTION
29	4	R10, R28, R29, R33	RES., 100Ω, 1/16W, 1%, 0402	YAGEO, RC0402FR-07100RL
30	6	R11, R12, R15, R25, R27, R32	RES., HIGH FREQ., 50Ω, 1/20W, 0.1%, 0402	VISHAY, FC0402E50R0BST1
31	1	R13	RES., 300Ω, 1/16W, 5%, 0402	YAGEO, RC0402JR-07300RL
32	1	R16	RES., 100Ω, 1/16W, 5%, 0402	YAGEO, RC0402JR-07100RL
34	3	R19, R20, R30	RES., HIGH POWER, 49.9Ω, 1/8W, 1%, 0402	VISHAY, CRCW040249R9FKEDHP
35	4	R18, R22, R35, R36	RES., 0Ω JUMPER, 1/16W, 0402	VISHAY, CRCW04020000Z0ED

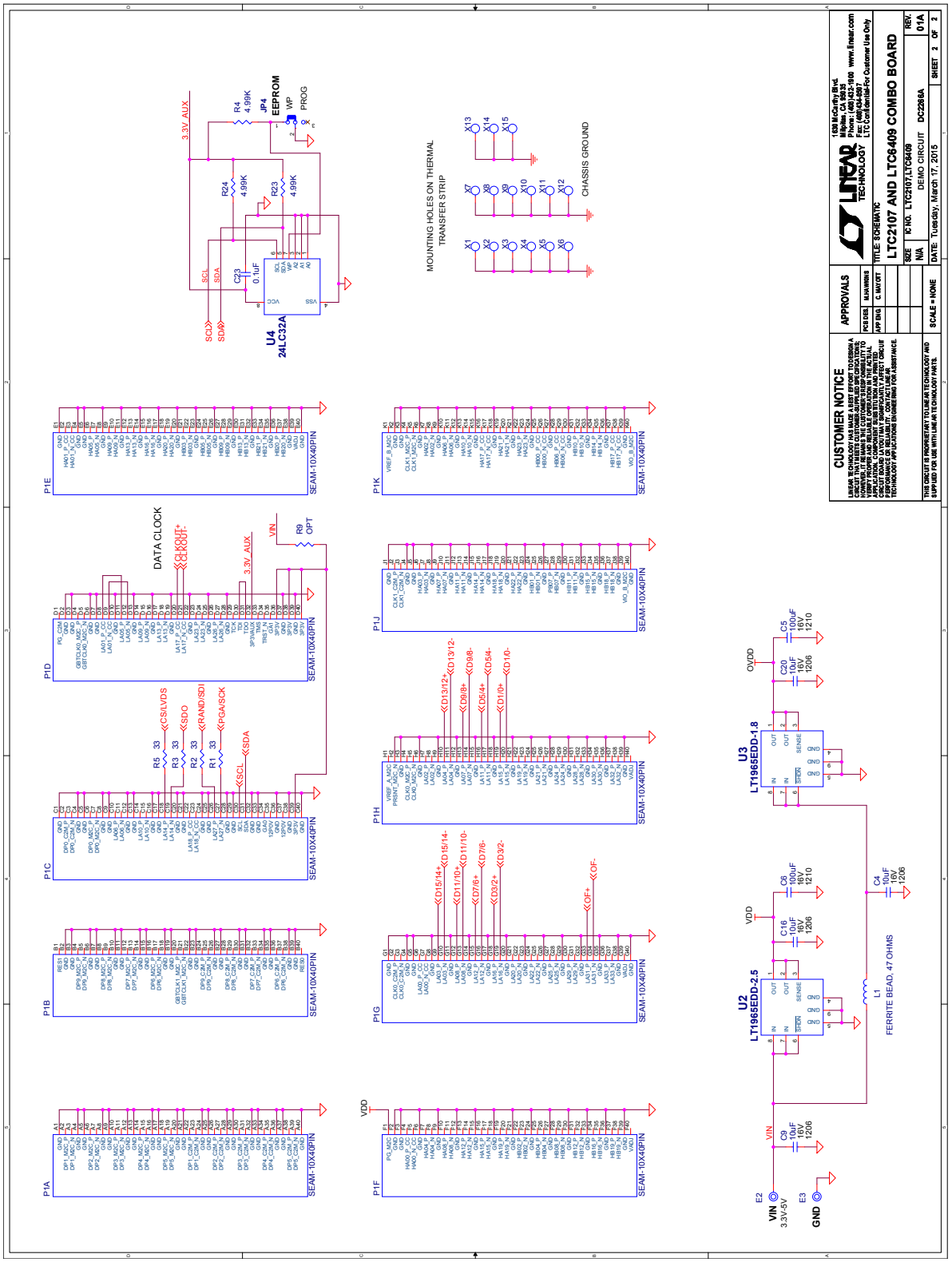
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
36	2	R26, R31	RES., 200Ω, 1/16W, 1%, 0402	VISHAY, CRCW0402200RFKED
37	1	R34	RES., 49.9Ω, 1/16W, 1%, 0402	YAGEO, RC0402FR-0749R9L
39	1	U1	ADC, 16-BIT, 210Msps, QFN	LINEAR TECH., LTC2107IUK#PBF
40	1	U2	IC, LDO LINEAR REGULATOR, 2.5V, DFN	LINEAR TECH., LT1965EDD-2.5#PBF
41	1	U3	IC, LDO LINEAR REGULATOR, 1.8V, DFN	LINEAR TECH., LT1965EDD-1.8#PBF
42	1	U4	IC, SERIAL EEPROM, TSSOP-8	MICROCHIP TECH., 24LC32A-I/ST
43	1	U5	IC, HIGH SPEED DIFF. AMP./DRIVER, QFN	LINEAR TECH., LTC6409IUDB#TRMPBF
44	7	XJP1, XJP2, XJP3, XJP4, XJP5, XJP6, XJP7	SHUNT, 2mm	SAMTEC, 2SN-BK-G

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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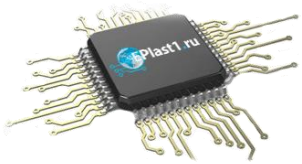

Как с нами связаться

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