19-4057; Rev 0; 3/08

50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

General Description

The MAX2066 high-linearity digital variable-gain amplifier (VGA) is a monolithic SiGe BiCMOS attenuator and amplifier designed to interface with 50Ω systems operating in the 50MHz to 1000MHz frequency range (See the *Typical Application Circuit*). The digital attenuator is controlled as a slave peripheral using either the SPI™-compatible interface or a parallel bus with 31dB total adjustment range in 1dB steps. An added feature allows "rapid-fire" gain selection between each of four steps, preprogrammed by the user through the SPI-compatible interface. The 2-pin control allows the user to quickly access any one of four customized attenuation states without reprogramming the SPI bus.

Because each stage has its own RF input and RF output, this component can be configured to either optimize NF (amplifier configured first), or OIP3 (amplifier last). The device's performance features include 22dB amplifier gain (amplifier only), 5.2dB NF at maximum gain (includes attenuator insertion loss), and a high OIP3 level of +42.4dBm. Each of these features makes the MAX2066 an ideal VGA for numerous receiver and transmitter applications.

In addition, the MAX2066 operates from a single +5V supply with full performance, or a single +3.3V supply with slightly reduced performance, and has an adjustable bias to trade current consumption for linearity performance. This device is available in a compact 40-pin thin QFN package (6mm x 6mm) with an exposed pad. Electrical performance is guaranteed over the extended temperature range (T_C = -40°C to +85°C).

Applications

- IF and RF Gain Stages
- Cellular Band WCDMA and cdma2000® Base Stations
- GSM 850/GSM 900 EDGE Base Stations
- WiMAX and LTE Base Stations and Customer Premise Equipment
- Fixed Broadband Wireless Access
- Wireless Local Loop
- Military Systems
- Video-on-Demand (VOD) and DOCSIS®-Compliant EDGE QAM Modulation
- Cable Modem Termination Systems (CMTS)
- RFID Handheld and Portal Readers

SPI is a trademark of Motorola, Inc.

Features

- **50MHz to 1000MHz RF Frequency Range**
- **Pin-Compatible Family Includes**
  - **MAX2065 (Analog/Digital VGA)**
  - **MAX2067 (Analog VGA)**
- **20.5dB (typ) Maximum Gain**
- **0.4dB Gain Flatness Over 100MHz Bandwidth**
- **31dB Gain Range**
- **Supports Four "Rapid-Fire" Preprogrammed Attenuator States**
  - **Quickly Access Any One of Four Customized Attenuation States Without Reprogramming the SPI Bus**
  - **Ideal for Fast-Attack, High-Level Blocker Protection**
  - **Prevents ADC Overdrive Condition**
- **Excellent Linearity (Configured with Amplifier Last)**
  - **+42.4dBm OIP3**
  - **+65dBm OIP2**
  - **+19dBm Output 1dB Compression Point**
  - **-68dBc HD2**
  - **-88dBc HD3**
- **5.2dB Typical Noise Figure (NF)**
- **Fast, 25ns Digital Switching**
- **Very Low Digital VGA Amplitude Overshoot/Undershoot**
- **Single +5V Supply (Optional +3.3V Operation)**
- **External Current-Setting Resistors Provide Option for Operating Device in Reduced-Power/Reduced-Performance Mode**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2066ETL+	-40°C to +85°C	40 Thin QFN-EP*
MAX2066ETL+T	-40°C to +85°C	40 Thin QFN-EP*

+Denotes a lead-free package.
**EP = Exposed pad.*
T = Tape and reel.

Pin Configuration appears at end of data sheet.

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ABSOLUTE MAXIMUM RATINGS

VCC_ to GND ....-0.3V to +5.5V
VDD_LOGIC, DATA, $\overline{CS}$, CLK,
SER/PAR..-0.3V to (VCC_ + 0.3V)
STATE_A, STATE_B, D0–D4 ....-0.3V to (VCC_ + 0.3V)
AMP_IN, AMP_OUT ....-0.3V to (VCC_ + 0.3V)
ATTEN_IN, ATTEN_OUT.......................................-1.2V to +1.2V
RSET to GND..-0.3V to +1.2V
RF Input Power (ATTEN_IN, ATTEN_OUT)....................+20dBm
RF Input Power (AMP_IN)..+18dBm
Continuous Power Dissipation (Note 1) 6.5W
θ_{JA} (Notes 2, 3)..+38°C/W
θ_{JC} (Note 3) ....+10°C/W
Operating Temperature Range (Note 4).....T_C = -40°C to +85°C
Maximum Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a printed-circuit board (PCB). See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Note 4: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

+3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, high-current (HC) mode, $V_{CC} = V_{DD}$ = +3.0V to +3.6V, T_C = -40°C to +85°C. Typical values are at $V_{CC} = V_{DD}$ = +3.3V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 5)	3.0	3.3	3.6	V
Supply Current	I_{CC}			58	80	mA
LOGIC INPUTS (DATA, $\overline{CS}$, CLK, SER/PAR, STATE_A, STATE_B, D0–D4)						
Input High Voltage	V_{IH}			2		V
Input Low Voltage	V_{IL}			0.8		V

+5V SUPPLY DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, $V_{CC} = V_{DD}$ = +4.75V to +5.25V, T_C = -40°C to +85°C. Typical values are at $V_{CC} = V_{DD}$ = +5V and T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{CC}	Low-current (LC) mode		70	90	mA
		High-current (HC) mode		121	144	
LOGIC INPUTS (DATA, $\overline{CS}$, CLK, SER/PAR, STATE_A, STATE_B, D0–D4)						
Input High Voltage	V_{IH}		3			V
Input Low Voltage	V_{IL}				0.8	V
Input Current Logic-High	I_{IH}		-1		+1	µA
Input Current Logic-Low	I_{IL}		-1		+1	µA

+3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = V_{DD} = +3.0V to +3.6V, T_C = -40°C to +85°C. Typical values are at V_{CC} = V_{DD} = +3.3V, HC mode with attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Notes 5, 7)	50		1000	MHz
Small-Signal Gain	G			20		dB
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone, maximum gain setting		38		dBm
Noise Figure	NF	Maximum gain setting		5.6		dB
Total Attenuation Range				31		dB

+5V SUPPLY AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = V_{DD} = +4.75 to +5.25V, HC mode with attenuator set for maximum gain, 50MHz ≤ f_{RF} ≤ 1000MHz, T_C = -40°C to +85°C. Typical values are at V_{CC} = V_{DD} = +5.0V, HC mode, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RF Frequency Range	f_{RF}	(Notes 5, 7)		50		1000	MHz
Small-Signal Gain	G	200MHz			20.5		dB
		350MHz, T_C = +25°C		18.6	19.9	21.1	
		450MHz			19.5		
		750MHz			18.1		
		900MHz			17.4		
Gain Variation vs. Temperature					-0.004		dB/°C
Gain Flatness vs. Frequency		Any 100MHz frequency band from 50MHz to 500MHz			0.4		dB
Noise Figure	NF	200MHz			5.2		dB
		350MHz, T_C = +25°C (Note 5)			5.5	6.6	
		450MHz			5.6		
		750MHz			6.2		
		900MHz			6.4		
Total Attenuation Range					31		dB
Output Second-Order Intercept Point	OIP2	P_{OUT} = 0dBm/tone, Δf = 1MHz, $f_1 + f_2$			65		dBm
Output Third-Order Intercept Point	OIP3	P_{OUT} = 0dBm/tone, HC mode, Δf = 1MHz	200MHz		42.4		dBm
			350MHz		40.4		
			450MHz		39.5		
			750MHz		37.3		
			900MHz		36.2		
		P_{OUT} = 0dBm/tone, LC mode, Δf = 1MHz	200MHz		40		
			350MHz		38		
			450MHz		37		
			750MHz		35		
			900MHz		33		

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+5V SUPPLY AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = V_{DD} = +4.75 to +5.25V, HC mode with attenuator set for maximum gain, 50MHz ≤ f_{RF} ≤ 1000MHz, T_C = -40°C to +85°C. Typical values are at V_{CC} = V_{DD} = +5.0V, HC mode, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output -1dB Compression Point	P_{1dB}	f_{RF} = 350MHz, T_C = +25°C (Note 5, 8)		17	18.7		dBm
Second Harmonic		P_{OUT} = +3dBm, f_{IN} = 200MHz, T_C = +25°C (Note 5)		-60	-68		dBc
Third Harmonic		P_{OUT} = +3dBm, f_{IN} = 200MHz, T_C = +25°C (Note 5)		-72	-88		dBc
Group Delay		Includes EV kit PCB trace delay			0.8		ns
Input Return Loss		50Ω source, maximum gain setting			23		dB
Output Return Loss		50Ω load, maximum gain setting			18		dB
DIGITAL ATTENUATOR							
Insertion Loss					2.5		dB
Input Second-Order Intercept Point	IIP2	P_{RF1} = 0dBm, P_{RF2} = 0dBm, Δf = 1MHz, $f_1 + f_2$			52		dBm
Input Third-Order Intercept Point	IIP3	P_{RF1} = 0dBm, P_{RF2} = 0dBm, Δf = 1MHz			41		dBm
Attenuation Range					31.2		dB
Step Size					1		dB
Relative Step Accuracy					0.2		dB
Absolute Step Accuracy					0.45		dB
Insertion Phase Step		f_{RF} = 170MHz	0dB to 16dB		4.8		degrees
			24dB		8		
			31dB		10.8		
Amplitude Overshoot/Undershoot		Between any two states	ET = 15ns		1.0		dB
			ET = 40ns		0.05		
Switching Speed		RF settled to within ±0.1dB	31dB to 0dB		25		ns
			0dB to 31dB		21		
Input Return Loss		50Ω source, maximum gain setting			19		dB
Output Return Loss		50Ω load, maximum gain setting			19		dB
SERIAL PERIPHERAL INTERFACE (SPI)							
Maximum Clock Speed	f_{CLK}				20		MHz
Data-to-Clock Setup Time	t_{CS}				2		ns
Data-to-Clock Hold Time	t_{CH}				2.5		ns
Clock-to-$\overline{CS}$ Setup Time	t_{ES}				3		ns
$\overline{CS}$ Positive Pulse Width	t_{EW}				7		ns
$\overline{CS}$ Setup Time	t_{EWS}				3.5		ns
Clock Pulse Width	t_{CW}				5		ns

Note 5: Guaranteed by design and characterization.

Note 6: All limits include external component losses. Output measurements are performed at RF output port of the *Typical Application Circuit*.

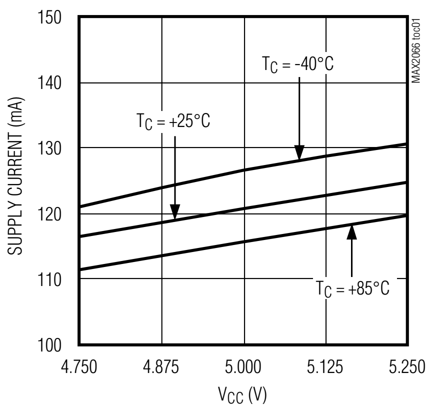
Note 7: Operating outside this range is possible, but with degraded performance of some parameters.

Note 8: It is advisable not to continuously operate the VGA RF input above +15dBm.

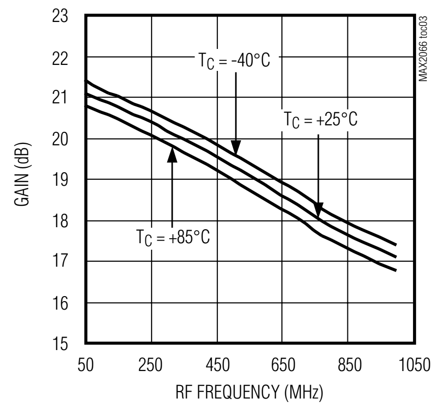
Typical Operating Characteristics

(**V_{CC} = V_{DD} = +5.0V, HC mode**, digital attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.)

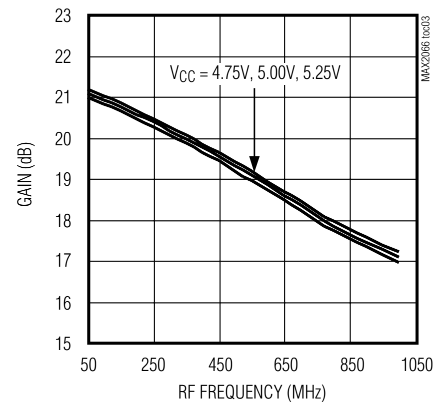
SUPPLY CURRENT vs. SUPPLY VOLTAGE



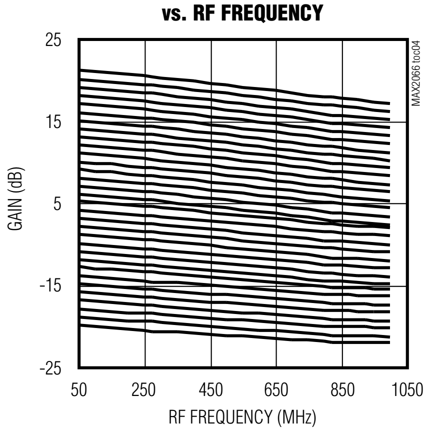
GAIN vs. RF FREQUENCY



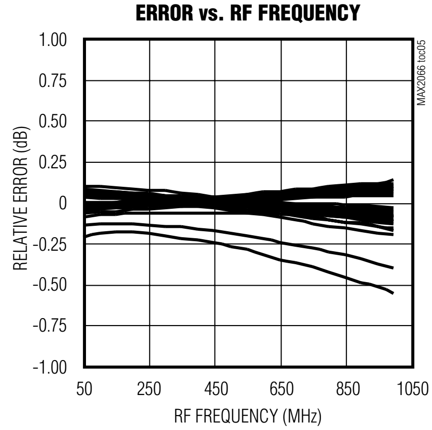
GAIN vs. RF FREQUENCY



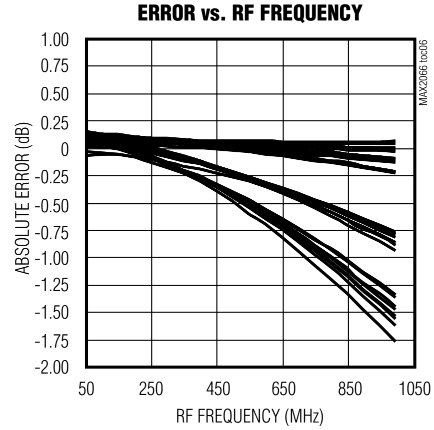
GAIN OVER ATTENUATOR SETTING vs. RF FREQUENCY



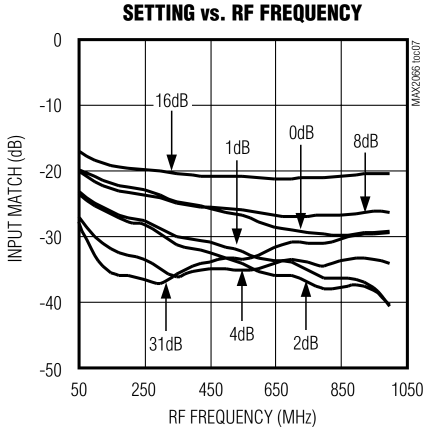
ATTENUATOR RELATIVE ERROR vs. RF FREQUENCY



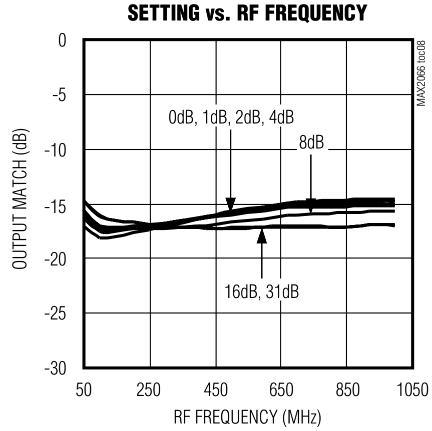
ATTENUATOR ABSOLUTE ERROR vs. RF FREQUENCY



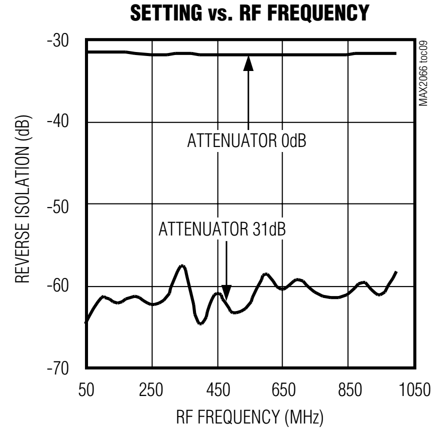
INPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY



OUTPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY



REVERSE ISOLATION OVER ATTENUATOR SETTING vs. RF FREQUENCY

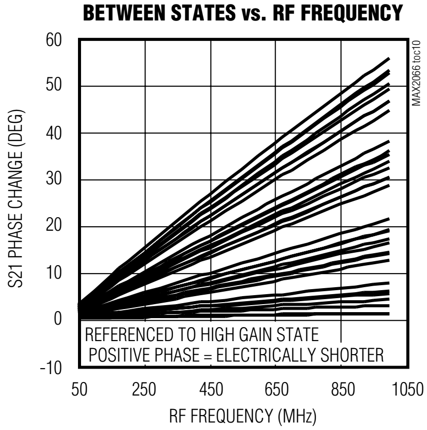


50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

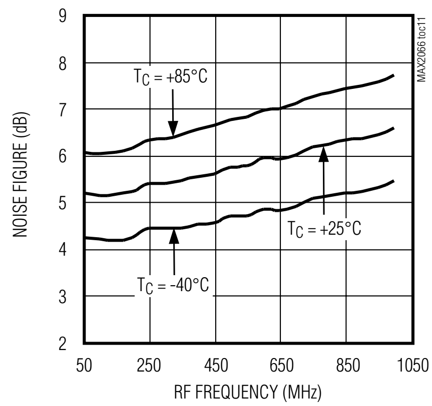
Typical Operating Characteristics (continued)

(**V_{CC} = V_{DD} = +5.0V, HC mode**, digital attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.)

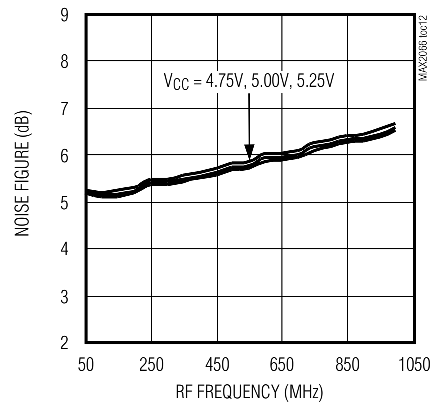
ATTENUATOR PHASE CHANGE BETWEEN STATES vs. RF FREQUENCY



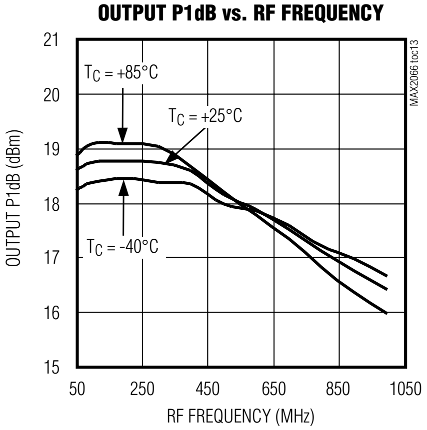
NOISE FIGURE vs. RF FREQUENCY



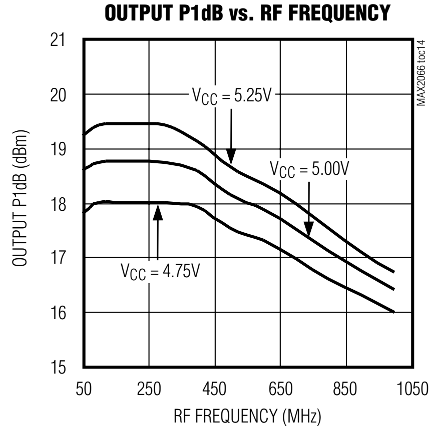
NOISE FIGURE vs. RF FREQUENCY



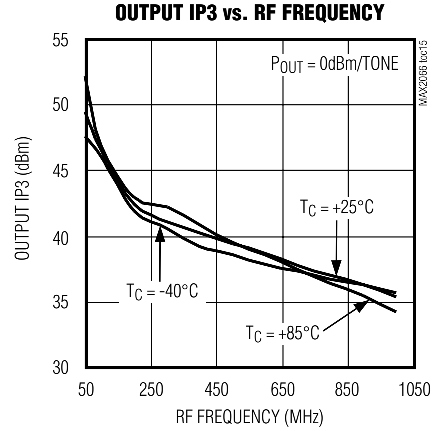
OUTPUT P1dB vs. RF FREQUENCY



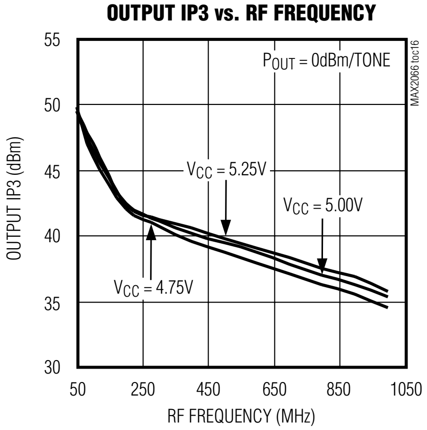
OUTPUT P1dB vs. RF FREQUENCY



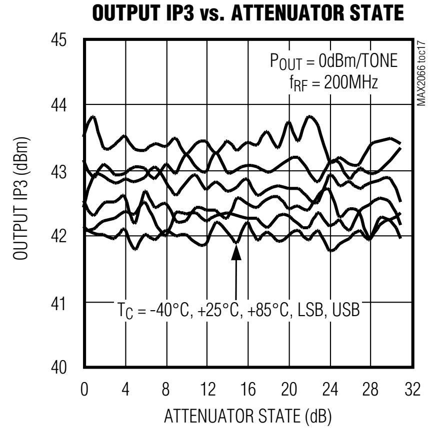
OUTPUT IP3 vs. RF FREQUENCY



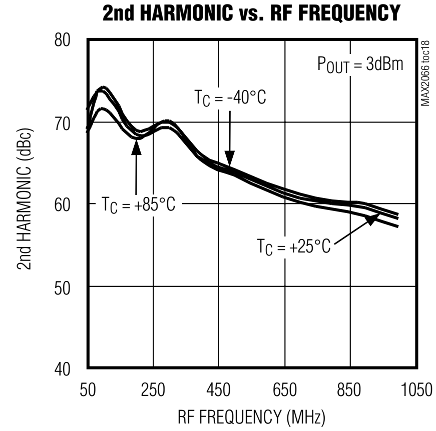
OUTPUT IP3 vs. RF FREQUENCY



OUTPUT IP3 vs. ATTENUATOR STATE



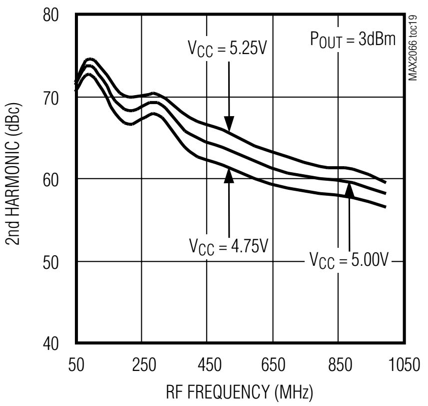
2nd HARMONIC vs. RF FREQUENCY



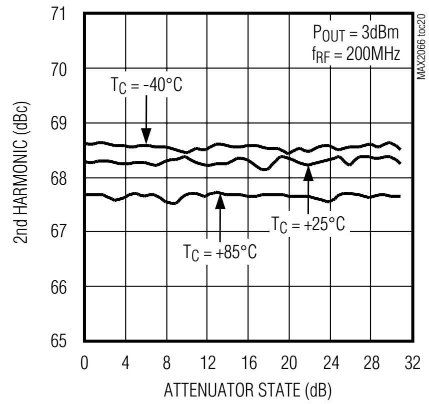
Typical Operating Characteristics (continued)

(**V_{CC} = V_{DD} = +5.0V, HC mode**, digital attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.)

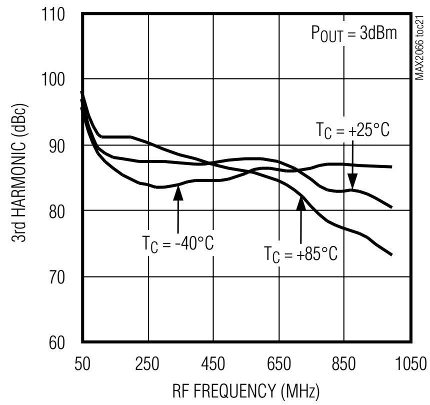
2nd HARMONIC vs. RF FREQUENCY



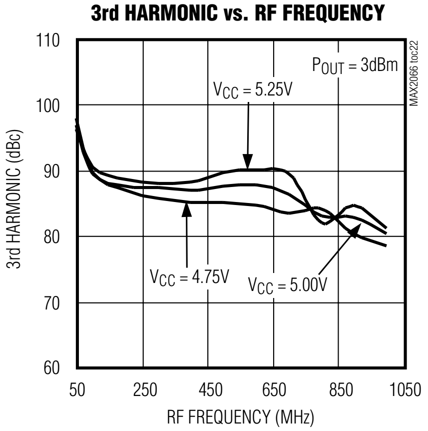
2nd HARMONIC vs. ATTENUATOR STATE



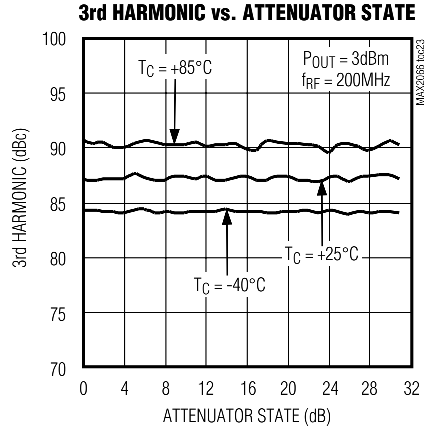
3rd HARMONIC vs. RF FREQUENCY



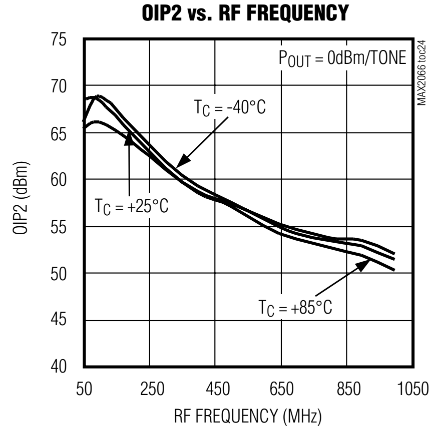
3rd HARMONIC vs. RF FREQUENCY



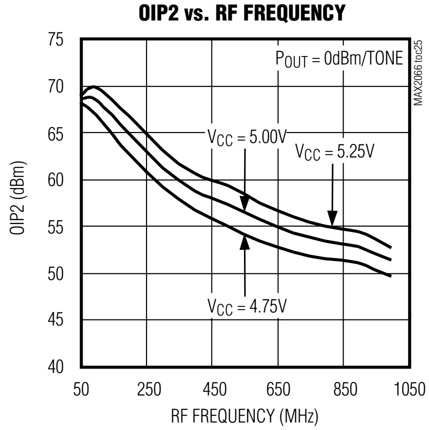
3rd HARMONIC vs. ATTENUATOR STATE



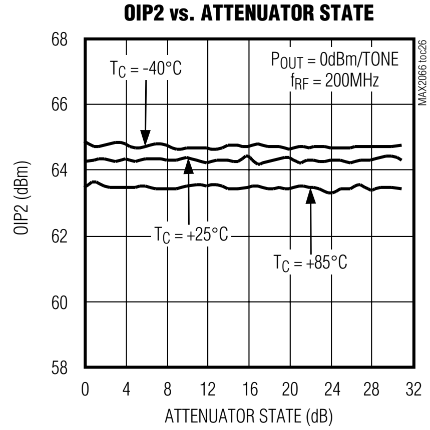
OIP2 vs. RF FREQUENCY



OIP2 vs. RF FREQUENCY



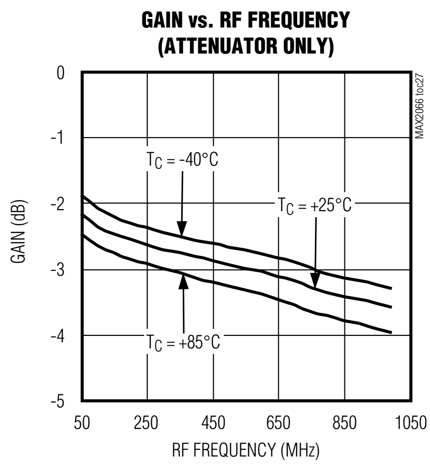
OIP2 vs. ATTENUATOR STATE

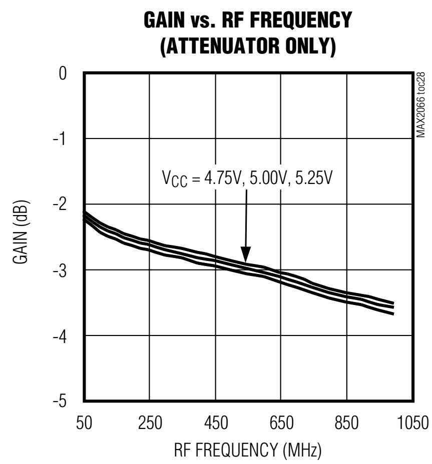


50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

Typical Operating Characteristics (continued)

(**V_{CC} = V_{DD} = +5.0V, digital attenuator only**, maximum gain, P_{IN} = -20dBm and T_C = +25°C, unless otherwise noted.)

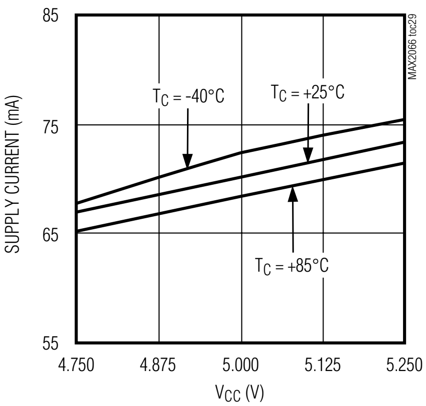




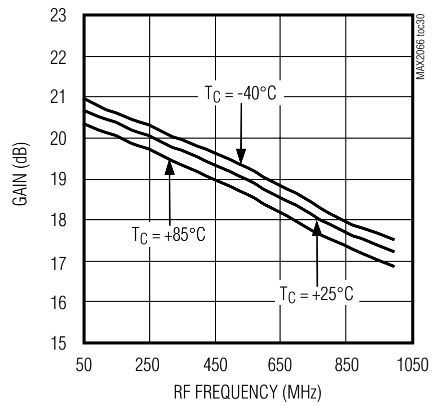
Typical Operating Characteristics (continued)

(V_{CC} = V_{DD} = +5.0V, **LC mode**, digital attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.)

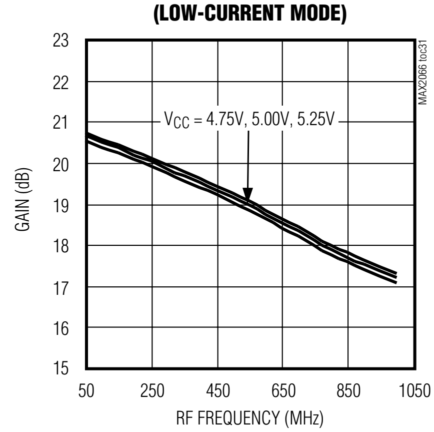
SUPPLY CURRENT vs. SUPPLY VOLTAGE (LOW-CURRENT MODE)



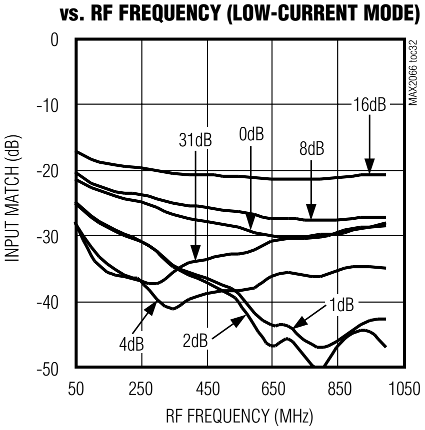
GAIN vs. RF FREQUENCY (LOW-CURRENT MODE)



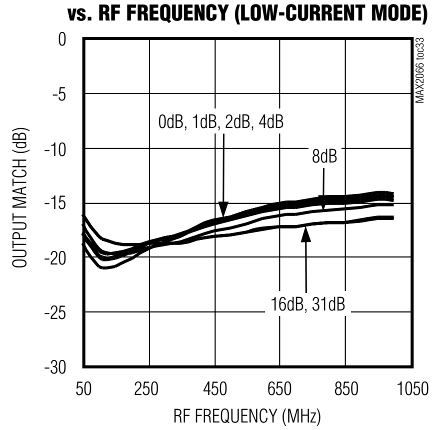
GAIN vs. RF FREQUENCY (LOW-CURRENT MODE)



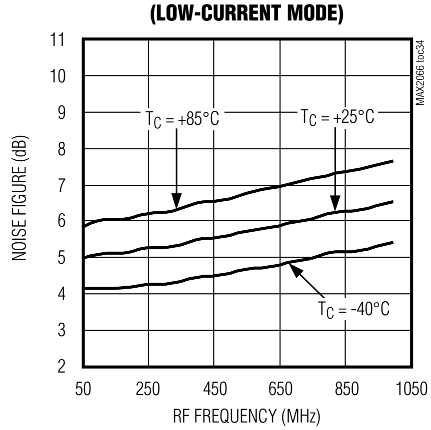
INPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY (LOW-CURRENT MODE)



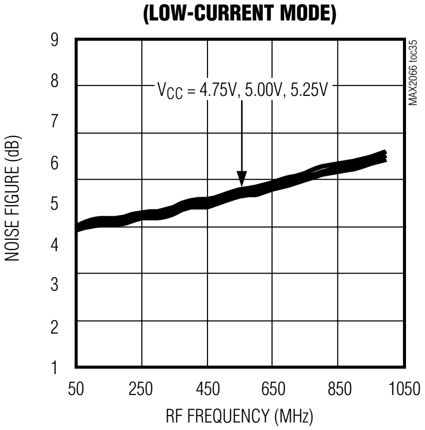
OUTPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY (LOW-CURRENT MODE)



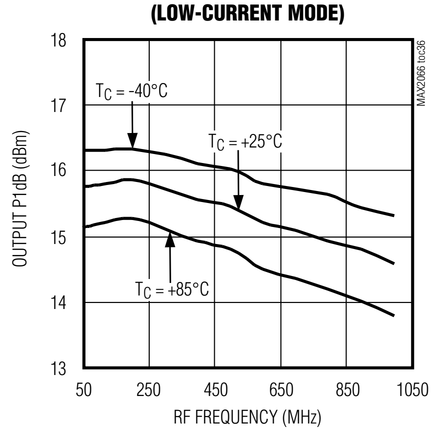
NOISE FIGURE vs. RF FREQUENCY (LOW-CURRENT MODE)



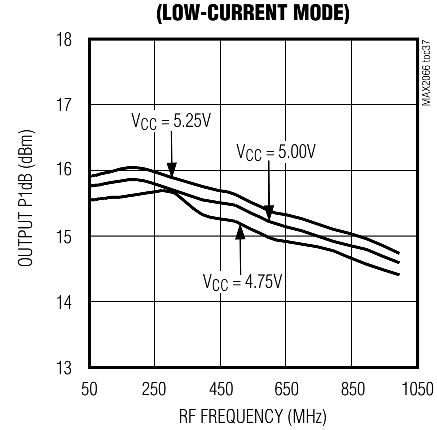
NOISE FIGURE vs. RF FREQUENCY (LOW-CURRENT MODE)



OUTPUT P1dB vs. RF FREQUENCY (LOW-CURRENT MODE)



OUTPUT P1dB vs. RF FREQUENCY (LOW-CURRENT MODE)

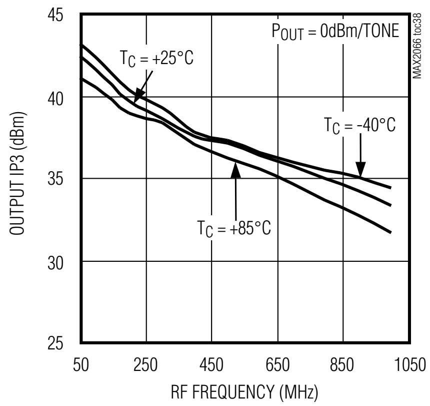


50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

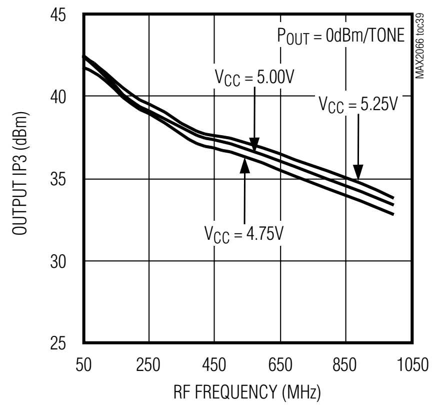
Typical Operating Characteristics (continued)

(**V_{CC} = V_{DD} = +5.0V, LC mode**, digital attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.)

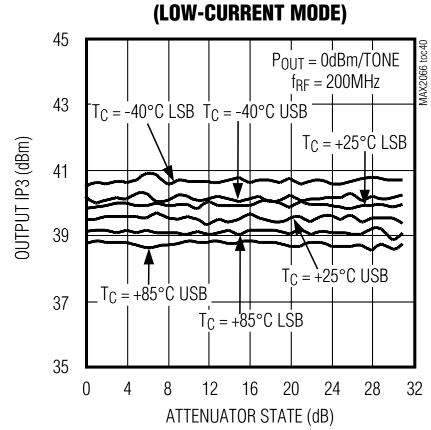
OUTPUT IP3 vs. RF FREQUENCY (LOW-CURRENT MODE)



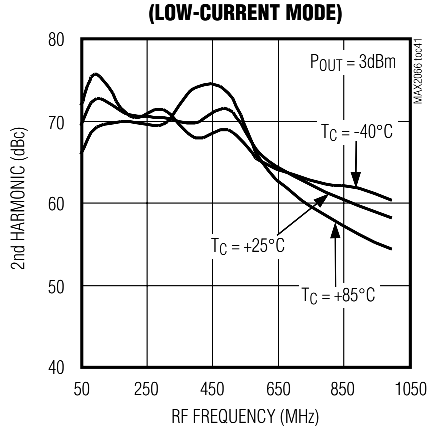
OUTPUT IP3 vs. RF FREQUENCY (LOW-CURRENT MODE)



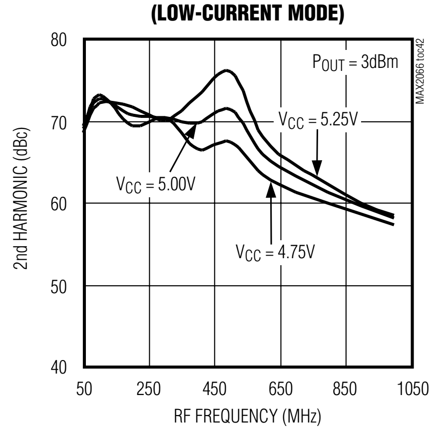
OUTPUT IP3 vs. ATTENUATOR STATE (LOW-CURRENT MODE)



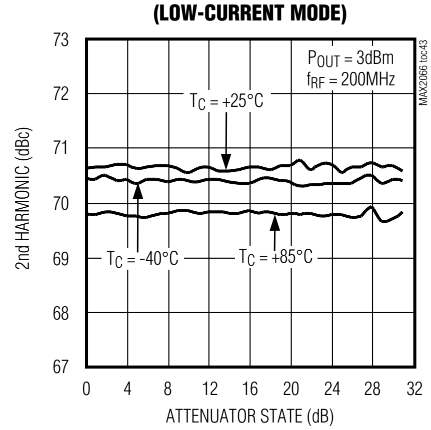
2nd HARMONIC vs. RF FREQUENCY (LOW-CURRENT MODE)



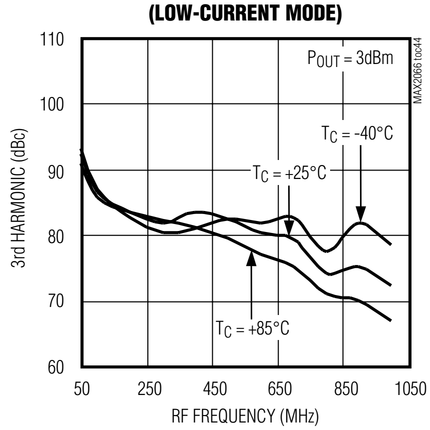
2nd HARMONIC vs. RF FREQUENCY (LOW-CURRENT MODE)



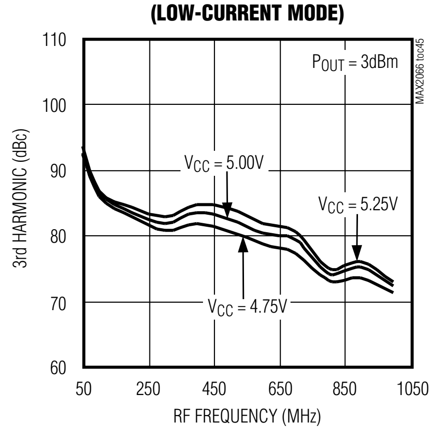
2nd HARMONIC vs. ATTENUATOR STATE (LOW-CURRENT MODE)



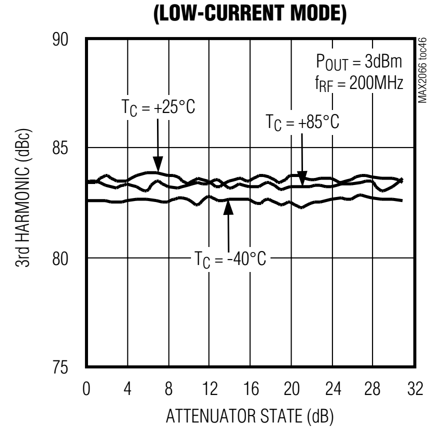
3rd HARMONIC vs. RF FREQUENCY (LOW-CURRENT MODE)



3rd HARMONIC vs. RF FREQUENCY (LOW-CURRENT MODE)

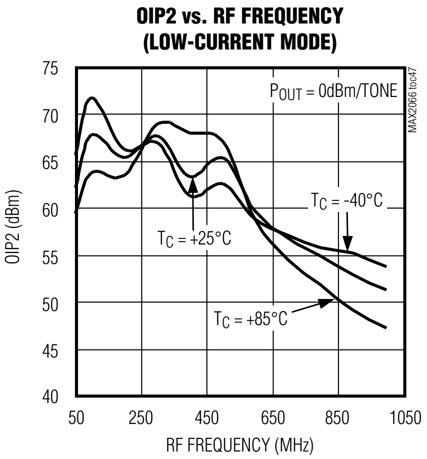


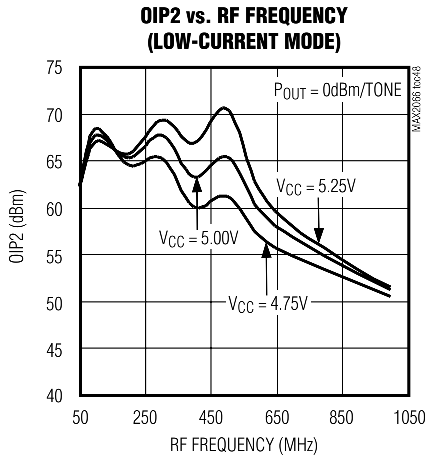
3rd HARMONIC vs. ATTENUATOR STATE (LOW-CURRENT MODE)

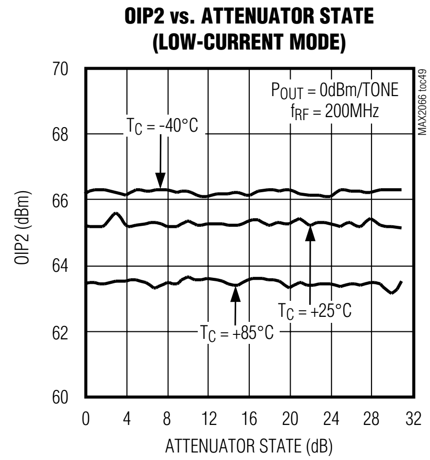


Typical Operating Characteristics (continued)

(**V_{CC} = V_{DD} = +5.0V, LC mode**, digital attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.)





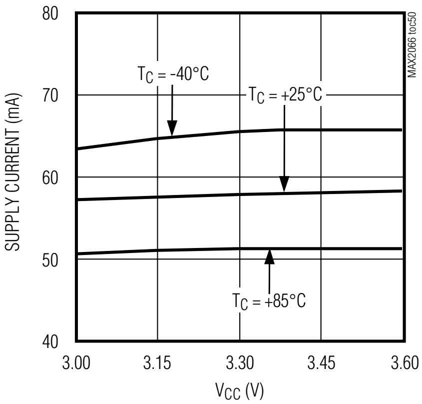


50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

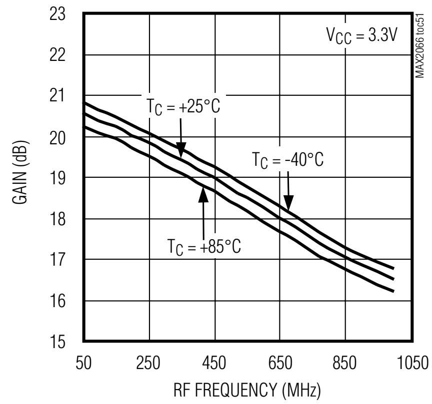
Typical Operating Characteristics (continued)

(**V_{CC} = V_{DD} = +3.3V, HC mode**, digital attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.)

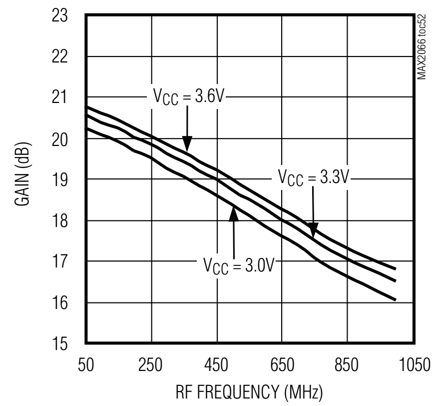
SUPPLY CURRENT vs. SUPPLY VOLTAGE



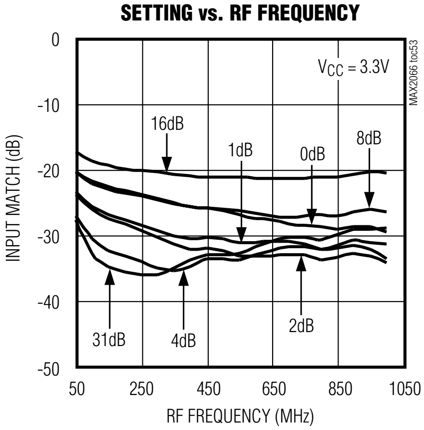
GAIN vs. RF FREQUENCY



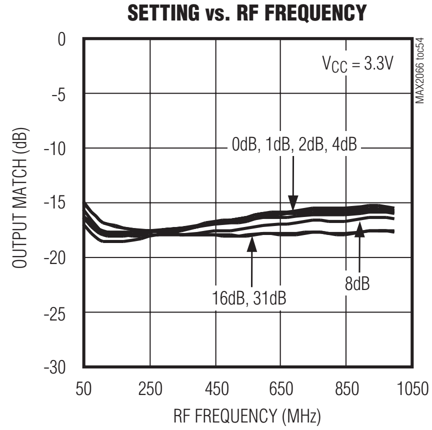
GAIN vs. RF FREQUENCY



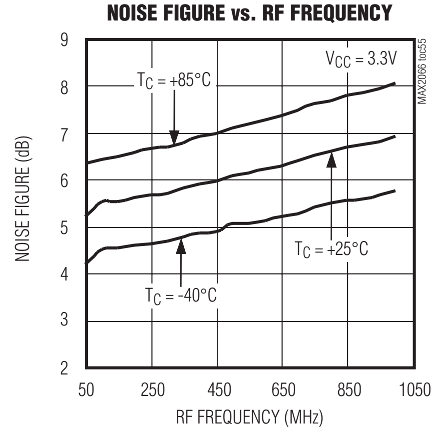
INPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY



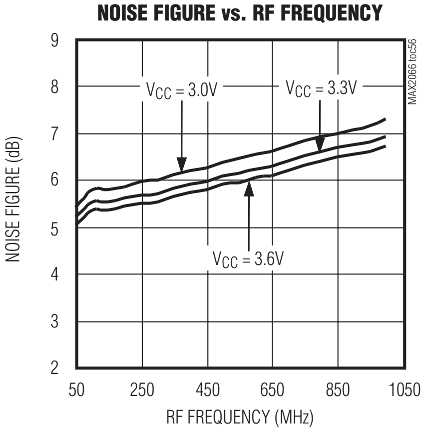
OUTPUT MATCH OVER ATTENUATOR SETTING vs. RF FREQUENCY



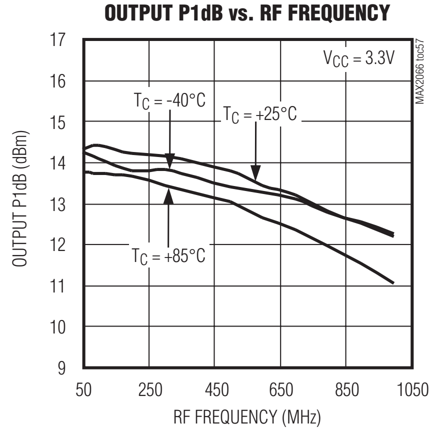
NOISE FIGURE vs. RF FREQUENCY



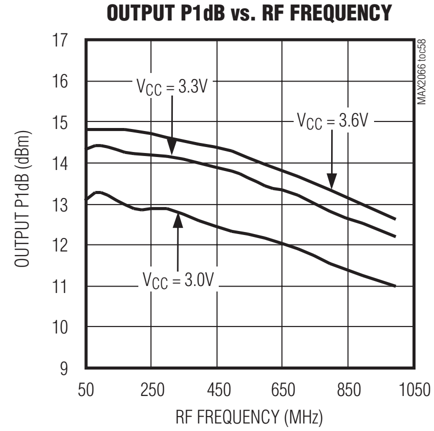
NOISE FIGURE vs. RF FREQUENCY



OUTPUT P1dB vs. RF FREQUENCY



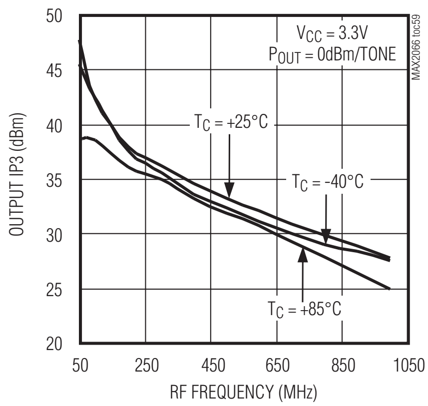
OUTPUT P1dB vs. RF FREQUENCY



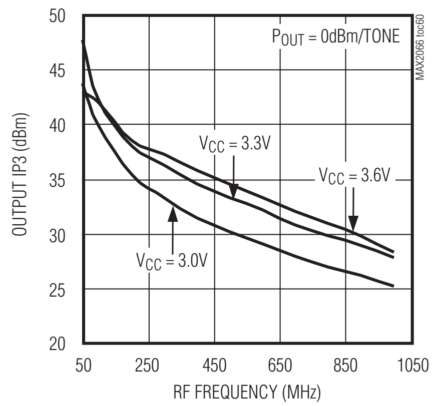
Typical Operating Characteristics (continued)

(**V_{CC} = V_{DD} = +3.3V, HC mode**, digital attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.)

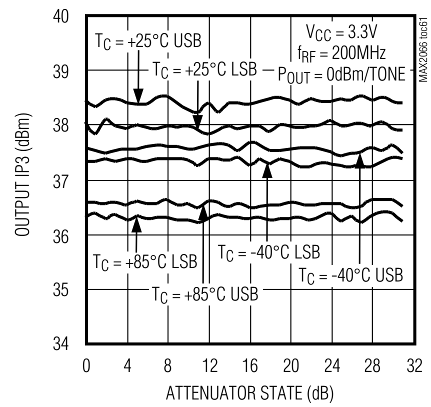
OUTPUT IP3 vs. RF FREQUENCY



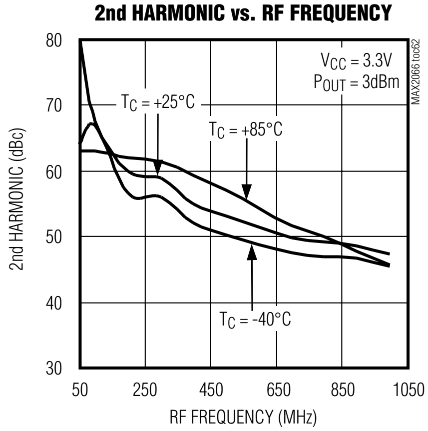
OUTPUT IP3 vs. RF FREQUENCY



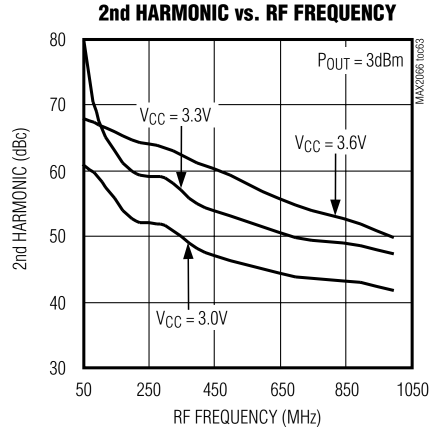
OUTPUT IP3 vs. ATTENUATOR STATE



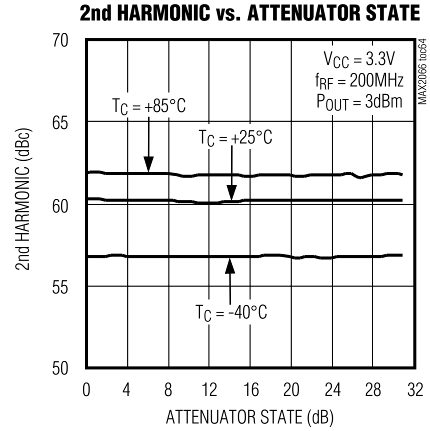
2nd HARMONIC vs. RF FREQUENCY



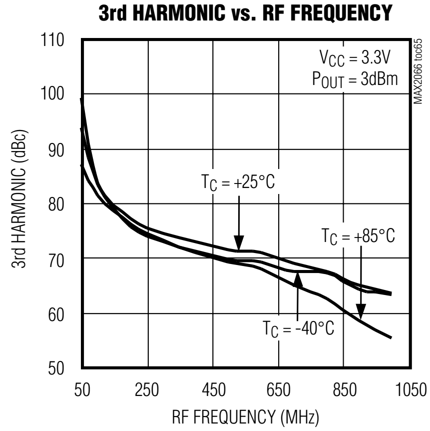
2nd HARMONIC vs. RF FREQUENCY



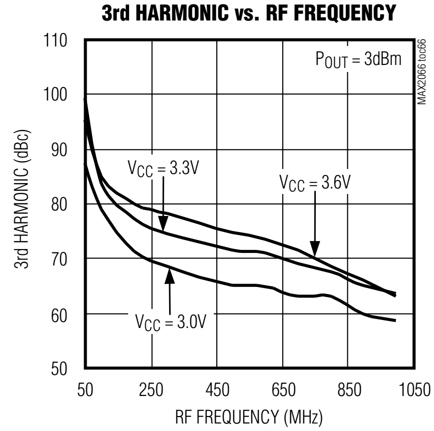
2nd HARMONIC vs. ATTENUATOR STATE



3rd HARMONIC vs. RF FREQUENCY



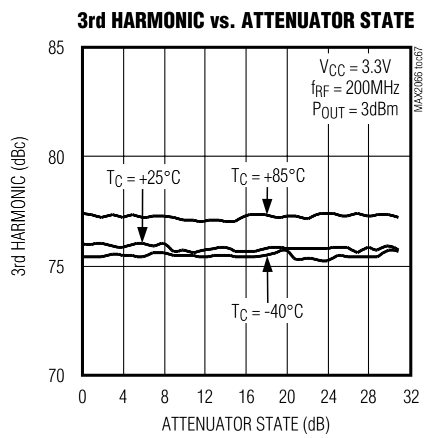
3rd HARMONIC vs. RF FREQUENCY

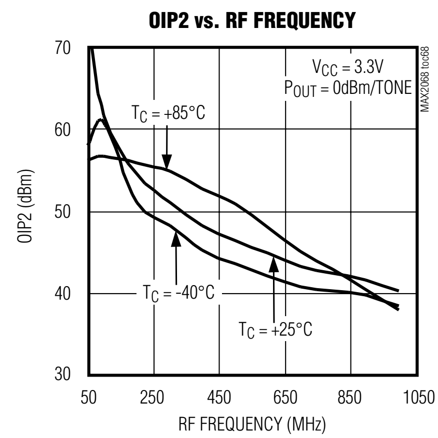


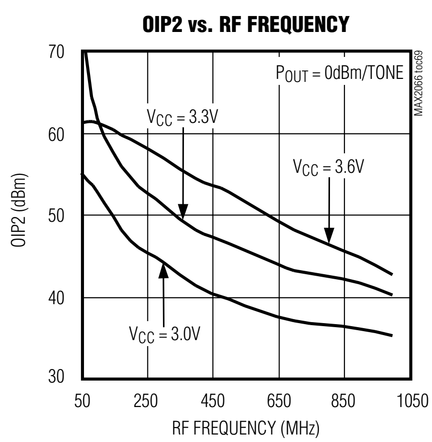
50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

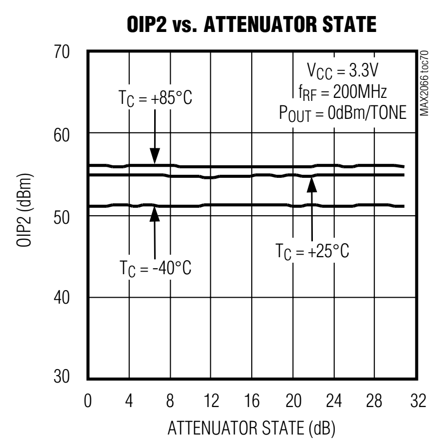
Typical Operating Characteristics (continued)

(**V_{CC} = V_{DD} = +3.3V, HC mode**, digital attenuator set for maximum gain, P_{IN} = -20dBm, f_{RF} = 200MHz, and T_C = +25°C, unless otherwise noted.)









Pin Description

PIN	NAME	DESCRIPTION
1, 16, 19, 22, 24–28, 30, 31, 33–36	GND	Ground
2, 3, 32, 37–40	GND	Ground. See the *Pin-Compatibility Considerations* section.
4	DATA	SPI Data Digital Input
5	CLK	SPI Clock Digital Input
6	$\overline{CS}$	SPI Chip-Select Digital Input
7	VDD_LOGIC	Digital Logic Supply Input. Connect to the digital logic power supply, V_{DD}. Bypass to GND with a 10nF capacitor as close as possible to the pin.
8	SER/PAR	Digital Attenuator SPI or Parallel Control Selection Logic Input. Logic 0 = parallel control, Logic 1 = serial control.
9	STATE_A	Digital Attenuator Preprogrammed Attenuation State Logic Input
10	STATE_B	**State A** / **State B** / **Digital Attenuator** Logic = 0 / Logic = 0 / Preprogrammed State 1 Logic = 1 / Logic = 0 / Preprogrammed State 2 Logic = 0 / Logic = 1 / Preprogrammed State 3 Logic = 1 / Logic = 1 / Preprogrammed State 4
11	D4	16dB Attenuator Logic Input. Logic 0 = disable, Logic 1 = enable.
12	D3	8dB Attenuator Logic Input. Logic 0 = disable, Logic 1 = enable.
13	D2	4dB Attenuator Logic Input. Logic 0 = disable, Logic 1 = enable.
14	D1	2dB Attenuator Logic Input. Logic 0 = disable, Logic 1 = enable.
15	D0	1dB Attenuator Logic Input. Logic 0 = disable, Logic 1 = enable.
17	AMP_OUT	Driver Amplifier Output (50Ω). See the *Typical Application Circuit* for details.
18	RSET	Driver Amplifier Bias Setting. See the *External Bias* section.
20	AMP_IN	Driver Amplifier Input (50Ω). See the *Typical Application Circuit* for details.
21	VCC_AMP	Driver Amplifier Supply Voltage Input. Connect to the V_{CC} power supply. Bypass to GND with 1000pF and 10nF capacitors as close as possible to the pin with the smaller value capacitor closer to the part.
23	ATTEN_OUT	5-Bit Digital Attenuator Output (50Ω). Internally matched to 50Ω. Requires an external DC blocking capacitor.
29	ATTEN_IN	5-Bit Digital Attenuator Input (50Ω). Internally matched to 50Ω. Requires an external DC blocking capacitor.
—	EP	Exposed Pad. Internally connected to GND. Connect EP to GND for proper RF performance and enhanced thermal dissipation.

50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

Detailed Description

The MAX2066 high-linearity digital variable-gain amplifier is a general-purpose, high-performance amplifier designed to interface with 50Ω systems operating in the 50MHz to 1000MHz frequency range.

The MAX2066 integrates a digital attenuator to provide 31dB of gain control, as well as a driver amplifier optimized to provide high gain, high IP3, low noise figure, and low power consumption. For applications that do not require high linearity, the bias current of the amplifier can be adjusted by an external resistor to further reduce power consumption.

The attenuator is controlled as a slave peripheral using either the SPI-compatible interface or a parallel bus with 31dB total adjustment range in 1dB steps. An added feature allows “rapid-fire” gain selection between each of the four unique steps (preprogrammed by the user through the SPI-compatible interface). The 2-pin control allows the user to quickly access any one of four customized attenuation states without reprogramming the SPI bus. Because each stage has its own external RF input and RF output, this component can be configured to either optimize NF (amplifier configured first), or OIP3 (amplifier last). The device’s performance features include 22dB standalone amplifier gain (amplifier only), 5.2dB NF at maximum gain (includes attenuator insertion loss), and a high OIP3 level of +42.4dBm. Each of these features makes the MAX2066 an ideal VGA for numerous receiver and transmitter applications.

In addition, the MAX2066 operates from a single +5V supply, or a single +3.3V supply with slightly reduced performance, and has adjustable bias to trade current consumption for linearity performance.

5-Bit Digital Attenuator Control

The MAX2066 integrates a 5-bit digital attenuator to achieve a high level of dynamic range. The digital attenuator has a 31dB control range, a 1dB step size, and is programmed either through a dedicated 5-bit parallel bus or through the 3-wire SPI. See the *Applications Information* section and Table 1 for attenuator programming details. The attenuator can be used for both static and dynamic power control.

Driver Amplifier

The MAX2066 includes a high-performance driver with a fixed gain of 22dB. The driver amplifier circuit is optimized for high linearity for the 50MHz to 1000MHz frequency range.

Applications Information

SPI Interface and Attenuator Settings

The attenuator can be programmed through the 3-wire SPI/MICROWIRE™-compatible serial interface using 5-bit words. Twenty-eight bits of data are shifted in MSB first and framed by $\overline{CS}$. When $\overline{CS}$ is low, the clock is active and data is shifted on the rising edge of the clock. When $\overline{CS}$ transitions high, the data is latched and the attenuator setting changes (Figure 1). See Table 2 for details on the SPI data format.

Table 1. Control Logic

SER/PAR	ATTENUATOR
0	Parallel controlled
1	SPI controlled

MICROWIRE is a trademark of National Semiconductor Corp.

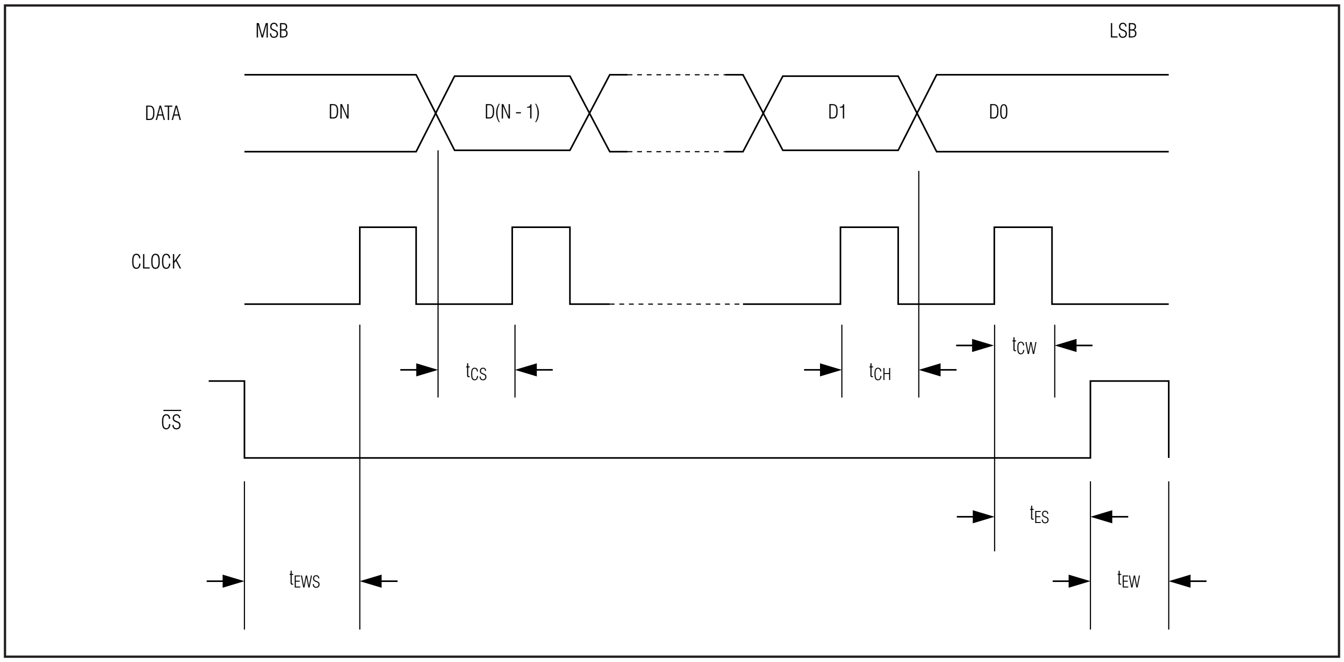


Figure 1. SPI Timing Diagram

Table 2. SPI Data Format

FUNCTION	BIT	DESCRIPTION
Digital Attenuator State 4	D27 (MSB)	16dB step (MSB of the 5-bit word used to program the digital attenuator state 4)
	D26	8dB step
	D25	4dB step
	D24	2dB step
	D23	1dB step (LSB)
Digital Attenuator State 3	D22	5-bit word used to program the digital attenuator state 3 (see the description for digital attenuator state 4)
	D21	
	D20	
	D19	
	D18	
Digital Attenuator State 2	D17	5-bit word used to program the digital attenuator state 2 (see the description for digital attenuator state 4)
	D16	
	D15	
	D14	
	D13	
Digital Attenuator State 1	D12	5-bit word used to program the digital attenuator state 1 (see the description for digital attenuator state 4)
	D11	
	D10	
	D9	
	D8	

50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

Table 2. SPI Data Format (continued)

FUNCTION	BIT	DESCRIPTION
Reserved	D7	Bits D[7:0] are reserved. Set to logic 0.
	D6	
	D5	
	D4	
	D3	
	D2	
	D1	
	D0 (LSB)	

Digital Attenuator Settings Using the Parallel Control Bus

To capitalize on its fast 25ns switching capability, the MAX2066 offers a supplemental 5-bit parallel control interface. The digital logic attenuator-control pins (D0–D4) enable the attenuator stages (Table 3).

Direct access to this 5-bit bus enables the user to avoid any programming delays associated with the SPI interface. One of the limitations of any SPI bus is the speed at which commands can be clocked into each peripheral device. By offering direct access to the 5-bit parallel interface, the user can quickly shift between digital attenuator states as needed for critical "fast-attack" automatic gain-control (AGC) applications.

"Rapid-Fire" Preprogrammed Attenuation States

The MAX2066 has an added feature that provides "rapid-fire" gain selection between four preprogrammed attenuation steps. As with the supplemental 5-bit bus mentioned above, this "rapid-fire" gain selection allows the user to quickly access any one of four customized digital attenuation states without incurring the delays associated with reprogramming the device through the SPI bus.

The switching speed is comparable to that achieved using the supplemental 5-bit parallel bus. However, by employing this specific feature, the digital attenuator I/O is further reduced by a factor of either 5 or 2.5 (5 control bits vs. 1 or 2, respectively) depending on the number of states desired.

The user can employ the STATE_A and STATE_B logic-input pins to apply each step as required (Table 4). Toggling just the STATE_A pin (one control bit) yields two preprogrammed attenuation states; toggling both the STATE_A and STATE_B pins together (two control bits) yields four preprogrammed attenuation states.

Table 3. Digital Attenuator Settings (Parallel Control)

INPUT	LOGIC = 0 (OR GROUND)	LOGIC = 1
D0	Disable 1dB attenuator, or when SPI is default programmer	Enable 1dB attenuator
D1	Disable 2dB attenuator, or when SPI is default programmer	Enable 2dB attenuator
D2	Disable 4dB attenuator, or when SPI is default programmer	Enable 4dB attenuator
D3	Disable 8dB attenuator, or when SPI is default programmer	Enable 8dB attenuator
D4	Disable 16dB attenuator, or when SPI is default programmer	Enable 16dB attenuator

As an example, assume that the AGC application requires a static attenuation adjustment to trim out gain inconsistencies within a receiver lineup. The same AGC circuit can also be called upon to dynamically attenuate an unwanted blocker signal that could de-sense the receiver and lead to an ADC overdrive condition. In this example, the MAX2066 would be preprogrammed (through the SPI bus) with two customized attenuation states—one to address the static gain trim adjustment, the second to counter the unwanted blocker condition. Toggling just the STATE_A control bit enables the user to switch quickly between the static and dynamic attenuation settings with only one I/O pin.

If desired, the user can also program two additional attenuation states by using the STATE_B control bit as a second I/O pin. These two additional attenuation settings are useful for software-defined radio applications where multiple static gain settings may be needed to account for different frequencies of operation, or where multiple dynamic attenuation settings are needed to account for different blocker levels (as defined by multiple wireless standards).

External Bias

Bias currents for the driver amplifier are set and optimized through external resistors. Resistors R1 and R1A connected to RSET (pin 18) set the bias current for the amplifier. The external biasing resistor values can be increased for reduced current operation at the expense of performance. See Tables 6 and 7 for details.

+5V and +3.3V Supply Voltage

The MAX2066 features an optional +3.3V supply voltage operation with slightly reduced linearity performance.

Pin-Compatibility Considerations

The MAX2066 is a simplified version of the MAX2065 analog/digital VGA. The MAX2066 does not contain an analog attenuator, on-chip DAC, or internal reference. The associated input/output pins are internally connected to ground (Table 5). Ground the unused input/output pins to optimize isolation. (See the *Typical Application Circuit*.)

Table 4. Preprogrammed Attenuation State Settings

STATE_A	STATE_B	DIGITAL ATTENUATOR
0	0	Preprogrammed attenuation state 1
1	0	Preprogrammed attenuation state 2
0	1	Preprogrammed attenuation state 3
1	1	Preprogrammed attenuation state 4

Layout Considerations

The pin configuration of the MAX2066 has been optimized to facilitate a very compact physical layout of the device and its associated discrete components.

The exposed paddle (EP) of the MAX2066's 40-pin thin QFN-EP package provides a low thermal-resistance path to the die. It is important that the PCB on which the MAX2066 is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP **must** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes.

Table 5. MAX2065/MAX2066 Pin Comparison

PIN	MAX2065	MAX2066
2	VREF_SELECT	GND
3	VDAC_EN	GND
32	ATTEN1_OUT	GND
37	ATTEN1_IN	GND
38	VCC_ANALOG	GND
39	ANALOG_VCTRL	GND
40	VREF_IN	GND

50MHz to 1000MHz High-Linearity, Serial/Parallel-Controlled Digital VGA

Table 6. Typical Application Circuit Component Values (HC Mode)

DESIGNATION	VALUE	SIZE	VENDOR	DESCRIPTION
C1, C2, C7	10nF	0402	Murata Mfg. Co., Ltd.	X7R
C3, C4, C6, C8, C9	1000pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitors
L1	470nH	1008	Coilcraft, Inc.	1008CS-471XJLC
R1, R1A	10Ω	0402	Vishay	1%
R2 (+3.3V applications only)	1kΩ	0402	Panasonic Corp.	1%
R3 (+3.3V applications only)	2kΩ	0402	Panasonic Corp.	1%
U1	—	40-pin thin QFN-EP (6mm x 6mm)	Maxim Integrated Products, Inc.	MAX2066ETL+

Table 7. Typical Application Circuit Component Values (LC Mode)

DESIGNATION	VALUE	SIZE	VENDOR	DESCRIPTION
C1, C2, C7	10nF	0402	Murata Mfg. Co., Ltd.	X7R
C3, C4, C6, C8, C9	1000pF	0402	Murata Mfg. Co., Ltd.	C0G ceramic capacitors
L1	470nH	1008	Coilcraft, Inc.	1008CS-471XJLC
R1	24Ω	0402	Vishay	1%
R1A	0.01µF	0402	Murata Mfg. Co., Ltd.	X7R
R2 (+3.3V applications only)	1kΩ	0402	Panasonic Corp.	1%
R3 (+3.3V applications only)	2kΩ	0402	Panasonic Corp.	1%
U1	—	40-pin thin QFN-EP (6mm x 6mm)	Maxim Integrated Products, Inc.	MAX2066ETL+

Amplitude Overshoot Reduction

To reduce amplitude overshoot during digital attenuator state change, connect a bandpass filter (parallel LC type) from ATTEN_OUT (pin 23) to ground. L = 18nH and C = 47pF are recommended for 169MHz operation (Figure 2). Contact the factory for recommended components for other operating frequencies.

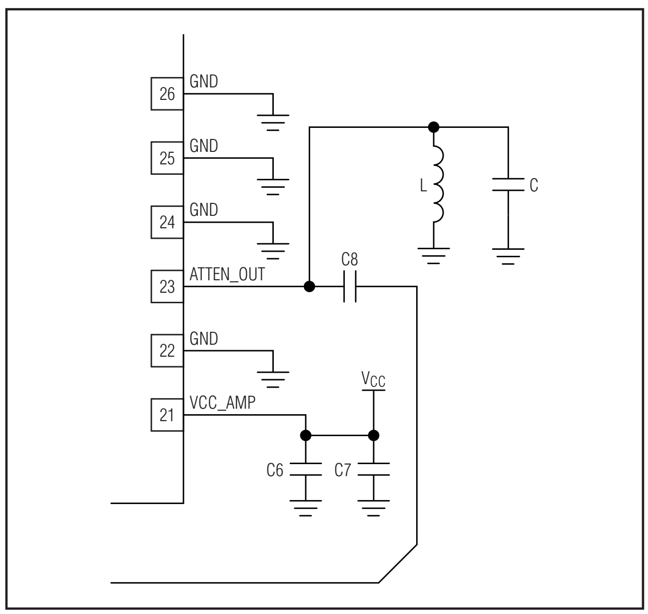
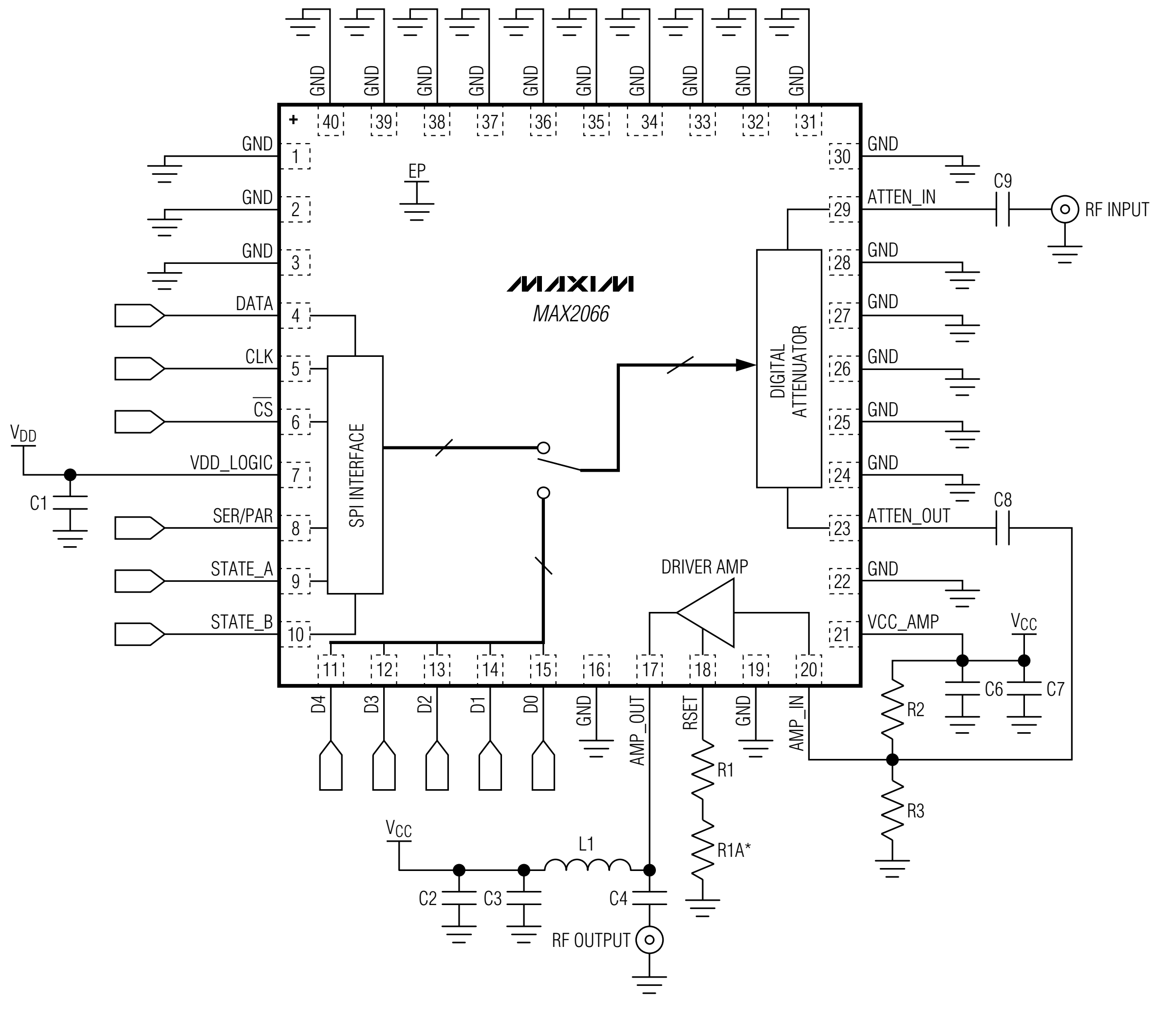


Figure 2. Bandpass Filter to Reduce Amplitude Overshoot

Typical Application Circuit



*IN LC MODE, R1A IS A 0.01µF CAPACITOR. SEE TABLE 7 FOR DETAILS.

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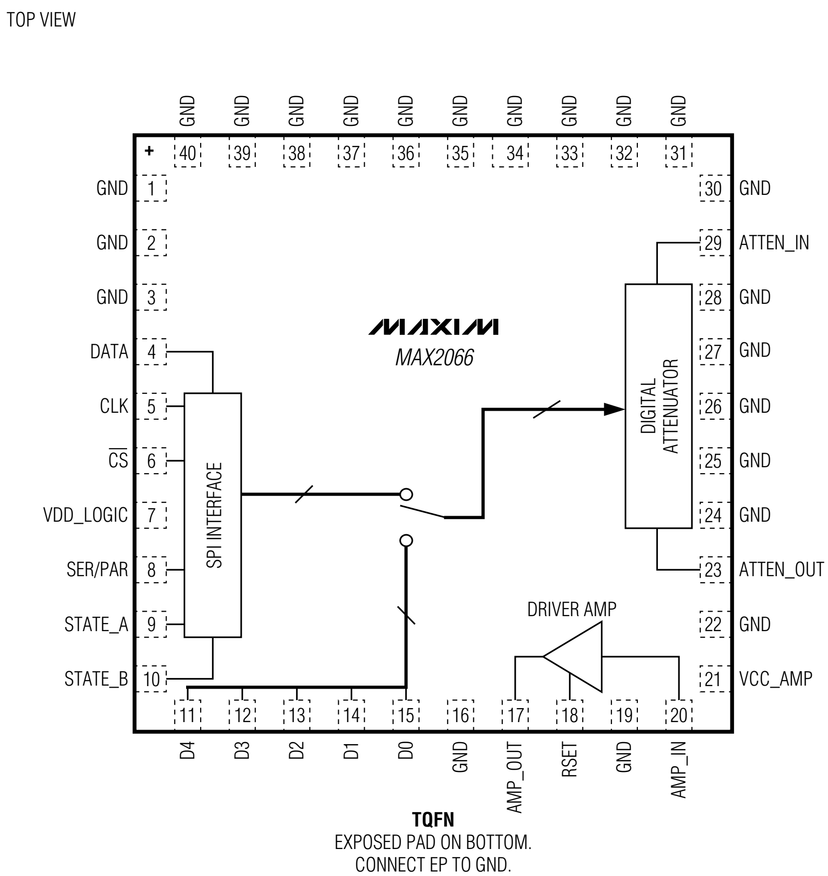
Pin Configuration/Functional Block Diagram



Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
40 Thin QFN-EP	T4066-3	21-0141

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- Техническая поддержка проекта;
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