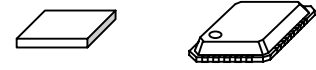


1/3, 1/4 Duty LCD Driver

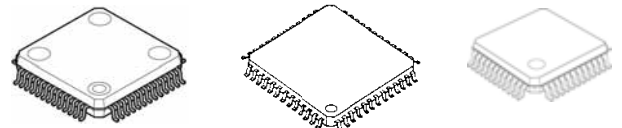
■ GENERAL DESCRIPTION

NJU6533 is a 1/3 or 1/4 duty segment type LCD driver. It incorporates 4 common driver circuits and 32 segment driver circuits. **NJU6533** can drive maximum 96 segments in 1/3 duty ratio and maximum 128 segments in 1/4 duty ratio. In addition, the **NJU6533's** useful functions and small package meet a wide range of applications.

■ PACKAGE OUTLINE



NJU6533C **NJU6533KQ1**

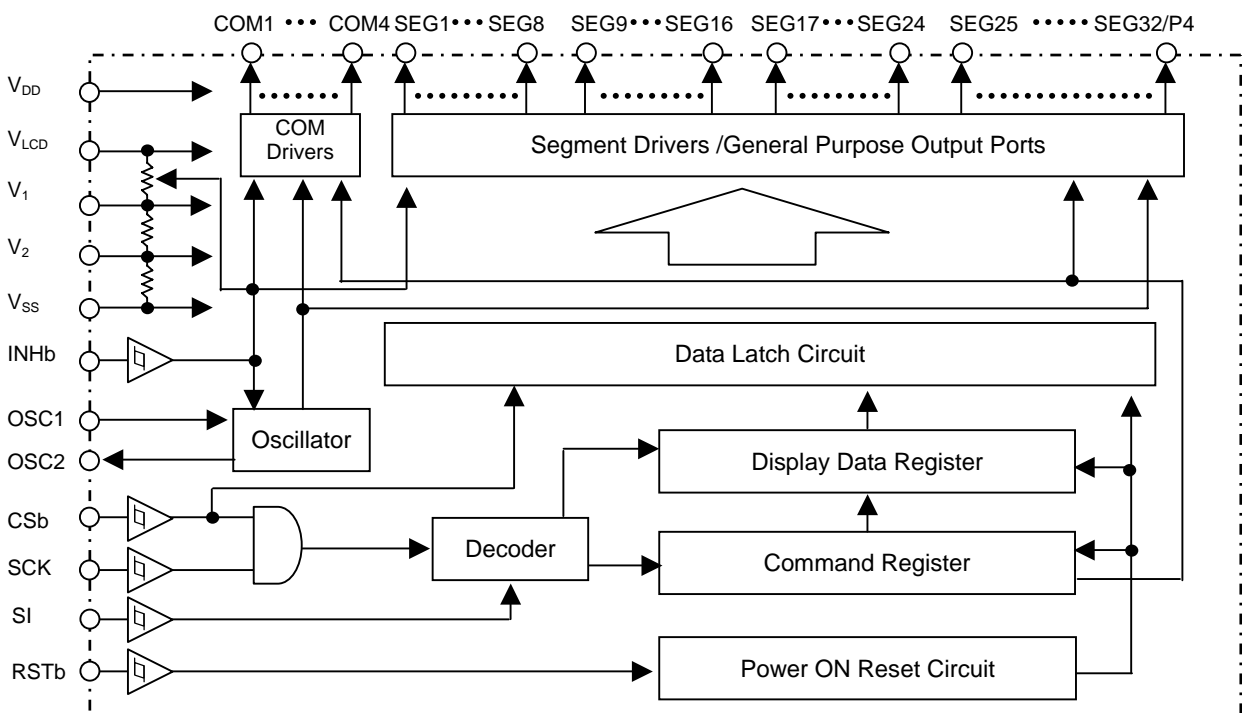


NJU6533FA2 **NJU6533FH2** **NJU6533FR3**

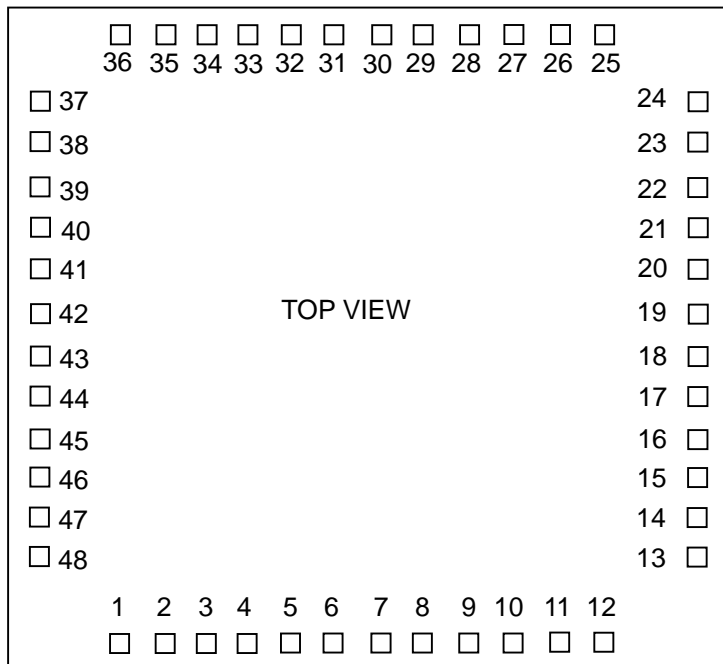
■ FEATURES

- LCD driving circuit :Max. 32outputs (4 outputs as for general purpose ports)
- Programmable Duty Ratio
 - 1/3 duty ratio :Driving max. 96 segments
 - 1/4 duty ratio :Driving max. 128 segments
- Programmable Bias Ratio :1/2, 1/3 bias ratio
- Serial Data Transfer :Shift clock max. 2MHz
- Built-in Oscillator :CR oscillation with external resistor, or external oscillation signal input
- Display OFF :INHb terminal
- Operating Voltage :3V / 5.0V
- C-MOS Technology :P-Sub
- Package Outline :Bare Chip, QFN48-Q1, QFP52-A2, LQFP52-H2, LQFP48-R3

■ BLOCK DIAGRAM



■ PAD LOCATION



Chip Center : X=0 μ m, Y=0 μ m
 Chip Size : X= 2.60 mm, Y= 2.36 mm
 Chip Thickness : 625 μ m \pm 25 μ m
 PAD Size : 90.0 μ m x 90.0 μ m
 PAD Pitch : 126 μ m
 Sub Striate : P

■ PAD COORDINATES

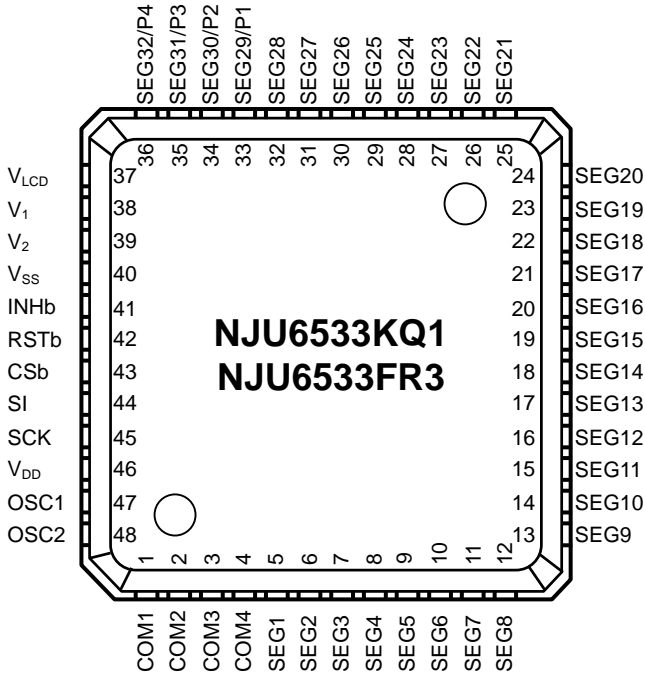
Chip Size 2.60 x 2.36 mm(Chip Center X=0 μ m, Y=0 μ m)

| PAD No. | PAD NAME | X= μ m | Y= μ m |
|---------|----------|------------|------------|
| 1 | COM1 | -686 | -1019 |
| 2 | COM2 | -560 | -1019 |
| 3 | COM3 | -434 | -1019 |
| 4 | COM4 | -308 | -1019 |
| 5 | SEG1 | -182 | -1019 |
| 6 | SEG2 | -56 | -1019 |
| 7 | SEG3 | 70 | -1019 |
| 8 | SEG4 | 196 | -1019 |
| 9 | SEG5 | 322 | -1019 |
| 10 | SEG6 | 448 | -1019 |
| 11 | SEG7 | 574 | -1019 |
| 12 | SEG8 | 700 | -1019 |
| 13 | SEG9 | 1138 | -739 |
| 14 | SEG10 | 1138 | -613 |
| 15 | SEG11 | 1138 | -487 |
| 16 | SEG12 | 1138 | -361 |
| 17 | SEG13 | 1138 | -235 |
| 18 | SEG14 | 1138 | -109 |
| 19 | SEG15 | 1138 | 17 |
| 20 | SEG16 | 1138 | 143 |
| 21 | SEG17 | 1138 | 269 |
| 22 | SEG18 | 1138 | 395 |
| 23 | SEG19 | 1138 | 521 |
| 24 | SEG20 | 1138 | 647 |

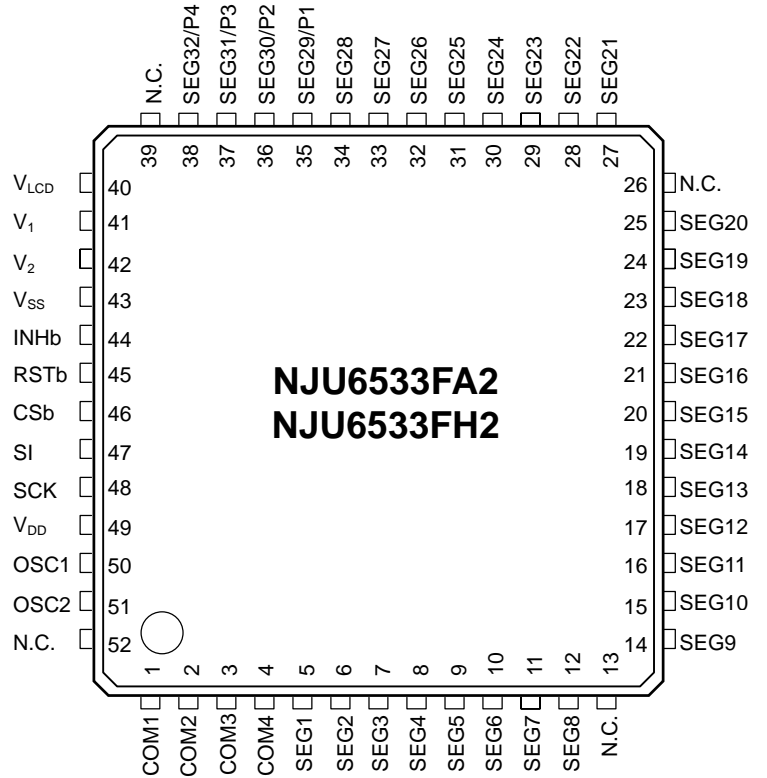
| PAD No. | PAD NAME | X= μ m | Y= μ m |
|---------|------------------|------------|------------|
| 25 | SEG21 | 784 | 1019 |
| 26 | SEG22 | 658 | 1019 |
| 27 | SEG23 | 532 | 1019 |
| 28 | SEG24 | 406 | 1019 |
| 29 | SEG25 | 280 | 1019 |
| 30 | SEG26 | 154 | 1019 |
| 31 | SEG27 | 28 | 1019 |
| 32 | SEG28 | -98 | 1019 |
| 33 | SEG29/P1 | -356 | 1019 |
| 34 | SEG30/P2 | -482 | 1019 |
| 35 | SEG31/P3 | -837 | 1019 |
| 36 | SEG32/P4 | -963 | 1019 |
| 37 | V _{LCD} | -1138 | 914 |
| 38 | V ₁ | -1138 | 790 |
| 39 | V ₂ | -1138 | 557 |
| 40 | V _{SS} | -1138 | 432 |
| 41 | INHb | -1138 | 236 |
| 42 | RSTb | -1138 | 112 |
| 43 | CSb | -1138 | -121 |
| 44 | SI | -1138 | -245 |
| 45 | SCK | -1138 | -479 |
| 46 | V _{DD} | -1138 | -603 |
| 47 | OSC1 | -1138 | -845 |
| 48 | OSC2 | -1138 | -971 |

■ PIN CONFIGURATION

• QFN48-Q1 / LQFP48-R3



• QFP52-A2 / LQFP52-H2



■ TERMINAL DISCRIPTION

| Bare Chip | No. | | Pad Name | Function |
|-----------|-----------------------|--------------------------|------------------------------------|---|
| | QFN48-Q1 LQFP48-R3 | QFP52-A2 LQFP52-H2 | | |
| 46 | 46 | 49 | V _{DD} | ● Power supply: 3V /5V |
| 37 | 37 | 40 | V _{LCD} | LCD driving voltage $V_{LCD} \geq V_1 \geq V_2 \geq V_{SS}$, $V_{LCD} \geq V_{DD}$ |
| 38, 39 | 38, 39 | 41, 42 | V ₁ , V ₂ | Bias At 1/3 bias ratio, keep V ₁ - V ₂ open. At 1/2 bias ratio, short V ₁ - V ₂ . |
| 40 | 40 | 43 | V _{SS} | GND V _{SS} =0V |
| 41 | 41 | 44 | INHb | Display OFF * When INHb is "H", display is ON, and when INHb is "L", display is off. When SEG29(P1)~SEG32 (P4) are selected as general purpose output ports, even if input "0" to INHb terminal, SEG29~32 will still be recognized as general purpose output ports. |
| 42 | 42 | 45 | RSTb | Reset When RSTb is "L", command register and latch circuit is reset. |
| 43 | 43 | 46 | CSb | Chip select When CSb is "L", data can be read in. |
| 44 | 44 | 47 | SI | Serial data input (8 bit=1 word) |
| 45 | 45 | 48 | SCK | Serial clock |
| 47, 48 | 47, 48 | 50, 51 | OSC1, OSC2 | External resistor connection terminal for CR oscillation, or external clock input terminal When external clock is used, input the signal to OSC1 and keep OSC2 open. |
| 1~4 | 1~4 | 1~4 | COM1 ~ COM4 | Common driver outputs |
| 5~32 | 5~32 | 5~12, 14~25, 27~34 | SEG1 ~ SEG28 | Segment driver outputs |
| 33~36 | 33~36 | 35~39 | SEG29/P1~ SEG32/P4 | Segment driver outputs/general purpose output ports These 4 terminals can be used as segment outputs or general purpose output ports by setting Command Register. When selected as general purpose ports, data can be outputted via these ports during COM1 timing. According to transferred data, "H"=V _{DD} or "L"=V _{SS} will be outputted. |
| - | - | 13,26, 39,52 | NC | Non Connection These pins must be open. |

*: For details about INHb, please refer to "■ FUNCTION DESCRIPTION (5) Display OFF function (INHb terminal)".

■ FUNCTION DESCRIPTION

(1) Block Function

- Oscillator
The oscillator includes a built-in capacitor and an external resistor. It generates clock signal for LCD driving. When use external clock, input the clock signal to OSC1 and keep OSC2 open.
- Decoder
Input serial data is decoded and sent to the appropriate block.
- Command Register
Command data is written to this 8 bits command register to control **NJU6533** operation.
- Display Data Register
Data is written to this 8 bits register as display data.
- Latch Circuit
Data stored in display data register is assigned to the corresponding SEG/port.
- Segment Driver/General Purpose Ports
Basing on display data, segment drivers output LCD SEG driving signal.
And, SEG29/P1 ~ SEG32/P4 terminals can be selected as segment driver output or general-purpose ports by instruction.
- Common Driver
Common drivers output LCD COM driving signal.
- Power On Reset
When power is on, **NJU6533** is automatically initialized. And if RSTb="L", **NJU6533** is reset too.

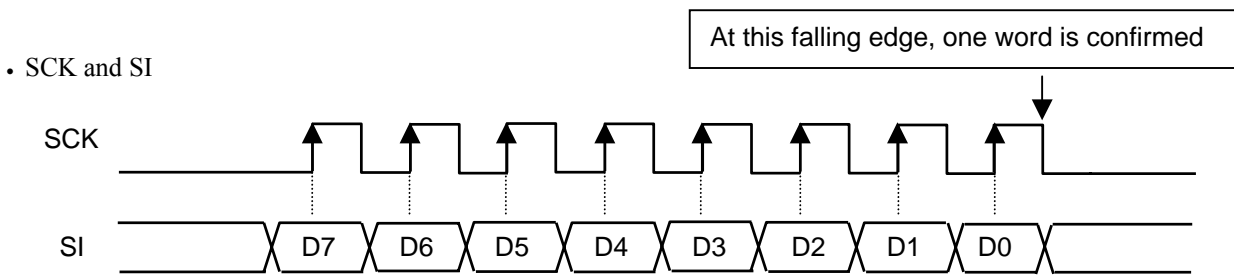
(2) Serial Data Transfer

The transfer of an 8-bit/word serial data is conducted by synchronizing clock via interface with CPU. During CSb="L", serial data is obtainable and will be read in at the rising edge of SCK signal.

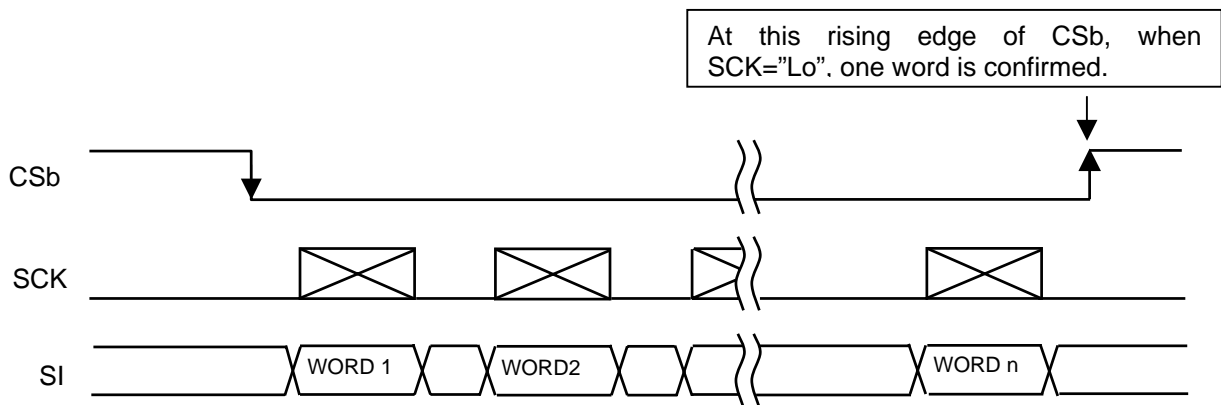
After CSb becoming low, if the first word is address data, the after data can be transferred continually and interrupted as display data even if CSb maintained low. In this case, every 8 bits data will be confirmed as a word either by the falling edge of the 8th SCK clock or by the rising edge of the CSb clock.

After CSb becoming low, if the first word is command data, the after data is invalid even though transfer can be continued without changing the polarity of CSb.

At the falling edge of CSb, SCK can be either "H" or "L", but, at the rising edge of CSb, SCK must be low.



Timing of Serial Data Transfer



Serial Interface Format

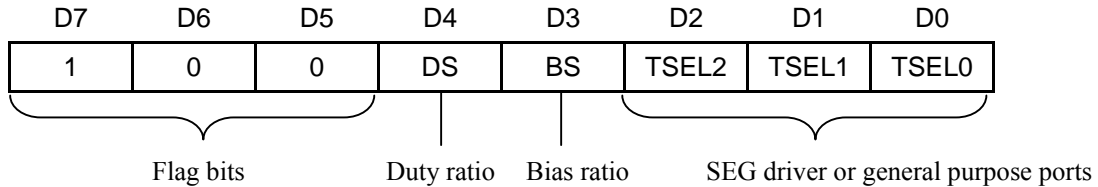
(3) Command Register

Command Register is used to set the duty ratio, the bias ratio, and the SEG driver/general purpose ports. When the D7 to D5 bits of the 1st word are (1,0,0), the D4 ~ D0 bits are recognized as command data.

The contents of Command Register will be initialized as following when applying Power On Reset or Reset.

The Default Value of Command Register

- Duty ratio : 1/4
- Bias ratio : 1/3
- SEG driver/General purpose ports : SEG drivers(SEG29, SEG30, SEG31, SEG32)



• Duty Ratio

| DS | Duty ratio |
|----|------------|
| 0 | 1/4 |
| 1 | 1/3 |

*) Do not change the duty ratio during display ON.

• Bias ratio

| BS | Bias ratio |
|----|------------|
| 0 | 1/3 |
| 1 | 1/2 |

• SEG driver or general purpose ports

| TSEL2 | TSEL1 | TSEL0 | SEG29/P1 | SEG30/P2 | SEG31/P3 | SEG32/P4 |
|-------|-------|-------|----------|----------|----------|----------|
| 0 | 0 | 0 | SEG29 | SEG30 | SEG31 | SEG32 |
| 0 | 0 | 1 | SEG29 | SEG30 | SEG31 | P4 |
| 0 | 1 | 0 | SEG29 | SEG30 | P3 | P4 |
| 0 | 1 | 1 | SEG29 | P2 | P3 | P4 |
| 1 | 0 | 0 | P1 | P2 | P3 | P4 |

***) If TSEL2 ~ TSEL0 is set to (1, 0, 1), (1, 1, 0), (1, 1, 1) all outputs are used as segment drivers.

(4) Output Address Counter

Output Address Counter will specify the addresses of the SEG and COM drivers for the display data.

When the MSB (D7 to D4) of the 1st data is "0111", the LSB 4 bits (D3 to D0) specify the addresses of COM and SEG drivers, and the 2nd data is the display data which will be sent to the 1st-data-specified drivers. At the same time, SEG and COM driver addresses will be increased automatically in turn as shown in **Table 1**. In other words, as of the SEG and COM driver addresses specified by the first data in the Output Address Counter, display data can be transferred to the SEG and COM drivers without further address setting.

The address setting range is from "0000" to "1111", if transfer data outnumber the address number which are from D3 ~ D0 to "1111", the SEG and COM driver address will be reset to "0000" and renew the auto-increment operation.

• Address Data

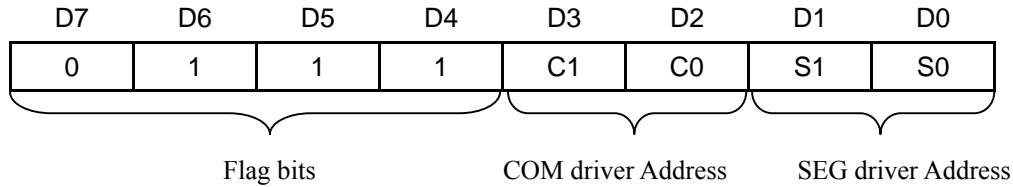


Table 1. The Relationship Between Output Address and SEG/COM Drivers

| Increment Direction | C1 | C0 | S1 | S0 | COM Driver | SEG Driver | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|----|----|----|----|------------|------------|-------|-------|-------|-------|-------|-------|-------|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | SEG6 | SEG7 | SEG8 | SEG9 | SEG10 | SEG11 | SEG12 | SEG13 | SEG14 | SEG15 | SEG16 | SEG17 | SEG18 | SEG19 | SEG20 | SEG21 | SEG22 | SEG23 | SEG24 | SEG25 | SEG26 | SEG27 | SEG28 | SEG29 | SEG30 | SEG31 | SEG32 |
| ↓ | 0 | 0 | 0 | 0 | COM1 | SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | SEG6 | SEG7 | SEG8 | SEG9 | SEG10 | SEG11 | SEG12 | SEG13 | SEG14 | SEG15 | SEG16 | SEG17 | SEG18 | SEG19 | SEG20 | SEG21 | SEG22 | SEG23 | SEG24 | SEG25 | SEG26 | SEG27 | SEG28 | SEG29 | SEG30 | SEG31 | SEG32 |
| | | | 0 | 1 | | SEG9 | SEG10 | SEG11 | SEG12 | SEG13 | SEG14 | SEG15 | SEG16 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 0 | | SEG17 | SEG18 | SEG19 | SEG20 | SEG21 | SEG22 | SEG23 | SEG24 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 1 | | SEG25 | SEG26 | SEG27 | SEG28 | SEG29 | SEG30 | SEG31 | SEG32 | | | | | | | | | | | | | | | | | | | | | | | | |
| ↓ | 0 | 1 | 0 | 0 | COM2 | SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | SEG6 | SEG7 | SEG8 | SEG9 | SEG10 | SEG11 | SEG12 | SEG13 | SEG14 | SEG15 | SEG16 | SEG17 | SEG18 | SEG19 | SEG20 | SEG21 | SEG22 | SEG23 | SEG24 | SEG25 | SEG26 | SEG27 | SEG28 | SEG29 | SEG30 | SEG31 | SEG32 |
| | | | 0 | 1 | | SEG9 | SEG10 | SEG11 | SEG12 | SEG13 | SEG14 | SEG15 | SEG16 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 0 | | SEG17 | SEG18 | SEG19 | SEG20 | SEG21 | SEG22 | SEG23 | SEG24 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 1 | | SEG25 | SEG26 | SEG27 | SEG28 | SEG29 | SEG30 | SEG31 | SEG32 | | | | | | | | | | | | | | | | | | | | | | | | |
| ↓ | 1 | 0 | 0 | 0 | COM3 | SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | SEG6 | SEG7 | SEG8 | SEG9 | SEG10 | SEG11 | SEG12 | SEG13 | SEG14 | SEG15 | SEG16 | SEG17 | SEG18 | SEG19 | SEG20 | SEG21 | SEG22 | SEG23 | SEG24 | SEG25 | SEG26 | SEG27 | SEG28 | SEG29 | SEG30 | SEG31 | SEG32 |
| | | | 0 | 1 | | SEG9 | SEG10 | SEG11 | SEG12 | SEG13 | SEG14 | SEG15 | SEG16 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 0 | | SEG17 | SEG18 | SEG19 | SEG20 | SEG21 | SEG22 | SEG23 | SEG24 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 1 | | SEG25 | SEG26 | SEG27 | SEG28 | SEG29 | SEG30 | SEG31 | SEG32 | | | | | | | | | | | | | | | | | | | | | | | | |
| ↓ | 1 | 1 | 0 | 0 | COM4 | SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | SEG6 | SEG7 | SEG8 | SEG9 | SEG10 | SEG11 | SEG12 | SEG13 | SEG14 | SEG15 | SEG16 | SEG17 | SEG18 | SEG19 | SEG20 | SEG21 | SEG22 | SEG23 | SEG24 | SEG25 | SEG26 | SEG27 | SEG28 | SEG29 | SEG30 | SEG31 | SEG32 |
| | | | 0 | 1 | | SEG9 | SEG10 | SEG11 | SEG12 | SEG13 | SEG14 | SEG15 | SEG16 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 0 | | SEG17 | SEG18 | SEG19 | SEG20 | SEG21 | SEG22 | SEG23 | SEG24 | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 1 | 1 | | SEG25 | SEG26 | SEG27 | SEG28 | SEG29 | SEG30 | SEG31 | SEG32 | | | | | | | | | | | | | | | | | | | | | | | | |

- ◇ If general purpose ports are selected by Command Register, under (C1, C0, S1, S0)=(0, 0, 1, 1), D3 ~ D0 bits are the addresses of (P1, P2, P3, P4) ports which corresponds to (SEG29, SEG30, SEG31, SEG32).
- ◇ When SEG29~SEG32 are set as general purpose output ports, data for SEG29~SEG32 during COM2~COM4 scanning will be ignored.
- ◇ When duty ratio is 1/3, do not set address between "1100"~"1111". Otherwise, unexpected address way be setup.

(5) Display OFF Function (INHb)

When INHb="L"

- All segment and common terminal output V_{SS}
(When general purpose output ports are selected, even INHb="L", these ports can output data)
- Suspending Oscillation (but, if RSTb="L", oscillator works)
- V_1 and V_2 become "H" (no current pass through the bleeder resistors)

Even during INHb="L", interface can be accessed, and data can be written into the command register, address counter and data register.

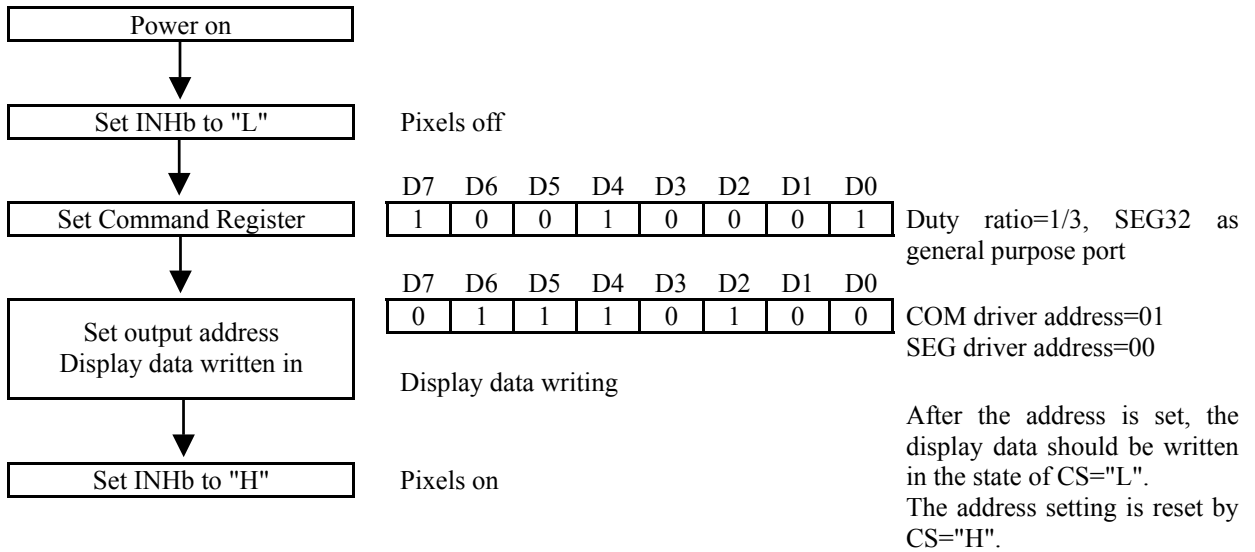
(6) Power ON Reset

After power ON, **NJU6533** is initialized to the following values:

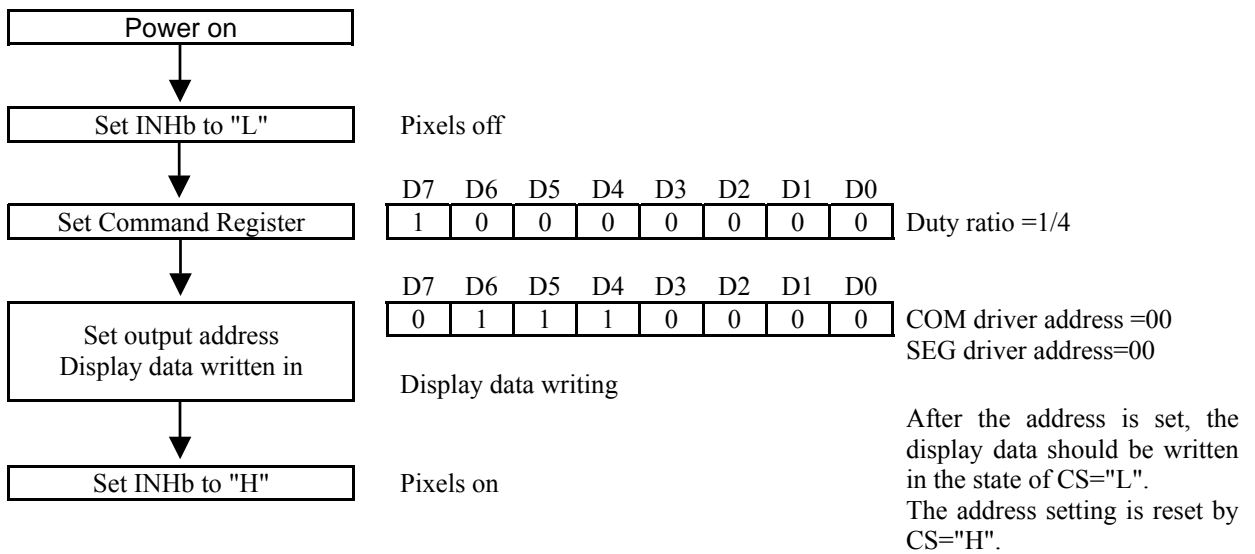
- Address counter (C1, C0, S1, S0)=(0, 0, 0, 0)
- Display Data Register all "0"
- Duty ratio 1/4duty
- Bias ratio 1/3 bias
- Segment/General purpose port: Segment output(SEG29, SEG30, SEG31, SEG32)

(7) Sequence of Initialization

(7-1) 1/3duty, SEG32 used as general purpose port, data written in from COM2.



(7-2) 1/4duty, SEG29 ~ 32 used as SEG drivers, data written in from COM1.



■ ABSOLUTE MAXIMAM RATINGS

(V_{SS}=0V, Ta=25°C)

| PARAMETER | SYMBOL | RATINGS | UNIT | CONDITIONS |
|-------------------|---------------------------------|---|------|---|
| Supply Voltage 1 | V _{DD} | -0.3 ~ +6.0 | V | |
| Supply Voltage 2 | V _{LCD} | -0.3 ~ +6.0 | V | |
| Supply Voltage 3 | V ₁ , V ₂ | -0.3 ~ V _{LCD} +0.3 | V | |
| Input Voltage | V _{IN} | -0.3 ~ V _{DD} +0.3 | V | INHb, CSb, SCK, SI, RSTb, OSC1 applicable. |
| Operating Temp. | T _{opr} | -40 ~ +85 | °C | |
| Storage Temp. | T _{stg} | -55 ~ +125 | °C | |
| Dissipation Power | P _D | 710(QFN48-Q1) 900(QFP52-A2) 890(LQFP52-H2) 1000(LQFP48-R3) | mW | The power dissipation is value mounted on a glass epoxy board in size: 50mm x50mm x1.6mm(QFN48-Q1), 76.2mm x114.3mm x1.6mm (QFP52-A2, LQFP52-H2, LQFP48-R3). |

Note-1) Do not exceed the absolute maximum ratings, otherwise the stress may cause a permanent damage to the IC. It is also recommended that the IC be used within the range specified in the DC electrical characteristics, or the electrical stress may cause mulfuctions and impact on the reliability.

Note-2) All voltages are relative to V_{SS} = 0V reference.

Note-3) The following relationship shall be maintained.

$$V_{LCD} \geq V_1 \geq V_2 \geq V_{SS}, V_{LCD} \geq V_{DD}, \text{ and } V_{LCD} \text{ shall be input after } V_{DD}.$$

Note-4) To stabilize the LSI operation, place decoupling capacitors between V_{DD}-V_{SS} and between V_{LCD}-V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• DC characteristics 1

($V_{DD}=2.4$ to $3.6V$, $V_{SS}=0V$, $T_a=-40$ to $85^{\circ}C$)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT | Note |
|----------------------------|------------|--|-------------------|---------------|-------------------|-----------|------|
| Power Supply | V_{DD} | | 2.4 | | 3.6 | V | |
| LCD Driving Voltage | V_{LCD} | $V_{LCD} \geq V_{DD}$ | 2.4 | | 5.5 | V | |
| LCD Bias Voltage | V_1 | $T_a=25^{\circ}C$ Testing via COM/SEG terminals COM/SEG without load | $2/3 V_{LCD}-0.2$ | $2/3 V_{LCD}$ | $2/3 V_{LCD}+0.2$ | V | |
| | V_2 | | $1/3 V_{LCD}-0.2$ | $1/3 V_{LCD}$ | $1/3 V_{LCD}+0.2$ | V | |
| "H" Level Input Voltage | V_{IH} | INHb, CSb, SCK, SI, RESb, OSC1 | $0.8 V_{DD}$ | | V_{DD} | V | |
| "L" Level Input Voltage | V_{IL} | INHb, CSb, SCK, SI, RESb, OSC1 | 0 | | $0.2 V_{DD}$ | V | |
| Hysteresis Voltage | V_H | INHb, CSb, SCK, SI, RESb | | $0.2V_{DD}$ | | V | |
| "H" Level Input Current | I_{IH} | $V_{IN}=V_{DD}$ INHb, CSb, SCK, SI, RESb | | | 1.0 | μA | |
| "L" Level Input Current | I_{IL} | $V_{IN}=V_{SS}$ INHb, CSb, SCK, SI, RESb | | | 1.0 | μA | |
| "H" Level Output Voltage | V_{OH} | $V_{DD}=3V$, $I_o=5mA$, P1 to P4 | $V_{DD}-0.6$ | | | V | |
| "L" Level Output Voltage | V_{OL} | $V_{DD}=3V$, $I_o=5mA$, P1 to P4 | | | 0.6 | V | |
| Driver-on Resistance (COM) | R_{COM} | $\pm I_d=1\mu A$, $V_{LCD}=3V/5.5V$ | - | - | 10 | $k\Omega$ | 5 |
| Driver-on Resistance (SEG) | R_{SEG} | $\pm I_d=1\mu A$, $V_{LCD}=3V/5.5V$ | - | - | 10 | $k\Omega$ | 5 |
| Oscillating Frequency | f_{OSC} | $V_{DD}=3V$, $R_{OSC}=750k\Omega$, $T_a=25^{\circ}C$ | 12.6 | 15.4 | 18.2 | kHz | |
| External Clock Frequency | f_{CP} | Input into OSC1 | 12.6 | 15.4 | 18.2 | kHz | |
| External Clock Duty | duty | Input into OSC1 | 45 | 50 | 55 | % | |
| Bleeder Resistor | R_B | $V_{LCD}-V_{SS}$ $T_a=25^{\circ}C$ | 127 | 150 | 173 | $k\Omega$ | |
| Operating Current | I_{DD1} | $V_{DD}=3V$, INHb="L", RSTb="H", $T_a=25^{\circ}C$ | | 1.7 | 8.0 | μA | |
| | I_{DD2} | $V_{DD}=3V$, $V_{LCD}=5V$, $T_a=25^{\circ}C$, Checker flag display, 1/3 bias Using internal oscillator, no output | | 7.0 | 25 | μA | |
| | I_{LCD1} | $V_{DD}=3V$, $V_{LCD}=5V$, RSTb="H", INHb="L", $T_a=25^{\circ}C$ | | 0.1 | 1.0 | μA | |
| | I_{LCD2} | $V_{DD}=3V$, $V_{LCD}=5V$, $T_a=25^{\circ}C$, Checker flag display, 1/3 bias Using internal oscillator, no output | | 34 | 60 | μA | |

Note-5) Driver-On resistance (R_{SEG}/R_{COM}) is measured from V_{LCD} , V_{SS} , V_1 or V_2 terminal to each SEG/COM terminal when I_d current flows through COM/SEG terminals.

Note-6) ["H" Level Input Voltage], ["L" Level Input Voltage], [Hysteresis Voltage], ["H" Level Input Current], ["L" Level Input Current], [External Clock Frequency] and [External Clock Duty] are as the same as if $V_{DD}=4.5$ to $5.5V$.

• DC characteristics 2

($V_{DD}=4.5$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $85^{\circ}C$)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT | Note |
|----------------------------|------------|--|-------------------|---------------|-------------------|-----------|------|
| Power Supply | V_{DD} | | 4.5 | | 5.5 | V | |
| LCD Driving Voltage | V_{LCD} | $V_{LCD} \geq V_{DD}$ | 4.5 | | 5.5 | V | |
| LCD Bias Voltage | V_1 | Ta=25°C Testing via COM/SEG terminals COM/SEG without load | 2/3 $V_{LCD}-0.2$ | 2/3 V_{LCD} | 2/3 $V_{LCD}+0.2$ | V | |
| | V_2 | | 1/3 $V_{LCD}-0.2$ | 1/3 V_{LCD} | 2/3 $V_{LCD}+0.2$ | V | |
| "H" Level Input Voltage | V_{IH} | INHb, CSb, SCK, SI, RESb, OSC1 | 0.8 V_{DD} | | V_{DD} | V | |
| "L" Level Input Voltage | V_{IL} | INHb, CSb, SCK, SI, RESb, OSC1 | 0 | | 0.2 V_{DD} | V | |
| Hysteresis Voltage | V_H | INHb, CSb, SCK, SI, RESb | | 0.2 V_{DD} | | V | |
| "H" Level Input Current | I_{IH} | $V_{IN}=V_{DD}$ INHb, CSb, SCK, SI, RESb | | | 1.0 | μA | |
| "L" Level Input Current | I_{IL} | $V_{IN}=V_{SS}$ INHb, CSb, SCK, SI, RESb | | | 1.0 | μA | |
| "H" Level Output Voltage | V_{OH} | $V_{DD}=5V$, $I_O=5mA$, P1 to P4 | $V_{DD}-1.0$ | | | V | |
| "L" Level Output Voltage | V_{OL} | $V_{DD}=5V$, $I_O=5mA$, P1 to P4 | | | 1.0 | V | |
| Driver-on Resistance (COM) | R_{COM} | $\pm I_d=1\mu A$, $V_{LCD}=3V/5.5V$ | - | - | 10 | $k\Omega$ | 7 |
| Driver-on Resistance (SEG) | R_{SEG} | $\pm I_d=1\mu A$, $V_{LCD}=3V/5.5V$ | - | - | 10 | $k\Omega$ | 7 |
| Oscillating Frequency | f_{OSC} | $V_{DD}=5V$, $R_{OSC}=750k\Omega$, $T_a=25^{\circ}C$ | 12.6 | 15.4 | 18.2 | kHz | |
| External Clock Frequency | f_{CP} | Input into OSC1 | 12.6 | 15.4 | 18.2 | kHz | |
| External Clock Duty | duty | Input into OSC1 | 45 | 50 | 55 | % | |
| Bleeder Resistor | R_B | $V_{LCD}-V_{SS}$, $T_a=25^{\circ}C$ | 127 | 150 | 173 | $k\Omega$ | |
| Operating Current | I_{DD1} | $V_{DD}=5V$, INHb="L", RSTb="H", $T_a=25^{\circ}C$ | | 3.2 | 10 | μA | |
| | I_{DD2} | $V_{DD}=5V$, $V_{LCD}=5V$, $T_a=25^{\circ}C$, Checker flag display, 1/3 bias Using internal oscillator, no output | | 15 | 35 | μA | |
| | I_{LCD1} | $V_{DD}=5V$, $V_{LCD}=5V$, INHb="L", RSTb="H", $T_a=25^{\circ}C$ | | 0.1 | 1.0 | μA | |
| | I_{LCD2} | $V_{DD}=5V$, $V_{LCD}=5V$, $T_a=25^{\circ}C$, Checker flag display, 1/3 bias Using internal oscillator, no output | | 34 | 60 | μA | |

Note-7) Driver-On resistance (R_{SEG}/R_{COM}) is measured from V_{LCD} , V_{SS} , V_1 or V_2 terminal to each SEG/COM terminal when I_d current flows through COM/SEG terminals.

Note-8) ["H" Level Input Voltage], ["L" Level Input Voltage], [Hysteresis Voltage], ["H" Level Input Current], ["L" Level Input Current], [External Clock Frequency] and [External Clock Duty] are as the same as if $V_{DD}=2.4$ to $3.6V$.

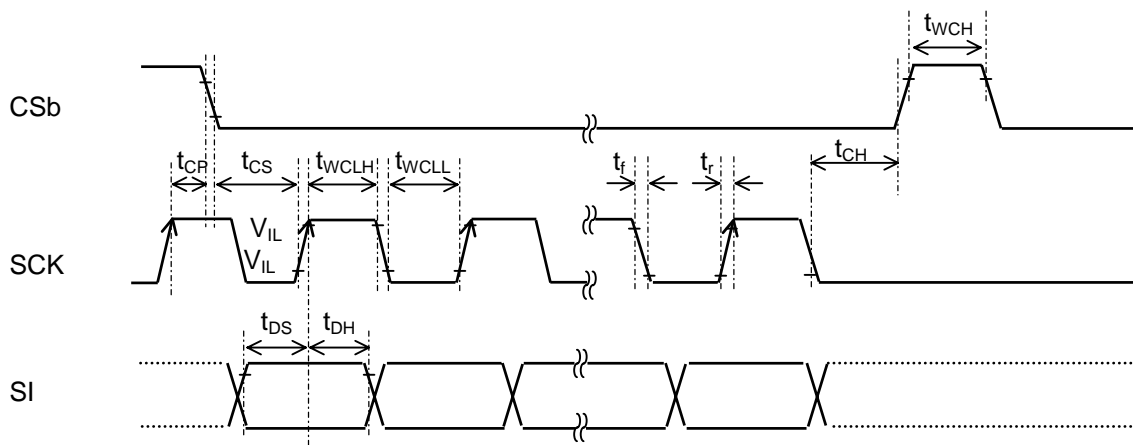
• AC characteristics

($V_{DD}=V_{LCD}=2.4$ to $5.5V$, $V_{SS}=0V$, $T_a=-40$ to $85^{\circ}C$)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT | Note |
|-----------------------------|------------|------------|-----|-----|-----|------|------|
| "L" Level Clock Pulse Width | t_{WCLL} | | 230 | | | ns | |
| "H" Level Clock Pulse Width | t_{WCLH} | | 230 | | | ns | |
| Data Setup Time | t_{DS} | | 20 | | | ns | |
| Data Hold Time | t_{DH} | | 20 | | | ns | |
| CSb Wait Time | t_{CP} | | 50 | | | ns | 9 |
| CSb Setup Time | t_{CS} | | 50 | | | ns | |
| CSb Hold Time | t_{CH} | | 50 | | | ns | |
| CSb"H" Level Pulse Width | t_{WCH} | | 50 | | | ns | |
| Rising Time | t_r | | | | 20 | ns | |
| Falling Time | t_f | | | | 20 | ns | |

Note-9) t_{CP} is the time when SCK is kept at "H" during CSb changed from "H" to "L".

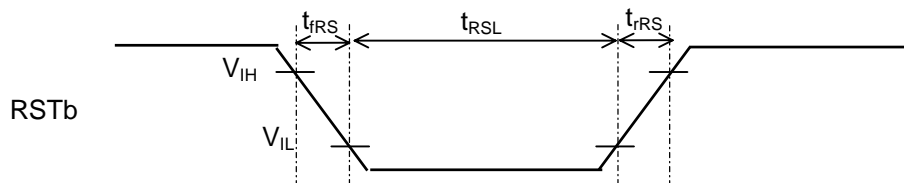
• Input Timing



• Input condition when hardware reset circuit is used

($T_a=25^{\circ}C$)

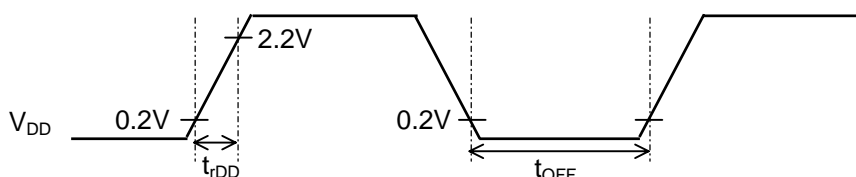
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------|-------------------|-----|-----|-----|------|
| Reset Input "L" Level Width | t_{RSL} | $f_{OSC}=15.4kHz$ | 1.5 | | | ms |
| Reset Rising Time | t_{RFS} | | | | 100 | ns |
| Reset Falling Time | t_{RFS} | | | | 100 | ns |



• Power supply condition when hardware reset circuit is used

($T_a=-40$ to $85^{\circ}C$)

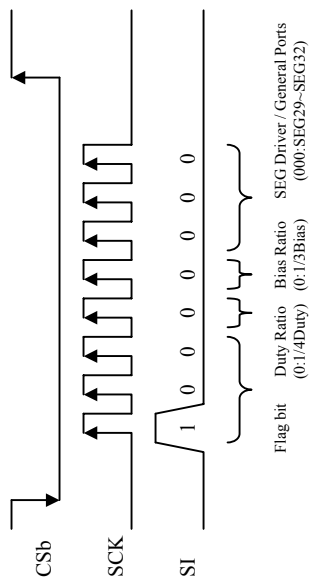
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|-----------|------------|-----|-----|-----|------|
| Power-on Rising Time | t_{rDD} | | 0.1 | | 5 | ms |
| Power-off Time | t_{OFF} | | 1 | | | ms |



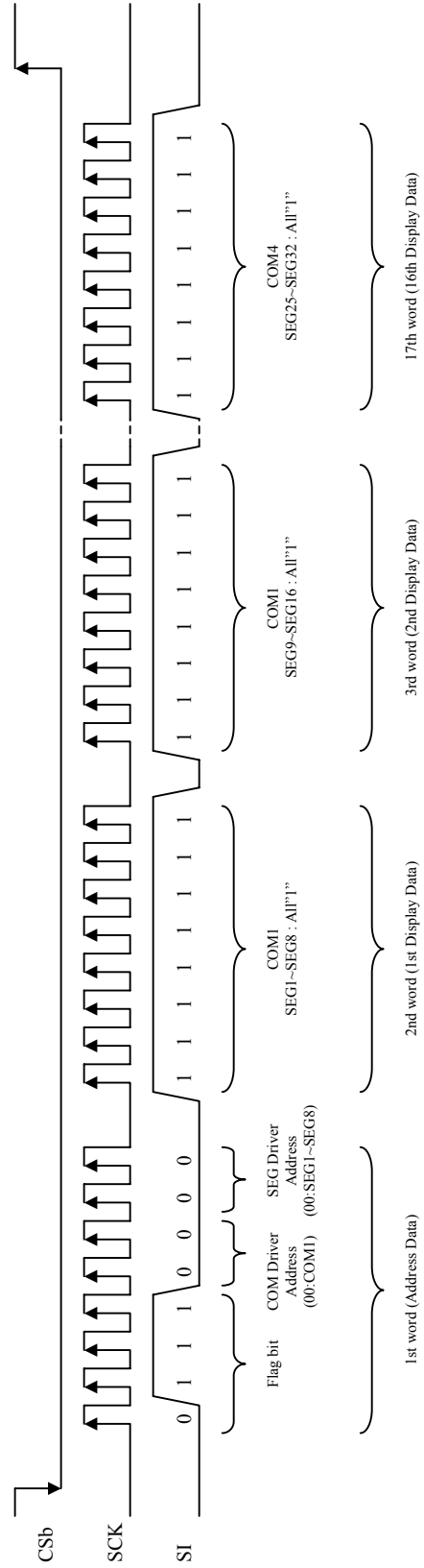
Note 10) t_{OFF} is the off time when power-supply turns off suddenly or cycles on/off.

■ EXAMPLE of SERIAL DATA TRANSFER

- Command Register Set

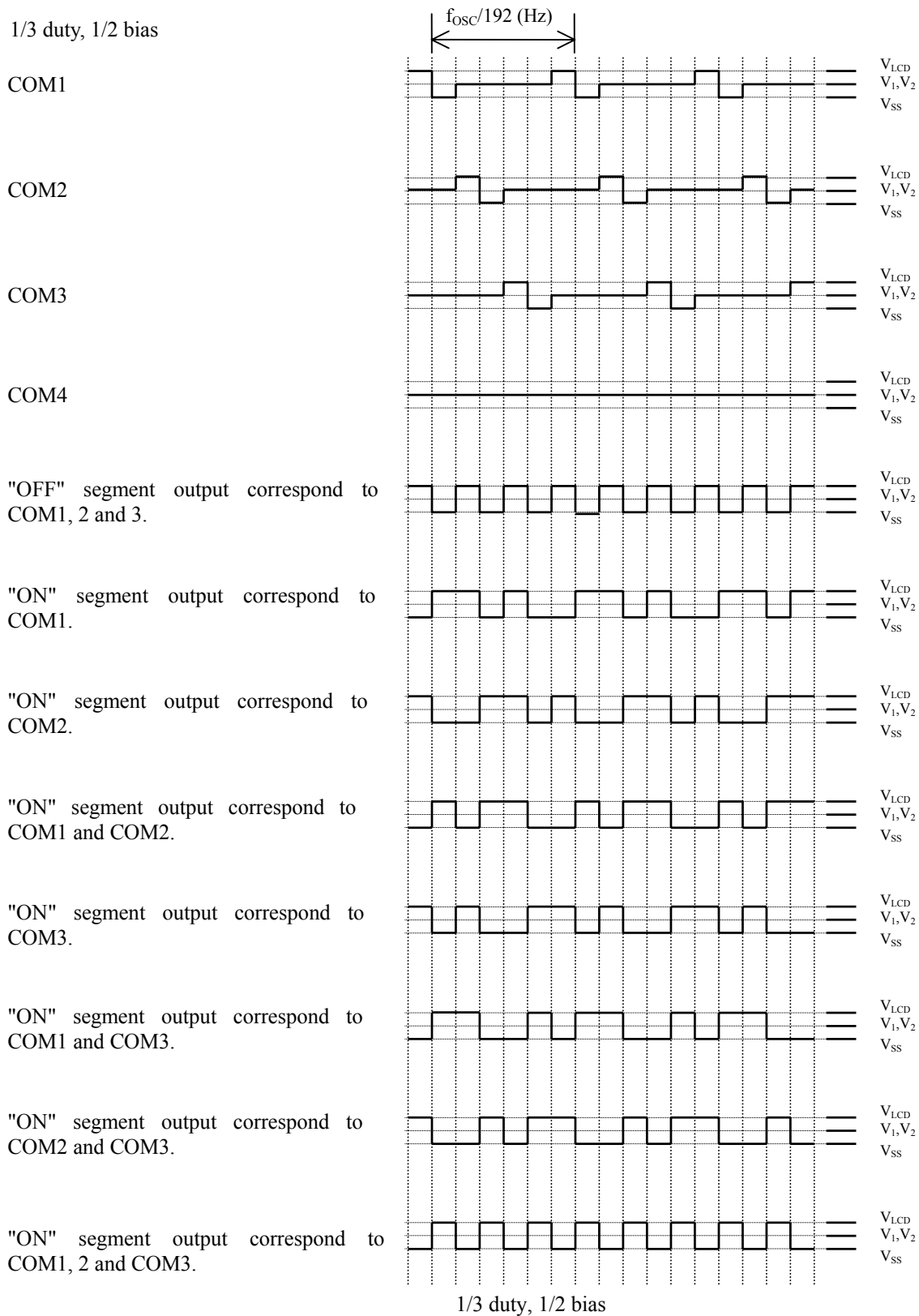


- Address Data & Display Data Set (example : all "1" data writing)

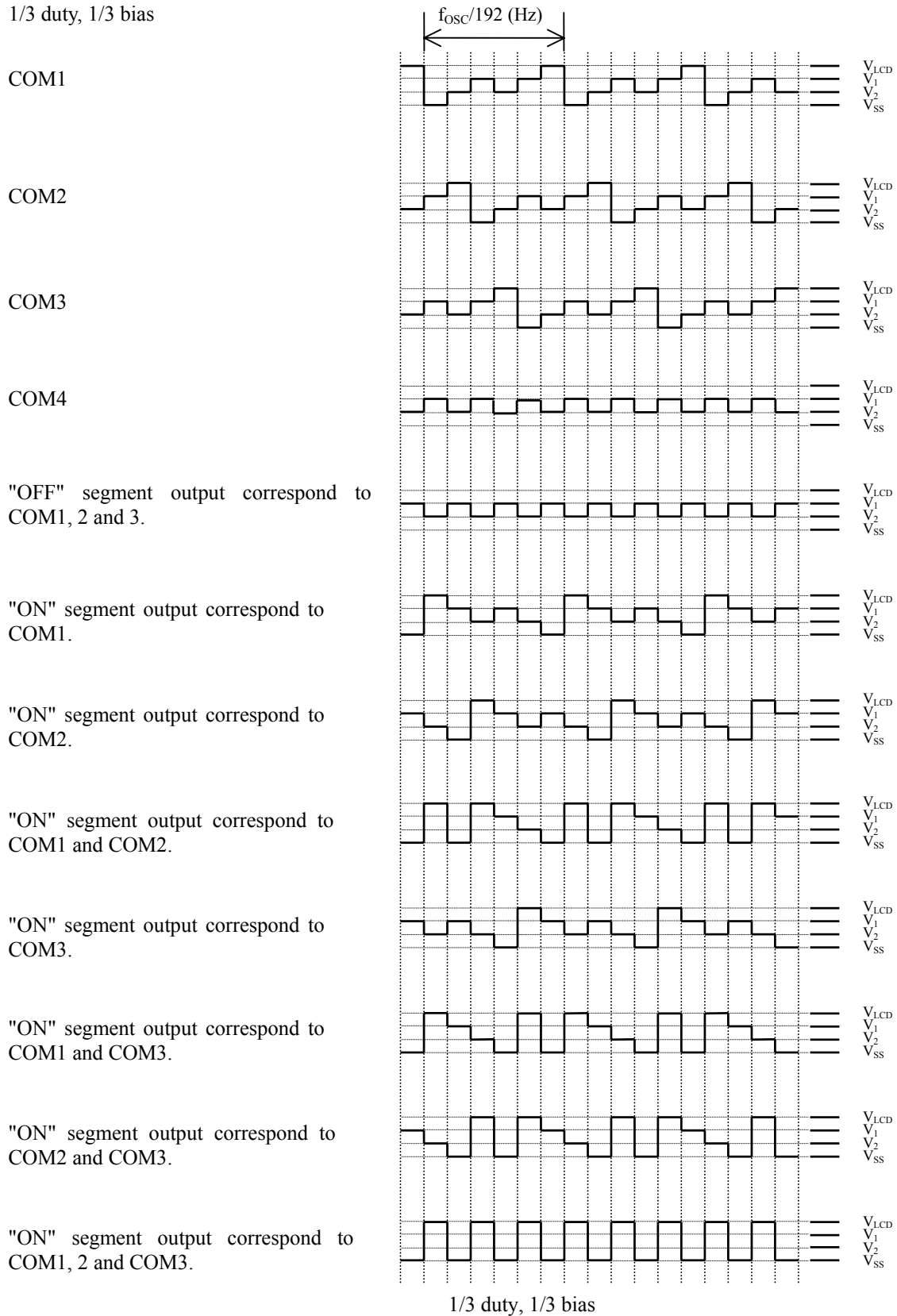


■ LCD DRIVING WAVEFORM

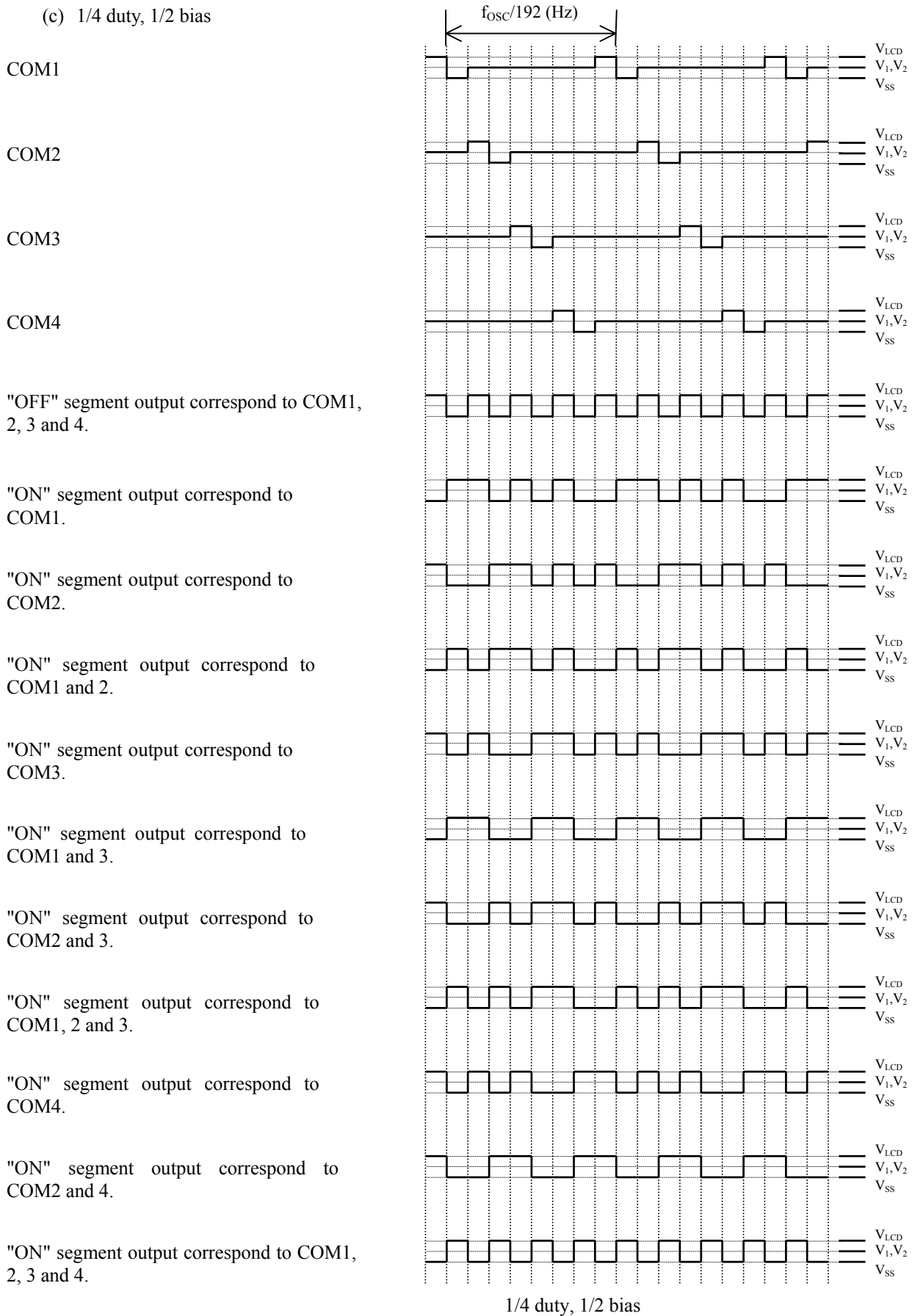
(a) 1/3 duty, 1/2 bias



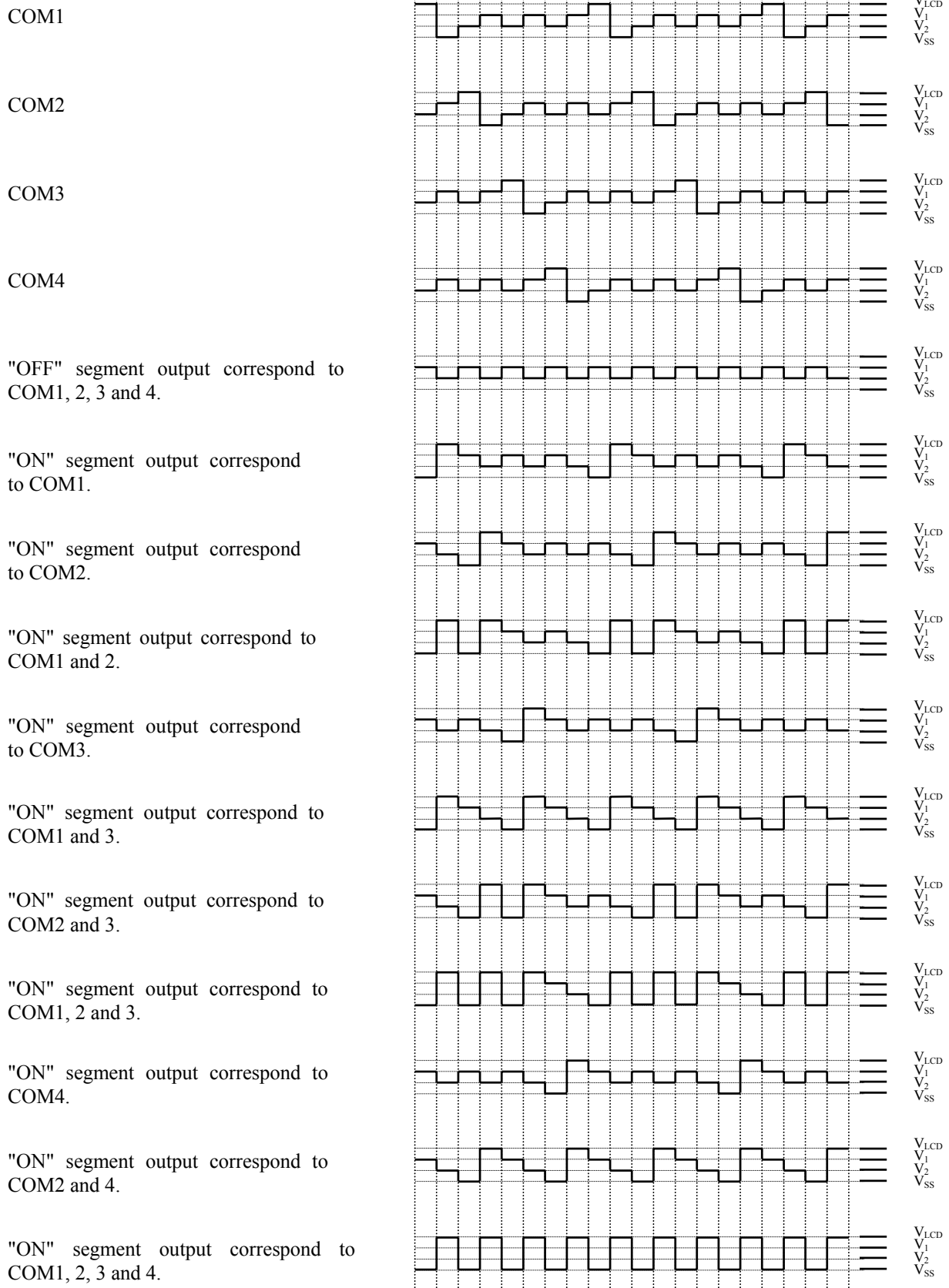
(b) 1/3 duty, 1/3 bias



(c) 1/4 duty, 1/2 bias



(d) 1/4 duty, 1/3 bias

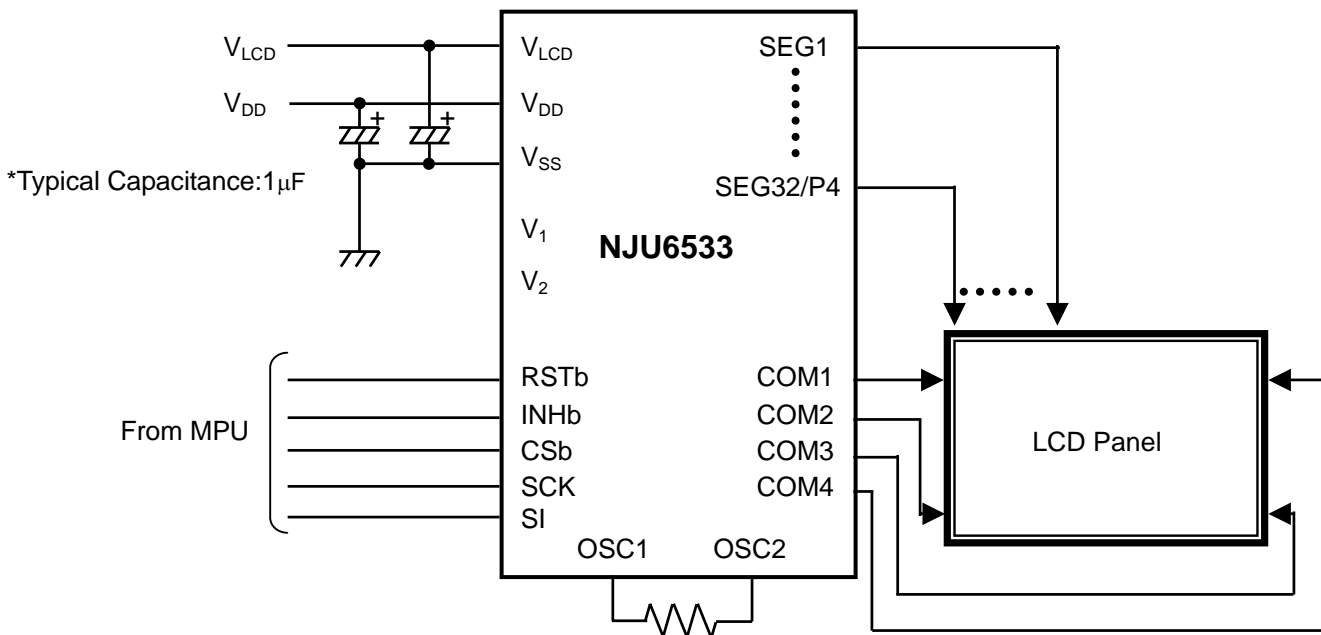


1/4 duty, 1/3 bias

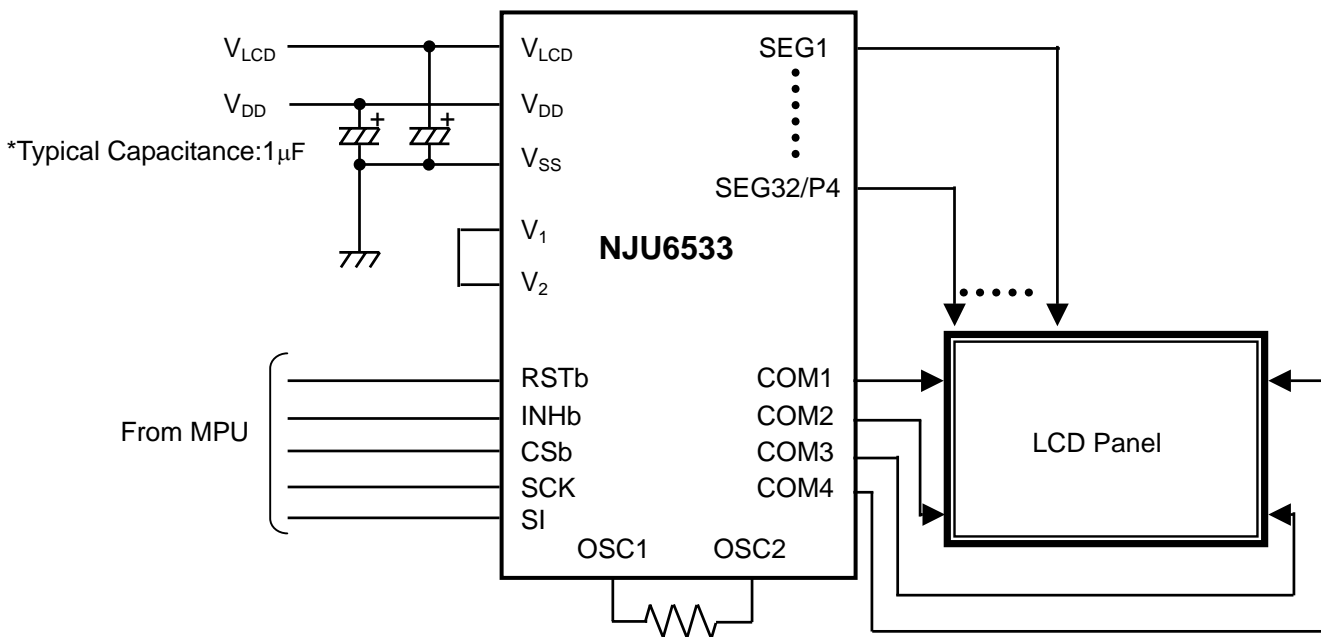
NJU6533

APPLICATION CIRCUIT

- 1/4 duty, 1/3 bias



- 1/4 duty, 1/2 bias



Note) Because display data is not yet stable just after V_{DD} on, if LCD panel is turned on, unexpected pattern will be displayed, therefore, keep INHb terminal to "L" level until data transfer from MPU is over.

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