EVALUATION KIT AVAILABLE

# MAX13325/MAX13326

# Dual Automotive, Audio Line Drivers with I²C Control and Diagnostic

## General Description

The MAX13325/MAX13326 dual audio line drivers provide a reliable differential interface between automotive audio components. The devices feature differential inputs and outputs, integrated output diagnostics, and are controlled using an I²C interface or operate in stand-alone mode. The outputs can deliver up to $4V_{RMS}$ into 100Ω loads.

The MAX13325 buffers analog audio signals for transmission over long cable distances with a fixed gain of 12dB, whereas the MAX13326 provides a 0dB fixed gain. The diagnostics on the outputs report conditions on a per channel basis, including short to GND, short to battery, overcurrent, overtemperature, and excessive offset. The output amplifiers can drive capacitive loads up to 4nF to ground and 3nF differentially.

The outputs are protected according to IEC 61000-4-2 ±8kV Contact Discharge, and ±15kV Air Gap. The MAX13325/MAX13326 are specified from -40°C to +105°C and are available in a 28-pin TSSOP package with an exposed pad.

## Applications

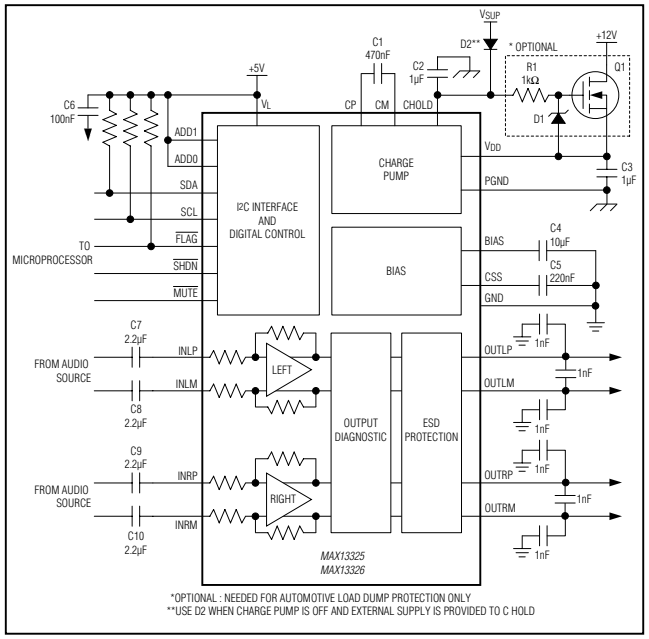
Automotive Radio and Rear Seat Entertainment

Professional Remote Audio Amplifiers

## Features

- **Comprehensive Programmability and Diagnostics Using I²C Interface**
- **Autoretry Function in Stand-Alone Mode**
- **Drive Capacitive Loads ≤ 3nF Differentially, ≤ 4nF to Ground**
- **112dB Signal-to-Noise Ratio**
- **Low 0.002% THD at $4V_{RMS}$ into 2.7kΩ Loads**
- **High PSRR (70dB at 1kHz)**
- **High CMRR (80dB at 1kHz)**
- **Low Output Noise ($3\mu V_{RMS}$), MAX13326**
- **Excellent Channel-to-Channel Matching**
- **Load-Dump Transient Protection**
- **Protected Output Against Various Short-Circuit Conditions**
- **ESD Protection for ±8kV Contact Discharge, ±15kV Air Gap**
- **Long-Distance Drive Capability Typically Up to 15m or Greater**
- **Noise-Rejecting Differential Inputs and Outputs**
- **Low-Power Shutdown Mode < 10µA**
- **Hardware or Software MUTE Function**
- **28-Pin TSSOP Package with Exposed Pad**

## Typical Operating Circuit




## Ordering Information

| PART | PIN-PACKAGE | TEMP RANGE | GAIN (dB) |
|---|---|---|---|
| **MAX13325**GUI/V+ | 28 TSSOP-EP* | -40°C to +105°C | 12 |
| **MAX13326**GUI/V+ | 28 TSSOP-EP* | -40°C to +105°C | 0 |

*/V denotes an automotive qualified part.*

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

**EP = Exposed pad.*

**For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.**

19-5136; Rev 5; 4/13

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to PGND .....-0.3V to +28V
CHOLD .....-0.3V to +28V
$V_L$ to GND .....-0.3V to +6V
GND, PGND .....-0.3V to +0.3V
OUT_ to PGND .....-0.3V to 28V
IN_, BIAS to AGND .....-0.3V to ($V_{DD}$ + 0.3V)
SCL, SDA, ADD0, ADD1, $\overline{MUTE}$, $\overline{SHDN}$, $\overline{FLAG}$ to GND .....-0.3V to +6V
OUT_ Short Circuit to PGND or $V_{DD}$.....Continuous
Short Circuits Between Any OUT_.....Continuous
Continuous Power Dissipation ($T_A$ = +70°C) (multilayer board)
28-Pin TSSOP (derate 27mW/°C above +70°C).....2162.2mW
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## PACKAGE THERMAL CHARACTERISTICS (Note 1)

Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .....37°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$) .....2°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 14.4V, $V_L$ = 5V, $R_L$ = ∞, load impedance from OUT_+ to OUT_-, $T_A$ = $T_J$ = -40°C to +105°C, typical values are $T_A$ = +25°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **AMPLIFIER DC CHARACTERISTICS** | | | | | | | |
| Transient Supply Voltage (Load Dump) | $V_{DDMAX}$ | Using external nMOS-RTR020N05, 300ms duration | | | | 50 | V |
| Operating Supply Voltage Range | $V_{DD}$ | | | 4.5 | | 18 | V |
| | $V_L$ | | | 2.7 | | 5.5 | |
| $V_{DD}$ OVLO Threshold | $V_{DDOV}$ | Rising edge | | 18.5 | 19.2 | | V |
| $V_{DD}$ UVLO Threshold | $V_{DDUV}$ | Falling edge | | 3.3 | 3.5 | | V |
| $V_L$ UVLO Threshold | $V_{LUV}$ | Falling edge | | 2.2 | 2.4 | | V |
| Supply Current | $I_{DD}$ | $T_A$ = +25°C, no load | | | 39 | | mA |
| | | $T_A$ = -40°C to +105°C, no load | | | | 50 | mA |
| Logic Supply Current | $I_L$ | $V_L$ = 5V | | | 1.7 | | mA |
| Shutdown Supply Current | $I_{SHDN}$ | $I_{DD}$ | $T_A$ = +25°C | | 0.5 | 10 | µA |
| | | | $T_A$ = -40°C to +105°C | | 0.5 | | |
| | | $I_L$ | | | < 0.1 | 2 | µA |
| Turn-On Time (from Shutdown) | | $\overline{MUTE}$ = $V_L$ | | | 220 | | ms |
| Turn-On Time (from Mute) | | $\overline{SHDN}$ = $V_L$, $C_{CSS}$ = 220nF | | | 6 | | ms |
| Differential Input Resistance | $R_{INDIF}$ | Measure across input | | 18 | 24 | 30 | kΩ |
| Single-Ended Input Impedance | $R_{IN}$ | Each input to ground (MAX13325) | | 15 | 20 | 25 | kΩ |
| | | Each input to ground (MAX13326) | | 12 | 16 | 20 | |
| Signal-Path Gain (Note 3) | $A_V$ | MAX13325 | | 11.8 | 12 | 12.2 | dB |
| | | MAX13326 | | -0.2 | 0 | +0.2 | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 14.4V, $V_L$ = 5V, $R_L$ = ∞, load impedance from OUT_+ to OUT_-, $T_A$ = $T_J$ = -40°C to +105°C, typical values are $T_A$ = +25°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Channel-to-Channel Gain Tracking | | | | | ±0.4 | dB |
| Differential Mode Output Balance OUT_+ to OUT_- (Note 4) | | | | -40 | | dB |
| Output Offset Voltage (OUT_+ to OUT_-) | $V_{OOS}$ | $\overline{MUTE}$ = GND, $T_A$ = +25°C | | ±0.5 | ±10 | mV |
| | | $\overline{MUTE}$ = $V_L$, $T_A$ = +25°C | | ±0.2 | ±3 | |
| BIAS Voltage | $V_{BIAS}$ | Relative to $V_{DD}$ | | 50 | 52.5 | % |
| BIAS Impedance | $Z_{BIAS}$ | $I_{BIAS}$ = ±10µA | 69 | 92 | 115 | kΩ |
| Output-Voltage Swing Differential | | $V_{DD}$ = 14.4V, $V_{IN}$ = ±14.4V, $R_L$ = 1kΩ | ±12.5 | | | V |
| | | $V_{DD}$ = 5.0V, $V_{IN}$ = ±5V, $R_L$ = 1kΩ | ±4.2 | | | |
| Power-Supply Rejection Ratio | PSRR | $V_{DD}$ = 4.5V to 18V | -80 | -96 | | dB |
| | | $V_{DD}$ = 14.5V, +500m$V_{P-P}$ ripple at 1kHz | | -95 | | |
| | | $V_{DD}$ = 14.5V, +500m$V_{P-P}$ ripple at 10kHz | | -80 | | |
| Common-Mode Rejection Ratio | CMRR | $V_{IN}$ = 1$V_{RMS}$, 100Hz to 10kHz | -48 | -80 | | dB |
| **AMPLIFIER AC CHARACTERISTICS** | | | | | | |
| Total Harmonic Distortion Plus Noise (Note 5) | THD+N | $V_{OUT}$ = 4$V_{RMS}$, $R_L$ = 2.7kΩ | | 0.002 | | % |
| | | $V_{OUT}$ = 4$V_{RMS}$, $R_L$ = 1kΩ | | 0.004 | | |
| | | $V_{OUT}$ = 4$V_{RMS}$, $R_L$ = 100Ω, $V_{DD}$ = 8V | | 0.03 | | |
| | | $V_{OUT}$ = 7$V_{RMS}$, $R_L$ = 1kΩ | | 0.2 | | |
| Total Harmonic Distortion Plus Noise at $V_{DD}$ = 5V (Note 5) | THD+N | $V_{OUT}$ = 1$V_{RMS}$, $R_L$ = 2.7kΩ | | 0.01 | | % |
| | | $V_{OUT}$ = 1$V_{RMS}$, $R_L$ = 1kΩ | | 0.02 | | |
| | | $V_{OUT}$ = 2$V_{RMS}$, $R_L$ = 1kΩ | | 0.8 | | |
| Capacitive-Load Stability | | | | | 3 | nF |
| Capacitive-Load Drive Capability | | No sustained oscillation, $C_{LOAD}$ to GND | | | 4 | nF |
| | | No sustained oscillation, $C_{LOAD}$ differential | | | 3 | |
| Signal-to-Noise Ratio (Note 5) | SNR | MAX13325, gain = 12dB, $V_{OUT}$ = 4$V_{RMS}$, A-weighted | | 112 | | dB |
| | | MAX13326, gain = 0dB, $V_{OUT}$ = 4$V_{RMS}$, A-weighted | | 122 | | |
| Unity-Gain Bandwidth | | | | 3 | | MHz |
| Output Slew Rate | | | | 2.5 | | V/µs |
| Output-Voltage Noise | | A-weighted, MAX13325 | | 10 | | µV |
| | | A-weighted, MAX13326 | | 3 | | |
| Crosstalk | | $V_{IN}$ = 1$V_{RMS}$, 1kHz | | -110 | | dB |
| Mute Time | | To achieve soft mute, $C_{CSS}$ = 220nF | | 4 | | ms |
| Mute Attenuation | | $V_{IN}$ = 1$V_{RMS}$, 1kHz | | -75 | | dB |
| Click-and-Pop Level (Note 6) | $K_{CP}$ | Into and out of mute | | -70 | | dBV |
| Click-and-Pop Level (Note 6) | $K_{CP}$ | Into and out of shutdown, 1kΩ | | -45 | | dBV |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 14.4V, $V_L$ = 5V, $R_L$ = ∞, load impedance from OUT_+ to OUT_-, $T_A$ = $T_J$ = -40°C to +105°C, typical values are $T_A$ = +25°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **CHARGE PUMP** | | | | | | | |
| Charge-Pump Overdrive Voltage, $V_{CHOLD}$ – $V_{DD}$ (Hard Mode) | $V_{CPH}$ | $V_{DD}$ = 4.5V, $I_{SOURCE}$ = 6.6mA | | 3.2 | 4.0 | | V |
| | | $V_{DD}$ = 18V, $I_{SOURCE}$ = 6.6mA | | 4.5 | | 5.5 | |
| $V_{CHOLD}$ - $V_{DD}$ (Soft Mode) | $V_{CPS}$ | $V_{DD}$ unconnected, $I_{SOURCE}$ = 40µA, $V_L$ = 3.3V | | | 2.1 | | V |
| | | $V_L$ = 5V | | | 3.9 | | |
| Charge-Pump Frequency | $f_{CP}$ | CPOFF = 0 | CPF[1:0] = 00 | | 333 | | kHz |
| | | | CPF[1:0] = 01 | | 190 | | |
| | | | CPF[1:0] = 10 | | 426 | | |
| | | | CPF[1:0] = 11 | | 260 | | |
| **DIAGNOSTICS** | | | | | | | |
| Output Current Limit | | Short to GND or battery | | | 580 | | mA |
| Current-Limit Warning Threshold | | | | | 230 | | mA |
| Open-Load Detection | | | | 10 | | | kΩ |
| Output Offset Detection | | Valid when muted | | | ±250 | | mV |
| Thermal Warning Threshold | | | | | 135 | | °C |
| Thermal Shutdown Threshold | | | | | 165 | | °C |
| Thermal Shutdown Hysteresis | | | | | 15 | | °C |
| **ESD PROTECTION** | | | | | | | |
| Air Gap IEC 61000-4-2 | | OUT_ pins | | | ±15 | | kV |
| Contact Discharge IEC 61000-4-2 | | OUT_ pins | | | ±8 | | kV |
| HBM | | All pins | | | ±2 | | kV |

## DIGITAL CHARACTERISTICS

($V_{DD}$ = 14.4V, $V_L$ = 3.3V, $T_A$ = $T_J$ = -40°C to +105°C, typical values are $T_A$ = +25°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DIGITAL INTERFACE** | | | | | | |
| Input-Voltage High | $V_{INH}$ | $V_L$ = 2.7V to 5.5V | 0.75 x $V_L$ | | | V |
| Input-Voltage Low | $V_{INL}$ | $V_L$ = 2.7V to 5.5V | | | 0.25 x $V_L$ | V |
| Input-Voltage Hysteresis | | | | 50 | | mV |
| Input Leakage Current | | | | | ±100 | µA |
| Output Low Voltage | | $\overline{FLAG}$, SDA, $I_{SINK}$ = 3mA | | | 0.4 | V |
| Output Leakage Current | | $\overline{FLAG}$, SDA = 5.5V | | | 2 | µA |
| Stand-Alone $\overline{FLAG}$ Pulse Width | | ADD0, ADD1 = GND | | 100 | | ms |
| Stand-Alone Fault Retry Time | | ADD0, ADD1 = GND | | 500 | | ms |
| **I²C TIMING** | | | | | | |
| Serial-Clock Frequency | $f_{SCL}$ | | 0 | | 400 | kHz |
| Bus Free Time | $t_{BUF}$ | Between START and STOP conditions | 1.3 | | | µs |
| Hold Time | $t_{HD:STA}$ | Repeated START condition | 0.6 | | | µs |
| SCL Low Time | $t_{LOW}$ | | 1.3 | | | µs |
| SCL High Time | $t_{HIGH}$ | | 0.6 | | | µs |
| Data Hold Time | $t_{HD:DAT}$ | | 0 | | 900 | ns |
| Data Setup Time | $t_{SU:DAT}$ | | 100 | | | ns |
| Bus Capacitance | $C_B$ | Per bus line | | | 400 | pF |
| Receiving Rise Time | $t_R$ | SCL, SDA | 20 + 0.1$C_B$ | | 300 | ns |
| Receiving Fall Time | $t_F$ | SCL, SDA | 20 + 0.1$C_B$ | | 300 | ns |
| Transmitting Fall Time | $t_F$ | SDA, $V_L$ = 3.6V | 20 + 0.05$C_B$ | | 250 | ns |
| STOP Condition Setup Time | $t_{SU:STO}$ | | 0.6 | | | µs |
| Pulse Width of Suppressed Spike | $t_{SP}$ | | 0 | | 50 | ns |

**Note 2:** All devices are 100% tested at $T_A$ = +25°C. Limits over temperature are guaranteed by design.

**Note 3:** Signal path gain is defined as: $20 \times \log\left(\frac{\left|(V_{OUT\_+}) - (V_{OUT\_-})\right|}{\left|(V_{IN\_+}) - (V_{IN\_-})\right|}\right)$.

**Note 4:** Measured in differential output mode, differential input voltage $4V_{P-P}$ (for 0dB gain), $1V_{P-P}$ (for 12dB gain) 1kHz.

Common-mode output balance is defined as: $20 \times \log\left(\frac{\left|(|V_{OUT\_+}|) - (|V_{OUT\_-}|)\right|}{\left|(|V_{OUT\_+}|) + (|V_{OUT\_-}|)\right| \times 2}\right)$.

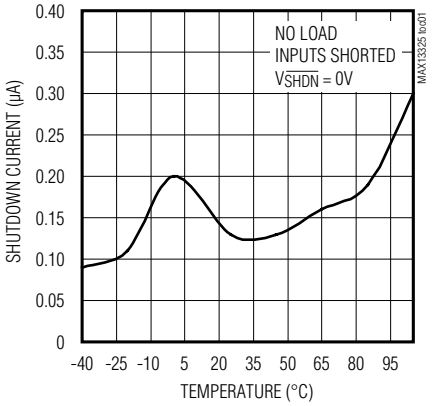
**Note 5:** 22Hz to 22kHz measurement bandwidth.

**Note 6:** KCP level is calculated as 20log[(peak voltage during mode transition, no input signal)/$1V_{RMS}$]. Units are expressed in dBV.

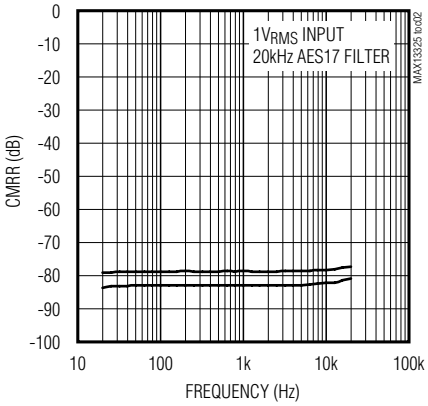
### Typical Operating Characteristics

($V_{DD}$ = 14.4V, $V_L$ = 5V, $R_L$ = 1kΩ, gain = 12dB, $T_A$ = +25°C, unless otherwise noted.)

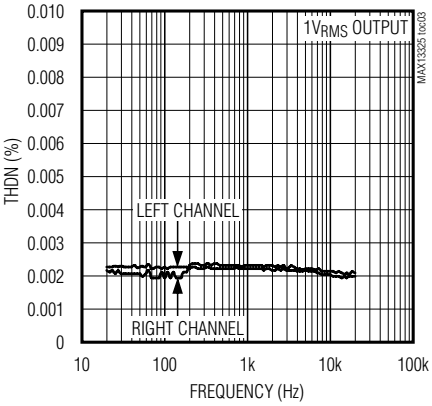
**SHUTDOWN CURRENT vs. TEMPERATURE**



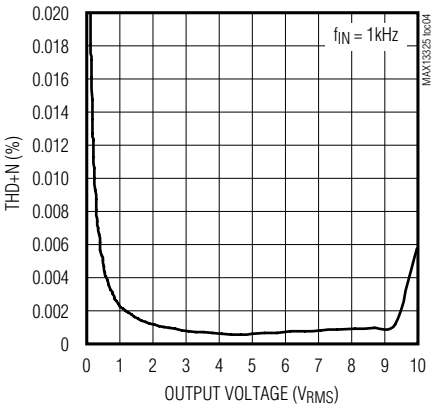

**COMMON-MODE REJECTION RATIO vs. FREQUENCY**



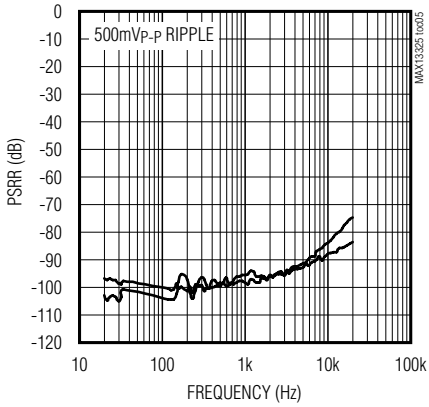

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**



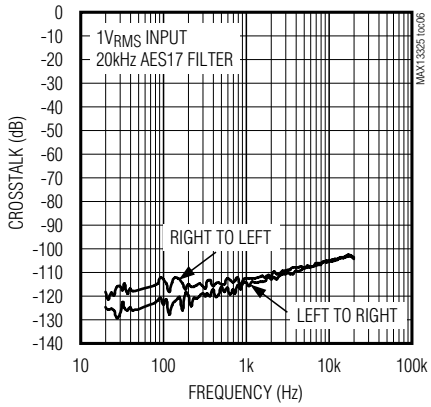

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE**



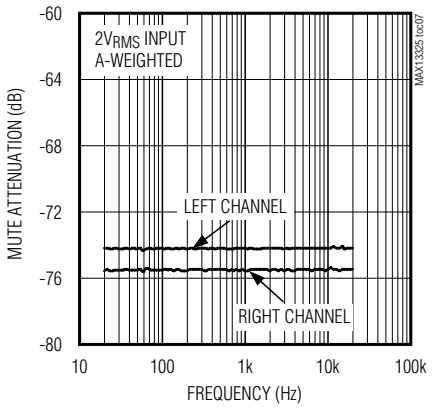

**POWER-SUPPLY REJECTION RATIO vs. FREQUENCY**



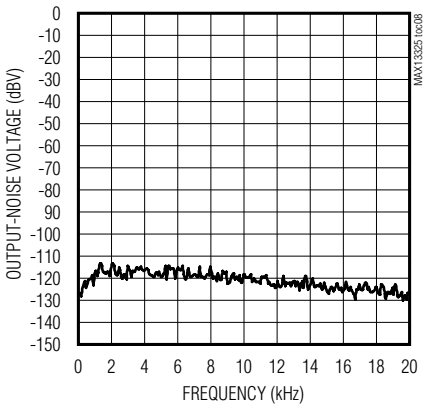

**CROSSTALK vs. FREQUENCY**



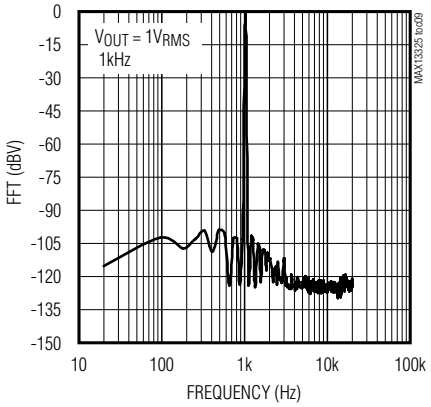

**MUTE ATTENUATION vs. FREQUENCY**




**OUTPUT-NOISE VOLTAGE vs. FREQUENCY**



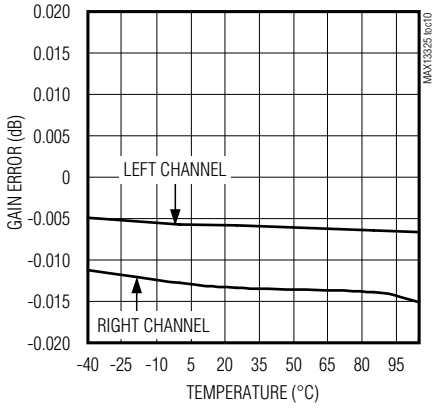

**FFT vs. FREQUENCY**



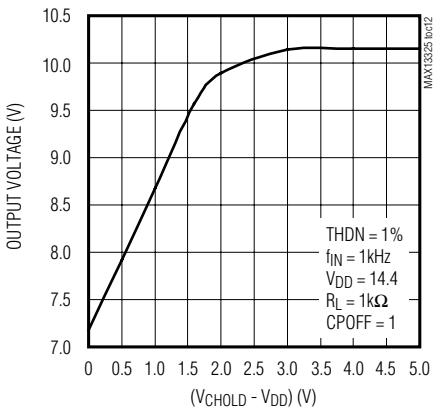
## Typical Operating Characteristics (continued)

($V_{DD}$ = 14.4V, $V_L$ = 5V, $R_L$ = 1kΩ, gain = 12dB, $T_A$ = +25°C, unless otherwise noted.)

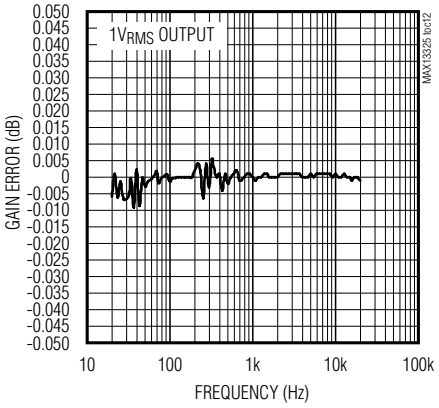
**GAIN ERROR vs. TEMPERATURE**



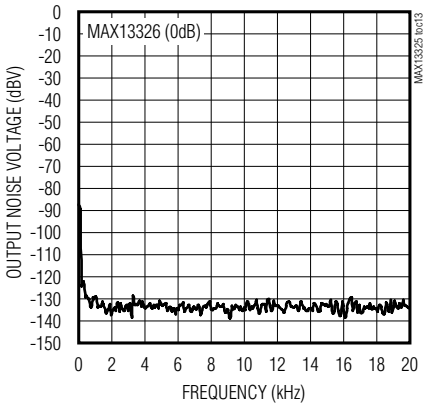

**OUTPUT VOLTAGE vs. CHARGE-PUMP OVERDRIVE VOLTAGE**



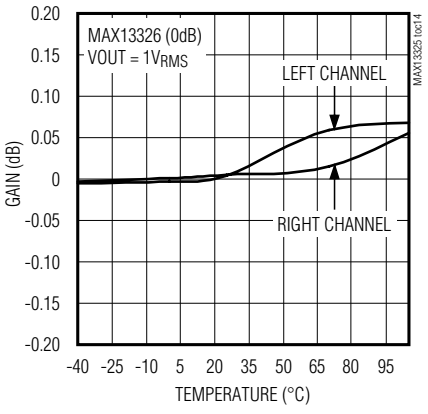

**GAIN ERROR vs. FREQUENCY**



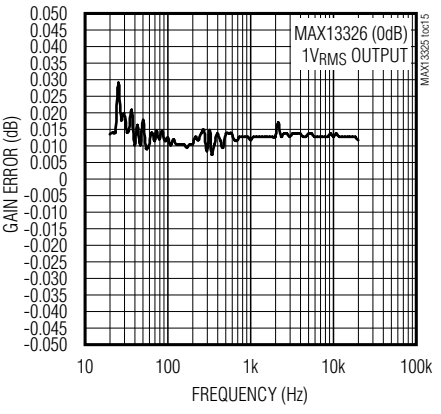

**OUTPUT-NOISE VOLTAGE vs. FREQUENCY**



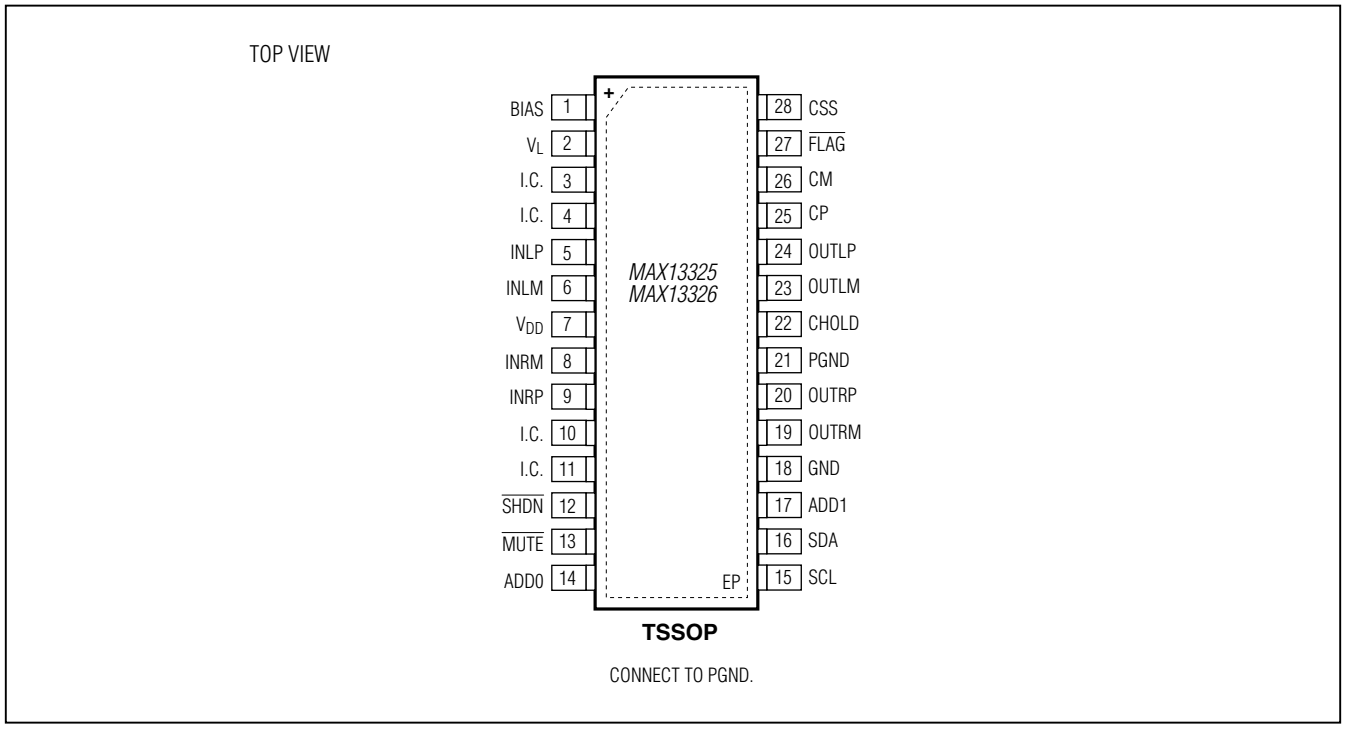

**GAIN vs. TEMPERATURE**




**GAIN ERROR vs. FREQUENCY**



## Pin Configuration




## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | BIAS | Analog Bias Voltage. Bypass BIAS to GND with a 10µF capacitor. |
| 2 | $V_L$ | Logic Supply Voltage. Connect $V_L$ to a 2.7V to 5V logic supply. Bypass $V_L$ to GND with a 0.1µF capacitor. |
| 3, 4, 10, 11 | I.C. | Internally Connected. Leave unconnected. |
| 5 | INLP | Left Audio Positive Input. Either input of each pair can be used as a single-ended input, with the complementary input bypassed to GND. |
| 6 | INLM | Left Audio Negative Input. Either input of each pair can be used as a single-ended input, with the complementary input bypassed to GND. |
| 7 | $V_{DD}$ | Power-Supply Input. Connect $V_{DD}$ to the supply voltage. Bypass $V_{DD}$ to GND through a 1µF capacitor. |
| 8 | INRM | Right Audio Negative Input. Either input of each pair can be used as a single-ended input, with the complementary input bypassed to GND. |
| 9 | INRP | Right Audio Positive Input. Either input of each pair can be used as a single-ended input, with the complementary input bypassed to GND. |
| 12 | $\overline{SHDN}$ | Shutdown Input. Drive $\overline{SHDN}$ low to power down the device. |
| 13 | $\overline{MUTE}$ | Mute Input. Drive $\overline{MUTE}$ low to mute the outputs. The outputs are low impedance in mute. |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 14 | ADD0 | I²C Address Inputs. Connect ADD0 and ADD1 to $V_L$, GND, SCL, or SDA to select 7 I²C addresses. Connect ADD0 and ADD1 to GND for stand-alone mode. |
| 15 | SCL | Serial Clock |
| 16 | SDA | Serial-Data IO |
| 17 | ADD1 | I²C Address Inputs. Connect ADD0 and ADD1 to $V_L$, GND, SCL, or SDA to select 7 I²C addresses. Connect ADD0 and ADD1 to GND for stand-alone mode. |
| 18 | GND | Analog Ground. Ground connection for the input bias and gain circuits. |
| 19 | OUTRM | Right Audio Negative Output. Each output is current limited. |
| 20 | OUTRP | Right Audio Positive Output . Each output is current limited. |
| 21 | PGND | Power Ground. Ground connection for the output stage drivers. |
| 22 | CHOLD | Charge-Pump Output (When Charge Pump is On; CPOFF = 0). When the charge pump is off, provide an external supply through a diode to the CHOLD input. Bypass CHOLD with 1µF to PGND. |
| 23 | OUTLM | Left Audio Negative Output. Each output is current limited. |
| 24 | OUTLP | Left Audio Positive Outputs. Each output is current limited. |
| 25 | CP | Charge-Pump Flying Capacitor, Positive Connection |
| 26 | CM | Charge-Pump Flying Capacitor, Negative Connection |
| 27 | $\overline{FLAG}$ | Open-Drain Fault Flag Output. $\overline{FLAG}$ indicates a fault on any one channel. In stand-alone mode, $\overline{FLAG}$ is stretched to a typical pulse width of 100ms. |
| 28 | CSS | Soft-Start Capacitor Connection. CSS is charged/discharged by < 100µA current to get soft mute/play transition. Bypass to GND through a 220nF capacitor. |
| — | EP | Exposed Pad. Connect to PGND. |

## Detailed Description

The MAX13325/MAX13326 audio line drivers are designed to transmit audio data across noisy environments. The differential interface is highly resistant to noise injection from external sources common to automotive applications.

The MAX13325/MAX13326 operate in stand-alone or I²C-compatible mode with diagnostic outputs capable of detecting short to GND or battery, overcurrent, overtemperature, or excessive offset. A short across another audio output signal line is also protected.

### Table 1. Register Address Map

| ADDRESS | REGISTER TYPE | NAME | READ/WRITE | DEFAULT |
|---|---|---|---|---|
| 0x00 | Configuration | CONFIG | Read/Write | 0x00 |
| 0x01 | Command Byte | CMD | Read/Write | 0x00 |
| 0x02 | General Fault | GFAULT | Read | 0x00 |
| 0x03 | Left-Channel Fault | LFAULT | Cleared on Read | 0x00 |
| 0x04 | Right-Channel Fault | RFAULT | Cleared on Read | 0x00 |
| 0x05 | Flag | FLAG | Read | 0x04 (12dB)<br>0x05 (0dB) |
| 0x06 | General Mask | GMASK | Read/Write | 0x00 |
| 0x07 | Left-Channel Mask | LMASK | Read/Write | 0x00 |
| 0x08 | Right-Channel Mask | RMASK | Read/Write | 0x00 |

***Configuration Register***

## Table 2. Configuration Register Format

| FUNCTION | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | | POR STATE (HEX) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Configuration Register | 0x00 | DIAG | ENABLE | MUTE | CPOFF | OLDL | OLDR | CPF1 | CPF0 | 0x00 |

DIAG: Set DIAG to 1 to enable diagnostic mode. Write '0' to disable diagnostic mode.

ENABLE: Set ENABLE bit to 1 to enable the device. Write ‘0’ disables the device. Low on the $\overline{SHDN}$ pin overrides the ENABLE bit.

MUTE: Set the MUTE bit to 1 to mute both the output channels. Output is low impedance when in mute. Low on the $\overline{MUTE}$ pin input overrides the MUTE bit.

CPOFF: Set the CPOFF bit to 1 to turn off the charge pump. CHOLD pin must be externally supplied (see the $V_{CPH}$ parameter in the *Electrical Characteristics* table). Charge pump is enabled when CPOFF = 0.

OLDL: Write 1 to the OLDL bit to initiate the open-load detection for the left channel. To run OLDL again, write ‘0’ and ‘1’ again.

OLDR: Write 1 to the OLDR bit to initiate the open-load detection for the right channel. To run OLDR again, write ‘0’ and ‘1’ again.

## Table 2a. Charge-Pump Frequency Bits

| CPF1 | CPF0 | FREQUENCY (kHz) |
|---|---|---|
| 0 | 0 | 333 |
| 0 | 1 | 190 |
| 1 | 0 | 426 |
| 1 | 1 | 260 |

CPF[1:0]: Sets the frequency of the charge pump.

***Command Byte Register***

## Table 3. Command Byte Register Format

| FUNCTION | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | | POR STATE (HEX) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Command Byte Register | 0x01 | RETRYL | RETRYR | x | x | x | x | x | x | 0x00 |

RETRYR: The right-channel power amplifier switches off after a fault condition. Write ‘1’ to turn it back on after the fault condition.

RETRYL: The left-channel power amplifier switches off after a fault condition. Write ‘1’ to turn on the left-channel power amplifier after the fault condition.

### General Faults

## Table 4. General Fault Register Format

| FUNCTION | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | | POR STATE (HEX) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| General Fault Register | 0x02 | x | TWARN | TSHDN | DUMP | x | x | x | x | 0x00 |

TWARN: The TWARN bit is set to '1' when the temperature warning threshold is reached.

TSHDN: The TSHDN is set to '1' when the temperature shutdown threshold is reached.

DUMP: The DUMP bit is set to '1' when the $V_{DD}$ voltage exceeds the overvoltage threshold.

Set the appropriate mask bit in the GMASK register to detect the general faults. See Table 8.

### Left-Channel Faults

## Table 5. Left-Channel Fault Register Format

| FUNCTION | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | | POR STATE (HEX) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Left-Channel Fault Register | 0x03 | SVDDL | SGNDL | LIMITL | x | OFFSETL | OPENL | x | x | 0x00 |

SVDDL: The SVDDL bit is set to '1' when a short to $V_{DD}$ is detected on the left channel.

SGNDL: The SGNDL bit is set to '1' when a short to GND is detected on the left channel.

LIMITL: The LIMITL bit is set to '1' when the current-limit threshold is tripped for left output.

OFFSETL: The OFFSETL bit is set to '1' when excessive offset is detected on the left-channel output.

OPENL: The OPENL bit is set to '1' when an open load is detected on the left channel.

Set the appropriate mask bit in the LMASK register to detect the faults on the left channel. See Table 9.

When any bit of the LFAULT register is high, the $\overline{FLAG}$ output is low.

### Right-Channel Faults

## Table 6. Right-Channel Fault Register Format

| FUNCTION | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | | POR STATE (HEX) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Right-Channel Fault Register | 0x04 | SVDDR | SGNDR | LIMITR | x | OFFSETR | OPENR | x | x | 0x00 |

SVDDR: The SVDDR bit is set to '1' when a short to $V_{DD}$ is detected on the right channel.

SGNDR: The SGNDR bit is set to '1' when a short to GND is detected on the right channel.

LIMITR: The LIMITR bit is set to '1' when the current-limit threshold is tripped for right output.

OFFSETR: The OFFSETR bit is set to '1' when excessive offset is detected on the right-channel output.

OPENR: The OPENR bit is set to '1' when an open load is detected on the right channel.

Set the appropriate mask bit in the RMASK register to detect the faults on the right channel. See Table 10.

When any bit of the RFAULT register is high, the $\overline{FLAG}$ output is pulled low.

### FLAG Register

## Table 7. Flag Register Format

| FUNCTION | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | | POR STATE (HEX) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| FLAG Register | 0x05 | FLAG | LHIGHZ | RHIGHZ | OFFSETL | OFFSETR | ID2 | ID1 | ID0 | 0x04/0x05 |

FLAG: FLAG bit is set to '1' when the $\overline{FLAG}$ output is logic-low. The FLAG bit allows to quickly access the status of the device without using the $\overline{FLAG}$ output and without having to read all the fault registers.

LHIGHZ: The LHIGHZ bit is set to '1' when the left-channel output is high impedance; for example due to a short circuit.

RHIGHZ: The RHIGHZ bit is set to '1' when the right-channel output is high impedance; for example due to a short circuit.

OFFSETL: The OFFSETL bit is set to '1' when excessive offset is detected on the left-channel output.

OFFSETR: The OFFSETR bit is set to '1' when excessive offset is detected on the right-channel output.

ID[2:0]: The ID[2:0] bits indicate the device type (12dB = 100 and 0dB = 101).

### General Mask Register

## Table 8. General Mask Register Format

| FUNCTION | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | | POR STATE (HEX) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| General Mask Register | 0x06 | 0 | MTWARN | MTSHDN | MDUMP | x | x | x | x | 0x00 |

MTWARN: Set MTWARN to '1' to enable the TWARN fault detection. See Table 4.

MTSHDN: Set MTSHDN to '1' to enable the TSHDN fault detection. See Table 4.

MDUMP: Set MDUMP to '1' to enable the DUMP fault detection. See Table 4.

### Left-Channel Mask Register

## Table 9. Left-Channel Mask Register

| FUNCTION | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | | POR STATE (HEX) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Left-Channel Mask Register | 0x07 | MSVDDL | MSGNDL | MLIMITL | 0 | MOFFSETL | MOPENL | x | x | 0x00 |

MSVDDL: Set MSVDDL to 1 to enable the short to $V_{DD}$ detection on the left channel.

MSGNDL: Set MSGNDL to 1 to enable the short to GND detection on the left channel.

MLIMITL: Set MLIMITL to 1 to enable overcurrent detection on the left channel.

MOFFSETL: Set MOFFSETL to 1 to enable excessive-offset detection on the left-channel output.

MOPENL: Set MOPENL to 1 to enable open-load detection on the left channel.

### Right-Channel Mask Register

**Table 10. Right-Channel Mask Register**

| FUNCTION | ADDRESS CODE (HEX) | REGISTER DATA | | | | | | | | POR STATE (HEX) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Right-Channel Mask Register | 0x08 | MSVDDR | MSGNDR | MLIMITR | 0 | MOFFSETR | MOPENR | x | x | 0x00 |

MSVDDR: Set MSVDDR to 1 to enable the short to $V_{DD}$ detection on the right channel.

MSGNDR: Set MSGNDR to 1 to enable the short to GND detection on the right channel.

MLIMITR: Set MLIMITR to 1 to enable overcurrent detection on the right channel.

MOFFSETR: Set MOFFSETR to 1 to enable excessive-offset detection on the right channel.

MOPENR: Set MOPENR to 1 to enable open-load detection on the right channel.

### I²C and Stand-Alone Diagnostics

When the DIAG bit and the appropriate mask bits are set to 1, the MAX13325/MAX13326 enter diagnostic mode. In this mode, the MAX13325/MAX13326 detect short to GND, short to battery, overcurrent condition, overtemperature condition, excessive offset, and report the diagnosis using the I²C serial interface, FLAG bit, and the $\overline{FLAG}$ output.

For stand-alone mode, there exists a 500ms stand-alone fault retry function (for autoretry) until the fault goes away. The $\overline{FLAG}$ output is pulsed to indicate a fault.

#### Output Short to $V_{DD}$

When in diagnostic mode, the MAX13325/MAX13326 detect if any of the differential outputs is shorted to $V_{DD}$ or battery. Upon detection of the short to $V_{DD}$ or battery, the faulted channel is switched off and its output goes into a high-impedance state. The fault is reported using the I²C interface and the $\overline{FLAG}$ output. See Table 11.

**Table 11. Output Short to $V_{DD}$/Battery Diagnostic**

| FAULT CONDITION | STATUS REPORT | UNMASK | RECOVERY |
|---|---|---|---|
| Left-Channel Output Short to $V_{DD}$ | $\overline{FLAG}$ is asserted low. | In LMASK register, set MSVDDL bit to 1. See Table 9. | Cleared on reading the LFAULT register. See Table 5. Note: 500ms autoretry in stand-alone mode. |
| | FLAG bit set. See Table 7. | | |
| | SVDDL bit is set in the LFAULT register. See Table 5. | | |
| | Left channel switches off and output goes to high-impedance state. | Cannot be masked. | Output is enabled by setting the RETRYL bit to 1 in the Common Byte register. See Table 3. |
| Right-Channel Output Short to $V_{DD}$ | $\overline{FLAG}$ is asserted low. | In RMASK register, set MSVDDR bit to 1. See Table 10. | Cleared on reading the RFAULT register. See Table 6. Note: 500ms autoretry in stand-alone mode. |
| | FLAG bit set. See Table 7. | | |
| | SVDDR bit is set in the RFAULT register. See Table 6. | | |
| | Right channel switches off and output goes to high-impedance state. | Cannot be masked. | Output is enabled by setting the RETRYR bit to 1 in the Command Byte register. See Table 3. |

### *Output Short to GND*

When in diagnostic mode, the MAX13325/MAX13326 detect if any of the differential outputs is shorted to ground. Upon detection of the short to ground, the faulted channel is switched off and its output goes into a high-impedance state. The fault is reported using the I²C interface and the $\overline{FLAG}$ output. See Table 12.

### *Overtemperature*

When in diagnostic mode, if the MAX13325/MAX13326 exceed the overtemperature warning or temperature shutdown thresholds the device reports the condition using the I²C interface and the $\overline{FLAG}$ output. See Table 13.

## Table 12. Output Short to GND Diagnostic

| FAULT CONDITION | STATUS REPORT | UNMASK | RECOVERY |
|---|---|---|---|
| Left-Channel Output Short to GND | $\overline{FLAG}$ is asserted low. | In LMASK register, set MSGNDL bit to 1. See Table 9. | Cleared on reading the LFAULT register. See Table 5. Note: 500ms autoretry in stand-alone mode. |
| | FLAG bit set. See Table 7. | | |
| | SGNDL bit is set in the LFAULT register. See Table 5. | | |
| | Left channel switches off and output goes to high-impedance state. | Cannot be masked. | Output is enabled by setting the RETRYL bit to 1 in the Command Byte register. See Table 3. |
| Right-Channel Output Short to GND | $\overline{FLAG}$ is asserted low. | In RMASK register, set MSGNDR bit to 1. See Table 10. | Cleared on reading the RFAULT register. See Table 6. Note: 500ms autoretry in stand-alone mode. |
| | FLAG bit set. See Table 7. | | |
| | SGNDR bit is set in the RFAULT register. See Table 6. | | |
| | Right channel switches off and output goes to high-impedance state. | Cannot be masked. | Output is enabled by setting the RETRYR bit to 1 in the Command Byte register. See Table 3. |

## Table 13. Overtemperature Diagnostic

| FAULT CONDITION | STATUS REPORT | UNMASK | RECOVERY |
|---|---|---|---|
| Overtemperature Warning | $\overline{FLAG}$ is asserted low. | In GMASK register, set MTWARN bit to 1. See Table 8. | Die temperature falls below warning threshold. Cleared on reading the GFAULT register. |
| | FLAG bit set. See Table 7. | | |
| | TWARN bit is set in the GFAULT register. See Table 4. | | |
| Overtemperature Shutdown | $\overline{FLAG}$ is asserted low. | In GMASK register, set MTSHDN bit to 1. See Table 8. | Die temperature falls below shutdown threshold. Cleared on reading the GFAULT register. Note: 500ms autoretry in stand-alone mode. |
| | FLAG bit set. See Table 7. | | |
| | TSHDN bit is set in the GFAULT Register. See Table 4. | | |
| | Left and right channels switch off and output goes to high-impedance state. | Cannot be masked. | Left channel is enabled by setting the RETRYL bit to 1 in the Command Byte register. Right channel is enabled by setting the RETRYR bit to 1 in the Command Byte register. See Table 3. |

### *Excessive Offset*

When in diagnostic mode with mute enabled, if there is excessive offset on any output, the MAX13325/MAX13326 reports the condition through the I²C interface and the $\overline{FLAG}$ output. See Table 14.

### *Overcurrent*

When in diagnostic mode, if any of the output pairs is excessively loaded, the MAX13325/MAX13326 issue a warning and report the condition through the I²C interface and the $\overline{FLAG}$ output. The faulted channel is not switched off. See Table 15.

### *Open Load*

When in diagnostic mode and the open-load detection is initiated, the selected channel is switched off for 1ms during which the diagnosis is taking place. Upon detecting an open load on any channel, the MAX13325/MAX13326 report the condition using the I²C interface and the $\overline{FLAG}$ output. See Table 16.

### *Overvoltage*

When in diagnostic mode, if the MAX13325/MAX13326 exceed the $V_{DD}$ overvoltage threshold (for example during a load-dump condition), the device reports the condition using the I²C interface and the $\overline{FLAG}$ output. See Table 17.

## Table 14. Excessive Offset Diagnostic

| FAULT CONDITION | STATUS REPORT | UNMASK | RECOVERY |
|---|---|---|---|
| Excessive Output Offset on Left Channel | $\overline{FLAG}$ is asserted low.<br>FLAG bit set. See Table 7.<br>OFFSETL bit is set in the LFAULT register. See Table 5. | In the LMASK register, set MOFFSETL bit to 1. See Table 9. | Cleared on reading the LFAULT register. |
| Excessive Output Offset on Right Channel | $\overline{FLAG}$ is asserted low.<br>FLAG bit set.<br>OFFSETR bit is set in the RFAULT register. See Table 6. | In the RMASK register, set MOFFSETR bit to 1. See Table 10. | Cleared on reading the RFAULT register. |

## Table 15. Overcurrent Diagnostic

| FAULT CONDITION | STATUS REPORT | UNMASK | RECOVERY |
|---|---|---|---|
| Overcurrent on Left Channel | $\overline{FLAG}$ is asserted low.<br>FLAG bit set. See Table 7.<br>LIMITL bit is set in the LFAULT register. See Table 5. | In the LMASK register, set MLIMITL bit to 1. See Table 9. | Load current falls below the current-limit threshold. Cleared on reading the LFAULT register. |
| Overcurrent on Right Channel | $\overline{FLAG}$ is asserted low.<br>FLAG bit set. See Table 7.<br>LIMITR bit is set in the RFAULT register. See Table 6. | In the RMASK register, set MLIMITR bit to 1. See Table 10. | Load current falls below the current-limit threshold. Cleared on reading the RFAULT register. |

## Table 16. Open-Load Diagnostic

| FAULT CONDITION | STATUS REPORT | UNMASK | RECOVERY |
|---|---|---|---|
| Left-Channel Open Load | $\overline{FLAG}$ is asserted low.<br>FLAG bit set. See Table 7.<br>OPENL bit is set in the LFAULT register. See Table 5. | In the LMASK register, set MOPENL bit to 1. See Table 9. | Cleared on reading the LFAULT register. |
| Right-Channel Open Load | $\overline{FLAG}$ is asserted low.<br>FLAG bit set. See Table 7.<br>OPENR bit is set in the RFAULT register. See Table 6. | In the RMASK register, set MOPENR bit to 1. See Table 10. | Cleared on reading the RFAULT register. |

**Table 17. Overvoltage Diagnostic**

| FAULT CONDITION | STATUS REPORT | UNMASK | RECOVERY |
|---|---|---|---|
| Overvoltage Shutdown | $\overline{\text{FLAG}}$ is asserted low. | In GMASK register, set MDUMP bit to 1. See Table 8. | $V_{DD}$ voltage falls below overvoltage threshold. Cleared on reading the GFAULT register. Note: 500ms autoretry in stand-alone mode. |
| | FLAG bit set. See Table 7. | | |
| | DUMP bit is set in the GFAULT register. See Table 4. | | |
| | Left and right channels switch off and output goes to a high-impedance state. | Cannot be masked. | Left channel is enabled by setting the RETRYL bit to 1. Right channel is enabled by setting the RETRYR bit to 1. See Table 3. |

## Applications Information

### Serial Interface

Writing to the MAX13325/MAX13326 using I²C requires that first the master sends a START (S) condition followed by the device's I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP (P) condition to relinquish control of the bus, or a Repeated START (Sr) condition to communicate to another I²C slave (see Figure 1).

#### Bit Transfer

Each SCL rising edge transfers one data bit. The data on SDA must remain stable during the high portion of the SCL clock pulse (see Figure 2). Changes in SDA while SCL is high are read as control signals (see the *START and STOP Conditions* section). When the serial interface is inactive, SDA and SCL idle high.

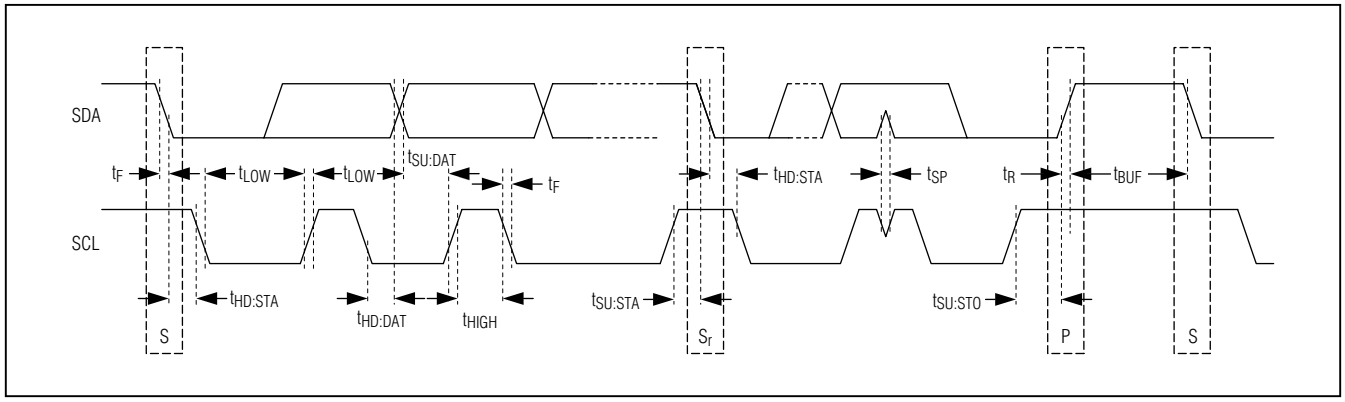



*Figure 1. I²C Timing*

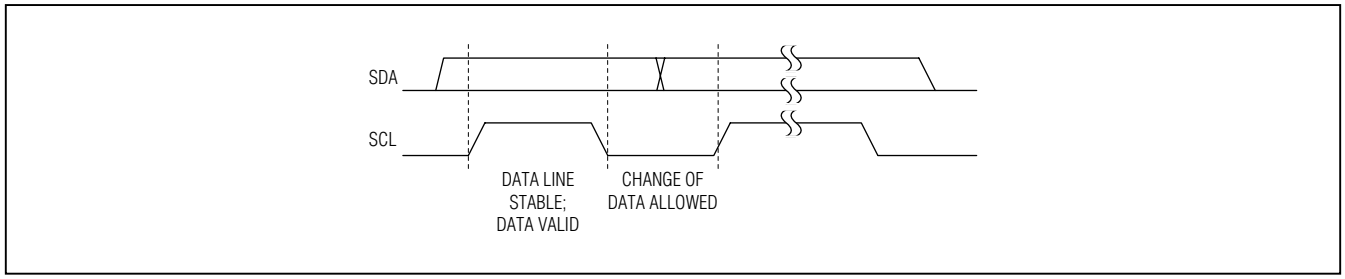



*Figure 2. Bit Transfer*

### START and STOP Conditions

A master device initiates communication by issuing a START condition, which is a high-to-low transition on SDA with SCL high. A START condition from the master signals the beginning of a transmission to the MAX13325/MAX13326. The master terminates transmission by a STOP condition (see the *Acknowledge Bit* section). A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 3). The STOP condition frees the bus. If a Repeated START condition is generated instead of a STOP condition, the bus remains active. When a STOP condition or incorrect slave ID is detected, the device internally disconnects SCL from the serial interface until the next START or Repeated START condition, minimizing digital noise and feedthrough.

### Acknowledge Bit

The acknowledge (ACK) bit is a clocked 9th bit that the MAX13325/MAX13326 use to handshake receipt of each byte of data when in write mode. The MAX13325/MAX13326 pull down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received (see Figure 4). Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event

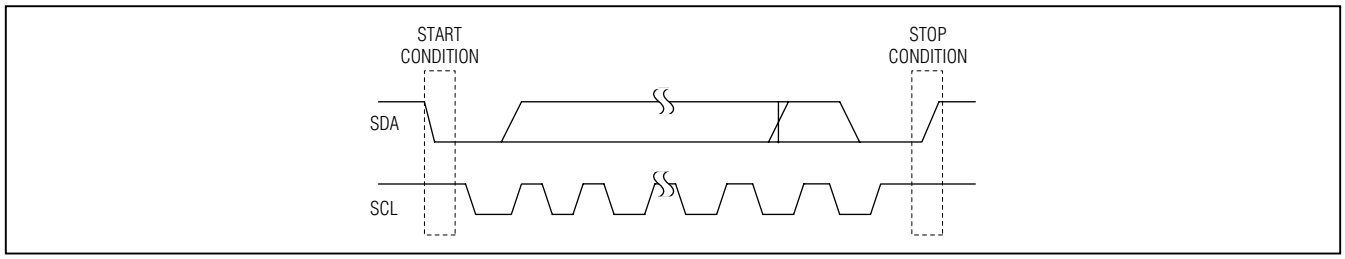



*Figure 3. START/STOP Conditions*

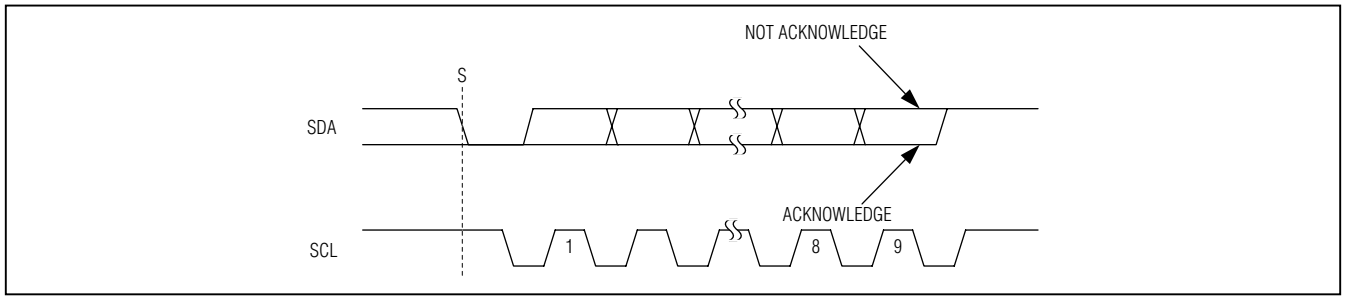



*Figure 4. Acknowledge and Not-Acknowledge Bits*

## Table 18. Slave Address

| ADD1 | ADD0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/$\overline{W}$ | SLAVE ADDRESS READ (HEX) | SLAVE ADDRESS WRITE (HEX) | MODE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | GND | — | — | — | — | — | — | — | — | — | — | Stand-alone |
| $V_L$ | GND | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1/0 | 0xC3 | 0xC2 | I²C |
| GND | $V_L$ | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1/0 | 0xC5 | 0xC4 | I²C |
| $V_L$ | $V_L$ | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1/0 | 0xC7 | 0xC6 | I²C |
| SCL | $V_L$ | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1/0 | 0xC9 | 0xC8 | I²C |
| SDA | $V_L$ | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1/0 | 0xCB | 0xCA | I²C |
| $V_L$ | SCL | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1/0 | 0xCD | 0xCC | I²C |
| $V_L$ | SDA | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1/0 | 0xCF | 0xCE | I²C |

of an unsuccessful data transfer, the bus master may retry communication. The master must pull down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX13325/MAX13326 are in read mode. An acknowledge must be sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX13325/MAX13326, followed by a STOP condition.

### Slave Address

The MAX13325/MAX13326 are programmable to one of seven I²C slave addresses. These slave addresses are unique device IDs. Connect ADD_ to GND, $V_L$, SCL, or SDA to set the I²C slave address. The address is defined as the seven most significant bits (MSBs) followed by the read/write bit. Set the read/write bit to 1 to configure the MAX13325/MAX13326 to read mode. Set the read/write bit to 0 to configure the device to write mode. The address is the first byte of information sent after the START condition.

### Register Address Map

#### Single-Byte Write Operation

For a single-byte write operation, send the slave address as the first byte followed by the register address and then a single data byte (see Figure 5).

#### Burst Write Operation

For a burst write operation, send the slave address as the first byte followed by the register address and then the data bytes (see Figure 6).

#### Single-Byte Read Operation

For a single-byte read operation, send the slave address with the read bit set, as the first byte followed by the register address. Then send a Repeated START condition followed by the slave address. After the slave sends the data byte, send a not-acknowledge followed by a STOP condition (see Figure 7).

#### Burst Read Operation

For a burst read operation, send the slave address with a write as the first byte followed by the register address. Then send a Repeated START condition followed by the slave address. The slave sends data bytes until a not-acknowledge condition is sent (see Figure 8).

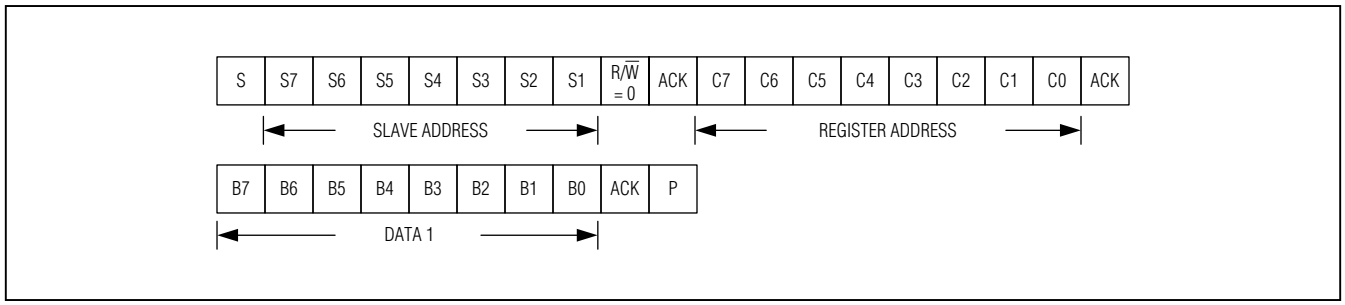



*Figure 5. A Single-Byte Write Operation*

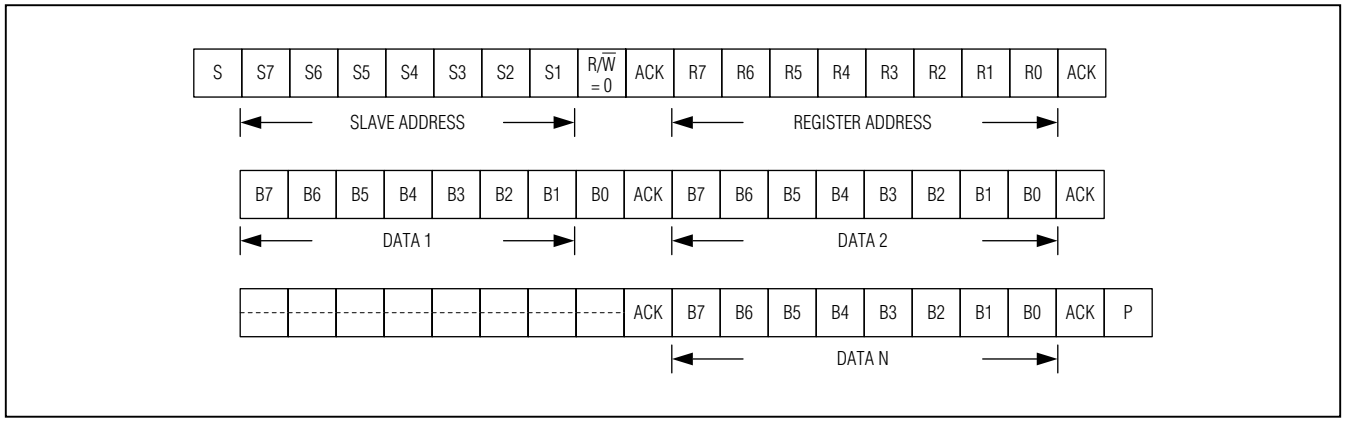



*Figure 6. A Burst Write Operation*

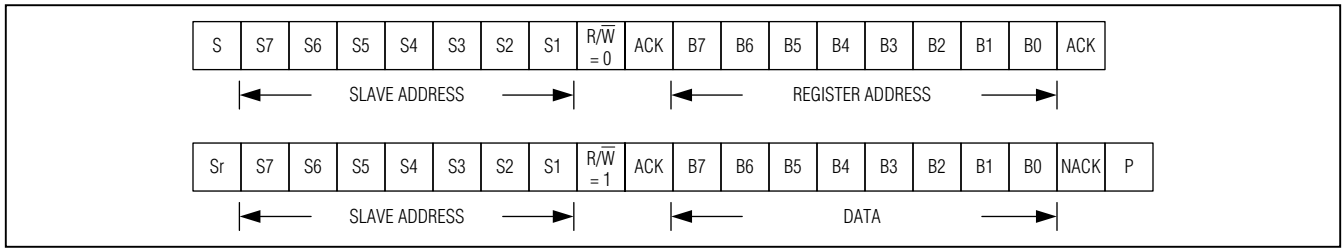



*Figure 7. A Single-Byte Read Operation*

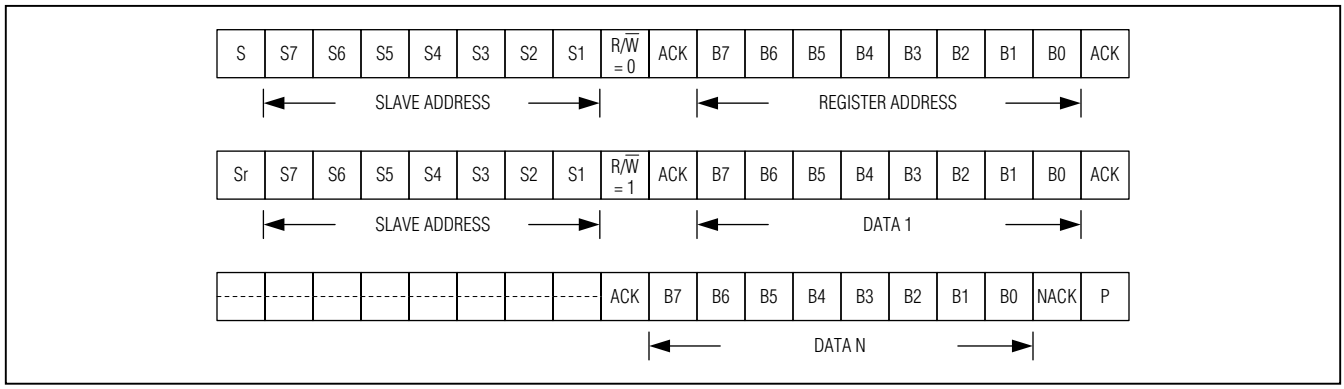



*Figure 8. A Burst Read Operation*

### Charge Pump

The MAX13325/MAX13326 charge pump can be disabled depending on application requirements. When charge pump is enabled [CPOFF = 0], please follow the charge-pump capacitor selections. When the charge pump is disabled [CPOFF = 1], the flying capacitor (C1) is not needed. There are internal diodes between $V_{DD}$/OUT_ to CHOLD, so it is important that CHOLD not be forced below $V_{DD}$ or any of the outputs. A series diode needs to be placed between the external supply ($V_{SUP}$) and CHOLD. See D2 in the *Typical Operating Circuit*.

### Charge-Pump Capacitor Selection

Use ceramic capacitors with a low ESR for optimum performance. For optimal performance over the extended temperature range, select capacitors with an X7R dielectric. Table 19 lists suggested manufacturers.

### Flying Capacitor (C1)

The value of the flying capacitor (see the *Typical Operating Circuit*) affects the charge pump's load regulation and output resistance. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C1 improves load regulation and reduces the charge-pump output resistance. For optimum performance, use a 470nF capacitor for C1. When the charge pump is disabled [CPOFF = 1], the flying capacitor (C1) is not needed.

### Hold Capacitor (C2)

The hold capacitor value (see the *Typical Operating Circuit*) and ESR directly affect the ripple at the internal negative rail. Increasing the value of C2 reduces output ripple. Likewise, decreasing the ESR of C2 reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. For optimum performance, use a 1µF capacitor for C2.

## Table 19. Suggested Capacitor Vendors

| SUPPLIER | PHONE | FAX | WEBSITE |
|---|---|---|---|
| Murata Electronics North America, Inc. | 770-436-1300 | 770-436-3030 | www.murata-northamerica.com |
| Taiyo Yuden | 800-348-2496 | 847-925-0899 | www.t-yuden.com |
| TDK Corp. | 847-803-6100 | 847-390-4405 | www.component.tdk.com |

### Power-Supply Bypass Capacitor (C3)

The power-supply bypass capacitor (see the *Typical Operating Circuit*) lowers the output impedance of the power supply, and reduces the impact of the MAX13325/MAX13326 charge-pump switching transients. Bypass $V_{DD}$ with C3, the same value as C2, and place it physically close to the $V_{DD}$ and PGND pins.

### Load-Dump Protection

With minimal external components, the MAX13325/MAX13326 can be protected against automotive load-dump conditions. See the *Typical Operating Circuit*.

### nMOSFET (Q1)

Q1 should be selected to withstand the full-voltage exposure ($BV_{DSS}$ > 45V). The gate-source turn-on voltage should be chosen to be less than $V_{CPS}$ to ensure initial startup. Using an external nMOS, RTR020N05, 300ms duration component provides 50V load-dump protection.

### Zener Diode (D1)

During short-to-battery condition, OUT_ lifts up CHOLD using an internal diode. In order not to violate the maximum gate-source voltage of Q1, a zener diode of appropriate clamping voltage should be added between the gate and source terminals.

### Series Resistor (R1)

Normally, a series resistor for current limitation is needed during short-to-battery condition. R1 should be chosen according to (18V - $V_{DD(min)}$ - $V_{ZENER}$)/1mA so that no excessive current is being drawn from CHOLD.

### Layout and Grounding

Proper layout and grounding are essential for optimum performance. Connect the EP and GND together at a single point on the PCB. Ensure ground return resistance is minimized for optimum crosstalk performance.

## Chip Information

PROCESS: BCD

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 28 TSSOP-EP | U28E+5 | 21-0108 | 90-0147 |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 1/10 | Initial release | — |
| 1 | 3/10 | Updated the *Typical Operating Circuit* | 1 |
| 2 | 4/10 | Added new register bits to Tables 1, 2, and 7. Revised *FLAG Register* section and added Table 2a and *Charge Pump* section. | 1, 4, 7, 8–12, 19, 20 |
| 3 | 6/10 | Introduced the MAX13326. Updated the *Electrical Characteristics* table and added new *Typical Operating Characteristics* graphs. | 1, 4, 5, 7 |
| 4 | 9/12 | Corrected slave addresses in Table 18 | 17 |
| 5 | 4/13 | Corrected bits D[7:6] in Table 3 | 10 |

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

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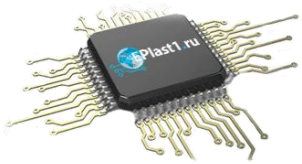
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.




**Как с нами связаться**

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