250 kSPS, 6-Channel, Simultaneous Sampling, Bipolar, 16-/14-/12-Bit ADC

Data Sheet

AD7656-1/AD7657-1/AD7658-1

FEATURES

- Pin and software compatible with AD7656/AD7657/AD7658 featuring reduced decoupling requirements
- 6 independent ADCs
- True bipolar analog inputs
- Pin-/software-selectable ranges: ±10 V, ±5 V
- Fast throughput rate: 250 kSPS
- *i*CMOS process technology
- Low power
  - 140 mW at 250 kSPS with 5 V supplies
- High noise performance with wide bandwidth
  - 88 dB SNR at 10 kHz input frequency
- On-chip reference and reference buffers
- High speed parallel, serial, and daisy-chain interface modes
- High speed serial interface
  - SPI/QSPI™/MICROWIRE™/DSP compatible
- Standby mode: 315 µW maximum
- 64-lead LQFP

APPLICATIONS

- Power line monitoring and measuring systems
- Instrumentation and control systems
- Multiaxis positioning systems

FUNCTIONAL BLOCK DIAGRAM

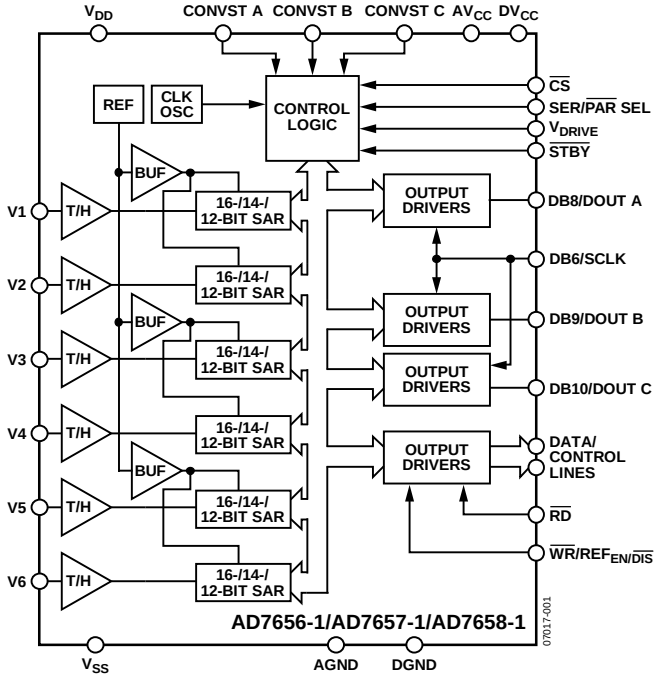

Figure 1.

GENERAL DESCRIPTION

The AD7656-1/AD7657-1/AD7658-1[1] are reduced decoupling pin- and software-compatible versions of AD7656/AD7657/AD7658. The AD7656-1/AD7657-1/AD7658-1 devices contain six 16-/14-/12-bit, fast, low power successive approximation ADCs in a package designed on the *i*CMOS® process (industrial CMOS). *i*CMOS is a process combining high voltage silicon with submicron CMOS and complementary bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts could achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can accept bipolar input signals while providing increased performance, which dramatically reduces power consumption and package size.

The AD7656-1/AD7657-1/AD7658-1 feature throughput rates of up to 250 kSPS. The parts contain low noise, wide bandwidth track-and-hold amplifiers that can handle input frequencies up to 4.5 MHz.

The conversion process and data acquisition are controlled using the CONVST signals and an internal oscillator. Three CONVST pins (CONVST A, CONVST B, and CONVST C) allow independent, simultaneous sampling of the three ADC pairs. The AD7656-1/AD7657-1/AD7658-1 have a high speed parallel and serial interface, allowing the devices to interface with microprocessors or DSPs. When the serial interface is selected, each part has a daisy-chain feature that allows multiple ADCs to connect to a single serial interface. The AD7656-1/AD7657-1/AD7658-1 can accommodate true bipolar input signals in the ±4 × V_{REF} and ±2 × V_{REF} ranges. Each AD7656-1/AD7657-1/AD7658-1 also contains an on-chip 2.5 V reference.

PRODUCT HIGHLIGHTS

1. Six 16-/14-/12-bit, 250 kSPS ADCs on board.
2. Six true bipolar, high impedance analog inputs.
3. High speed parallel and serial interfaces.
4. Reduced decoupling requirements and reduced bill of materials cost compared with the AD7656/AD7657/AD7658 devices.

[1] Protected by U.S. Patent No. 6,731,232.

Rev. D

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SPECIFICATIONS

AD7656-1

V_{REF} = 2.5 V internal/external, AV_{CC} = 4.75 V to 5.25 V, DV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V; for the ±4 × V_{REF} range, V_{DD} = 10 V to 16.5 V, V_{SS} = −10 V to −16.5 V; for the ±2 × V_{REF} range, V_{DD} = 5 V to 16.5 V, V_{SS} = −5 V to −16.5 V; f_{SAMPLE} = 250 kSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 10 kHz sine wave
Signal-to-(Noise + Distortion) (SINAD)[1]		88		dB	
Signal-to-Noise Ratio (SNR)[1]		88		dB	
Total Harmonic Distortion (THD)[1]			−90	dB	
		−105		dB	V_{DD}/V_{SS} = ±5 V to ±16.5 V
Peak Harmonic or Spurious Noise (SFDR)[1]		−100		dB	
Intermodulation Distortion (IMD)[1]					fa = 10.5 kHz, fb = 9.5 kHz
Second-Order Terms		−112		dB	
Third-Order Terms		−107		dB	
Aperture Delay			10	ns	
Aperture Delay Matching			4	ns	
Aperture Jitter		35		ps	
Channel-to-Channel Isolation[1]		−100		dB	f_{IN} on unselected channels up to 100 kHz
Full-Power Bandwidth		4.5		MHz	@ −3 dB
		2.2		MHz	@ −0.1 dB
DC ACCURACY					
Resolution	16			Bits	
No Missing Codes					
B Version	15			Bits	
Y Version	14			Bits	
Integral Nonlinearity[1]			±3	LSB	
		±1		LSB	
Positive Full-Scale Error[1]			±0.8	% FSR	±0.381% FSR typical
Positive Full-Scale Error Matching[1]			±0.35	% FSR	
Bipolar Zero-Scale Error[1]					±0.0137% FSR typical
B Version			±0.048	% FSR	
Y Version			±0.048	%F SR	
Bipolar Zero-Scale Error Matching[1]			±0.038	% FSR	
Negative Full-Scale Error[1]			±0.8	% FSR	±0.381% FSR typical
Negative Full-Scale Error Matching[1]			±0.35	% FSR	
ANALOG INPUT					See Table 8 for minimum V_{DD}/V_{SS} for each range
Input Voltage Ranges	−4 × V_{REF}		+4 × V_{REF}	V	RNGx bits or RANGE pin = 0
	−2 × V_{REF}		+2 × V_{REF}	V	RNGx bits or RANGE pin = 1
DC Leakage Current			±1	µA	
Input Capacitance[2]		10		pF	±4 × V_{REF} range when in track
		14		pF	±2 × V_{REF} range when in track
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range	2.5		2.5	V	
DC Leakage Current			±1	µA	
Input Capacitance[2]		18.5		pF	$REF_{EN/\overline{DIS}}$ = 1
Reference Output Voltage	2.49		2.51	V	
Long-Term Stability		150		ppm	1000 hours
Reference Temperature Coefficient			25	ppm/°C	
		6		ppm/°C	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
Input High Voltage (V_{INH})	$0.7 \times V_{DRIVE}$			V	
Input Low Voltage (V_{INL})			$0.3 \times V_{DRIVE}$	V	
Input Current (I_{IN})			±10	μA	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance (C_{IN})[2]			10	pF	
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	V_{DRIVE} − 0.2			V	I_{SOURCE} = 200 μA
Output Low Voltage (V_{OL})			0.2	V	I_{SINK} = 200 μA
Floating-State Leakage Current			±10	μA	
Floating-State Output Capacitance[2]			10	pF	
Output Coding	Twos complement				
CONVERSION RATE					
Conversion Time			3.1	μs	
Track-and-Hold Acquisition Time[1, 2]			550	ns	
Throughput Rate			250	kSPS	Parallel interface mode only
POWER REQUIREMENTS					
V_{DD}	−5		+16.5	V	For the 4 × V_{REF} range, V_{DD} = 10 V to 16.5 V
V_{SS}	−5		−16.5	V	For the 4 × V_{REF} range, V_{SS}= −10 V to −16.5 V
AV_{CC}	4.75		5.25	V	
DV_{CC}	4.75		5.25	V	
V_{DRIVE}	2.7		5.25	V	
I_{TOTAL}[3]					Digital inputs = 0 V or V_{DRIVE}
Normal Mode—Static			18	mA	AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
Normal Mode—Operational			26	mA	f_{SAMPLE} = 250 kSPS, AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{SS} (Operational)			0.25	mA	V_{SS} = −16.5 V, f_{SAMPLE} = 250 kSPS
I_{DD} (Operational)			0.25	mA	V_{DD} = +16.5 V, f_{SAMPLE} = 250 kSPS
Partial Power-Down Mode			7	mA	AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
Full Power-Down Mode ($\overline{STBY}$ Pin)			60	μA	SCLK on or off, AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
Power Dissipation					AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
Normal Mode—Static			94	mW	
Normal Mode—Operational			140	mW	f_{SAMPLE} = 250 kSPS
Partial Power-Down Mode			40	mW	
Full Power-Down Mode ($\overline{STBY}$ Pin)			315	μW	

[1] See the Terminology section.
[2] Sample tested during initial release to ensure compliance.
[3] Includes I_{AVCC}, I_{VDD}, I_{VSS}, I_{VDRIVE}, and I_{DVCC}.

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V_{REF} = 2.5 V internal/external, AV_{CC} = 4.75 V to 5.25 V, DV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V; for the ±4 × V_{REF} range, V_{DD} = 10 V to 16.5 V, V_{SS} = −10 V to −16.5 V; for the ±2 × V_{REF} range, V_{DD} = 5 V to 16.5 V, V_{SS} = −5 V to −16.5 V; f_{SAMPLE} = 250 kSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 10 kHz sine wave
Signal-to-(Noise + Distortion) (SINAD)[1]		82.5		dB	
Signal-to-Noise Ratio (SNR)[1]		83.5		dB	
Total Harmonic Distortion (THD)[1]			−90	dB	
		−105		dB	
Peak Harmonic or Spurious Noise (SFDR)[1]		−100		dB	
Intermodulation Distortion (IMD)[1]					fa = 10.5 kHz, fb = 9.5 kHz
Second-Order Terms		−109		dB	
Third-Order Terms		−104		dB	
Aperture Delay			10	ns	
Aperture Delay Matching			4	ns	
Aperture Jitter		35		ps	
Channel-to-Channel Isolation[1]		−100		dB	f_{IN} on unselected channels up to 100 kHz
Full-Power Bandwidth		4.5		MHz	@ −3 dB
		2.2		MHz	@ −0.1 dB
DC ACCURACY					
Resolution	14			Bits	
No Missing Codes	14			Bits	
Integral Nonlinearity[1]			±1	LSB	
		±1			
Positive Full-Scale Error[1]			±0.95	% FSR	±0.27% FSR typical
Positive Full-Scale Error Matching[1]			±0.366	% FSR	
Bipolar Zero-Scale Error[1]			±0.04	% FSR	±0.016% FSR typical
Bipolar Zero-Scale Error Matching[1]			±0.0427	% FSR	
Negative Full-Scale Error[1]			±0.95	% FSR	±0.27% FSR typical
Negative Full-Scale Error Matching[1]			±0.366	% FSR	
ANALOG INPUT					See Table 8 for minimum V_{DD}/V_{SS} for each range
Input Voltage Ranges	−4 × V_{REF}		+4 × V_{REF}	V	RNGx bits or RANGE pin = 0
	−2 × V_{REF}		+2 × V_{REF}	V	RNGx bits or RANGE pin = 1
DC Leakage Current			±1	µA	
Input Capacitance[2]		10		pF	±4 × V_{REF} range when in track
		14		pF	±2 × V_{REF} range when in track
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range	2.5		2.5	V	
DC Leakage Current			±1	µA	
Input Capacitance[2]		18.5		pF	$REF_{EN/\overline{DIS}}$ = 1
Reference Output Voltage	2.49		2.51	V	
Long-Term Stability		150		ppm	1000 hours
Reference Temperature Coefficient			25	ppm/°C	
		6		ppm/°C	
LOGIC INPUTS					
Input High Voltage (V_{INH})	0.7 × V_{DRIVE}			V	
Input Low Voltage (V_{INL})			0.3 × V_{DRIVE}	V	
Input Current (I_{IN})			±10	µA	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance (C_{IN})[2]			10	pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	V_{DRIVE} − 0.2			V	I_{SOURCE} = 200 µA
Output Low Voltage (V_{OL})			0.2	V	I_{SINK} = 200 µA
Floating-State Leakage Current			±10	µA	
Floating-State Output Capacitance[2]			10	pF	
Output Coding		Twos complement			
CONVERSION RATE					
Conversion Time			3.1	µs	
Track-and-Hold Acquisition Time[1, 2]			550	ns	
Throughput Rate			250	kSPS	Parallel interface mode only
POWER REQUIREMENTS					
V_{DD}	−5		+16.5	V	For the 4 × V_{REF} range, V_{DD} = 10 V to 16.5 V
V_{SS}	−5		−16.5	V	For the 4 × V_{REF} range, V_{SS}= −10 V to −16.5 V
AV_{CC}	4.75		5.25	V	
DV_{CC}	4.75		5.25	V	
V_{DRIVE}	2.7		5.25	V	
I_{TOTAL}[3]					Digital inputs = 0 V or V_{DRIVE}
Normal Mode—Static			18	mA	AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
Normal Mode—Operational			26	mA	f_{SAMPLE} = 250 kSPS, AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{SS} (Operational)			0.25	mA	V_{SS} = −16.5 V, f_{SAMPLE} = 250 kSPS
I_{DD} (Operational)			0.25	mA	V_{DD} = 16.5 V, f_{SAMPLE} = 250 kSPS
Partial Power-Down Mode			7	mA	AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
Full Power-Down Mode ($\overline{STBY}$ Pin)			60	µA	SCLK on or off, AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
Power Dissipation					AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
Normal Mode—Static			94	mW	
Normal Mode—Operational			140	mW	f_{SAMPLE} = 250 kSPS
Partial Power-Down Mode			40	mW	
Full Power-Down Mode ($\overline{STBY}$ Pin)			315	µW	

[1] See the Terminology section.
[2] Sample tested during initial release to ensure compliance.
[3] Includes I_{AVCC}, I_{VDD}, I_{VSS}, I_{VDRIVE}, and I_{DVCC}.

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V_{REF} = 2.5 V internal/external, AV_{CC} = 4.75 V to 5.25 V, DV_{CC} = 4.75 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V; for ±4 × V_{REF} range, V_{DD} = 10 V to 16.5 V, V_{SS} = −10 V to −16.5 V; for ±2 × V_{REF} range, V_{DD} = 5 V to 16.5 V, V_{SS} = −5 V to −16.5 V; f_{SAMPLE} = 250 kSPS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 10 kHz sine wave
Signal-to-(Noise + Distortion) (SINAD)[1]		73.5		dB	
		73.5		dB	
Total Harmonic Distortion (THD)[1]			−88	dB	
		−100		dB	
Peak Harmonic or Spurious Noise (SFDR)[1]		−97		dB	
Intermodulation Distortion (IMD)[1]					fa = 10.5 kHz, fb = 9.5 kHz
Second-Order Terms		−106		dB	
Third-Order Terms		−101		dB	
Aperture Delay			10	ns	
Aperture Delay Matching			4	ns	
Aperture Jitter		35		ps	
Channel-to-Channel Isolation[1]		−100		dB	f_{IN} on unselected channels up to 100 kHz
Full-Power Bandwidth		4.5		MHz	@ −3 dB
		2.2		MHz	@ −0.1 dB
DC ACCURACY					
Resolution	12			Bits	
No Missing Codes	12			Bits	
Differential Nonlinearity			±0.7	LSB	
Integral Nonlinearity[1]			±0.5	LSB	
Positive Full-Scale Error[1]			±0.95	% FSR	±0.317% FSR typical
Positive Full-Scale Error Matching[1]			±0.366	% FSR	
Bipolar Zero-Scale Error[1]			±2	LSB	±0.0125% FSR typical
Bipolar Zero-Scale Error Matching[1]			±2	LSB	
Negative Full-Scale Error[1]			±0.95	% FSR	±0.317% FSR typical
Negative Full-Scale Error Matching[1]			±0.366	% FSR	
ANALOG INPUT					See Table 8 for minimum V_{DD}/V_{SS} for each range
Input Voltage Ranges	−4 × V_{REF}		+4 × V_{REF}	V	RNGx bits or RANGE pin = 0
	−2 × V_{REF}		+2 × V_{REF}	V	RNGx bits or RANGE pin = 1
DC Leakage Current			±1	µA	
Input Capacitance[2]		10			±4 × V_{REF} range when in track
		14		pF	±2 × V_{REF} range when in track
REFERENCE INPUT/OUTPUT					
Reference Input Voltage Range	2.5		2.5	V	
DC Leakage Current			±1	µA	
Input Capacitance[2]		18.5		pF	$REF_{EN/\overline{DIS}}$ = 1
Reference Output Voltage	2.49		2.51	V	
Long-Term Stability		150		ppm	1000 hours
Reference Temperature Coefficient			25	ppm/°C	
		6		ppm/°C	
LOGIC INPUTS					
Input High Voltage (V_{INH})	0.7 × V_{DRIVE}			V	
Input Low Voltage (V_{INL})			0.3 × V_{DRIVE}	V	
Input Current (I_{IN})			±10	µA	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance (C_{IN})[2]			10	pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	V_{DRIVE} − 0.2			V	I_{SOURCE} = 200 µA
Output Low Voltage (V_{OL})			0.2	V	I_{SINK} = 200 µA
Floating-State Leakage Current			±10	µA	
Floating-State Output Capacitance[2]			10	pF	
Output Coding	Twos complement				
CONVERSION RATE					
Conversion Time			3.1	µs	
Track-and-Hold Acquisition Time[1, 2]			550	ns	
Throughput Rate			250	kSPS	Parallel interface mode only
POWER REQUIREMENTS					
V_{DD}	−5		+16.5	V	For the 4 × V_{REF} range, V_{DD} = 10 V to 16.5 V
V_{SS}	−5		−16.5	V	For the 4 × V_{REF} range, V_{SS}= −10 V to −16.5 V
AV_{CC}	4.75		5.25	V	
DV_{CC}	4.75		5.25	V	
V_{DRIVE}	2.7		5.25	V	
I_{TOTAL}[3]					Digital inputs = 0 V or V_{DRIVE}
Normal Mode—Static			18	mA	AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} =−16.5 V
Normal Mode—Operational			26	mA	f_{SAMPLE} = 250 kSPS, AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{SS} (Operational)			0.25	mA	V_{SS} = −16.5 V, f_{SAMPLE} = 250 kSPS
I_{DD} (Operational)			0.25	mA	V_{DD} = 16.5 V, f_{SAMPLE} = 250 kSPS
Partial Power-Down Mode			7	mA	AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
Full Power-Down Mode ($\overline{STBY}$ Pin)			60	µA	SCLK on or off, AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
Power Dissipation					AV_{CC} = DV_{CC} = V_{DRIVE} = +5.25 V, V_{DD} = +16.5 V, V_{SS} = −16.5 V
Normal Mode—Static			94	mW	
Normal Mode—Operational			140	mW	f_{SAMPLE} = 250 kSPS
Partial Power-Down Mode			40	mW	
Full Power-Down Mode ($\overline{STBY}$ Pin)			315	µW	

[1] See the Terminology section.
[2] Sample tested during initial release to ensure compliance.
[3] Includes I_{AVCC}, I_{VDD}, I_{VSS}, I_{VDRIVE}, and I_{DVCC}.

TIMING SPECIFICATIONS

AV_{CC} and DV_{CC} = 4.75 V to 5.25 V, V_{DD} = 5 V to 16.5 V, V_{SS} = −5 V to −16.5 V, V_{DRIVE} = 2.7 V to 5.25 V, V_{REF} = 2.5 V internal/external, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 4.

	Limit at t_{MIN}, t_{MAX}			
Parameter[1]	**V_{DRIVE} < 4.75 V**	**V_{DRIVE} = 4.75 V to 5.25 V**	**Unit**	**Description**
PARALLEL INTERFACE				
$t_{CONVERT}$	3	3	µs typ	Conversion time, internal clock
t_{QUIET}	150	150	ns min	Minimum quiet time required between bus relinquish and start of next conversion
t_{ACQ}	550	550	ns min	Acquisition time
t_{10}	25	25	ns min	Minimum CONVST low pulse
t_1	60	60	ns max	CONVST high to BUSY high
$t_{WAKE-UP}$	2	2	ms max	$\overline{STBY}$ rising edge to CONVST rising edge
	25	25	µs max	Partial power-down mode
PARALLEL READ OPERATION				
t_2	0	0	ns min	BUSY to $\overline{RD}$ delay
t_3	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ setup time
t_4	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ hold time
t_5	45	36	ns min	$\overline{RD}$ pulse width
t_6	45	36	ns max	Data access time after $\overline{RD}$ falling edge
t_7	10	10	ns min	Data hold time after $\overline{RD}$ rising edge
t_8	12	12	ns max	Bus relinquish time after $\overline{RD}$ rising edge
t_9	6	6	ns min	Minimum time between reads
PARALLEL WRITE OPERATION				
t_{11}	15	15	ns min	$\overline{WR}$ pulse width
t_{12}	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ setup time
t_{13}	5	5	ns min	$\overline{CS}$ to $\overline{WR}$ hold time
t_{14}	5	5	ns min	Data setup time before $\overline{WR}$ rising edge
t_{15}	5	5	ns min	Data hold after $\overline{WR}$ rising edge
SERIAL INTERFACE				
f_{SCLK}	18	18	MHz max	Frequency of serial read clock
t_{16}	12	12	ns max	Delay from $\overline{CS}$ until DOUTx three-state disabled
t_{17}[2]	22	22	ns max	Data access time after SCLK rising edge/$\overline{CS}$ falling edge
t_{18}	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK low pulse width
t_{19}	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK high pulse width
t_{20}	10	10	ns min	SCLK to data valid hold time after SCLK falling edge
t_{21}	18	18	ns max	$\overline{CS}$ rising edge to DOUTx high impedance

[1] Sample tested during initial release to ensure compliance. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.
[2] A buffer is used on the DOUTx pins (Pin 5 to Pin 7) for this measurement.

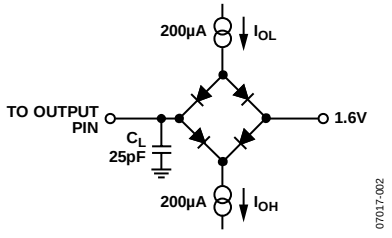

Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to AGND, DGND	−0.3 V to +16.5 V
V_{SS} to AGND, DGND	+0.3 V to −16.5 V
V_{DD} to AV_{CC}	V_{CC} − 0.3 V to +16.5 V
AV_{CC} to AGND, DGND	−0.3 V to +7 V
DV_{CC} to AV_{CC}	−0.3 V to AV_{CC} + 0.3 V
DV_{CC} to DGND, AGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
V_{DRIVE} to DGND	−0.3 V to DV_{CC} + 0.3 V
Analog Input Voltage to AGND[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{DRIVE} + 0.3 V
REFIN/REFOUT to AGND	−0.3 V to AV_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[2]	±10 mA
Operating Temperature Range	
B Version	−40°C to +85°C
Y Version	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb/Sn Temperature, Soldering Reflow (10 sec to 30 sec)	240(+0)°C
Pb-Free Temperature, Soldering Reflow	260(+0)°C
ESD	1.5 kV

[1] If the analog inputs are driven from alternative V_{DD} and V_{SS} supply circuitry, a 240 Ω series resistor should be placed on the analog inputs and Schottky diodes should be placed in series with the V_{DD} and V_{SS} supplies of the AD7656-1/AD7657-1/AD7658-1.

[2] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. These specifications apply to a 4-layer board.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
64-Lead LQFP	45	11	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

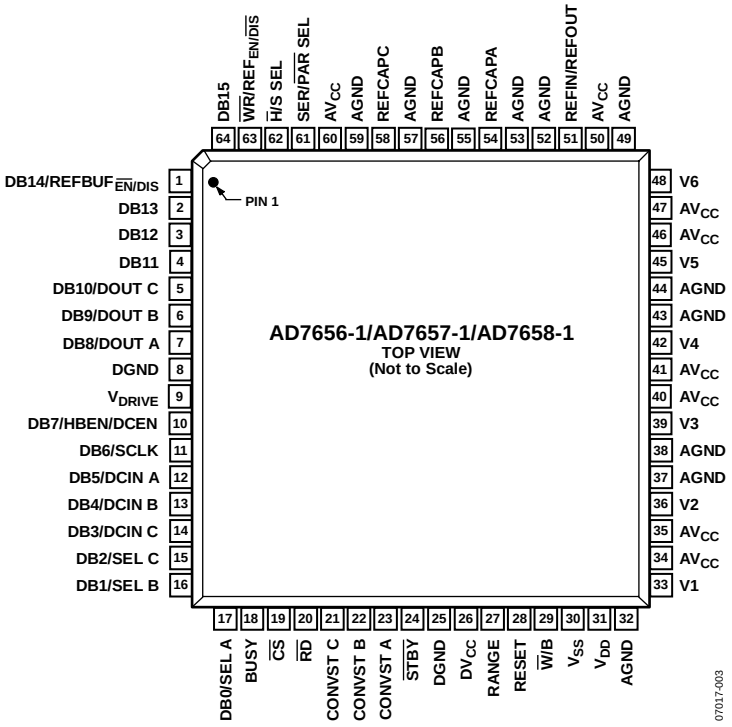

Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
54, 56, 58	REFCAPA, REFCAPB, REFCAPC	Reference Capacitor A, Reference Capacitor B, and Reference Capacitor C. Decoupling capacitors are connected to these pins to decouple the reference buffer for each ADC pair. Decouple each REFCAP pin to AGND using a 1 µF capacitor.
33, 36, 39, 42, 45, 48	V1 to V6	Analog Input 1 to Analog Input 6. These pins are single-ended analog inputs. In hardware mode, the analog input range of these channels is determined by the RANGE pin. In software mode, it is determined by the RNGC to RNGA bits of the control register (see Table 11).
32, 37, 38, 43, 44, 49, 52, 53, 55, 57, 59	AGND	Analog Ground. This pin is the ground reference point for all analog circuitry on the AD7656-1/ AD7657-1/AD7658-1. Refer all analog input signals and external reference signals to this pin. Connect all AGND pins to the AGND plane of the system. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
26	DV_{CC}	Digital Power, 4.75 V to 5.25 V. The DV_{CC} and AV_{CC} voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. Decouple this supply to DGND by placing a 1 µF decoupling capacitor on the DV_{CC} pin.
9	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface.
8, 25	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7656-1/AD7657-1/ AD7658-1. Connect both DGND pins to the DGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
34, 35, 40, 41, 46, 47, 50, 60	AV_{CC}	Analog Supply Voltage, 4.75 V to 5.25 V. This is the supply voltage for the ADC cores. The AV_{CC} and DV_{CC} voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
21, 22, 23	CONVST C, CONVST B, CONVST A	Conversion Start Input A, Conversion Start Input B, and Conversion Start Input C. These logic inputs are used to initiate conversions on the ADC pairs. CONVST A is used to initiate simultaneous conversions on V1 and V2. CONVST B is used to initiate simultaneous conversions on V3 and V4. CONVST C is used to initiate simultaneous conversions on V5 and V6. When one of these pins switches from low to high, the track-and-hold switch on the selected ADC pair switches from track to hold, and the conversion is initiated. These inputs can also be used to place the ADC pairs into partial power-down mode.

Pin No.	Mnemonic	Description
19	$\overline{CS}$	Chip Select. This active low logic input frames the data transfer. If both $\overline{CS}$ and $\overline{RD}$ are logic low and the parallel interface is selected, the output bus is enabled and the conversion result is output on the parallel data bus lines. If both $\overline{CS}$ and $\overline{WR}$ are logic low and the parallel interface is selected, DB[15:8] are used to write data to the on-chip control register. When the serial interface is selected, the $\overline{CS}$ is used to frame the serial read transfer and clock out the MSB of the serial output data.
20	$\overline{RD}$	Read Data. If both $\overline{CS}$ and $\overline{RD}$ are logic low and the parallel interface is selected, the output bus is enabled. When the serial interface is selected, the $\overline{RD}$ line should be held low.
63	$\overline{WR}$/$REF_{EN/\overline{DIS}}$	Write Data/Reference Enable and Disable. When the $\overline{H}$/S SEL pin is high and both $\overline{CS}$ and $\overline{WR}$ are logic low, DB[15:8] are used to write data to the internal control register. When the $\overline{H}$/S SEL pin is low, this pin is used to enable or disable the internal reference. When $\overline{H}$/S SEL = 0 and $REF_{EN/\overline{DIS}}$ = 0, the internal reference is disabled and an external reference should be applied to the REFIN/REFOUT pin. When $\overline{H}$/S SEL = 0 and $REF_{EN/\overline{DIS}}$ = 1, the internal reference is enabled and the REFIN/REFOUT pin should be decoupled. See the Internal/External Reference section.
18	BUSY	Busy Output. This pin transitions to high when a conversion is started and remains high until the conversion is complete and the conversion data is latched into the output data registers. A new conversion cannot be initiated on the AD7656-1/AD7657-1/AD7658-1 when the BUSY signal is high because any applied CONVST edges are ignored.
51	REFIN/REFOUT	Reference Input/Reference Output. The on-chip reference is available via this pin. Alternatively, the internal reference can be disabled and an external reference can be applied to this input. See the Internal/External Reference section. When the internal reference is enabled, decouple this pin using at least a 1 µF decoupling capacitor.
61	SER/$\overline{PAR}$ SEL	Serial/Parallel Selection Input. When this pin is low, the parallel interface is selected. When this pin is high, the serial interface is selected. When the serial interface is selected, DB[10:8] function as DOUT[C:A], DB[0:2] function as DOUT, and DB7 functions as DCEN. When the serial interface is selected, tie DB15 and DB[13:11] to DGND.
17	DB0/SEL A	Data Bit 0/Select DOUT A. When SER/$\overline{PAR}$ SEL = 0, this pin acts as a three-state parallel digital output pin. When SER/$\overline{PAR}$ SEL = 1, this pin functions as SEL A and is used to configure the serial interface. If this pin is 1, the serial interface operates with one, two, or three DOUT output pins and enables DOUT A as a serial output. When the serial interface is selected, always set this pin to 1.
16	DB1/SEL B	Data Bit 1/Select DOUT B. When SER/$\overline{PAR}$ SEL = 0, this pin acts as a three-state parallel digital output pin. When SER/$\overline{PAR}$ SEL = 1, this pin functions as SEL B and is used to configure the serial interface. If this pin is 1, the serial interface operates with two or three DOUT output pins and enables DOUT B as a serial output. If this pin is 0, the DOUT B is not enabled to operate as a serial data output pin and only one DOUT output pin, DOUT A, is used. Unused serial DOUT pins should be left unconnected.
15	DB2/SEL C	Data Bit 2/Select DOUT C. When SER/$\overline{PAR}$ SEL = 0, this pin acts as a three-state parallel digital output pin. When SER/$\overline{PAR}$ SEL = 1, this pin functions as SEL C and is used to configure the serial interface. If this pin is 1, the serial interface operates with three DOUT output pins and enables DOUT C as a serial output. If this pin is 0, the DOUT C is not enabled to operate as a serial data output pin. Unused serial DOUT pins should be left unconnected.
14	DB3/DCIN C	Data Bit 3/Daisy-Chain Input C. When SER/$\overline{PAR}$ SEL = 0, this pin acts as a three-state parallel digital output pin. When SER/$\overline{PAR}$ SEL = 1 and DCEN = 1, this pin acts as Daisy-Chain Input C. When the serial interface is selected but the device is not used in daisy-chain mode, tie this pin to DGND.
13	DB4/DCIN B	Data Bit 4/Daisy-Chain Input B. When SER/$\overline{PAR}$ SEL = 0, this pin acts as a three-state parallel digital output pin. When SER/$\overline{PAR}$ SEL = 1 and DCEN = 1, this pin acts as Daisy-Chain Input B. When the serial interface is selected but the device is not used in daisy-chain mode, tie this pin to DGND.
12	DB5/DCIN A	Data Bit 5/Daisy-Chain Input A. When SER/$\overline{PAR}$ SEL is low, this pin acts as a three-state parallel digital output pin. When SER/$\overline{PAR}$ SEL = 1 and DCEN = 1, this pin acts as Daisy-Chain Input A. When the serial interface is selected but the device is not used in daisy-chain mode, tie this pin to DGND.
11	DB6/SCLK	Data Bit 6/Serial Clock. When SER/$\overline{PAR}$ SEL = 0, this pin acts as a three-state parallel digital output pin. When SER/$\overline{PAR}$ SEL = 1, this pin functions as SCLK input and is the read serial clock for the serial transfer.
10	DB7/HBEN/DCEN	Data Bit 7/High Byte Enable/Daisy-Chain Enable. When the parallel interface is selected and the device is used in word mode (SER/$\overline{PAR}$ SEL = 0 and $\overline{W}$/B = 0), this pin functions as Data Bit 7. When the parallel interface is selected and the device is used in byte mode (SER/$\overline{PAR}$ SEL = 0 and $\overline{W}$/B = 1), this pin functions as HBEN. If the HBEN pin is logic high, the data is output MSB byte first on DB[15:8]. If the HBEN pin is logic low, the data is output LSB byte first on DB[15:8]. When the serial interface is selected (SER/$\overline{PAR}$ SEL = 1), this pin functions as DCEN. If the DCEN pin is logic high, the parts operate in daisy-chain mode with DB[5:3] functioning as DCIN[A:C]. When the serial interface is selected but the device is not used in daisy-chain mode, this pin should be tied to DGND.

Pin No.	Mnemonic	Description
7	DB8/DOUT A	Data Bit 8/Serial Data Output A. When SER/$\overline{\text{PAR}}$ SEL = 0, this pin acts as a three-state parallel digital output pin. When SER/$\overline{\text{PAR}}$ SEL = 1 and SEL A = 1, this pin functions as DOUT A and outputs serial conversion data.
6	DB9/DOUT B	Data Bit 9/Serial Data Output B. When SER/$\overline{\text{PAR}}$ SEL = 0, this pin acts as a three-state parallel digital output pin. When SER/$\overline{\text{PAR}}$ SEL = 1 and SEL B = 1, this pin functions as DOUT B and outputs serial conversion data. This configures the serial interface to have two DOUT output lines.
5	DB10/DOUT C	Data Bit 10/Serial Data Output C. When SER/$\overline{\text{PAR}}$ SEL = 0, this pin acts as a three-state parallel digital output pin. When SER/$\overline{\text{PAR}}$ SEL = 1 and SEL C = 1, this pin functions as DOUT C and outputs serial conversion data. This configures the serial interface to have three DOUT output lines.
4	DB11	Data Bit 11/Digital Ground. When SER/$\overline{\text{PAR}}$ SEL = 0, this pin acts as a three-state parallel digital output pin. When SER/$\overline{\text{PAR}}$ SEL = 1, tie this pin to DGND.
2, 3, 64	DB13, DB12, DB15	Data Bit 12, Data Bit 13, Data Bit 15. When SER/$\overline{\text{PAR}}$ SEL = 0, these pins act as three-state parallel digital input/output pins. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, these pins are used to output the conversion result. When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are low, these pins are used to write to the control register. When SER/$\overline{\text{PAR}}$ SEL = 1, tie these pins to DGND. For the AD7657-1, DB15 contains a leading 0. For the AD7658-1, DB15, DB13, and DB12 contain leading 0s.
1	DB14/REFBUF$\overline{\text{EN}}_{/\text{DIS}}$	Data Bit 14/Reference Buffer Enable and Disable. When SER/$\overline{\text{PAR}}$ SEL = 0, this pin acts as a three-state digital input/output pin. For the AD7657-1 and AD7658-1, DB14 contains a leading 0. When SER/$\overline{\text{PAR}}$ SEL = 1, this pin can be used to enable or disable the internal reference buffers.
28	RESET	Reset Input. When set to logic high, this pin resets the AD7656-1/AD7657-1/AD7658-1. In software mode, the current conversion is aborted and the internal register is set to all 0s. In hardware mode, the AD7656-1/AD7657-1/AD7658-1 are configured depending on the logic levels on the hardware select pins. In all modes, the parts should receive a RESET pulse after power-up. The RESET high pulse should be typically 100 ns wide. The CONVST pin may be held high during the RESET pulse. However, if the CONVST pin is held low during the RESET pulse, then after the RESET pulse, the AD7656-1/AD7657-1 /AD7658-1 need to receive a complete CONVST pulse to initiate the first conversion; this should consist of a high-to-low CONVST edge followed by a low-to-high CONVST edge. In hardware mode, the user can initiate a RESET pulse between conversion cycles, that is, a 100 ns RESET pulse can be applied to the device after BUSY has transitioned from high to low and the data has been read. The RESET can then be issued prior to the next complete CONVST pulse. Ensure that in such a case, RESET has returned to logic low prior to the next complete CONVST pulse.
27	RANGE	Analog Input Range Selection. Logic input. The logic level on this pin determines the input range of the analog input channels. When this pin is Logic 1 at the falling edge of BUSY, the range for the next conversion is $\pm 2 \times V_{REF}$. When this pin is Logic 0 at the falling edge of BUSY, the range for the next conversion is $\pm 4 \times V_{REF}$. In hardware select mode, the RANGE pin is checked on the falling edge of BUSY. In software mode ($\overline{\text{H}}$/S SEL = 1), the RANGE pin can be tied to DGND, and the input range is determined by the RNGA, RNGB, and RNGC bits in the control register.
31	V_{DD}	Positive Power Supply Voltage. This is the positive supply voltage for the analog input section.
30	V_{SS}	Negative Power Supply Voltage. This is the negative supply voltage for the analog input section.
24	$\overline{\text{STBY}}$	Standby Mode Input. This pin is used to put all six on-chip ADCs into standby mode. The $\overline{\text{STBY}}$ pin is high for normal operation and low for standby operation.
62	$\overline{\text{H}}$/S SEL	Hardware/Software Select Input. Logic input. When $\overline{\text{H}}$/S SEL = 0, the AD7656-1/AD7657-1/AD7658-1 operate in hardware select mode, and the ADC pairs to be simultaneously sampled are selected by the $\overline{\text{CONVST}}$ pins. When $\overline{\text{H}}$/S SEL = 1, the ADC pairs to be sampled simultaneously are selected by writing to the control register. When the serial interface is selected, CONVST A is used to initiate conversions on the selected ADC pairs.
29	$\overline{\text{W}}$/B	Word/Byte Input. When this pin is logic low, data can be transferred to and from the AD7656-1/ AD7657-1/AD7658-1 using the parallel data lines DB[15:0]. When this pin is logic high and the parallel interface is selected, byte mode is enabled. In this mode, data is transferred using Data Lines DB[15:8], and DB 7 functions as HBEN. To obtain the 16-bit conversion result, 2-byte reads are required. When the serial interface is selected, tie this pin to DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

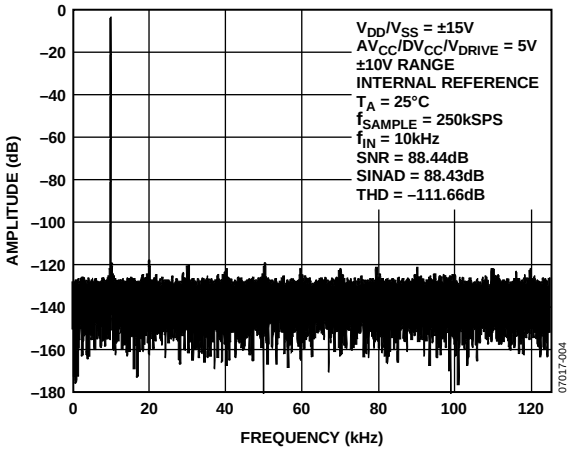

Figure 4. AD7656-1 FFT for ±5 V Range (V_{DD}/V_{SS} = ±15 V)

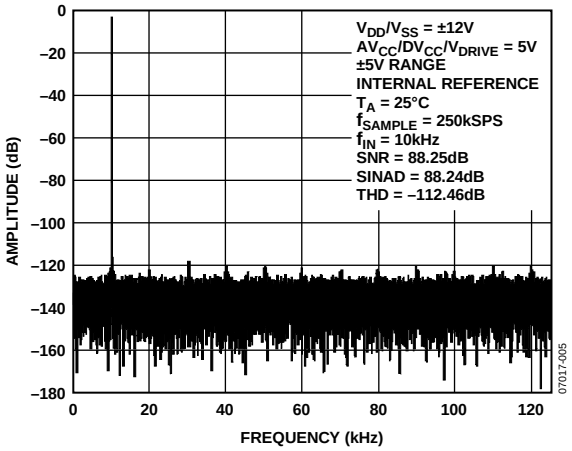

Figure 5. AD7656-1 FFT for ±5 V Range (V_{DD}/V_{SS} = ±12 V)

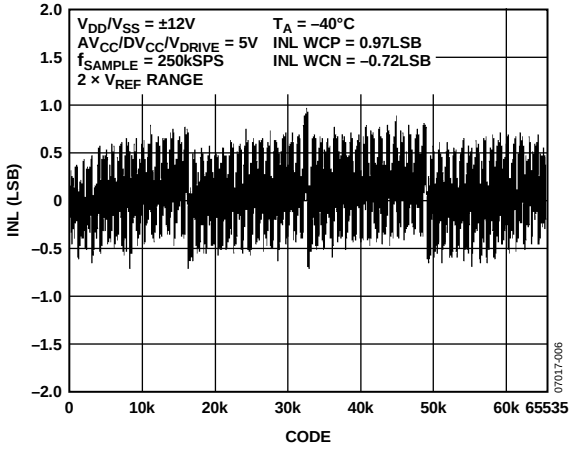

Figure 6. AD7656-1 Typical INL

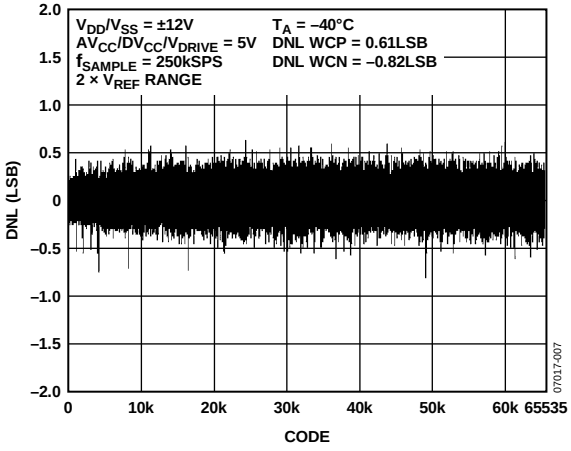

Figure 7. AD7656-1 Typical DNL

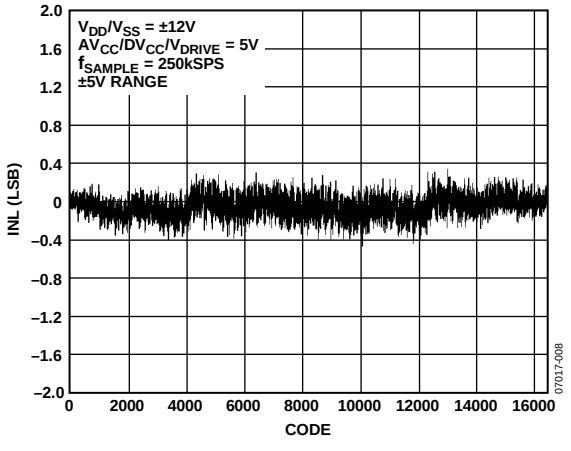

Figure 8. AD7657-1 Typical INL

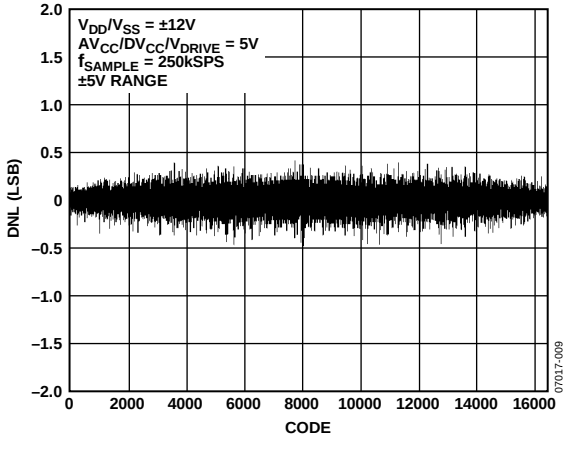

Figure 9. AD7657-1 Typical DNL

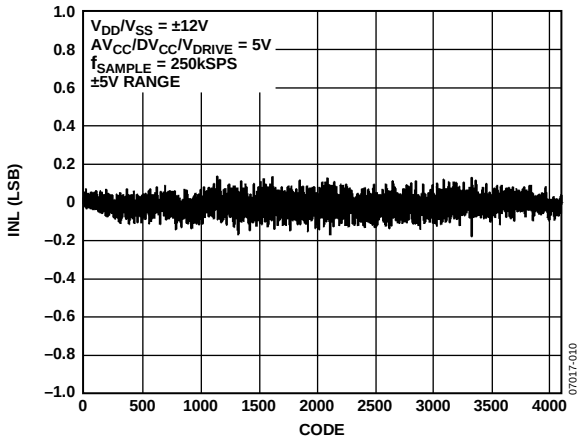

Figure 10. AD7658-1 Typical INL

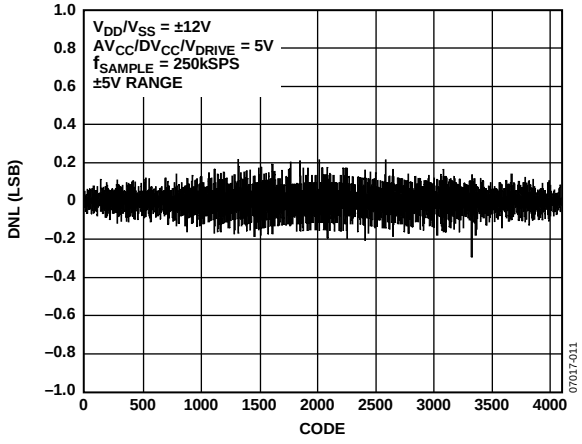

Figure 11. AD7658-1 Typical DNL

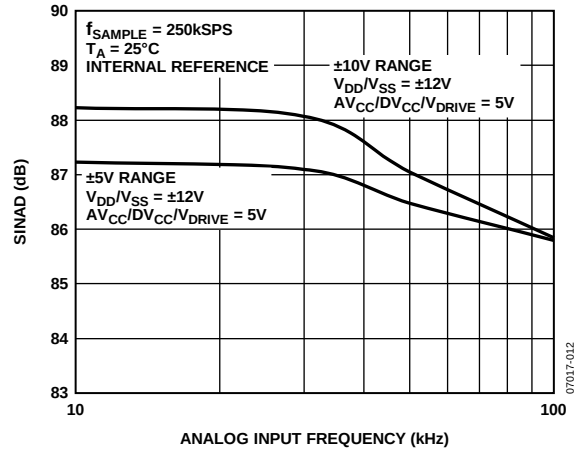

Figure 12. AD7656-1 SINAD vs. Analog Input Frequency

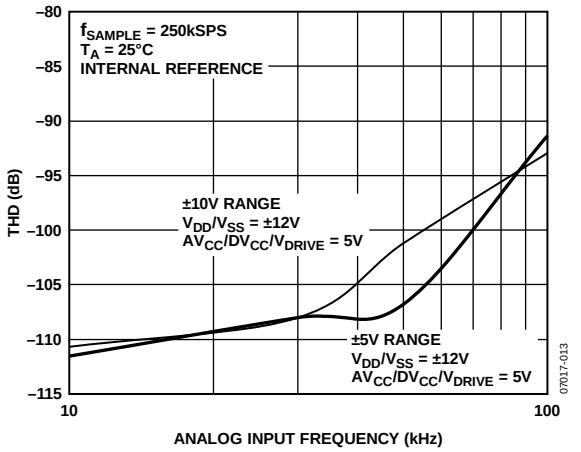

Figure 13. AD7656-1 THD vs. Analog Input Frequency

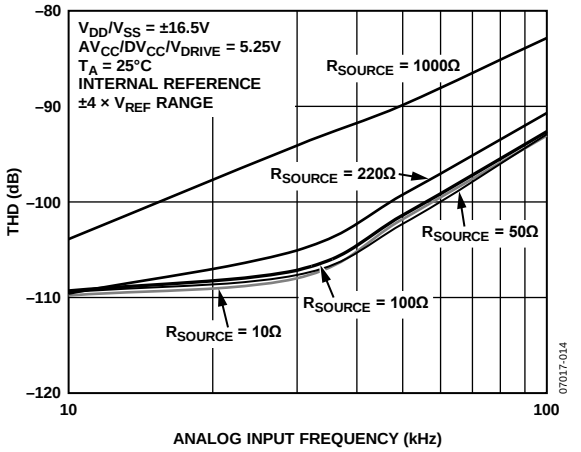

Figure 14. AD7656-1 THD vs. Analog Input Frequency for Various Source Impedances, ±4 × V_{REF} Range

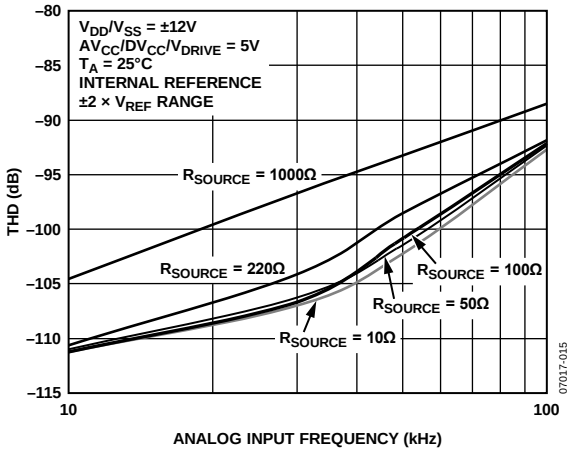

Figure 15. AD7656-1 THD vs. Analog Input Frequency for Various Source Impedances, ±2 × V_{REF} Range

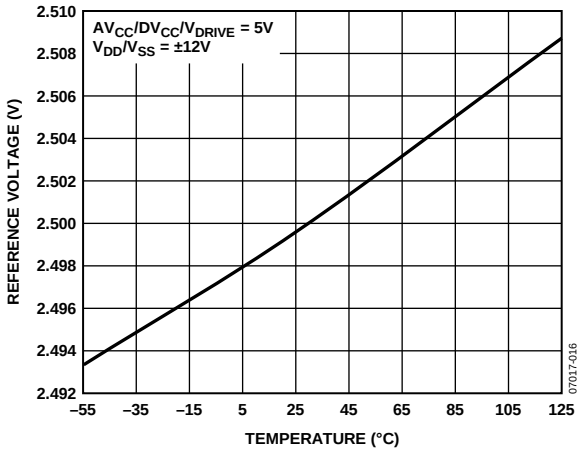

Figure 16. Reference Voltage vs. Temperature

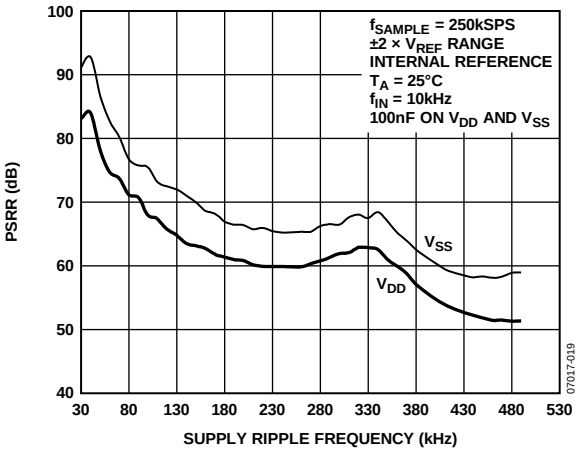

Figure 19. PSRR vs. Supply Ripple Frequency

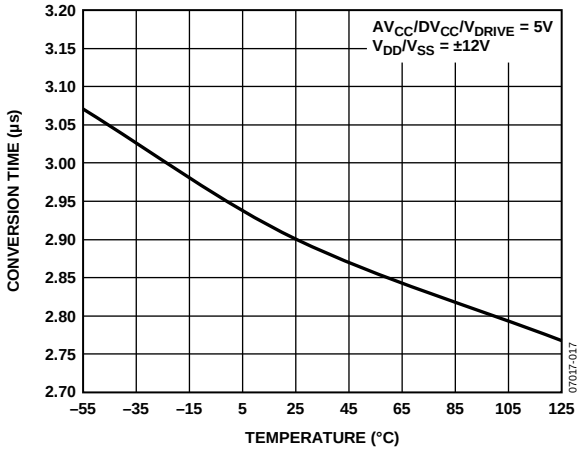

Figure 17. Conversion Time vs. Temperature

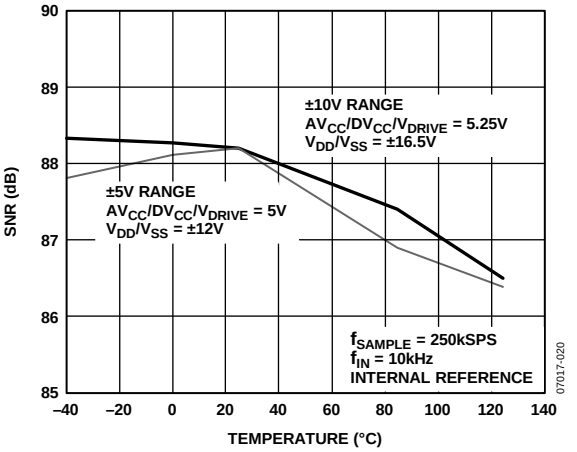

Figure 20. AD7656-1 SNR vs. Temperature

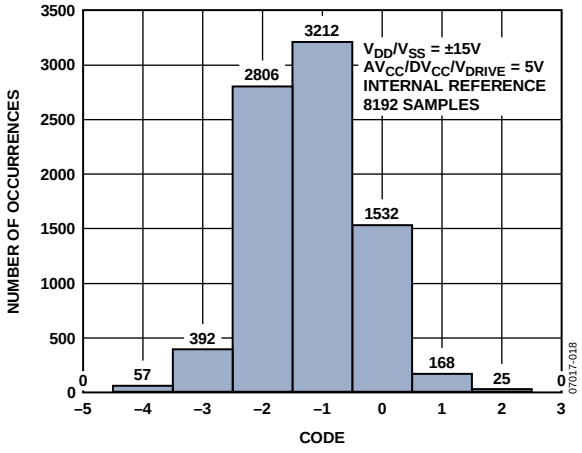

Figure 18. AD7656-1 Histogram of Codes

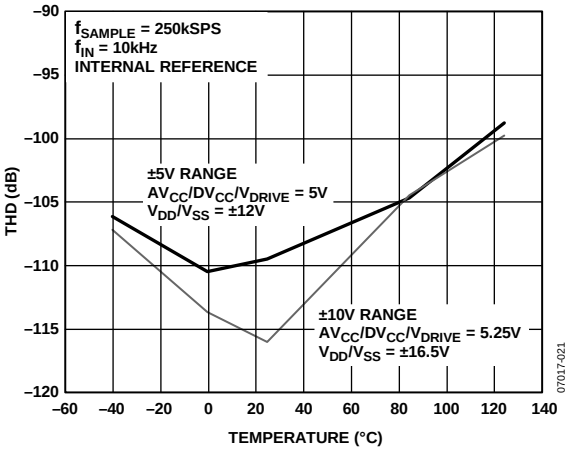

Figure 21. AD7656-1 THD vs. Temperature

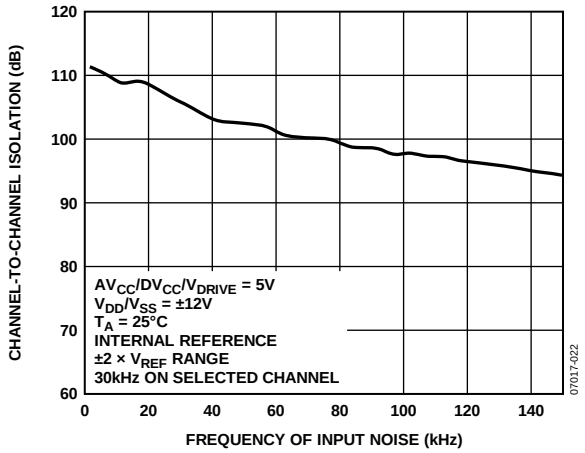

Figure 22. Channel-to-Channel Isolation vs. Frequency of Input Noise

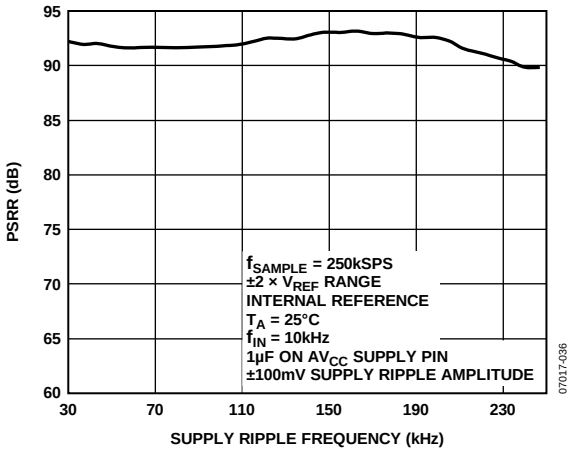

Figure 24. PSRR vs. Supply Ripple Frequency for AV_{CC} Supply

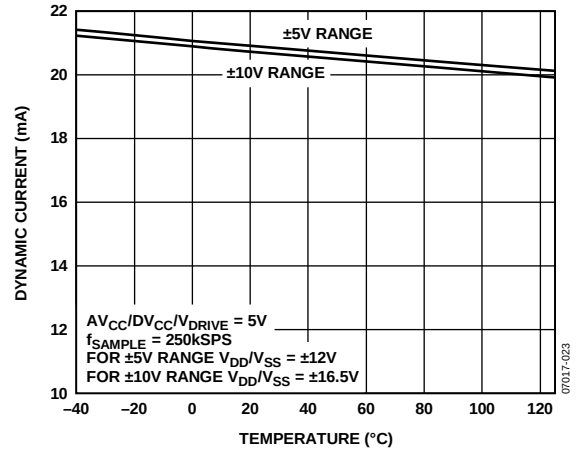

Figure 23. Dynamic Current vs. Temperature

TERMINOLOGY

Integral Nonlinearity (INL)
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale at a ½ LSB below the first code transition and full scale at ½ LSB above the last code transition.

Differential Nonlinearity (DNL)
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Bipolar Zero Scale Error
The deviation of the midscale transition (all 1s to all 0s) from the ideal V_{IN} voltage, that is, AGND − 1 LSB.

Bipolar Zero Scale Error Matching
The difference in bipolar zero code error between any two input channels.

Positive Full-Scale Error
The deviation of the last code transition (011 … 110 to 011 … 111) from the ideal (+4 × V_{REF} − 1 LSB, +2 × V_{REF} − 1 LSB) after adjusting for the bipolar zero scale error.

Positive Full-Scale Error Matching
The difference in positive full-scale error between any two input channels.

Negative Full-Scale Error
The deviation of the first code transition (10 … 000 to 10 … 001) from the ideal (−4 × V_{REF} + 1 LSB, −2 × V_{REF} + 1 LSB) after adjusting for the bipolar zero scale error.

Negative Full-Scale Error Matching
The difference in negative full-scale error between any two input channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of the conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of the conversion. See the Track-and-Hold section for more details.

Signal-to-(Noise + Distortion) Ratio (SINAD)
The measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f_{SAMPLE}/2, excluding dc).

The ratio depends on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical SINAD ratio for an ideal N-bit converter with a sine wave input is given by

$$SINAD = (6.02\ N + 1.76)\ \text{dB}$$

Therefore, SINAD is 98 dB for a 16-bit converter, 86.04 dB for a 14-bit converter, and 74 dB for a 12-bit converter.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the harmonics to the fundamental. For the AD7656-1/AD7657-1/AD7658-1, it is defined as

$$THD\ (\text{dB}) = 20\ \log\frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + V_5{}^2 + V_6{}^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to f_{SAMPLE}/2, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is determined by a noise peak.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities create distortion products at the sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7656-1/AD7657-1/AD7658-1 are tested using the CCIF standard in which two input frequencies near the maximum input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals and is expressed in decibels.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between any two channels. It is measured by applying a full-scale, 100 kHz sine wave signal to all unselected input channels and determining the degree to which the signal attenuates in the selected channel with a 30 kHz signal.

Power Supply Rejection (PSR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. Power supply rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value. See the Typical Performance Characteristics section.

Figure 19 shows the power supply rejection ratio vs. supply ripple frequency for the AD7656-1/AD7657-1/AD7658-1. The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200 mV p-p sine wave applied to the V_{DD} and V_{SS} supplies of the ADC at a frequency sampled, f_{SAMPLE}, as follows:

$$PSRR \text{ (dB)} = 10 \log(Pf/Pf_S)$$

where:
Pf is equal to the power at Frequency f in the ADC output.
Pf_S is equal to the power at Frequency f_{SAMPLE} coupled onto the V_{DD} and V_{SS} supplies.

% FSR
%FSR is calculated using the full theoretical span of the ADC.

THEORY OF OPERATION

CONVERTER DETAILS

The AD7656-1/AD7657-1/AD7658-1 are pin- and software-compatible, reduced decoupling versions of the AD7656/AD7657/AD7658 devices. In addition, the AD7656-1/AD7657-1/AD7658-1 are high speed, low power converters that allow the simultaneous sampling of six on-chip ADCs. The analog inputs on the AD7656-1/AD7657-1/AD7658-1 can accept true bipolar input signals. The RANGE pin or RNGx bits are used to select either $\pm 4 \times V_{REF}$ or $\pm 2 \times V_{REF}$ as the input range for the next conversion.

Each AD7656-1/AD7657-1/AD7658-1 contains six SAR ADCs, six track-and-hold amplifiers, an on-chip 2.5 V reference, reference buffers, and high speed parallel and serial interfaces. The parts allow the simultaneous sampling of all six ADCs when the three CONVST pins (CONVST A, CONVST B, and CONVST C) are tied together. Alternatively, the six ADCs can be grouped into three pairs. Each pair has an associated CONVST signal used to initiate simultaneous sampling on each ADC pair, on four ADCs, or on all six ADCs. CONVST A is used to initiate simultaneous sampling on V1 and V2, CONVST B is used to initiate simultaneous sampling on V3 and V4, and CONVST C is used to initiate simultaneous sampling on V5 and V6.

A conversion is initiated on the AD7656-1/AD7657-1/AD7658-1 by pulsing the CONVST input. On the rising edge of CONVST, the track-and-hold amplifier of the selected ADC pair is placed into hold mode and the conversions are started. After the rising edge of CONVST, the BUSY signal goes high to indicate that the conversion is taking place. The conversion clock for the AD7656-1/AD7657-1/AD7658-1 is internally generated, and the conversion time for the parts is 3 µs. Any further CONVST rising edges on either CONVST A, CONVST B or CONVST C are ignored as long as BUSY is high. The BUSY signal returns low to indicate the end of a conversion. On the falling edge of BUSY, the track-and-hold amplifier returns to track mode. Data can be read from the output register via the parallel or serial interface.

Track-and-Hold Amplifiers

The track-and-hold amplifiers on the AD7656-1/AD7657-1/AD7658-1 allow the ADCs to accurately convert an input sine wave of full-scale amplitude to 16-/14-/12-bit resolution, respectively. The input bandwidth of the track-and-hold amplifiers is greater than the Nyquist rate of the ADC, even when the AD7656-1/AD7657-1/AD7658-1 are operating at the maximum throughput rate. The parts can handle input frequencies of up to 4.5 MHz.

The track-and-hold amplifiers sample their respective inputs simultaneously on the rising edge of CONVST. The aperture time (that is, the delay time between the external CONVST signal actually going into hold) for the track-and-hold amplifier is 10 ns. This is well matched across all six track-and-hold amplifiers on one device and from device to device. This allows more than six ADCs to be sampled simultaneously. The end of the conversion is signaled by the falling edge of BUSY, and it is at this point that the track-and-hold amplifiers return to track mode and the acquisition time begins.

Analog Input

The AD7656-1/AD7657-1/AD7658-1 can handle true bipolar input voltages. The logic level on the RANGE pin or the value written to the RNGx bits in the control register determines the analog input range on the AD7656-1/AD7657-1/AD7658-1 for the next conversion. When the RANGE pin or RNGx bits are 1, the analog input range for the next conversion is $\pm 2 \times V_{REF}$. When the RANGE pin or RNGx bits are 0, the analog input range for the next conversion is $\pm 4 \times V_{REF}$.

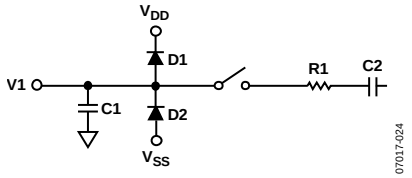

Figure 25. Equivalent Analog Input Structure

Figure 25 shows an equivalent circuit of the analog input structure of the AD7656-1/AD7657-1/AD7658-1. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the V_{DD} and V_{SS} supply rails by more than 300 mV. Signals exceeding this value cause these diodes to become forward-biased and to start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the parts is 10 mA. Capacitor C1 in Figure 25 is typically about 4 pF and can be attributed primarily to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a switch (that is, a track-and-hold switch). This resistor is typically about 3.5 kΩ. Capacitor C2 is the ADC sampling capacitor and has a capacitance of 10 pF typically.

The AD7656-1/AD7657-1/AD7658-1 require V_{DD} and V_{SS} dual supplies for the high voltage analog input structures. These supplies must be equal to or greater than the analog input range (see Table 8 for the requirements on these supplies for each analog input range). The AD7656-1/AD7657-1/AD7658-1 require a low voltage AV_{CC} supply of 4.75 V to 5.25 V to power the ADC core, a DV_{CC} supply of 4.75 V to 5.25 V for the digital power, and a V_{DRIVE} supply of 2.7 V to 5.25 V for the interface power.

To meet the specified performance when using the minimum supply voltage for the selected analog input range, it may be necessary to reduce the throughput rate from the maximum throughput rate.

Table 8. Minimum V_{DD}/V_{SS} Supply Voltage Requirements

Analog Input Range (V)	Reference Voltage (V)	Full-Scale Input (V)	Minimum V_{DD}/V_{SS} (V)
$\pm 4 \times V_{REF}$	2.5	±10	±10
$\pm 2 \times V_{REF}$	2.5	±5	±5

ADC TRANSFER FUNCTION

The output coding of the AD7656-1/AD7657-1/AD7658-1 is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB, 3/2 LSB. The LSB size is FSR/65,536 for the AD7656-1, FSR/16,384 for the AD7657-1, and FSR/4096 for the AD7658-1. The ideal transfer characteristic is shown in Figure 26.

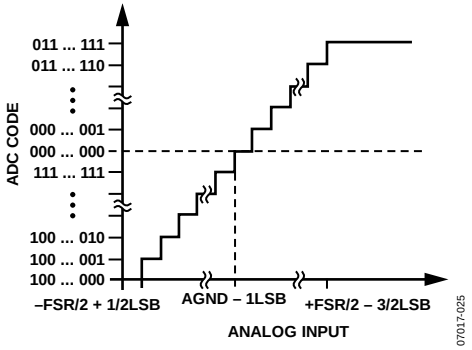

Figure 26. AD7656-1/AD7657-1/AD7658-1 Transfer Characteristic

The LSB size is dependent on the analog input range selected (see Table 9).

INTERNAL/EXTERNAL REFERENCE

The REFIN/REFOUT pin allows access to the 2.5 V reference of the AD7656-1/AD7657-1/AD7658-1, or it allows an external reference to be connected to provide the reference source for conversions.

The AD7656-1/AD7657-1/AD7658-1 can each accommodate a 2.5 V external reference. When applying an external reference via the REFIN/REFOUT pin, the internal reference must be disabled and the reference buffers must be enabled. Alternatively, an external refernce can be applied via the REFCAPx pins, in which case the internal reference should be disabled and it is recommended to disable the reference buffers to save power and minimize crosstalk. After a reset, the AD7656-1/AD7657-1/AD7658-1 default to operating in external reference mode with the internal reference disabled and the reference buffers enabled.

The internal reference can be enabled in either hardware or software mode. To enable the internal reference in hardware mode, set the $\overline{H}$/S SEL pin to 0 and the $REF_{EN/\overline{DIS}}$ pin to 1. To enable the internal reference in software mode, set $\overline{H}$/S SEL to 1 and write to the control register to set DB9 of the register to 1. For the internal reference mode, decouple the REFIN/REFOUT pin using a 1 µF capacitor.

The AD7656-1/AD7657-1/AD7658-1 each contain three on-chip reference buffers as shown in Figure 27. Each of the three ADC pairs has an associated reference buffer. These reference buffers require external decoupling capacitors, using 1 µF capacitors, on the REFCAPA, REFCAPB, and REFCAPC pins. The internal reference buffers can be disabled in software mode by writing to Bit DB8 in the internal control register. If a serial interface is selected, the internal reference buffers can be disabled in hardware mode by setting the $DB14/REFBUF_{\overline{EN}/DIS}$ pin high. If the internal reference and its buffers are disabled, apply an external buffered reference to the REFCAPx pins.

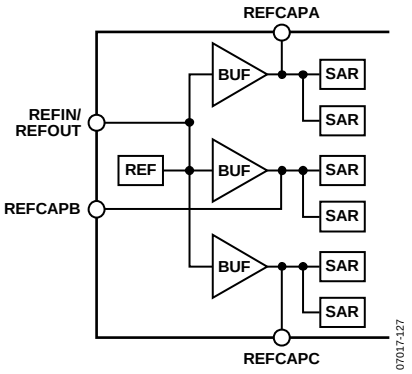

Figure 27. Reference Circuit

TYPICAL CONNECTION DIAGRAM

Figure 28 shows the typical connection diagram for the AD7656-1/AD7657-1/AD7658-1, illustrating the reduction in the number and value of decoupling capacitors that are required. There are eight AV_{CC} supply pins on each part. The AV_{CC} supplies are the supplies used for the AD7656-1/AD7657-1/AD7658-1 conversion process; therefore, they should be well decoupled. The AV_{CC} supply which is applied to eight AV_{CC} pins can be decoupled using just one 1 µF capacitor. The AD7656-1/AD7657-1/AD7658-1 can operate with the internal reference or an externally applied reference. In this configuration, the parts are configured to operate with the external reference. The REFIN/REFOUT pin is decoupled with a 1 µF capacitor. The three internal reference buffers are enabled. Each of the REFCAPx pins is decoupled with a 1 µF capacitor.

If the same supply is being used for the AV_{CC} and DV_{CC} supplies, place a ferrite or small RC filter between the supply pins.

AGND pins are connected to the AGND plane of the system. The DGND pins are connected to the digital ground plane in the system. Connect the AGND and DGND planes together at one place in the system. This connection should be as close as possible to the AD7656-1/AD7657-1/AD7658-1 in the system.

Table 9. LSB Size for Each Analog Input Range

	Input Range for AD7656-1		Input Range for AD7657-1		Input Range for AD7658-1	
Parameter	**±10 V**	**±5 V**	**±10 V**	**±5 V**	**±10 V**	**±5 V**
LSB Size	0.305 mV	0.152 mV	1.22 mV	0.610 mV	4.88 mV	2.44 mV
FS Range	20 V/65,536	10 V/65,536	20 V/16,384	10 V/16,384	20 V/4096	10 V/4096

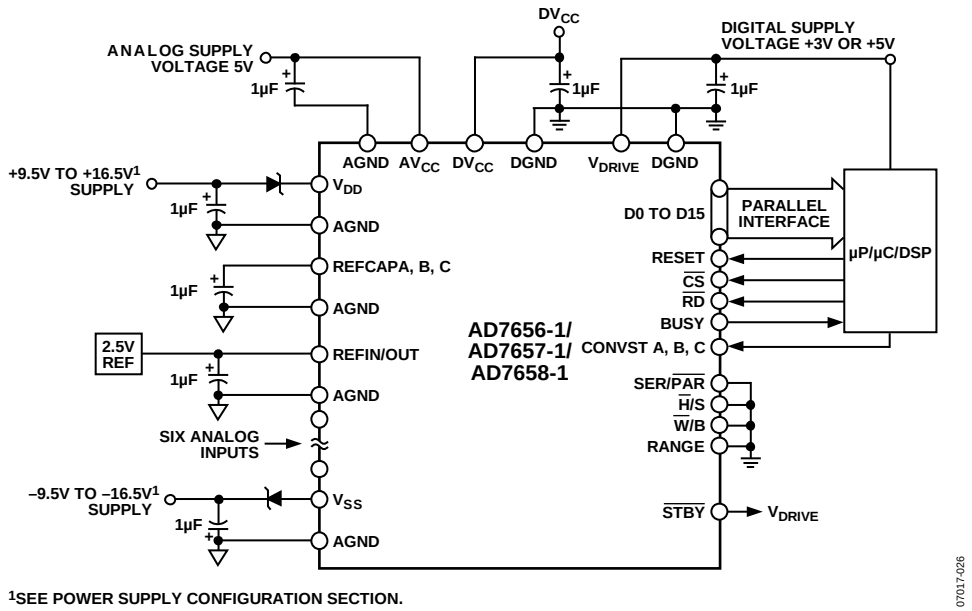

Figure 28. Typical Connection Diagram

The V_{DRIVE} supply is connected to the same supply as the processor. The voltage on V_{DRIVE} controls the voltage value of the output logic signals.

Decouple the V_{DD} and V_{SS} signals with a minimum 1 µF decoupling capacitor. These supplies are used for the high voltage analog input structures on the AD7656-1/AD7657-1/AD7658-1 analog inputs.

DRIVING THE ANALOG INPUTS

Together, the driver amplifier and the analog input circuit used for the AD7656-1 must settle for a full-scale step input to a 16-bit level (0.0015%), which is within the specified 550 ns acquisition time of the AD7656-1. The noise generated by the driver amplifier needs to be kept as low as possible to preserve the SNR and transition noise performance of the AD7656-1. In addition, the driver also needs to have a THD performance suitable for the AD7656-1.

The AD8021 meets these requirements. The AD8021 needs an external compensation capacitor of 10 pF. If a dual version of the AD8021 is required, the AD8022 can be used. The AD8610 and the AD797 can also be used to drive the AD7656-1/AD7657-1/AD7658-1.

INTERFACE OPTIONS

The AD7656-1/AD7657-1/AD7658-1 provide two interface options: a high speed parallel interface and a high speed serial interface. The required interface mode is selected via the SER/$\overline{\text{PAR}}$ SEL pin. The parallel interface can operate in word ($\overline{\text{W}}$/B = 0) or byte ($\overline{\text{W}}$/B = 1) mode. When in serial mode, the AD7656-1/AD7657-1/AD7658-1 can be configured into daisy-chain mode.

When in parallel mode, a read operation only accesses the results related to conversions which have just occurred. For example, consider the case where CONVST A and CONVST C are toggled simultaneously but CONVST B is not used. At end of the conversion process when BUSY goes low a read is implemented. Four read pulses (in parallel mode) are applied and data from V1, V2, V5, and V6 are output. Data from V3 and V4 is not output since CONVST B was not toggled in this cycle. However, when in serial mode all zeros are output in place of the ADC result for ADCs not included in the conversion cycle. See the Serial Interface section for more information.

Parallel Interface (SER/$\overline{\text{PAR}}$ SEL = 0)

The AD7656-1/AD7657-1/AD7658-1 consist of six 16-/14-/12-bit ADCs, respectively. A simultaneous sample of all six ADCs can be performed by connecting all three CONVST pins (CONVST A, CONVST B, and CONVST C) together. The AD7656-1/AD7657-1/AD7658-1 need to see a CONVST pulse to initiate a conversion; this should consist of a falling CONVST edge followed by a rising CONVST edge. The rising edge of CONVST initiates simultaneous conversions on the selected ADCs. The AD7656-1/AD7657-1/AD7658-1 each contain an on-chip oscillator that is used to perform the conversions. The conversion time, t_{CONV}, is 3 µs. The BUSY signal goes low to indicate the end of a conversion. The falling edge of the BUSY signal is used to place the track-and-hold amplifier into track mode.

The AD7656-1/AD7657-1/AD7658-1 also allow the six ADCs to be converted simultaneously in pairs by pulsing the three CONVST pins independently. CONVST A is used to initiate simultaneous conversions on V1 and V2, CONVST B is used to initiate simultaneous conversions on V3 and V4, and CONVST C is used to initiate simultaneous conversions on V5 and V6. The conversion results from the simultaneously sampled ADCs are stored in the output data registers. Note that once a rising edge occurs on any one CONVST pin to initiate a conversion, then any

further CONVST rising edges on any of the CONVST pins are ignored while BUSY is high.

Data can be read from the AD7656-1/AD7657-1/AD7658-1 via the parallel data bus with standard $\overline{CS}$ and $\overline{RD}$ signals ($\overline{W}/B = 0$). To read the data over the parallel bus, tie SER/$\overline{PAR}$ SEL low. The $\overline{CS}$ and $\overline{RD}$ input signals are internally gated to enable the conversion result onto the data bus. The data lines DB0 to DB15 leave their high impedance state when both $\overline{CS}$ and $\overline{RD}$ are logic low.

The $\overline{CS}$ signal can be permanently tied low, and the $\overline{RD}$ signal can be used to access the conversion results. A read operation can take place after the BUSY signal goes low. The number of required read operations depends on the number of ADCs that are simultaneously sampled (see Figure 29). If CONVST A and CONVST B are simultaneously brought low, four read operations are required to obtain the conversion results from V1, V2, V3, and V4. If CONVST A and CONVST C are simultaneously brought low, four read operations are required to obtain the conversion results from V1, V2, V5, and V6. The conversion results are output in ascending order. For the AD7657-1, DB15 and DB14 contain two leading 0s, and DB[13:0] output the 14-bit conversion result. For the AD7658-1, DB[15:12] contain four leading 0s, and DB[11:0] output the 12-bit conversion result.

When using the three CONVST signals to independently initiate conversions on the three ADC pairs, once a rising edge occurs on any one CONVST pin to initiate a conversion then any further CONVST rising edges on any of the CONVST pins are ignored while BUSY is high.

Although a conversion can be initiated during a read sequence, it is not recommended practice, because doing so may affect the performance of the conversion. For the specified performance, it is recommended to perform the read after the conversion. For unused input channel pairs, tie the associated CONVST pin to V_{DRIVE}.

If there is only an 8-bit bus available, the AD7656-1/AD7657-1/AD7658-1 parallel interface can be configured to operate in byte mode ($\overline{W}/B = 1$). In this configuration, the DB7/HBEN/DCEN pin takes on its HBEN function. Each channel conversion result from the AD7656-1/AD7657-1/AD7658-1 can be accessed in two read operations, with eight bits of data provided on DB15 to DB8 for each of the read operations (see Figure 30). The HBEN pin determines whether the read operation first accesses the high byte or the low byte of the 16-bit conversion result. To always access the low byte first on DB15 to DB8, tie the HBEN pin low. To always access the high byte first on DB15 to DB8, tie the HBEN pin high. In byte mode when all three CONVST pins are pulsed together to initiate simultaneous conversions on all six ADCs, 12 read operations are necessary to read back the six 16-/14-/12-bit conversion results. DB[6:0] should be left unconnected in byte mode.

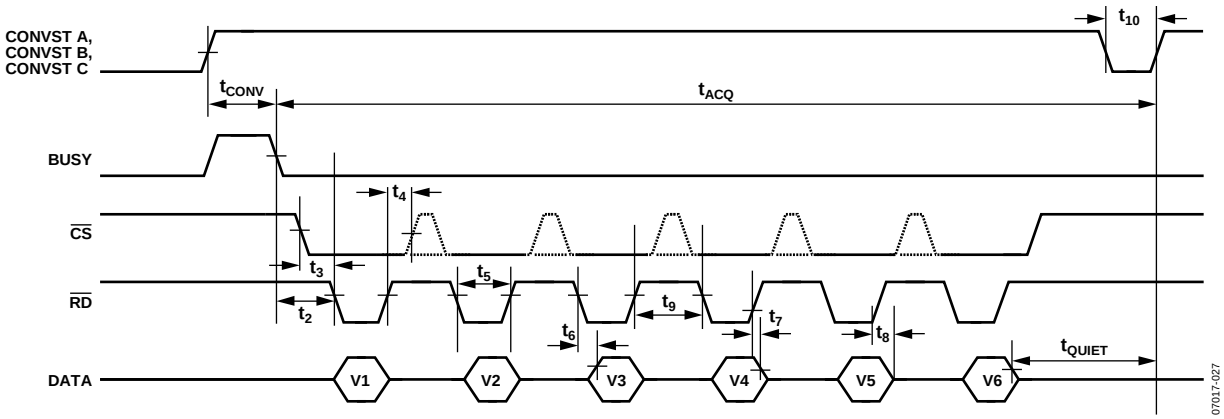

Figure 29. Parallel Interface Timing Diagram ($\overline{W}/B = 0$)

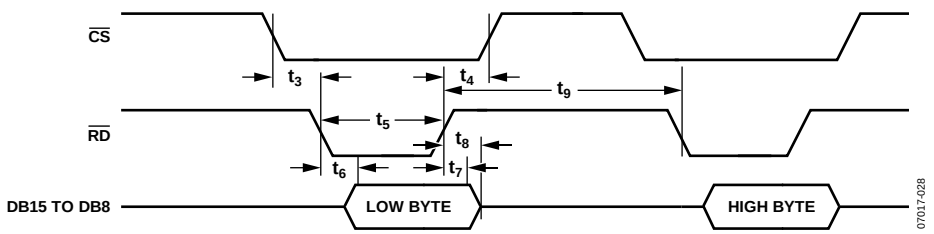

Figure 30. Parallel Interface—Read Cycle for Byte Mode of Operation ($\overline{W}/B = 1$, HBEN = 0)

SOFTWARE SELECTION OF ADCS

The $\overline{H}$/S SEL pin determines the source of the combination of ADCs that are to be simultaneously sampled. When the $\overline{H}$/S SEL pin is logic low, the combination of channels to be simultaneously sampled is determined by the CONVST A, CONVST B, and CONVST C pins. When the $\overline{H}$/S SEL pin is logic high, the combination of channels selected for simultaneous sampling is determined by the contents of the DB15 to DB13 control registers. In this mode, a write to the control register is necessary.

The control register is an 8-bit write-only register. Data is written to this register using the $\overline{CS}$ and $\overline{WR}$ pins and the DB[15:8] data pins (see Figure 31). The control register is detailed in Table 10 and Table 11. To select an ADC pair to be simultaneously sampled, set the corresponding data line high during the write operation.

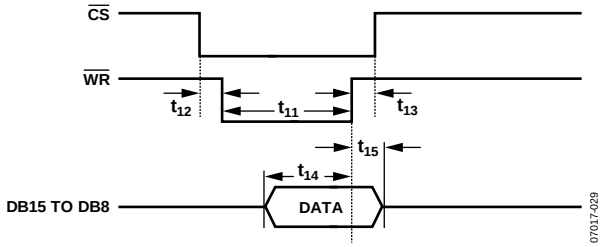

Figure 31. Parallel Interface—Write Cycle for Word Mode ($\overline{W}$/B = 0)

The AD7656-1/AD7657-1/AD7658-1 control register allows individual ranges to be programmed on each ADC pair. DB12 to DB10 in the control register are used to program the range on each ADC pair.

After a reset occurs on the AD7656-1/AD7657-1/AD7658-1, the control register contains all 0s.

The CONVST A signal is used to initiate a simultaneous conversion on the combination of channels selected via the control register. The CONVST B and CONVST C signals can be tied low when operating in software mode ($\overline{H}$/S SEL = 1). The number of read pulses required depends on the number of ADCs selected in the control register and on whether the devices are operating in word or byte mode. The conversion results are output in ascending order.

During the write operation, Data Bus Bit DB15 to Data Bus Bit DB8 are bidirectional and become inputs to the control register when $\overline{RD}$ is logic high and $\overline{CS}$ and $\overline{WR}$ are logic low. The logic state on DB15 through DB8 is latched into the control register when $\overline{WR}$ goes logic high.

Table 10. Control Register Bit Map[1]

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8
VC	VB	VA	RNGC	RNGB	RNGA	REFEN	REFBUF

[1] Default all 0s.

Table 11. Control Register Bit Function Descriptions

Bit	Mnemonic	Description
DB15	VC	This bit is used to select the V5 and V6 analog inputs for the next conversion. When this bit is set to 1, V5 and V6 are simultaneously converted on the next CONVST A rising edge.
DB14	VB	This bit is used to select the V3 and V4 analog inputs for the next conversion. When this bit is set to 1, V3 and V4 are simultaneously converted on the next CONVST A rising edge.
DB13	VA	This bit is used to select the V1 and V2 analog inputs for the next conversion. When this bit is set to 1, V1 and V2 are simultaneously converted on the next CONVST A rising edge.
DB12	RNGC	This bit is used to select the analog input range for the V5 and V6 analog inputs. When this bit is set to 1, the $\pm 2 \times V_{REF}$ range is selected for the next conversion. When this bit is set to 0, the $\pm 4 \times V_{REF}$ range is selected for the next conversion.
DB11	RNGB	This bit is used to select the analog input range for the V3 and V4 analog inputs. When this bit is set to 1, the $\pm 2 \times V_{REF}$ range is selected for the next conversion. When this bit is set to 0, the $\pm 4 \times V_{REF}$ range is selected for the next conversion.
DB10	RNGA	This bit is used to select the analog input range for the V1 and V2 analog inputs. When this bit is set to 1, the $\pm 2 \times V_{REF}$ range is selected for the next conversion. When this bit is set to 0, the $\pm 4 \times V_{REF}$ range is selected for the next conversion.
DB9	REFEN	This bit is used to select the internal reference or an external reference. When this bit is set to 0, the external reference mode is selected. When this bit is set to 1, the internal reference is selected.
DB8	REFBUF	This bit is used to select between using the internal reference buffers and choosing to bypass these reference buffers. When this bit is set to 0, the internal reference buffers are enabled and decoupling is required on the REFCAPx pins. When this bit is set to 1, the internal reference buffers are disabled and a buffered reference should be applied to the REFCAPx pins.

CHANGING THE ANALOG INPUT RANGE ($\overline{H}$/S SEL = 0)

The AD7656-1/AD7657-1/AD7658-1 RANGE pin allows the user to select either ±2 × V_{REF} or ±4 × V_{REF} as the analog input range for the six analog inputs. When the $\overline{H}$/S SEL pin is low, the logic state of the RANGE pin is sampled on the falling edge of the BUSY signal to determine the range for the next simultaneous conversion. When the RANGE pin is logic high at the falling edge of the BUSY signal, the range for the next conversion is ±2 × V_{REF}. When the RANGE pin is logic low at the falling edge of the BUSY signal, the range for the next conversion is ±4 × V_{REF}. After a RESET pulse, the range is updated on the first falling BUSY edge.

CHANGING THE ANALOG INPUT RANGE ($\overline{H}$/S SEL = 1)

When the $\overline{H}$/S SEL pin is high, the range can be changed by writing to the control register. DB[12:10] in the control register are used to select the analog input ranges for the next conversion. Each analog input pair has an associated range bit, allowing independent ranges to be programmed on each ADC pair. When the RNGx bit is set to 1, the range for the next conversion is ±2 × VREF. When the RNGx bit is set to 0, the range for the next conversion is ±4 × VREF.

Serial Interface (SER/$\overline{PAR}$ SEL = 1)

By pulsing one, two, or all three CONVST signals, the AD7656-1/AD7657-1/AD7658-1 use their on-chip trimmed oscillator to simultaneously convert the selected channel pairs on the rising edge of CONVST. After the rising edge of CONVST, the BUSY signal goes high to indicate that the conversion has started. It returns low when the conversion is complete, 3 µs later. Any further CONVST rising edges on either CONVST A, CONVST B, or CONVST C are ignored as long as BUSY is high. The output register is loaded with the new conversion results, and data can be read from the AD7656-1/AD7657-1/AD7658-1. To read the data back from the parts over the serial interface, SER/$\overline{PAR}$ SEL should be tied high. The $\overline{CS}$ and SCLK signals are used to transfer data from the AD7656-1/AD7657-1/AD7658-1. The parts have three DOUT pins: DOUT A, DOUT B, and DOUT C. Data can be read back from each part using one, two, or all three DOUT lines.

Figure 32 shows six simultaneous conversions and the read sequence using three DOUT lines. Also in Figure 32, 32 SCLK transfers are used to access data from the AD7656-1/AD7657-1/AD7658-1; however, two 16-SCLK individually framed transfers with the $\overline{CS}$ signal can also be used to access the data on the three DOUT lines. Any additional SCLKs applied after this result in an output of all zeros. When the serial interface is selected and conversion data is clocking out on all three DOUT lines, tie DB0/SEL A, DB1/SEL B, and DB2/SEL C to V_{DRIVE}. These pins are used to enable the DOUT A to DOUT C lines, respectively.

If it is required to clock conversion data out on two data output lines, use DOUT A and DOUT B. To enable DOUT A and DOUT B, tie DB0/SEL A and DB1/SEL B to VDRIVE, and DB2/SEL C should be tied low. When six simultaneous conversions are performed and only two DOUT lines are used, a 48-SCLK transfer can be used to access the data from the AD7656-1/AD7657-1/AD7658-1. Any additional SCLKs applied after this result in an output of all zeros. The read sequence is shown in Figure 33 for a simultaneous conversion on all six ADCs using two DOUT lines. If a simultaneous conversion occurred on all six ADCs, and only two DOUT lines are used to read the results from the AD7656-1/AD7657-1/AD7658-1, DOUT A clocks out the result from V1, V2, and V5, whereas DOUT B clocks out the results from V3, V4, and V6.

Data can also be clocked out using just one DOUT line, in which case useDOUT A to access the conversion data. To configure the AD7656-1/AD7657-1/AD7658-1 to operate in this mode, tie DB0/SEL A to V_{DRIVE}, and tie DB1/SEL B and DB2/SEL C low. The disadvantage of using only one DOUT line is that the throughput rate is reduced. Data can be accessed from the AD7656-1/AD7657-1/AD7658-1 using one 96-SCLK transfer, three 32-SCLK individually framed transfers, or six 16-SCLK individually framed transfers. Any additional SCLKs applied after this result in an output of all zeros. When using the serial interface, tie the $\overline{RD}$ signal low and leave the unused DOUT line(s) unconnected.

Whether one, two, or three data output lines are used, if a particular CONVST pin is not used in the conversion cycle then all zeros are output in place of the ADC result for the associated ADCs even though they were not used in the conversion cycle. This means that if, for example, only CONVST B is pulsed and one data output pin is in use, then 64 SCLKs are required to access the results from V3 and V4, but only 32 SCLKs are required if two or three data output lines are in use.

SERIAL READ OPERATION

Figure 34 shows the timing diagram for reading data from the AD7656-1/AD7657-1/AD7658-1 when the serial interface is selected. The SCLK input signal provides the clock source for the serial interface. The $\overline{CS}$ signal goes low to access data from the AD7656-1/AD7657-1/AD7658-1. The falling edge of $\overline{CS}$ takes the bus out of three-state and clocks out the MSB of the 16-bit conversion result. The ADCs output 16 bits for each conversion result; the data stream of the AD7656-1 consists of 16 bits of conversion data, provided MSB first. The data stream for the AD7657-1 consists of two leading 0s followed by 14 bits of conversion data, provided MSB first. The data stream for the AD7658-1 consists of four leading 0s and 12 bits of conversion data, provided MSB first.

The first bit of the conversion result is valid on the first SCLK falling edge after the $\overline{CS}$ falling edge. The subsequent 15 data bits are clocked out on the rising edge of the SCLK signal. Data is valid on the SCLK falling edge. To access each conversion result, 16 clock pulses must be provided to the AD7656-1/AD7657-1/AD7658-1. Figure 34 shows how a 16-SCLK read is used to access the conversion results.

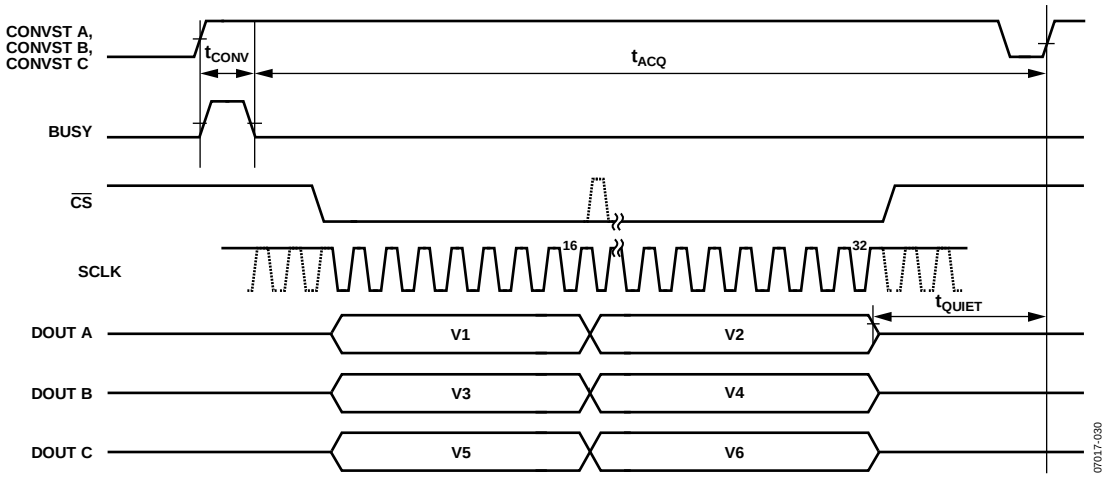

Figure 32. Serial Interface with Three DOUT Lines

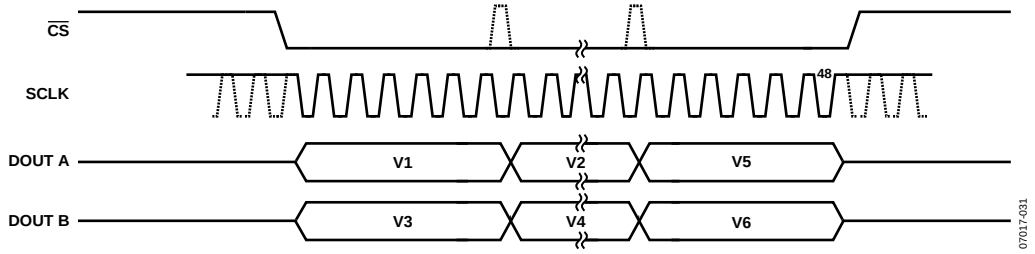

Figure 33. Serial Interface with Two DOUT Lines

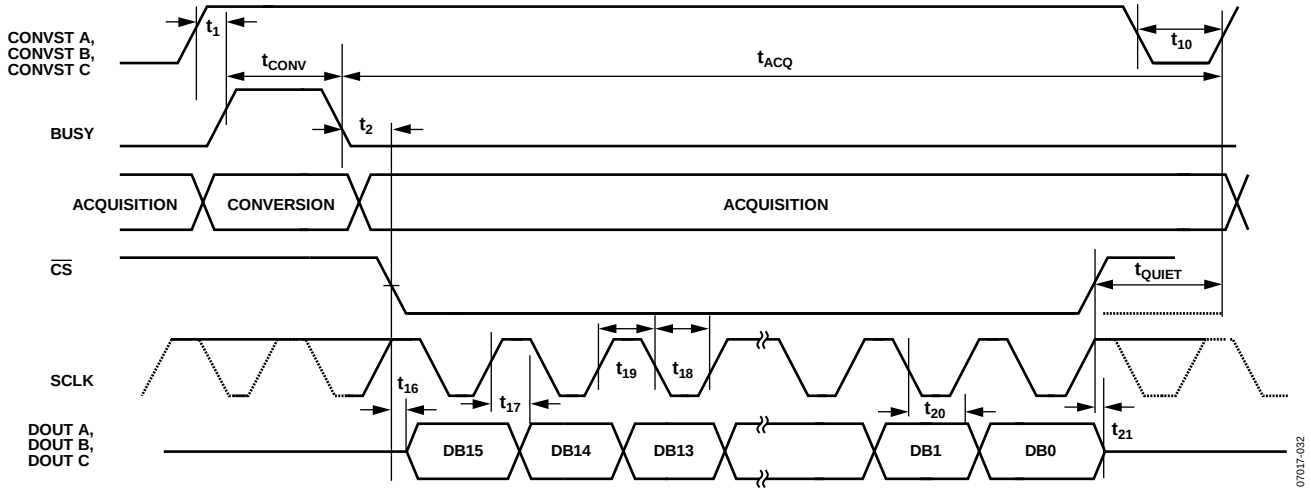

Figure 34. Serial Read Operation

DAISY-CHAIN MODE (DCEN = 1, SER/$\overline{\text{PAR}}$ SEL = 1)

When reading conversion data back from the AD7656-1/AD7657-1/AD7658-1 using one/two/three DOUT pins, it is possible to configure the parts to operate in daisy-chain mode by using the DCEN pin. This daisy-chain feature allows multiple AD7656-1/AD7657-1/AD7658-1 devices to be cascaded together and is useful for reducing the component count and wiring connections. An example connection of two devices is shown in Figure 36. This configuration shows two DOUT lines being used for each device. Simultaneous sampling of the 12 analog inputs is possible by using a common CONVST signal. The DB5, DB4, and DB3 data pins are used as the DCIN[A:C] data input pins for the daisy-chain mode.

The rising edge of CONVST is used to initiate a conversion on the AD7656-1/AD7657-1/AD7658-1. After the BUSY signal has gone low to indicate that the conversion is complete, the user can begin to read the data from the two devices. Figure 37 shows the serial timing diagram when operating two AD7656-1/AD7657-1/AD7658-1 devices in daisy-chain mode.

The $\overline{\text{CS}}$ falling edge is used to frame the serial transfer from the AD7656-1/AD7657-1/AD7658-1 devices, to take the bus out of three-state, and to clock out the MSB of the first conversion result. In the example shown in Figure 37, all 12 ADC channels are simultaneously sampled. Two DOUT lines are used to read the conversion results in this example. $\overline{\text{CS}}$ frames a 96-SCLK transfer. During the first 48 SCLKs, the conversion data is transferred from Device 2 to Device 1. DOUT A on Device 2 transfers conversion data from V1, V2, and V5 into DCIN A in Device 1; DOUT B on Device 2 transfers conversion results from V3, V4, and V6 to DCIN B in Device 1. During the first 48 SCLKs, Device 1 transfers data into the digital host. DOUT A on Device 1 transfers conversion data from V1, V2, and V5; DOUT B on Device 1 transfers conversion data from V3, V4, and V6. During the last 48 SCLKs, Device 2 clocks out 0s, and Device 1 shifts the data clocked in from Device 2 during the first 48 SCLKs into the digital host. This example can also be implemented using six 16-SCLK individually framed transfers if DCEN remains high during the transfers.

Figure 38 shows the timing if two AD7656-1/AD7657-1/AD7658-1 devices are configured in daisy-chain mode and are operating with three DOUT lines. Assuming that a simultaneous sampling of all 12 inputs occurs, the $\overline{\text{CS}}$ frames a 64 SCLK transfer during the read operation. During the first 32 SCLKs of this transfer, the conversion results from Device 1 are clocked into the digital host and the conversion results from Device 2 are clocked into Device 1. During the last 32 SCLKs of the transfer, the conversion results from Device 2 are clocked out of Device 1 and into the digital host, and Device 2 clocks out 0s.

The maximum number of devices in the chain is limited by the throughput required per channel depending on the application needs, the SCLK frequency used, and the number of serial data lines used.

Standby/Partial Power-Down Modes of Operation (SER/$\overline{\text{PAR}}$ SEL = 0 or 1)

Each ADC pair can be individually placed into partial power-down mode at the end of their conversion by bringing the associated CONVST signal low before the falling edge of BUSY. If a CONVST pin is low when BUSY goes low, the associated ADC pair only enters partial power-down mode if they were actually converting within that cycle, that is, if that particular CONVST pin was used to trigger conversions. To power an ADC pair back up, the CONVST signal should be brought high to tell the ADC pair to power up and place the track-and-hold amplifier into track mode. After the power-up time from partial power-down has elapsed, the CONVST signal can receive a rising edge to initiate a valid conversion. In partial power-down mode, the reference buffers remain powered up. When an ADC pair is in partial power-down mode, conversions can still occur on the other fully powered ADCs. In Figure 35 at Point A, ADC 1 and ADC 2 enter partial power-down while ADC 3 to ADC 6 remain fully powered. At Point B in Figure 35, ADC1 and ADC 2 begin to power up. Once the required power up time has elapsed then a conversion can be initiated on the next CONVST rising edge as shown.

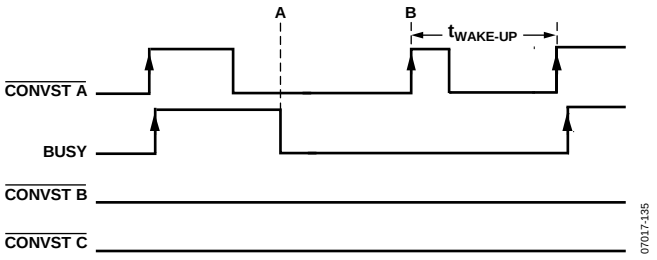

Figure 35. Entering and Exiting Partial Power-Down Mode

The AD7656-1/AD7657-1/AD7658-1 have a standby mode whereby the devices can be placed into a low power consumption mode (315 μW maximum). The AD7656-1/AD7657-1/AD7658-1 are placed into standby mode by bringing the input $\overline{\text{STBY}}$ logic low and can be powered up again for normal operation by bringing $\overline{\text{STBY}}$ logic high. The output data buffers are still operational when the AD7656-1/AD7657-1/AD7658-1 are in standby mode, meaning the user can continue to access the conversion results of the parts. This standby feature can be used to reduce the average power consumed by the AD7656-1/AD7657-1/AD7658-1 when operating at lower throughput rates. The parts can be placed into standby at the end of each conversion when BUSY goes low and are taken out of standby mode prior to the next conversion. The time for the AD7656-1/AD7657-1/AD7658-1 to come out of standby is called the wake-up time. The wake-up time limits the maximum throughput rate at which the AD7656-1/AD7657-1/AD7658-1 can operate when powering down between conversions. See the Specifications section.

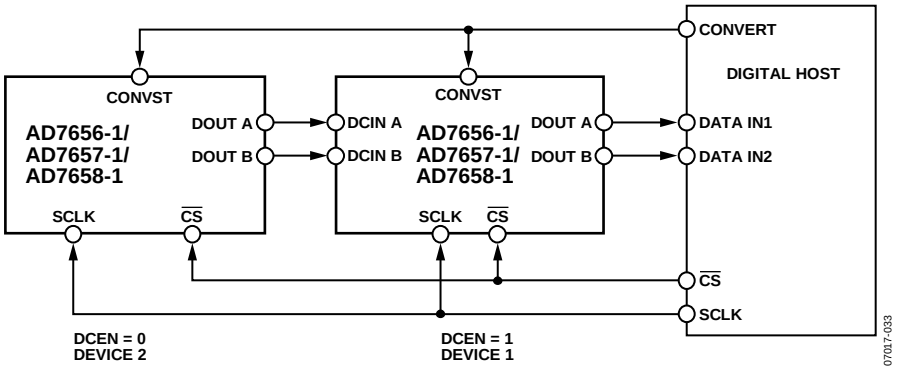

Figure 36. Daisy-Chain Configuration

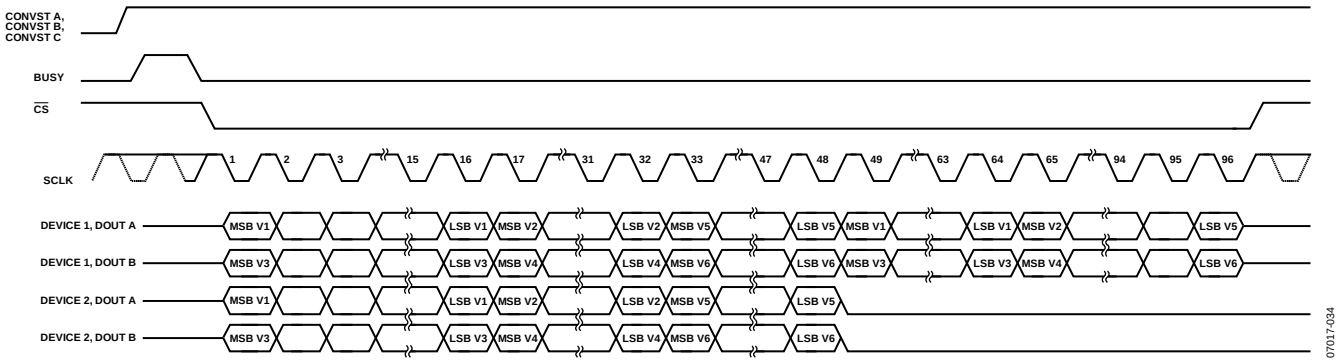

Figure 37. Daisy-Chain Serial Interface Timing with Two DOUT Lines

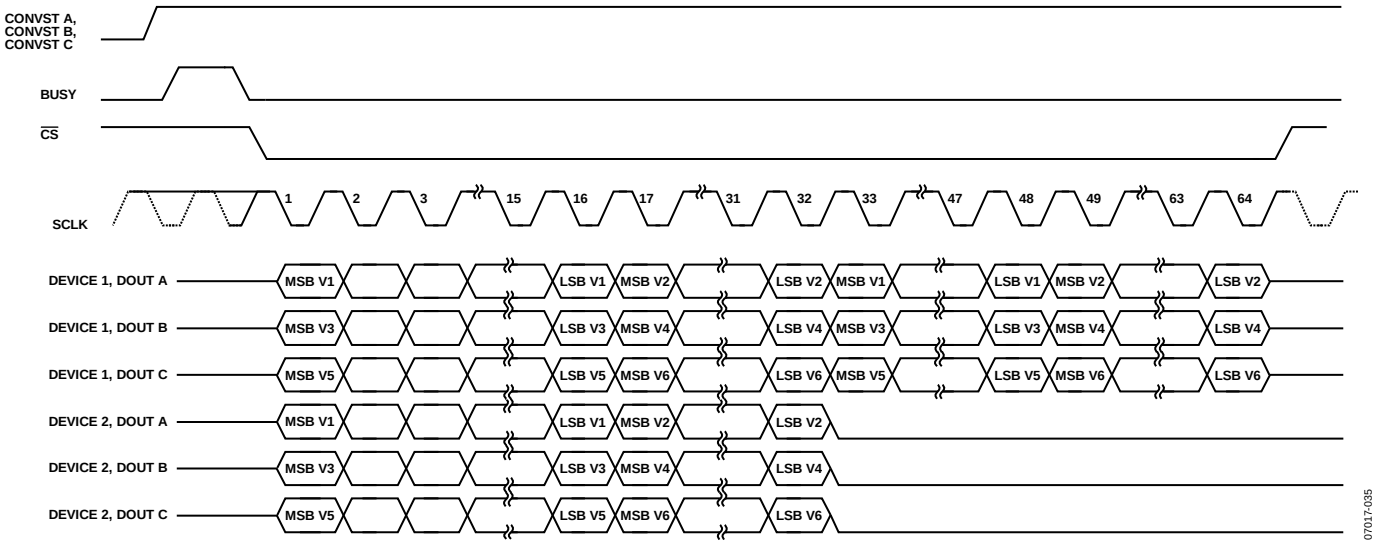

Figure 38. Daisy-Chain Serial Interface Timing with Three DOUT Lines

APPLICATION HINTS

LAYOUT

Design the printed circuit board (PCB) that houses the AD7656-1/AD7657-1/AD7658-1 so that the analog and digital sections are separated and confined to different areas of the board.

Use at least one ground plane. It can be common or split between the digital and analog sections. In the case of the split plane, join the digital and analog ground in only one place, preferably underneath the AD7656-1/AD7657-1/AD7658-1, or at least as close as possible to the part.

If the AD7656-1/AD7657-1/AD7658-1 are in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at only one point, a star ground point, established as close as possible to the AD7656-1/AD7657-1/AD7658-1. Make good connections to the ground plane. Avoid sharing one connection for multiple ground pins. Individual vias or multiple vias to the ground plane should be used for each ground pin.

Avoid running digital lines under the devices because doing so couples noise onto the die. Allow the analog ground plane to run under the AD7656-1/AD7657-1/AD7658-1 to avoid noise coupling. Shield fast-switching signals like CONVST or clocks with digital ground to avoid radiating noise to other sections of the board, and the fast switching signals should never run near analog signal paths. Avoid crossover of digital and analog signals. Traces on layers in close proximity on the board should run at right angles to each other to reduce the effect of feedthrough through the board.

The power supply lines to the AV_{CC}, DV_{CC}, V_{DRIVE}, V_{DD}, and V_{SS} pins on the AD7656-1/AD7657-1/AD7658-1 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Establish good connections between the AD7656-1/AD7657-1/AD7658-1 supply pins and the power tracks on the board; this should involve the use of a single via or multiple vias for each supply pin.

Good decoupling is also important to lower the supply impedance presented to the AD7656-1/AD7657-1/AD7658-1 and to reduce the magnitude of the supply spikes. Place the decoupling capacitors close to, ideally right up against, these pins and their corresponding ground pins. Additionally, place low ESR 1 µF capacitors on each of the supply pins, the REFIN/REFOUT pin, and each REFCAPx pin. Avoid sharing these capacitors between pins, and use vias to connect the capacitors to the power and ground planes. In addition, use wide, short traces between each via and the capacitor pad, or place the vias adjacent to the capacitor pad to minimize parasitic inductances. The AD7656-1/AD7657-1/AD7658-1 offer the user a reduced decoupling solution that is pin and software compatible with AD7656/AD7657/AD7658. The recommended reduced decoupling required for AD7656-1/AD7657-1/AD7658-1 is outlined in Figure 28.

POWER SUPPLY CONFIGURATION

As outlined in the Absolute Maximum Ratings section, the analog inputs should not be applied to the AD7656-1/AD7657-1/AD7658-1 until after the AD7656-1/AD7657-1/AD7658-1 power supplies have been applied to the device. However, if a condition exists where the system analog signal conditioning circuitry supplies are different to the V_{DD} and V_{SS} supplies of the AD7656-1/AD7657-1/AD7658-1, or if the analog inputs may be applied prior to the AD7656-1/AD7657-1/AD7658-1 supplies being established, then an analog input series resister and Schottky diodes in series with the V_{DD} and V_{SS} supplies are recommended (see Figure 39).

This configuration should also be used if AV_{CC} is applied to the AD7656-1/AD7657-1/AD7658-1 prior to V_{DD} and V_{SS} being applied.

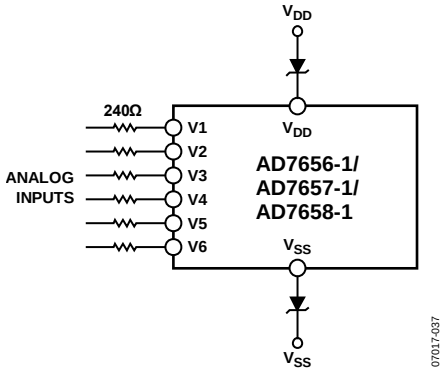

Figure 39. Power Supply Configuration

OUTLINE DIMENSIONS

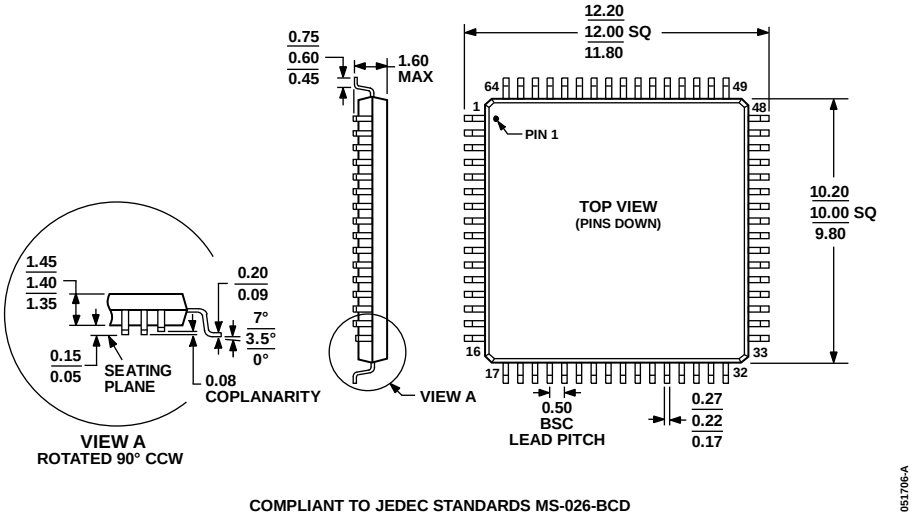

Figure 40. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Notes	Temperature Range	Package Description	Package Option
AD7656BSTZ-1		−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7656BSTZ-1-RL		−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7656YSTZ-1		−40°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7656YSTZ-1-RL		−40°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7657BSTZ-1		−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7657BSTZ-1-RL		−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7657YSTZ-1		−40°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7657YSTZ-1-RL		−40°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7658BSTZ-1		−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7658BSTZ-1-RL		−40°C to +85°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7658YSTZ-1		−40°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7658YSTZ-1-RL		−40°C to +125°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
EVAL-AD7656-1CBZ	[2]		Evaluation Board	
EVAL-AD7657-1CBZ	[2]		Evaluation Board	
EVAL-AD7658-1CBZ	[2]		Evaluation Board	
EVAL-CONTROL BRD2Z	[3]		Controller Board	

[1] Z = RoHS Compliant Part.
[2] This can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL board for evaluation/demonstration purposes.
[3] This board is a complete unit allowing a PC to control and communicate with all Analog Devices, Inc., evaluation boards ending in the CB designators. To order a complete evaluation kit, the particular ADC evaluation board, for example, EVAL-AD7656-1/AD7657-1/AD7658-1CB, the EVAL-CONTROL BRD2, and a 12 V transformer must be ordered. See the relevant evaluation board technical note for more information.

NOTES

NOTES

D07017-0-3/12(D)

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- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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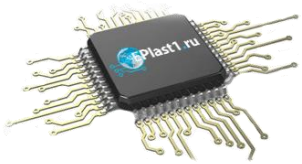
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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