PCA9517A

Product Preview

Level-Translating I²C-Bus Repeater

The PCA9517A is an I²C−bus repeater that provides level shifting between low voltage (down to 0.9 V) and higher voltage (2.7 V to 5.5 V) for I²C−bus or SMBus applications.

Features

- 2 Channel, Bidirectional Buffer Isolates Capacitance and Allows 400 pF on Either Side of the Device
- Voltage Level Translation from 0.9 V to 5.5 V and from 2.7 V to 5.5 V
- Footprint and Functional Replacement for PCA9515/15A
- I²C−bus and SMBus Compatible
- Active HIGH Repeater Enable
- Open−Drain Inputs/Outputs
- Lock−up Free Operation
- Supports Arbitration and Clock Stretching Across the Repeater, and Multiple Masters
- I²C and SMBus SCL Clock Frequency up to 1 MHz (The maximum system operating frequency may be less than 1 MHz because of the delays added by the repeater.)
- Powered−Off High−Impedance I²C−bus Pins
- A Side Operating Supply Voltage Range of 0.9 V to 5.5 V
- B Side Operating Supply Voltage Range of 2.7 V to 5.5 V
- 5 V Tolerant I²C−bus and Enable Pins
- Available in: Micro−8, SOIC8
- ESD Performance: 8 kV HBM, 700 V MM, 2000 V CDM
- These are Pb−Free Devices

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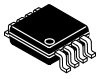
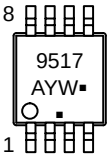
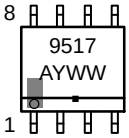
MARKING DIAGRAMS



Micro8™
DM SUFFIX
CASE 846A



SOIC−8
CASE 751



A = Assembly Location
L = Wafer Lot
M = Date Code
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

General Description

The PCA9517A is an I^2C−bus repeater that provides level shifting between low voltage (down to 0.9 V) and higher voltage (2.7 V to 5.5 V) for I^2C−bus or SMBus applications. While retaining all the operating modes and features of the I^2C−bus system during the level shifts, it also permits extension of the I^2C−bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 400 pF. Using the PCA9517A enables the system designer to isolate two halves of a bus for both voltage and capacitance. The SDA and SCL pins are overvoltage tolerant and are high−impedance when the PCA9517A is unpowered.

The 2.7 V to 5.5 V bus B side drivers behave much like the drivers on the PCA9515A device, while the adjustable voltage bus A side drivers drive more current and eliminate the static offset voltage. This results in a LOW on the B side translating into a nearly 0 V LOW on the A side which accommodates smaller voltage swings of lower voltage logic.

The static offset design of the B side PCA9517A I/O drivers prevents them from being connected to another device that has a rise time accelerator including the PCA9510, PCA9511, PCA9512, PCA9513, PCA9514, PCA9515A, PCA9516A, PCA9517A (port B), or PCA9518. The A side of two or more PCA9517As can be connected together, however, to allow a star topology with the A side on the common bus, and the A side can be connected directly to any other buffer with static or dynamic offset voltage. Multiple PCA9517As can be connected in series, A side to B side, with no build−up in offset voltage with only time−of−flight delays to consider.

The PCA9517A drivers are not enabled unless the bus is idle, $V_{CC(A)}$ is above 0.8 V and $V_{CC(B)}$ is above 2.5 V. The EN pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the enable pin when the bus is idle.

The output pull−down on the B side internal buffer LOW is set for approximately 0.5 V, while the input threshold of the internal buffer is set about 70 mV lower (0.43 V). When the B side I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock−up condition from occurring. The output pull−down on the A side drives a hard LOW and the input level is set at 0.3 $V_{CC(A)}$ to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.9 V.

BLOCK DIAGRAM

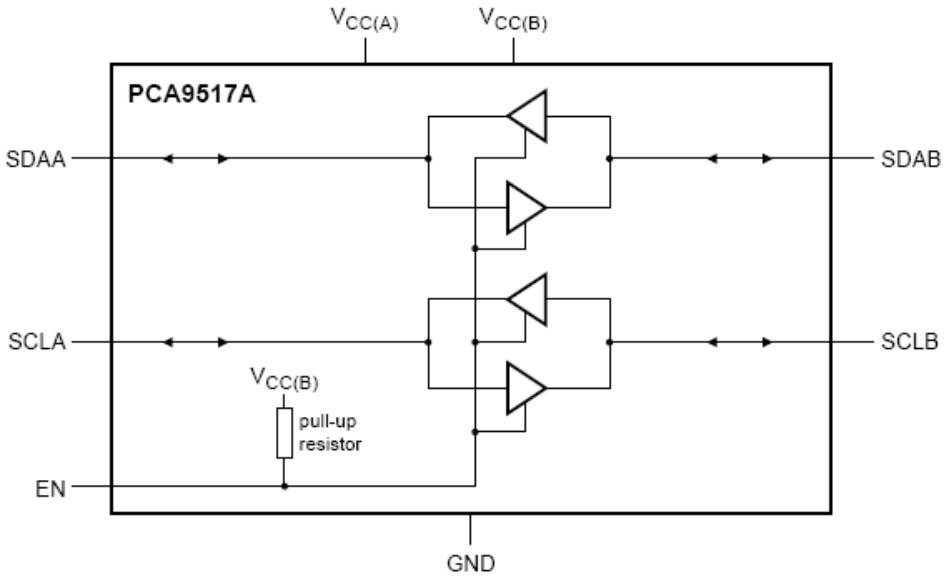


Figure 1. Block Diagram of PCA9517A

PIN ASSIGNMENT

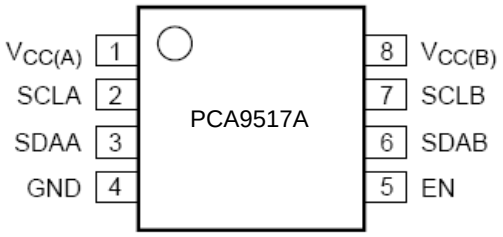


Figure 2. SOIC8 / Micro8

PIN DESCRIPTIONS

Symbol	Pin	Description
$V_{CC(A)}$	1	A−Side Supply Voltage (0.9 V to 5.5 V)
SCLA	2	Open−Drain I/O, Serial Clock A−Side Bus
SDAA	3	Open−Drain I/O, Serial Data A−Side Bus
GND	4	Ground
EN	5	Active−HIGH Repeater Enable
SDAB	6	Open−Drain I/O, Serial Data B−Side Bus
SCLB	7	Open−Drain I/O, Serial Clock B−Side Bus
$V_{CC(B)}$	8	B−Side Supply Voltage (2.7 V to 5.5 V)

FUNCTIONAL DESCRIPTION

Please refer to Figure 1 “Block Diagram of PCA9517A”.

The PCA9517A enables I^2C−bus or SMBus translation down to $V_{CC(A)}$ as low as 0.9 V without degradation of system performance. The PCA9517A contains two bidirectional open−drain buffers specifically designed to support up−translation/down−translation between the low voltage (as low as 0.9 V) and a 3.3 V or 5 V I^2C−bus or SMBus. All inputs and I/Os are overvoltage tolerant to 5.5 V even when the device is unpowered ($V_{CC(B)}$ and/or $V_{CC(A)}$ = 0 V). The PCA9517A includes a power−up circuit that keeps the output drivers turned off until $V_{CC(B)}$ is above 2.5 V and the $V_{CC(A)}$ is above 0.8 V. $V_{CC(B)}$ and $V_{CC(A)}$ can be applied in any sequence at power−up.

After power−up and with the enable (EN) HIGH, a LOW level on port A (below 0.3 $V_{CC(A)}$) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0.5 V. When port A rises above 0.3 $V_{CC(A)}$, the port B pull−down driver is turned off and the external pull−up resistor pulls the pin HIGH. When port B falls first and goes below 0.3$V_{CC(B)}$, the port A driver is turned on and port A pulls down to 0 V. The port B pull−down is not enabled unless the port B voltage goes below 0.4 V. If the port B low voltage does not go below 0.5 V, the port A driver will turn off when port B voltage is above 0.7 $V_{CC(B)}$. If the port B low voltage goes below 0.4 V, the port B pull−down driver is enabled and port B will only be able to rise to 0.5 V until port A rises above 0.3 $V_{CC(A)}$, then port B will continue to rise being pulled up by the external pull−up resistor. The $V_{CC(A)}$ is only used to provide the 0.3 $V_{CC(A)}$ reference to the port A input comparators and for the power good detect circuit. The PCA9517A logic and all I/Os are powered by the $V_{CC(B)}$ pin.

Enable Pin (EN)

The EN pin is active HIGH with an internal pull−up to $V_{CC(B)}$ and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power−up until after the system power−up reset. It should never change state during an I^2C−bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I^2C−bus parts being enabled.

The EN pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

I^2C−Bus Systems

As with the standard I^2C−bus system, pull−up resistors are required to provide the logic HIGH levels on the buffered bus (standard open−collector configuration of the I^2C−bus). The size of these pull−up resistors depends on the system, but each side of the repeater must have a pull−up resistor.

This part designed to work with Standard−mode, Fast−mode and Fast−mode+ I^{2}C−bus devices, in addition to SMBus devices. Standard−mode I^{2}C−bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I^{2}C−bus system where Standard−mode devices and multiple masters are possible. Under certain conditions, higher termination currents can be used.

APPLICATION DESIGN−IN INFORMATION

A typical application is shown in Figure 3. In this example, the system master is running on a 3.3 V I2C−bus while the slave is connected to a 1.2 Vbus. Both buses run at 400 kHz. Master devices can be placed on either bus.

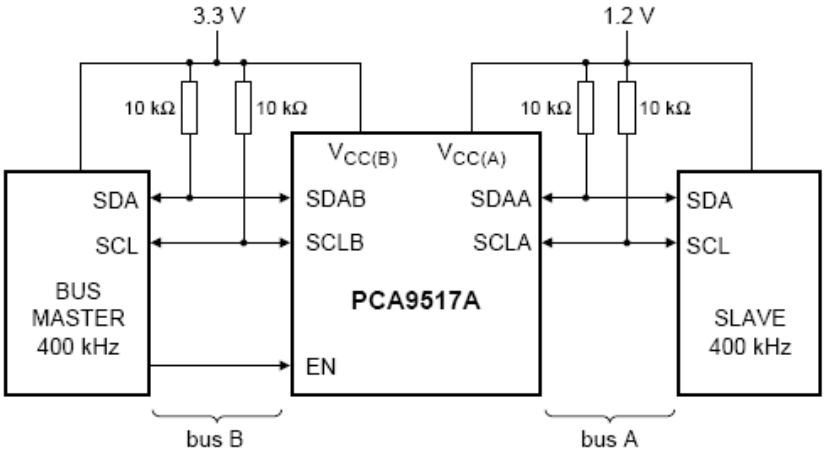


Figure 3. Typical Application

The PCA9517A is 5 V tolerant, so it does not require any additional circuitry to translate between 0.9 V to 5.5 V bus voltages and 2.7 V to 5.5 V bus voltages.

When the A side of the PCA9517A is pulled LOW by a driver on the I^{2}C−bus, a comparator detects the falling edge when it goes below 0.3 $V_{CC(A)}$ and causes the internal driver on the B side to turn on, causing the B side to pull down to about 0.5 V. When the B side of the PCA9517A falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on the A side to turn on and pull the A side pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figures 4 and 5. If the bus master in Figure 3 were to write to the slave through the PCA9517A, waveforms shown in Figure 4 would be observed on the A bus. This looks like a normal I^{2}C−bus transmission except that the HIGH level may be as low as 0.9 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

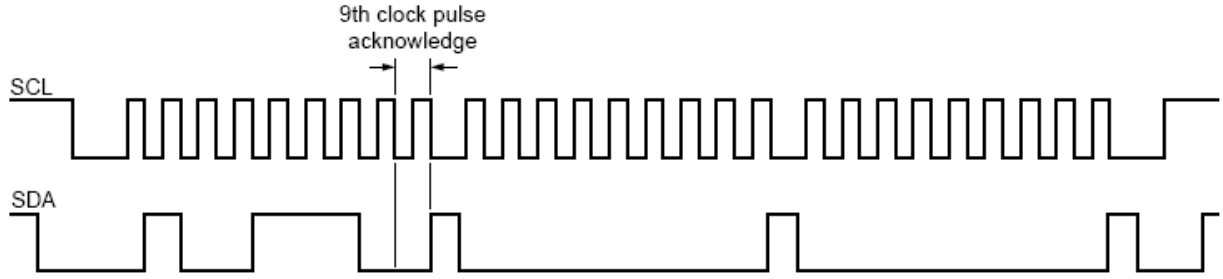


Figure 4. Bus A (0.9 V to 5.5 V Bus) Waveform

On the B bus side of the PCA9517A (Figure 5), the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9517A. After the 8th clock pulse, the data line will be pulled to the V_{OL} of the slave device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PCA9517A for a short delay while the A bus side rises above 0.3$V_{CC(A)}$, then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the PCA9517A (V_{IL}) be at or below 0.4 V to be recognized by the PCA9517A and then transmitted to the A bus side.

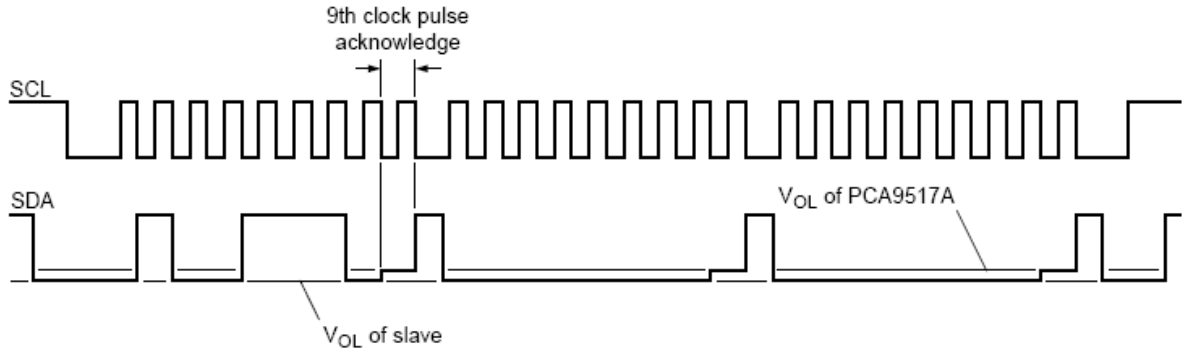


Figure 5. Bus B (2.7 V to 5.5 V Bus) Waveform

Multiple PCA9517A A sides can be connected in a star configuration (Figure 6), allowing all nodes to communicate with each other.

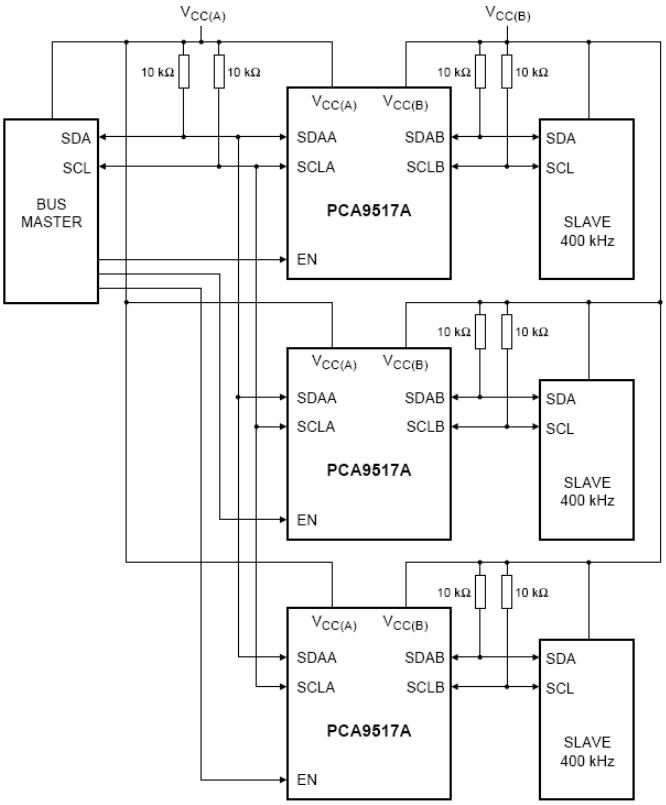


Figure 6. Typical Star Application

Multiple PCA9517As can be connected in series (Figure 7) as long as the A side is connected to the B side. I^{2}C−bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time−of−flight considerations on the maximum bus speed requirements.

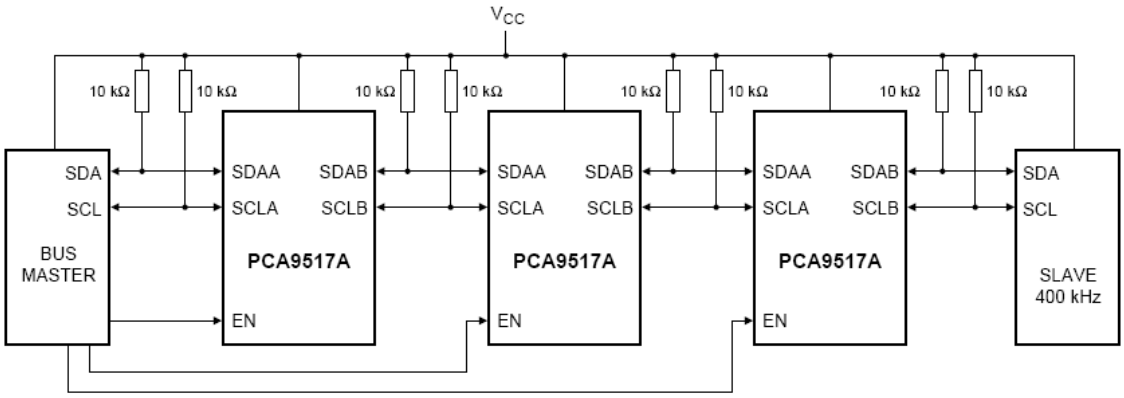


Figure 7. Typical Series Application

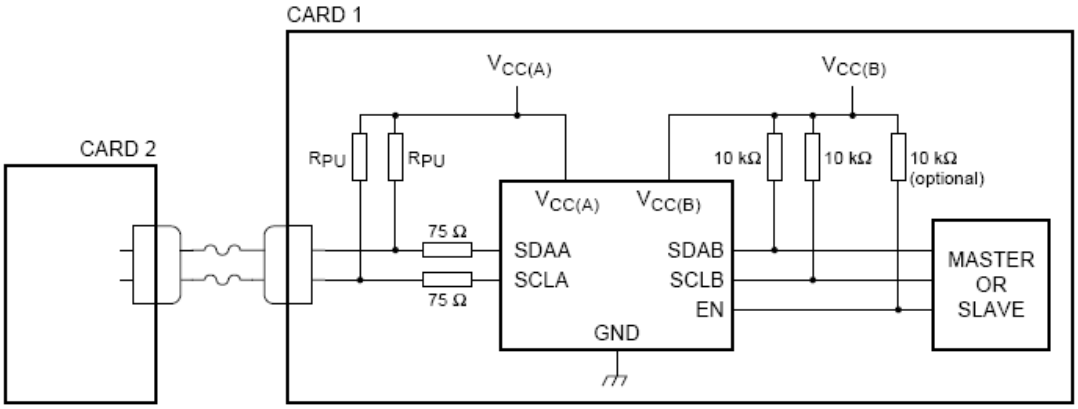


Figure 8. Typical Application of PCA9517A Driving a Short Cable

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
$V_{CC(B)}$	Supply Voltage Port B		−0.5 to +7.0	V
$V_{CC(A)}$	Supply Voltage Port A		−0.5 to +7.0	V
$V_{I/O}$	Input/Output Pin Voltage SDAB, SCLB, EN		−0.5 to +7.0	V
$I_{I/O}$	Input/Output Current SDAA, SDAB, SCLA, SCLB		±50	mA
I_I	Input Current EN		±50	mA
I_{CC}	DC Supply Current		±100	mA
I_{GND}	DC Ground Current		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		150	°C
θ_{JA}	Thermal Resistance	SOIC8 (Note 1) MIcro8	146 205	°C/W
P_D	Power Dissipation in Still Air at 85°C	SOIC8 MIcro8	856 609	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Mode (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 8000 > 700 >2000	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)		±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA / JESD22−A114−A.
3. Tested to EIA / JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC(B)}$	Supply Voltage Port B	2.7	5.5	V
$V_{CC(A)}$ (Note 6)	Supply Voltage Port A	0.9	5.5	V
$V_{I/O}$	Input/Output Pin Voltage	0	5.5	V
T_A	Operating Free−Air Temperature	−40	+85	°C

6. Low Level Supply Voltage.

DC CHARACTERISTICS $V_{CC(B)}$, $V_{CC(A)}$ = 2.7 V to 5.5 V, unless otherwise specified.

Symbol	Parameter	Conditions	T_A = −40°C to +85°C			Unit
			Min	Typ	Max	
SUPPLIES						
$I_{CC(A)}$	Supply Current Port A	Pin $V_{CC(A)}$			1	mA
I_{CCH}	HIGH−Level Supply Current	Both Channels HIGH; V_{CC} = 5.5 V; SDAn = SCLn = V_{CC}		1.5	5	mA
I_{CCL}	LOW−Level Supply Current	Both Channels LOW; V_{CC} = 5.5 V; One SDA and SCL = GND; Other SDA and SCL Open		1.5	5	mA
$I_{CC(A)c}$	Contention Port A Supply Current	V_{CC} = 5.5 V; SDAn = SCLn = V_{CC}		1.5	5	mA
INPUT / OUTPUT SDAB, SCLB						
V_{IH}	High−Level Input Voltage		0.7 x $V_{CC(B)}$			V
V_{IL} (Note 7)	Low−Level Input Voltage				0.3 x $V_{CC(B)}$	V
V_{ILc}	Contention Low−Level Input Voltage		−0.5	0.4		V
V_{IK}	Input Clamping Voltage	I_I = −18 mA			−1.2	V
V_{OL}	LOW−Level Output Voltage	I_{OL} = 100 μA or 6 mA	0.43	0.52	0.6	V
V_{OL} − V_{ILc} (Note 8)	Difference between LOW−Level Output Voltage and LOW−Level Input Voltage Contention			80		mV
I_{LI}	Input Leakage Current	V_I = 3.6 V			±1	μA
I_{IL}	LOW−Level Input Current	SDA, SCL, V_I = 0.2 V			10	μA
I_{LOH}	HIGH−Level Output Leakage Current	V_O = 3.6 V			10	μA
$C_{I/O}$	Input/Output Capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V		5	7	pF
		V_I = 3 V or 0 V; V_{CC} = 0 V		5	7	
INPUT / OUTPUT SDAA, SCLA						
V_{IH}	High−Level Input Voltage		0.7 x $V_{CC(A)}$			V
V_{IL} (Note 9)	Low−Level Input Voltage				0.3 x $V_{CC(A)}$	V
V_{IK}	Input Clamping Voltage	I_I = −18 mA			−1.2	V
V_{OL}	LOW−Level Output Voltage	I_{OL} = 6 mA		0.1	0.2	V
I_{LI}	Input Leakage Current	V_I = 3.6 V			±1	μA
I_{IL}	LOW−Level Input Current	SDA, SCL, V_I = 0.2 V			10	μA
I_{LOH}	HIGH−Level Output Leakage Current	V_O = 3.6 V			10	μA
$C_{I/O}$	Input/Output Capacitance	V_I = 3 V or 0 V; V_{CC} = 3.3 V		5	7	pF
		V_I = 3 V or 0 V; V_{CC} = 0 V		5	7	
INPUT EN						
V_{IH}	High−Level Input Voltage		0.7 x $V_{CC(B)}$			V

7. V_{IL} specification is for the first LOW level seen by the SDAB/SCLB lines. V_{ILc} is for the second and subsequent LOW levels seen by the SDAB/SCLB lines.
8. Guaranteed by design, not production tested.
9. V_{IL} for port A with envelope noise must be below 0.3 $V_{CC(A)}$ for stable performance.

DC CHARACTERISTICS $V_{CC(B)}$, $V_{CC(A)}$ = 2.7 V to 5.5 V, unless otherwise specified.

Symbol	Parameter	Conditions	T_A = −40°C to +85°C			Unit
			Min	Typ	Max	
INPUT EN						
V_{IL}	Low−Level Input Voltage				0.3 x $V_{CC(B)}$	V
I_{LI}	Input Leakage Current	$V_I = V_{CC}$			±1	μA
I_{IL}	LOW−Level Input Current	V_I = 0.2 V, EN; V_{CC} = 3.6 V		−10	−35	μA
C_I	Input Capacitance	V_I = 3 V or 0 V		6	7	pF

7. V_{IL} specification is for the first LOW level seen by the SDAB/SCLB lines. V_{ILc} is for the second and subsequent LOW levels seen by the SDAB/SCLB lines.
8. Guaranteed by design, not production tested.
9. V_{IL} for port A with envelope noise must be below 0.3 $V_{CC(A)}$ for stable performance.

AC CHARACTERISTICS V_{CC} = 2.7 V to 5.5 V, unless otherwise specified. (Notes 10 and 11)

Symbol	Parameter	Conditions	T_A = −40°C to +85°C			Unit
			Min	Typ (Note 12)	Max	
t_{PLH} (Note 13)	LOW−to−HIGH Propagation Delay	B−Side to A−Side; Figure 11	100	170	250	ns
t_{PHL} (Note 14)	HIGH−to−LOW Propagation Delay	B−Side to A−Side; Figure 9				ns
		$V_{CC(A)} \le 2.7$ V	10	80	110	
		$V_{CC(A)} \ge 3.0$ V	5	66	300	
t_{TLH} (Note 14)	LOW−to−HIGH Output Transition Time	A−Side; Figure 9	10	20	30	ns
		$V_{CC(A)} < 2.7$ V	5	20	30	
		$V_{CC(A)} > 3.0$ V	10	50	70	
t_{THL} (Note 14)	HIGH−to−LOW Output Transition Time	A−Side; Figure 9				ns
		$V_{CC(A)} \le 2.7$ V		77	105	
		$V_{CC(A)} > 3.0$ V		70	105	
t_{PLH} (Note 15)	LOW−to−HIGH Propagation Delay	A−Side to B−Side; Figure 10	25	53	150	ns
t_{PHL} (Note 15)	HIGH−to−LOW Propagation Delay	A−Side to B−Side; Figure 10	60	79	230	ns
t_{TLH}	LOW−to−HIGH Output Transition Time	B−Side; Figure 10	120	140	170	ns
t_{THL}	HIGH−to−LOW Output Transition Time	B−Side; Figure 10	1	48	90	ns
t_{su} (Note 16)	Setup Time	EN HIGH Before START Condition	100			ns
t_h (Note 16)	Hold Time	EN HIGH After STOP Condition	160			ns

10. Times are specified with loads indicated in Figure 12. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times.
11. Pull−up voltages are $V_{CC(A)}$ on the A side and $V_{CC(B)}$ on the B side.
12. Typical values were measured with $V_{CC(A)}$ = 3.3 V at T_{amb} = 25°C, unless otherwise noted.
13. The t_{PLH} delay data from B side to A side is measured at 0.5 V on the B side to 0.5 $V_{CC(A)}$ on the A side when $V_{CC(A)}$ is less than 2 V, and 1.5 V on the A side if $V_{CC(A)}$ is greater than 2 V.
14. Typical value measured with $V_{CC(A)}$ = 2.7 V at T_{amb} = 25°C.
15. The propagation delay data from A side to B side is measured at 0.3 $V_{CC(A)}$ on the A side to 1.5 V on the B side.
16. The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.

AC WAVEFORMS

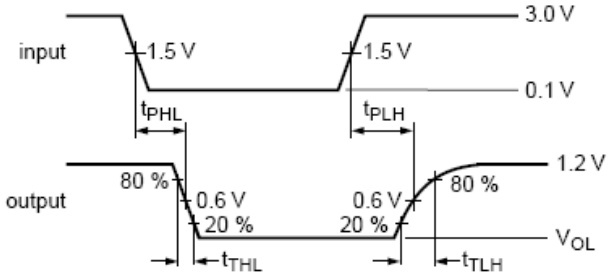


Figure 9. Propagation Delay and Transition Times; B−Side to A−Side

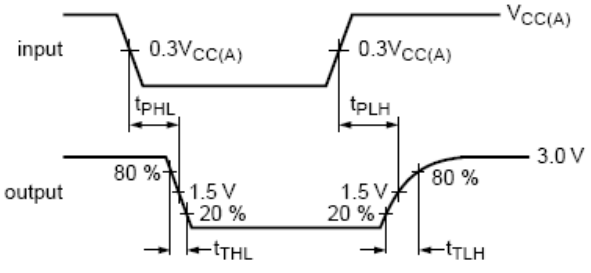


Figure 10. Propagation Delay and Transition Times; A−Side to B−Side

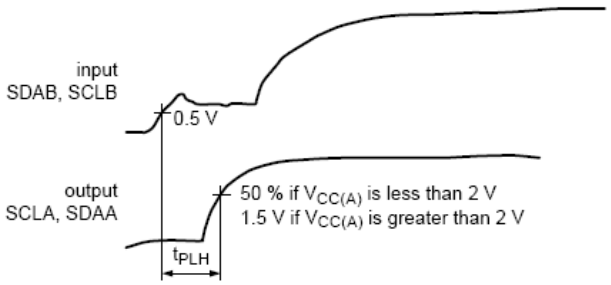
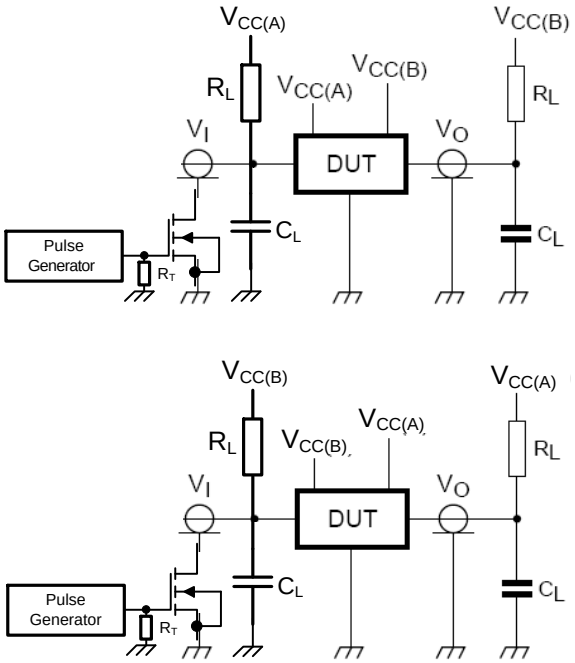


Figure 11. Propagation Delay; B−Side to A−Side

TEST SETUP



R_L = load resistor; 1.35 kΩ on port B; 167 Ω on port A (0.9 V to 2.7 V) and 450 Ω on port A (3.0 V to 5.5 V).

C_L = load capacitance includes jig and probe capacitance; 57 pF

R_T = termination resistance should be equal to Z_o of pulse generators

Figure 12. Test Circuit for Open−Drain Outputs

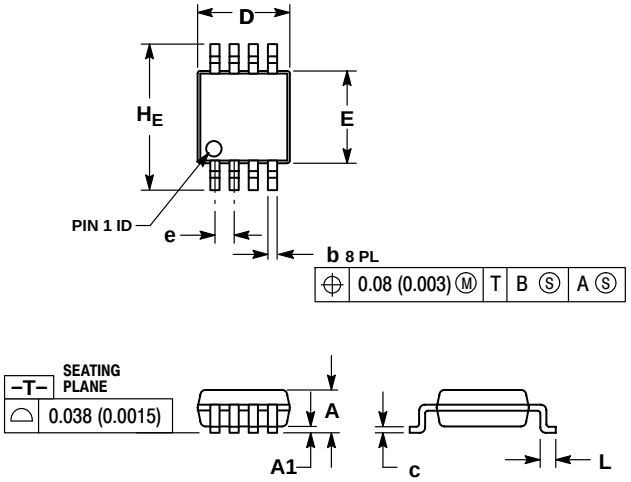
ORDERING INFORMATION

Device	Package	Shipping
PCA9517ADR2G In Development	SOIC8 (Pb−Free)	3000 / Tape & Reel
PCA9517ADMR2G	Micro−8 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

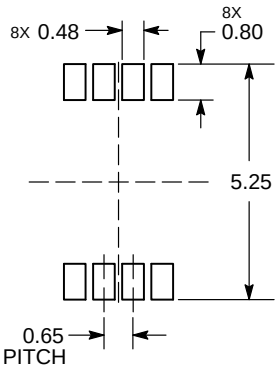
Micro8™
CASE 846A−02
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−	−−	1.10	−−	−−	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65 BSC			0.026 BSC	
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

RECOMMENDED SOLDERING FOOTPRINT*

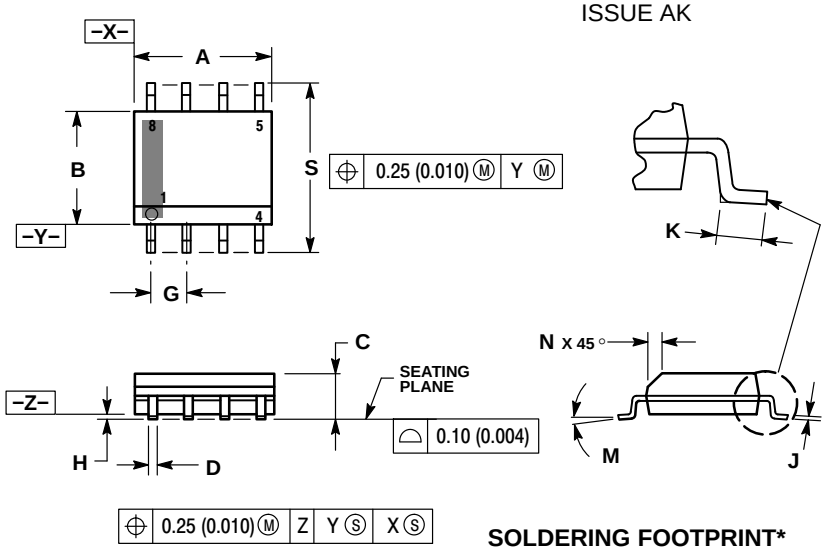


DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

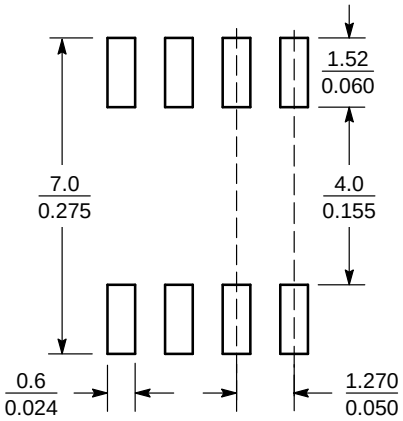
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
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- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

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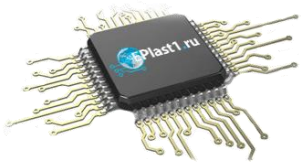
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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