User Guide for

FEBFAN9611_S388V1

FAN9611 400-W Interleaved Dual-BCM PFC Controller Evaluation Board

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Fairchild Semiconductor.com

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The following user guide supports the FAN9611 400-W evaluation board for interleaved boundary-conduction-mode power-factor-corrected supply. It should be used in conjunction with the FAN9611 datasheet as well as the Fairchild application note *AN-6086 Design Considerations for Interleaved Boundary-Conduction Mode PFC Using FAN9611 / FAN9612*. The evaluation board can be interchangeably used to evaluate either the FAN9611 (10 V turn-on threshold) or FAN9612 controller (12.5 V turn-on threshold). Please visit Fairchild's website at www.fairchildsemi.com for additional information. This Evaluation board can be identified by the top side silkscreen marking "FAN9612 400W INTERLEAVED PFC CONVERTER" and "FEB388".

1. Overview of the Evaluation Board

The FAN9611 interleaved dual Boundary-Conduction-Mode (BCM) Power-Factor-Correction (PFC) controllers operate two parallel-connected boost power trains 180º out of phase. Interleaving extends the maximum practical power level of the control technique from about 300 W to greater than 800 W. Unlike the continuous conduction mode (CCM) technique often used at higher power levels, BCM offers inherent zero-current switching of the boost diodes (no reverse-recovery losses), which permits the use of less expensive diodes without sacrificing efficiency. Furthermore, the input and output filters can be smaller due to ripple current cancellation between the power trains and doubling of effective switching frequency.

The advanced line feedforward with peak detection circuit minimizes the output voltage variation during line transients. To guarantee stable operation with less switching loss at light load, the maximum switching frequency is clamped at 525 kHz. Synchronization is maintained under all operating conditions.

Protection functions include output over-voltage, over-current, open-feedback, under-voltage lockout, brownout, and redundant latching over-voltage protection. The FAN9611 is available in a lead-free 16-lead SOIC package.

This FAN9611 evaluation board is a four-layer board designed for 400 W (400 V / 1 A) rated power. Thanks to the phase management, the efficiency is maintained above 96% at low-line and high-line, even down to 10% of the rated output power. Efficiency is 96.4% at line voltage 115 V_{AC} and 98.2% at 230 V_{AC} under full-load conditions.

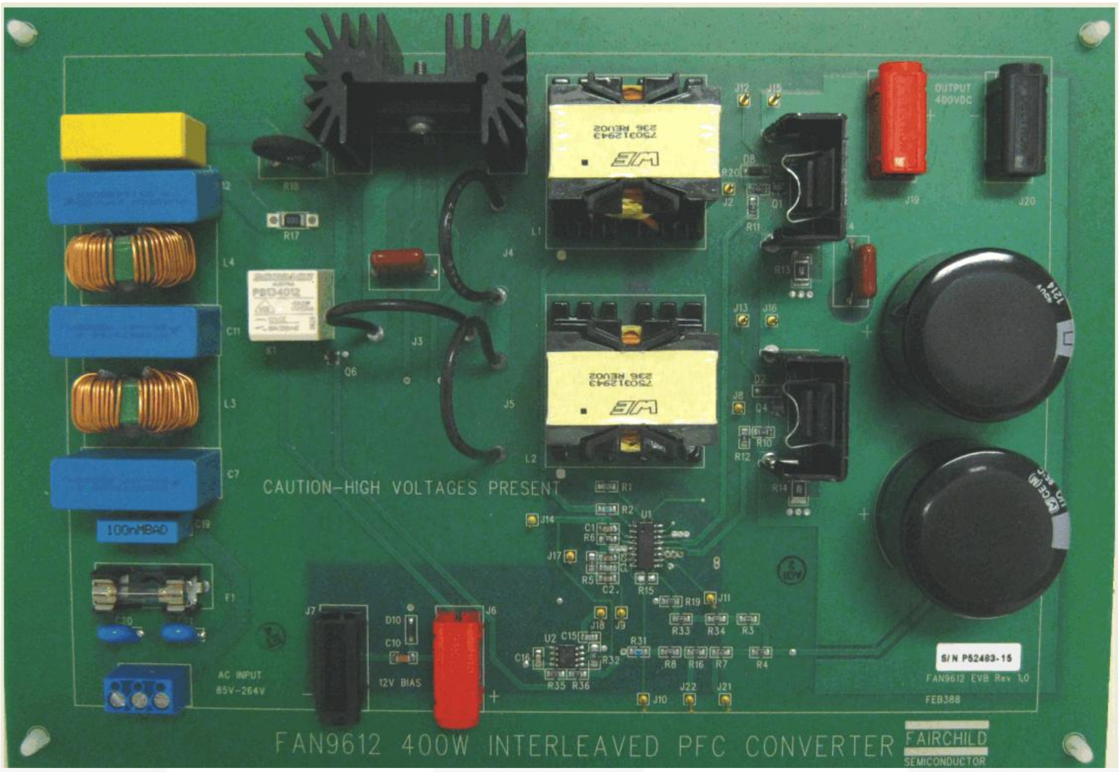


Figure 1. Top View

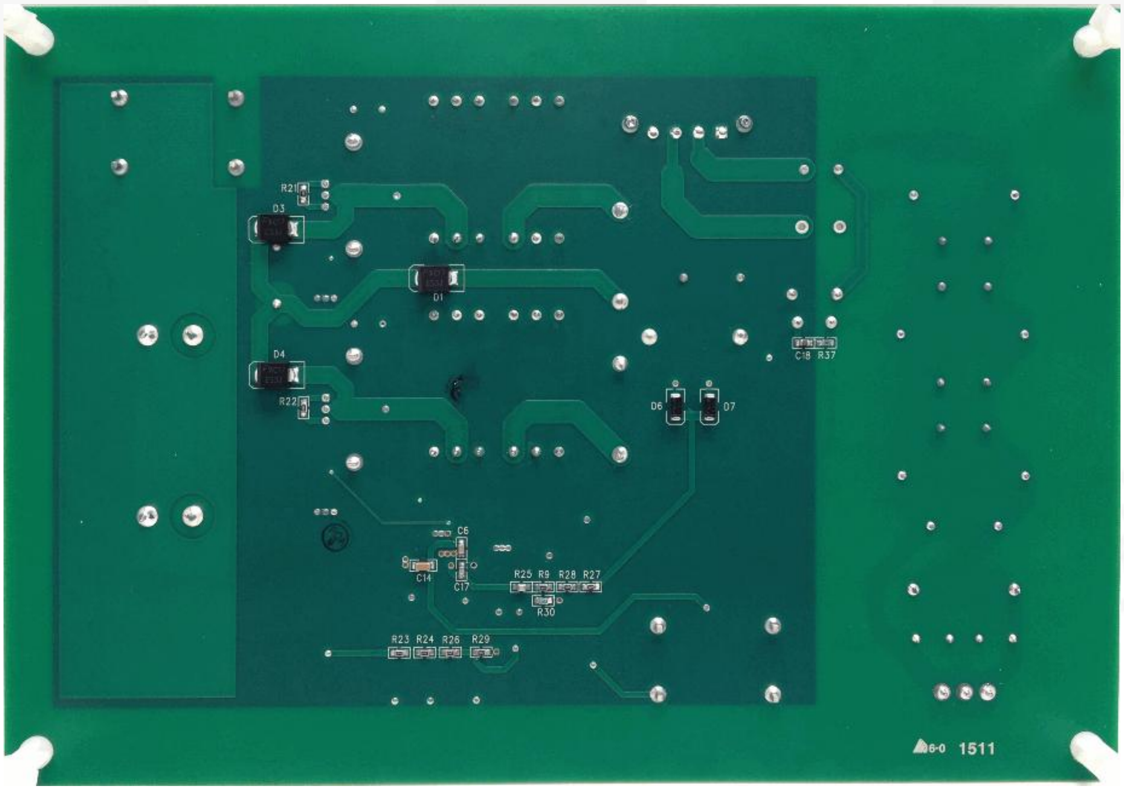


Figure 2. Bottom View

2. Key Features

- Low Total Harmonic Distortion, High Power Factor
- 180° Out-of-Phase Synchronization
- Automatic Phase Disable at Light Load
- 1.8-A Sink, 1.0-A Source, High-Current Gate Drivers
- Transconductance (g_M) Error Amplifier for Reduced Overshoot
- Voltage-Mode Control with $(V_{IN})^2$ Feed-forward
- Closed-Loop Soft-Start with Programmable Soft-Start Time for Reduced Overshoot
- Minimum Restart Timer Frequency to Avoid Audible Noise
- Maximum Switching Frequency Clamp
- Brownout Protection with Soft Recovery
- Non-Latching OVP on FB Pin and Second-Level Latching Protection on OVP Pin
- Open-Feedback Protection
- Over-Current and Power-Limit Protection for Each Phase
- Low Startup Current: 80 µA Typical
- Works with DC Input Voltage and 50-Hz to 400-Hz AC Inputs

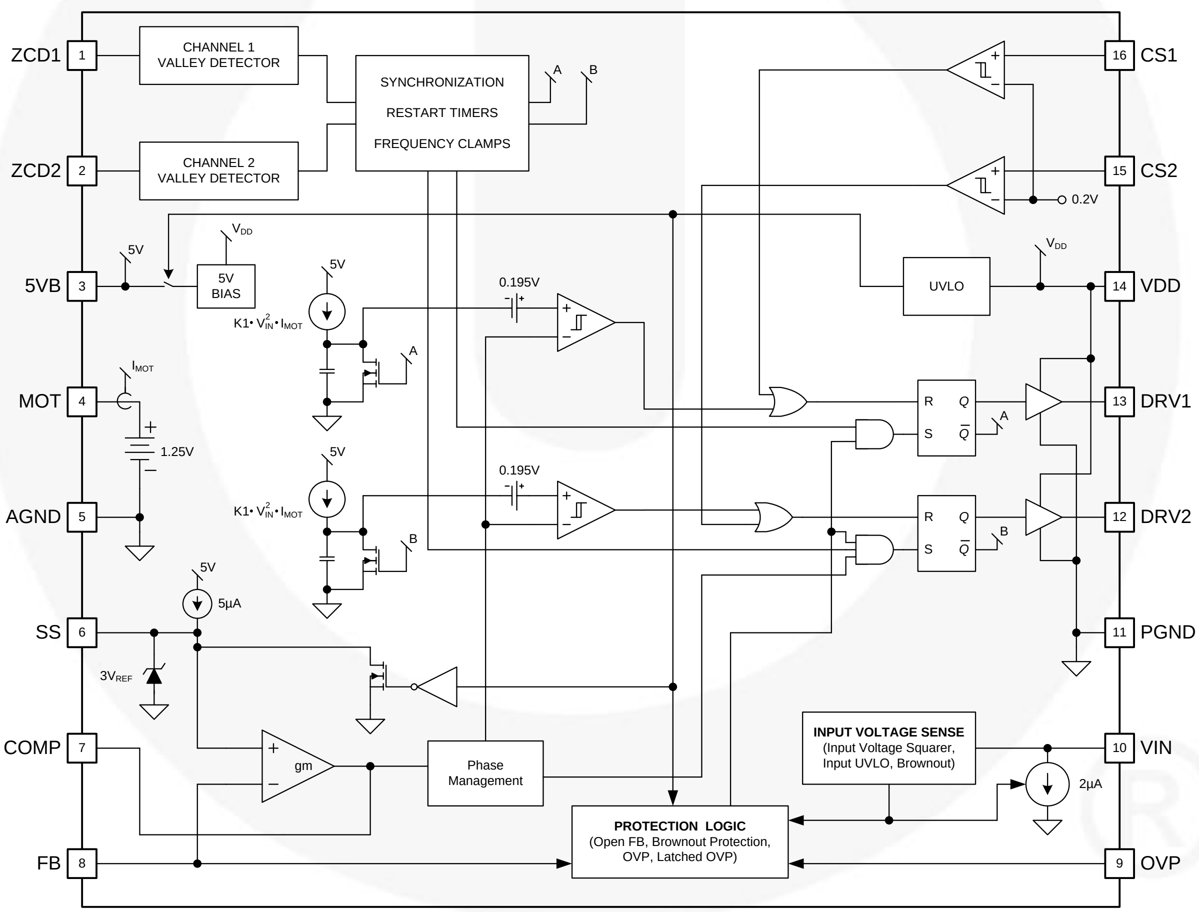


Figure 3. Block Diagram

3. Specifications

This board has been designed and optimized for the following conditions:

Input Voltage Range	Rated Output Power	Output Voltage (Rated Current)
V_{IN} Nominal : 85~264 V_{AC} V_{DD} Supply : 13 V_{DC}~18 V_{DC}	400 W	400 V - 1 A

Note:

1. Minimum output voltage during the 20 ms hold-up time is 330 V_{DC}.

- V_{LINE} = 85~264 V_{AC}
- V_{OUT} = 400 V
- f_{SW} > 50 kHz
- Efficiency > 96% down to 20% load (115 V_{AC})
- Efficiency > 97% down to 20% load (230 V_{AC})
- PF > 0.99 at full load

The trip points for the built-in protections are set as below in the evaluation board.

- The non-latching output OVP trip point is set at 108% of the nominal output voltage.
- The latching output OVP trip point is set at 117% of the nominal output voltage.
- The line UVLO (brownout protection) trip point is set at 68 V_{AC} (10 V_{AC} hysteresis).
- The pulse-by-pulse current limit for each MOSFET is set at 9.1 A.

The maximum power limit is set at ~120% of the rated output power. The phase management function permits phase shedding/adding ~15% of the nominal output power for high line (230 V_{AC}). This level can be programmed by modifying MOT resistor (R6).

4. Test Procedure

Before testing the board; DC voltage supply for V_{DD}, AC voltage supply for line input, and DC electric load for output should be connected to the board properly.

1. Supply V_{DD} for the control chip first. It should be higher than 13 V *(refer to the specification for V_{DD} turn-on threshold voltage in Table 1).*

Table 1. Specification Excerpt from FAN9611 Datasheet

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
$I_{STARTUP}$	Startup Supply Current	$V_{DD} = V_{ON} – 0.2$ V		80	110	µA
I_{DD}	Operating Current	Output Not Switching		3.7	5.2	mA
I_{DD_DYM}	Dynamic Operating Current	f_{SW} = 50 kHz; C_{LOAD} = 2 nF		4	6	mA
V_{ON}	UVLO Start Threshold	V_{DD} Increasing	9.5	10.0	10.5	V
V_{OFF}	UVLO Stop Threshold	V_{DD} Decreasing	7.0	7.5	8.0	V
V_{HYS}	UVLO Hysteresis	$V_{ON} – V_{OFF}$		2.5		V

2. Connect the AC voltage (85~265 V_{AC}) to start the FAN9611 / 12 evaluation board. Since FAN9611 / 12 has brownout protection, any input voltages lower than operation range triggers the protection.
3. Change load current (0~1 A) and check the operation.

5. Schematic

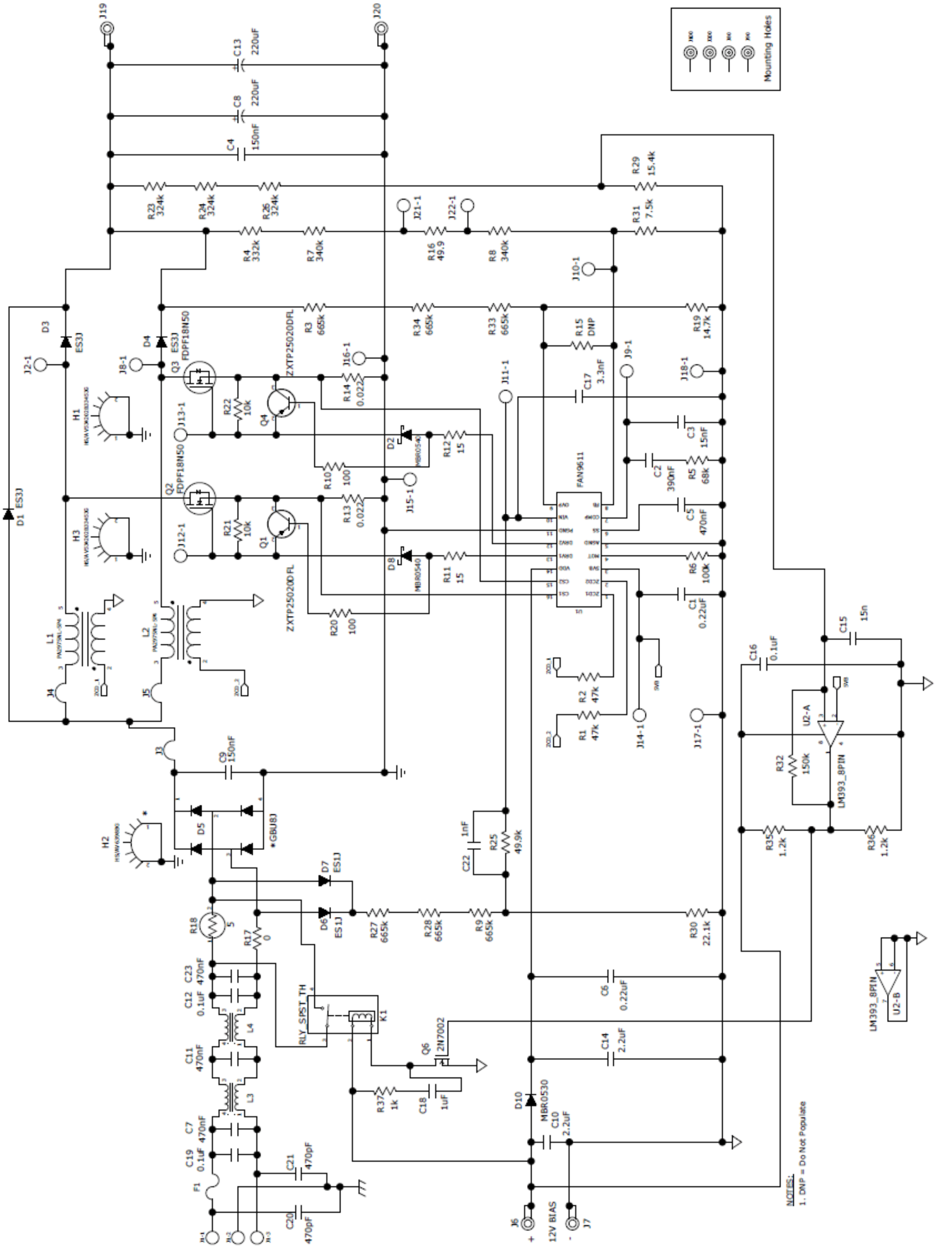


Figure 4. FAN9611 400-W Evaluation Board Schematic

6. Boost Inductor Specification

750312943 from Wurth Electronics Midcom (www.we-online.com/midcom)

OR

PA2975NL-5P4 from Pulse Electronics (www.pulseelectronics.com)

- Core: PQ3230 (Ae=161 mm^2)
- Bobbin: PQ3230
- Inductance : 200 μH

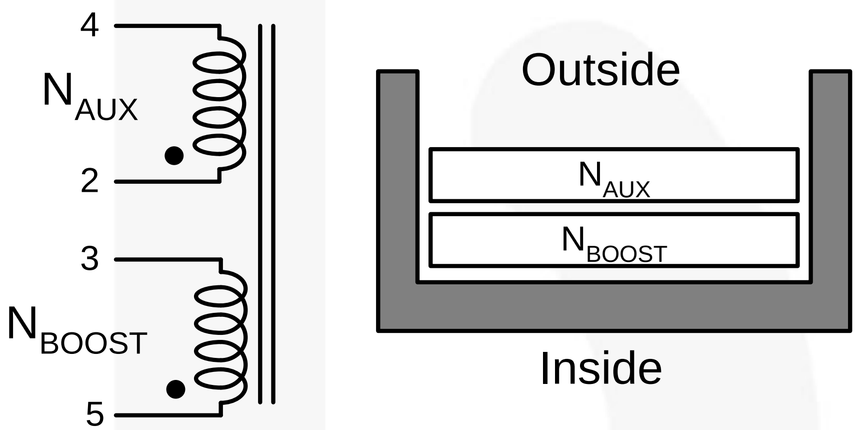
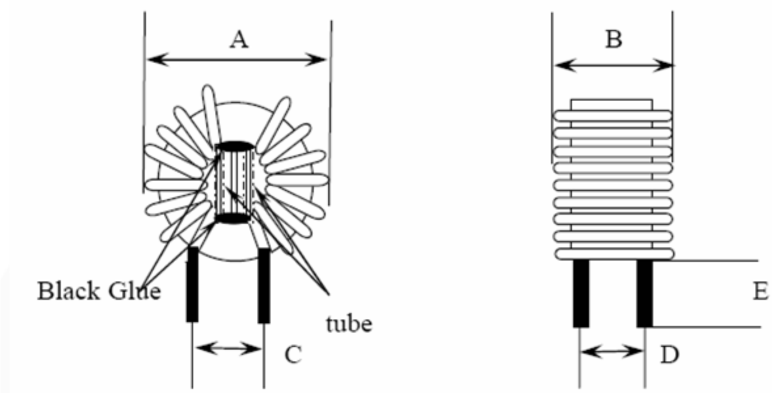


Figure 5. Boost Inductor used in this FAN9611 / 12 Evaluation Board

Table 2. Inductor Turns Specifications

	Pin	Turns
N1	5 → 3	30
Insulation Tape		
N2	2 → 4	3
Insulation Tape		

7. Line Filter Inductor Specifications



A : 30 mm (max.)
B: 15 mm (max.)
C: 11 mm
D: 13 mm
E: 15± mm

Electrical Specifications (1 kHz, 1 V)

- Inductance: 9.0 mH (min.) for each winding
- DC resistance: 0.05 Ω (max.) for each winding
- Number of turns: 0.9 mm×2/30.5 turns for each winding

Figure 6. Line Filter Inductor Specification

Table 3. Materials List

Component	Material	Manufacturer	UL File Number
Core	T22x14x08	Core T22x14x08, TOMITA	
Wire	THFN-216	Ta Ya Electric Wire Co,. Ltd.	E197768
	UEWN/U	PACIFIC Wire and cable Co., Ltd.	E201757
	UEWE	Tai-1 Electric Wire & Cable Co., Ltd.	E85640
	UWY	Jang Shing Wire Co., Ltd.	E174837
Solder	96.5%, Sn, 3%, Ag, 0.5% Cu	Xin Yuan Co., Ltd.	

8. PCB Layout

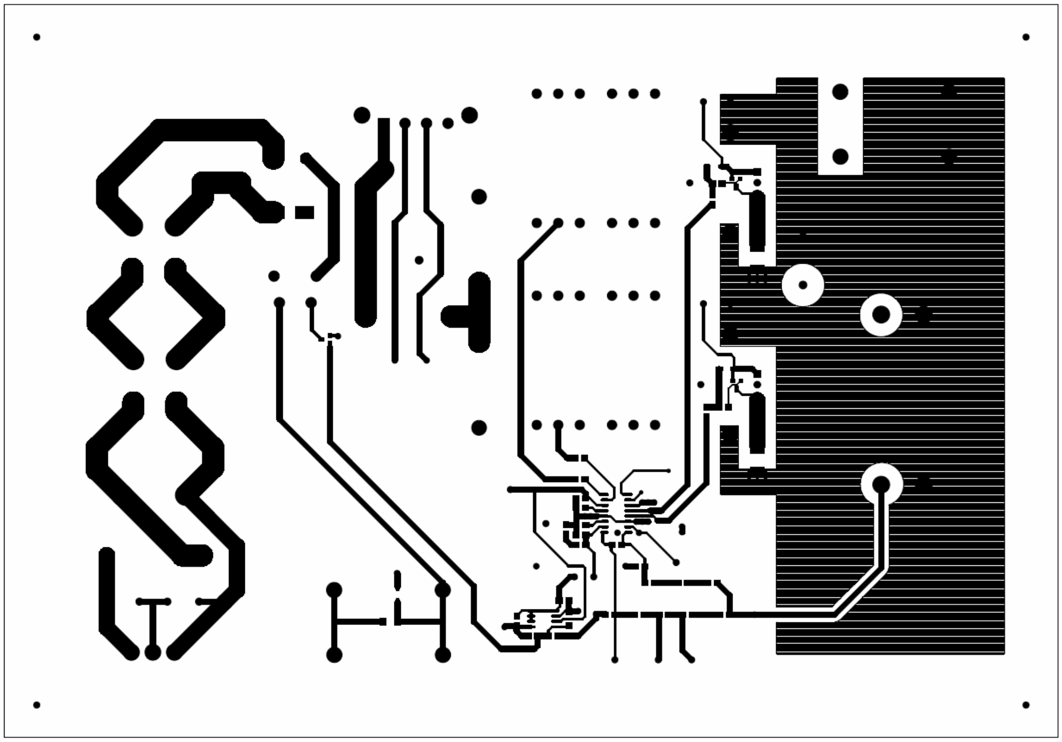


Figure 7. First Layer (Top Side)

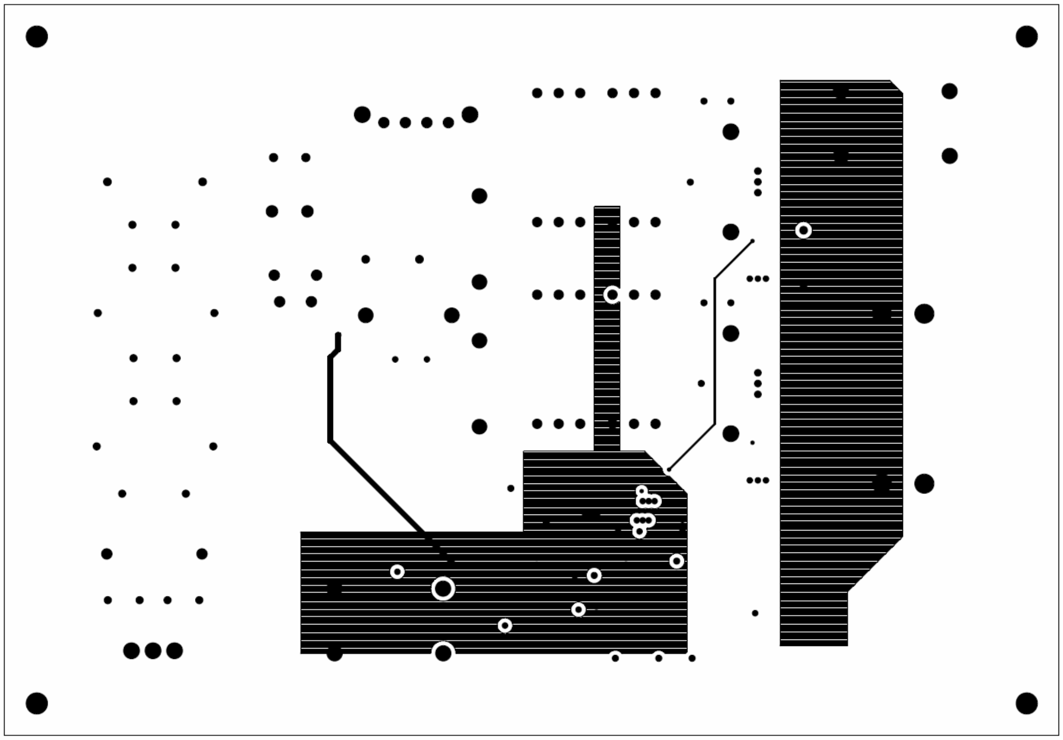


Figure 8. Second Layer (Plane Layer)

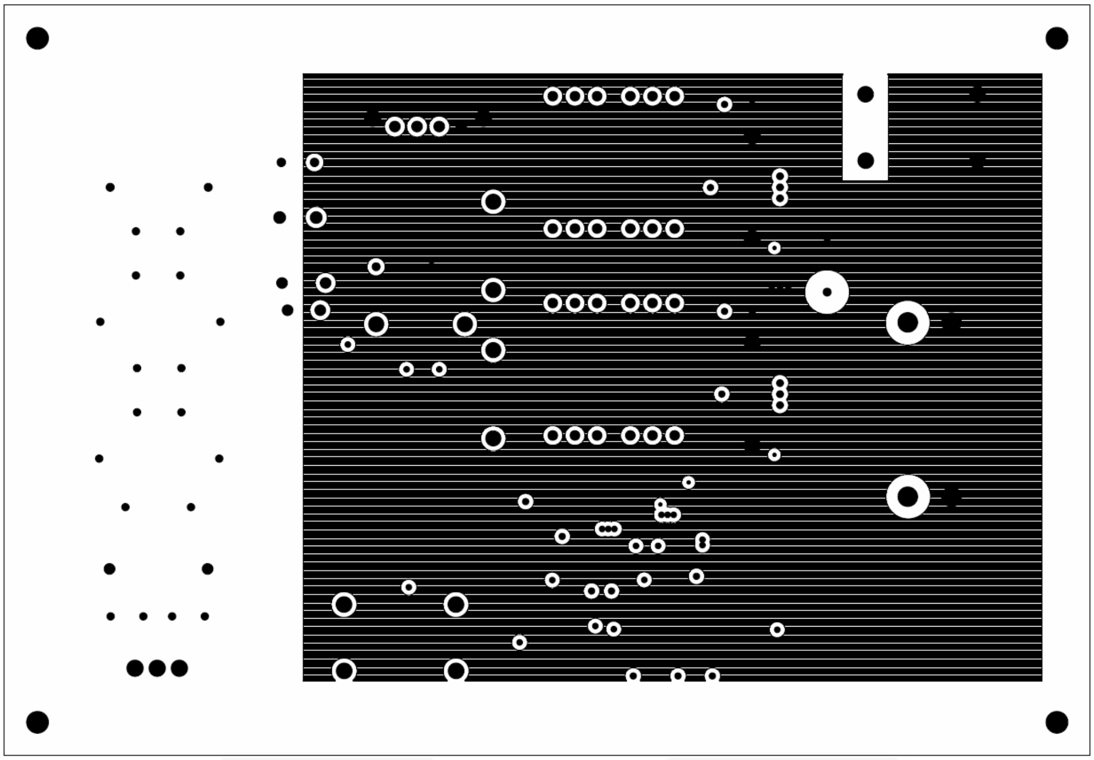


Figure 9. Third Layer (Ground Layer)

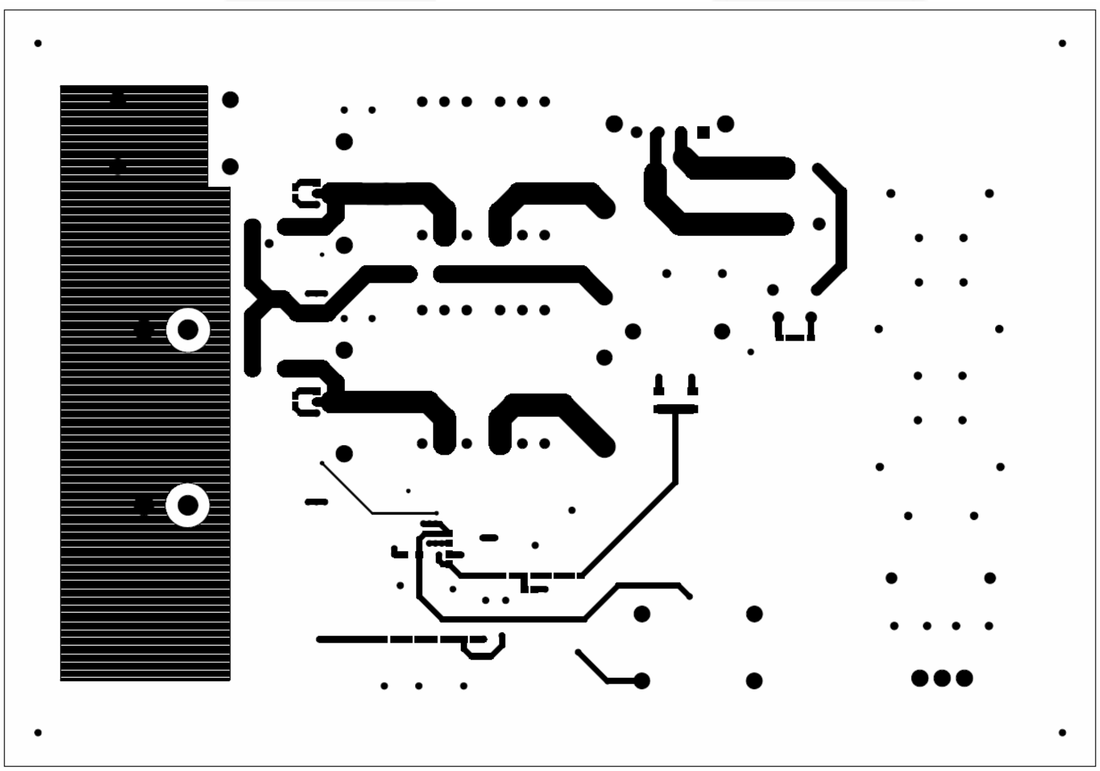


Figure 10. Fourth Layer (Bottom Side)

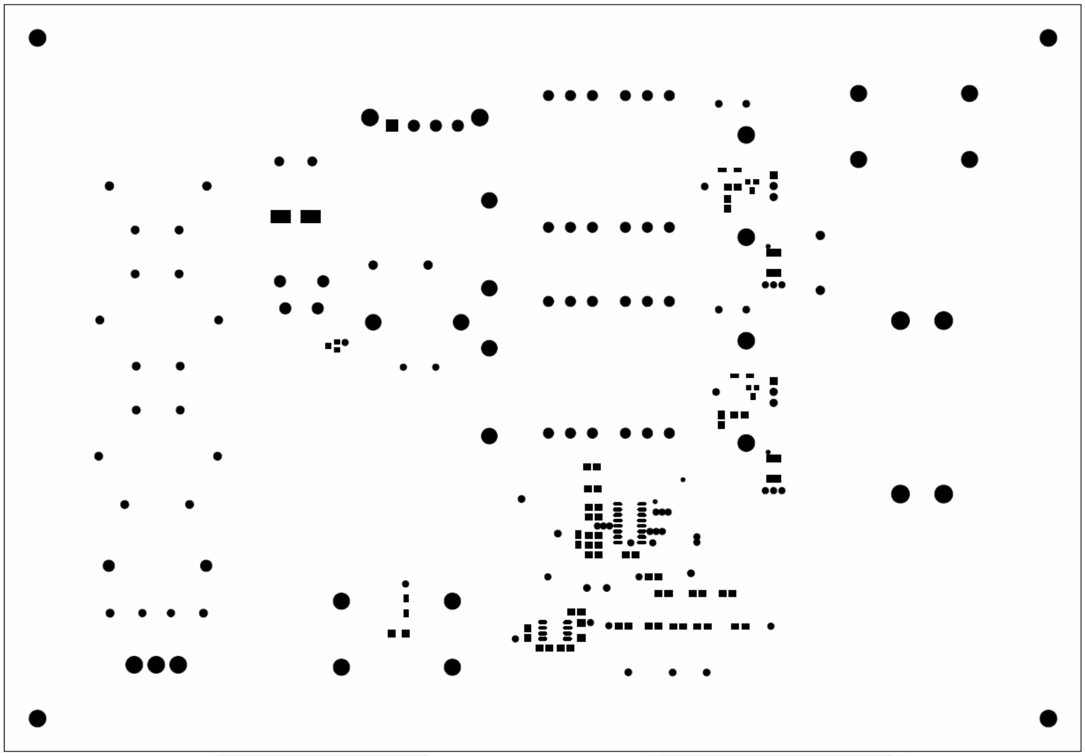


Figure 11. Top Solder Mask

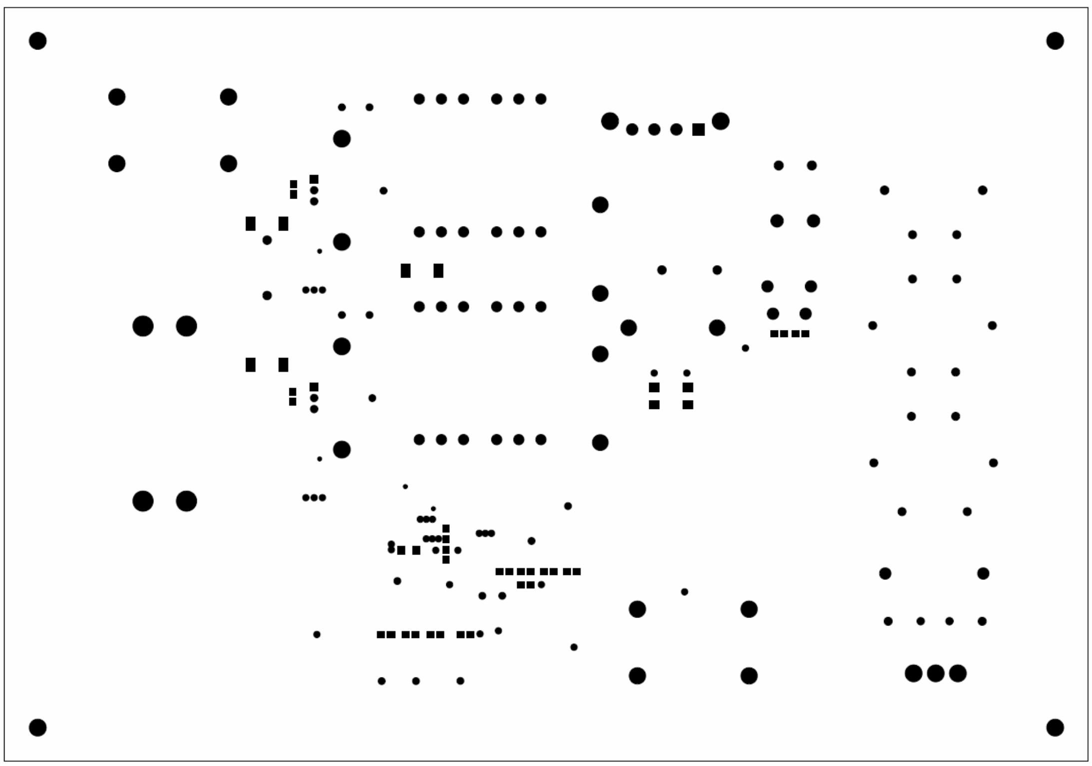


Figure 12. Bottom Solder Mask

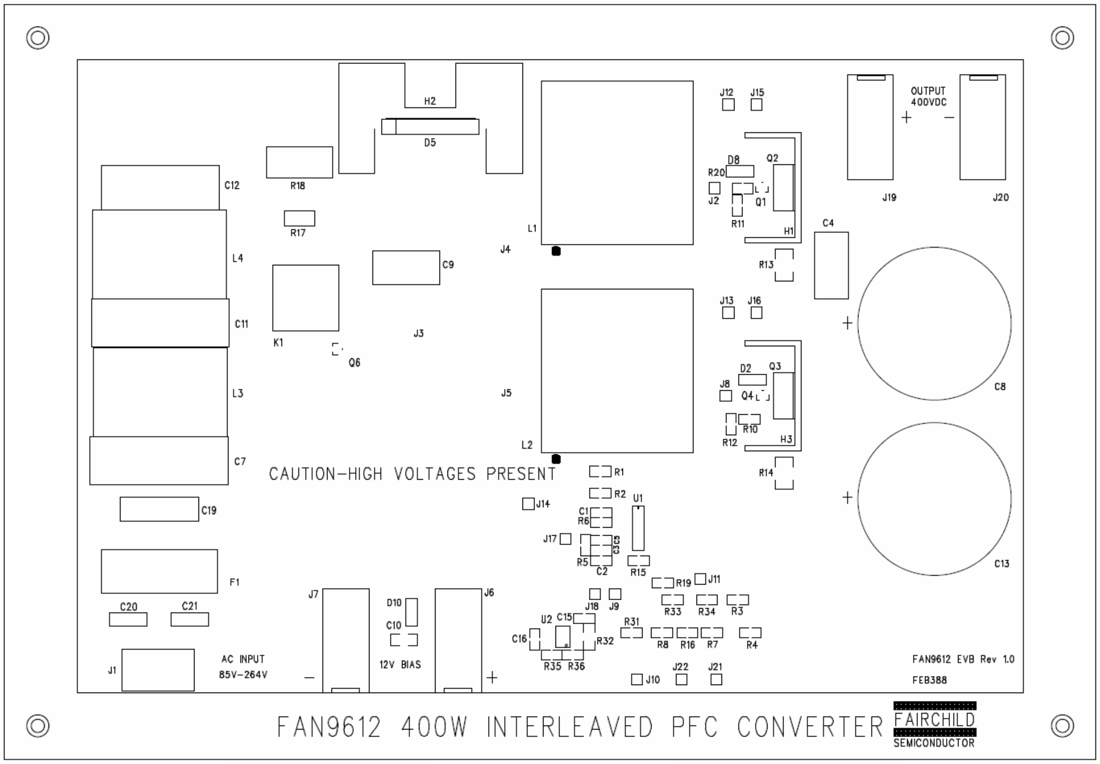


Figure 13. Top Silkscreen

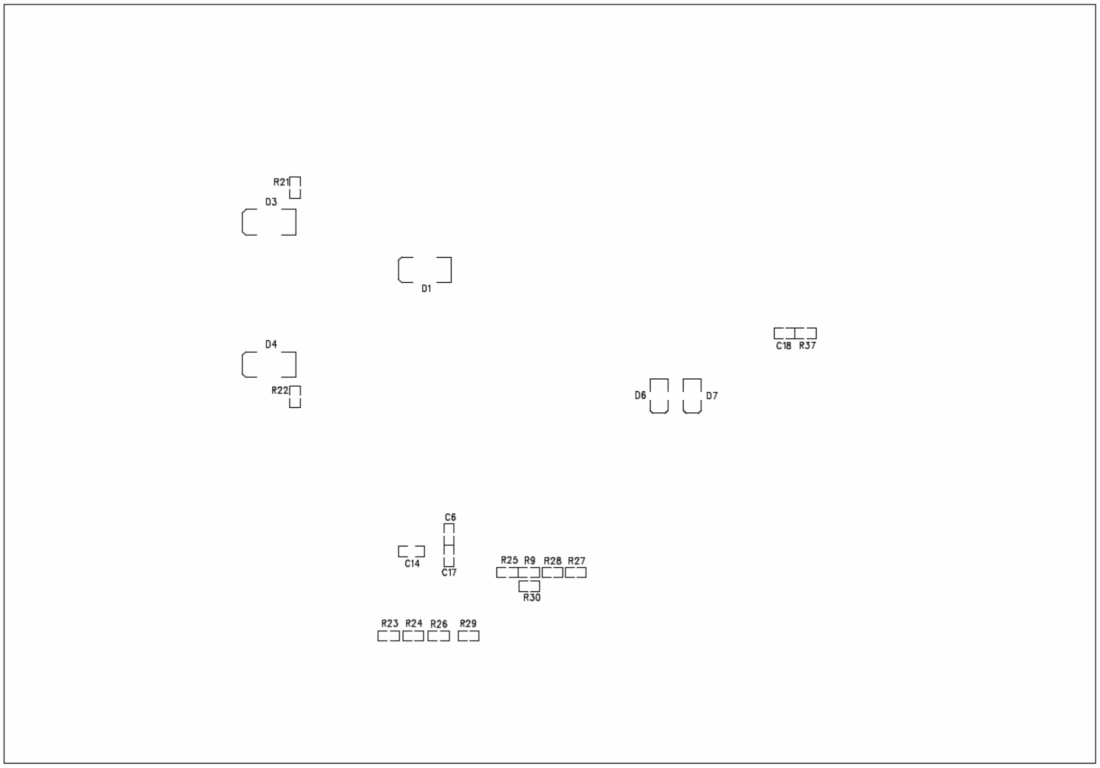


Figure 14. Bottom Silkscreen

9. Bill of Materials (BOM)

Qty.	Reference	Part Number	Value	Description	Package Type	Manufacturer
2	C1 C6		0.22 µF	CAP, SMD, CERAMIC, 25 V, X7R	805	STD
1	C2		390 nF	CAP, SMD, CERAMIC, 25 V, X7R	805	STD
2	C4 C9	ECWF2W154JAQ	150 nF	CAP, 400 V, 5%, POLYPROPYLENE	Radial, Thru-Hole	Panasonic-ECG
1	C5		470 nF	CAP, SMD, CERAMIC,25 V, X7R	805	STD
2	C7 C11 C23	B32914A3474	470 nF, 330 V	CAP, 330 V_{AC}, 10%, POLYPROPYLENE	Box, Thru-Hole	EPCOS
2	C8 C13	EETUQ2W221E	220 µF	CAP, ALUM, ELECT.	Radial, Thru-Hole	Panasonic
2	C10 C14		2.2 µF	CAP, SMD, CERAMIC, 25 V, X7R	1206	STD
1	C12	HQX104K275R2	0.1 µF, 275 V	CAP, X SERIES, 250 V_{AC}, 5%, POLYPROPYLENE	Box, Thru-Hole	Fuhjyyu Electronic Industrial Co.
1	C15		15 nF	CAP, SMD, CERAMIC,25 V, X7R	805	STD
1	C16		0.1 µF	CAP, SMD, CERAMIC, 25 V, X7R	805	STD
1	C18		1 µF	CAP, SMD, CERAMIC,50 V, X5R	805	STD
1	C19	PHE840MB 6100MB05R17	0.1 µF	CAP, X TYPE, 275 V_{AC}, 10%, POLYPROPYLENE	Box, Axial	KEMET
2	C20-21	CS85-B2GA471KYNS	470 pF	CAP, CERAMIC, 250 V_{AC}, 10%, Y5P,	Disc, Thru-hole	TDK Corporation
1	C22		1 nF	CAP, SMD, CERAMIC, 25 V, X7R	805	STD
3	D1 D3-4	S3J		Diode, 600 V, 3 A, Std recovery	SMC	Fairchild Semiconductor
2	D2 D8	MBR0540		Diode, Schottky,40 V, 500 mA	SOD-123	Fairchild Semiconductor
1	D5	GBU8J		Bridge Rectifier, 600 V, 8 A	Thru-Hole	Fairchild Semiconductor
2	D6-7	ES1J		DIODE FAST REC 1 A 600 V	SMA	Fairchild Semiconductor
1	D10	MBR0530		DIODE SCHOTTKY 30 V 500 mA SOD-123	SOD-123	Fairchild Semiconductor
1	F1	31.8201		Fuseholder, 5x20 mm, 250 V_{AC}, 10 A	PCB mount, Thru-hole	Schurter Inc
2	H1 H3	534202B33453G		Heatsink, 13.4°C/W, TO-220 with Tab-Koolclip for Q2-3	1"x0.475"x1.18"	Aavid Thermalloy
1	H2	639BG		TO-220 Heat sink for D5, Bridge Rectifier	1.65"x1.5"	Aavid Thermalloy
1	J1	ED100/3DS		Terminal Block, 5 mm Vert., 3 Pos.	Thru-hole	On Shore Technology, Inc.
14	J2 J8-18 J21-22	3103-1-00-15-00-00-08-0		Probe-pin, Gold, 0.3" x 40mil dia., 31mil mounting length	Thru-Hole	Mill-Max
3	J3-5			Jumper wire, #16, Insulated, for current probe measurement	Thru-Hole	Custom
2	J6 J19	571-0500		Banana Jack, .175, Horizontal, Insulated_RED	Thru-Hole	Deltron
2	J7 J20	571-0100		Banana Jack, .175, Horizontal, Insulated_BLK	Thru-Hole	Deltron
2	L1-2	750312943 PA2975NL-5P4	200 µH	Coupled Inductor, PQ3230, Pri-30T, Sec-3T	Thru-Hole	Wurth Midcom Pulse Electronics
2	L3-4	TRN-0197		Common Mode Choke	Thru-Hole	SEN HUEI INDUSTRIAL CO.,LTD
2	Q1 Q4	ZXTP25020DFL		Transistor, PNP, 20 V, 1.5 A	SOT-23	Zetex
2	Q2-3	FDPF18N50		MOSFET, NCH, 500 V, 18 A, 0.265 Ω	TO-220	Fairchild Semiconductor

BOM (Continued)

Qty.	Reference	Part Number	Value	Description	Package Type	Manufacturer
2	R1-2		47 kΩ	RES, SMD, 1/8 W	805	STD
6	R3 R9 R27-28 R33-34		665 kΩ	RES, SMD, 1/8 W	805	STD
1	R4		332 kΩ	RES, SMD, 1/8 W	805	STD
1	R5		68 kΩ	RES, SMD, 1/8 W	805	STD
1	R6		100 kΩ	RES, SMD, 1/8 W	805	STD
2	R7-8		340 kΩ	RES, SMD, 1/8 W	805	STD
2	R10 R20		100 Ω	RES, SMD, 1/8 W	805	STD
2	R11-12		15 Ω	RES, SMD, 1/8 W	805	STD
1	R15		DNP	RES, SMD, 1/8 W	805	STD
1	R16		49.9 Ω	RES, SMD, 1/8 W	805	STD
1	R17		0	RES, SMD, 1/2 W	2010	STD
1	R18	B57237S0509M000	5 Ω	Thermistor, 5 Ω	Thru-Hole	EPCOS
1	R19		14.7 kΩ	RES, SMD, 1/8 W	805	STD
4	1 inserted into each corner of PCB	LCBS-12-01		LOCKING BOARD SUPPORT 3/4", 1 for each PCB corner	Standoff	Richco Plastic Company
1	1 at D5, H2	3103		Nylon Shoulder Washer #4x0.187", Black	Washer	Keystone Electronics
1	1 at D5, H2	MLWZ 003		Split Lock Washer, Metric M 3 Zinc	Washer	B&F Fastener
1	1 at D5, H2	HNZ440		Nut Hex, #4-40 Zinc	Nut	B&F Fastener
1	1 at D5, H2	PMS 440 0050 PH		Screw Machine Phillips, 4-40x1/2" Zinc	Screw	B&F Fastener
1	PWB	FAN9611/12 FEB388 Rev. 0.0.1	FEB388	PWB, 9.8" x 6.8"	PWB	Fairchild Semiconductor
2	R1-2		47 kΩ	RES, SMD, 1/8 W	805	STD
6	R3 R9 R27-28 R33-34		665 kΩ	RES, SMD, 1/8 W	805	STD
1	R4		332 kΩ	RES, SMD, 1/8 W	805	STD
1	R5		68 kΩ	RES, SMD, 1/8 W	805	STD
1	R6		100 kΩ	RES, SMD, 1/8 W	805	STD
2	R7-8		340 kΩ	RES, SMD, 1/8 W	805	STD
2	R10 R20		100 Ω	RES, SMD, 1/8 W	805	STD
2	R11-12		15 Ω	RES, SMD, 1/8 W	805	STD
2	R13-14		0.022 Ω	RES, SMD, 1/2 W	1812	STD
1	R15		DNP	RES, SMD, 1/8 W	805	STD
1	R16		49.9 Ω	RES, SMD, 1/8 W	805	STD
1	U1	FAN9611		Interleaved Dual-BCM PFC Controller	SOIC-16	Fairchild Semiconductor

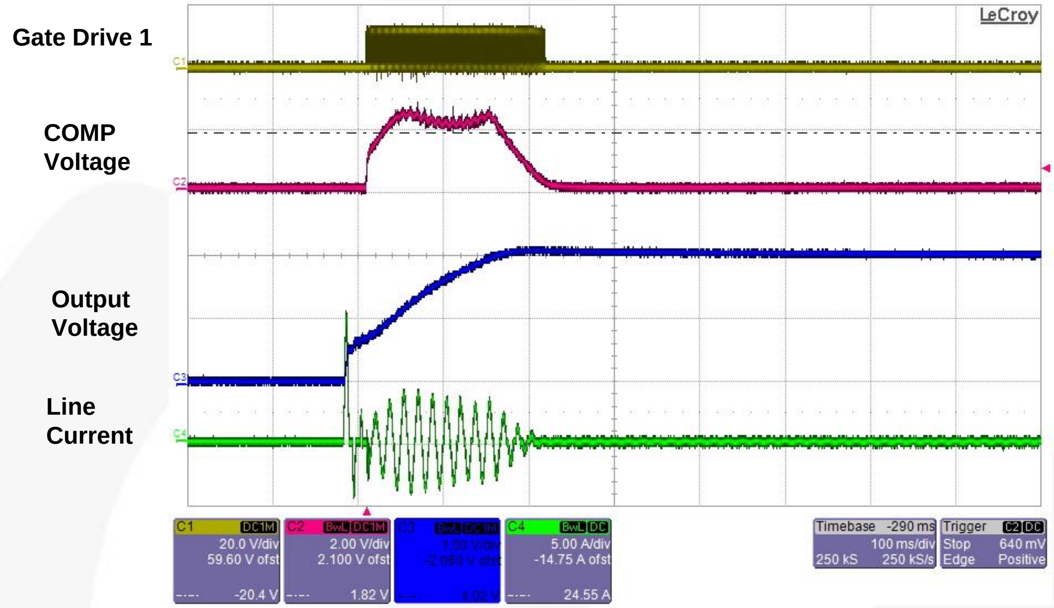
Note:

2. DNP = Do not populate. STD = standard components.

10. Test Results

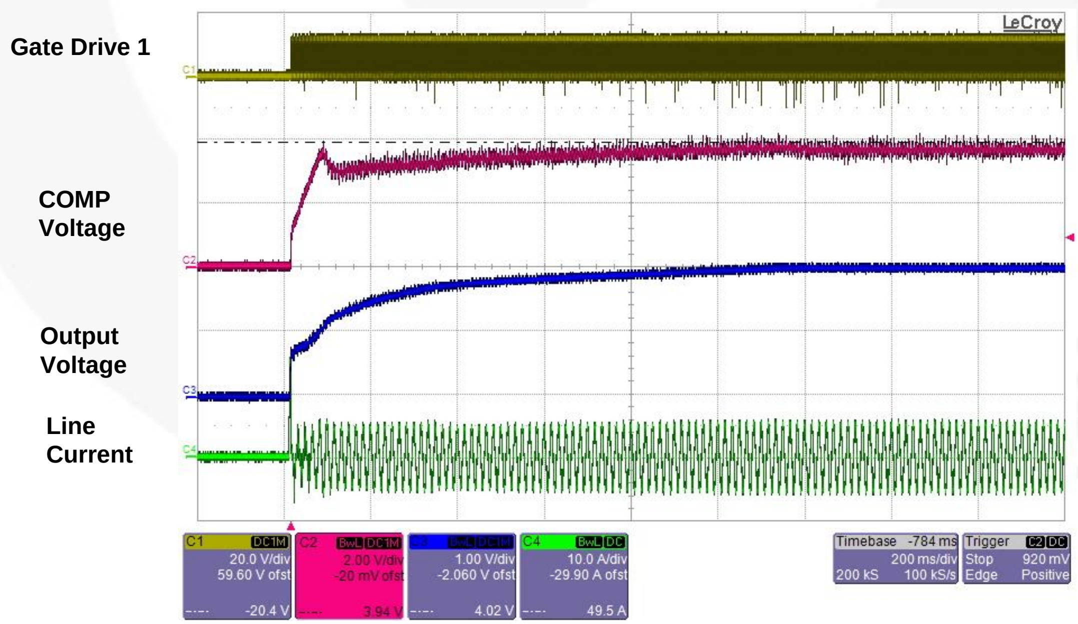
10.1. Startup

Figure 15 and Figure 16 show the startup operation at 115 V_{AC} line voltage for no-load and full-load condition, respectively. Due to the closed-loop soft-start, almost no overshoot is observed for no-load startup and full-load startup.



CH1: Gate Drive 1 Voltage (20 V / div), CH2: COMP Voltage (2 V / div),
CH3: Output Voltage (200 V / div), CH4: Line Current (5 A / div), Time (100 ms / div)

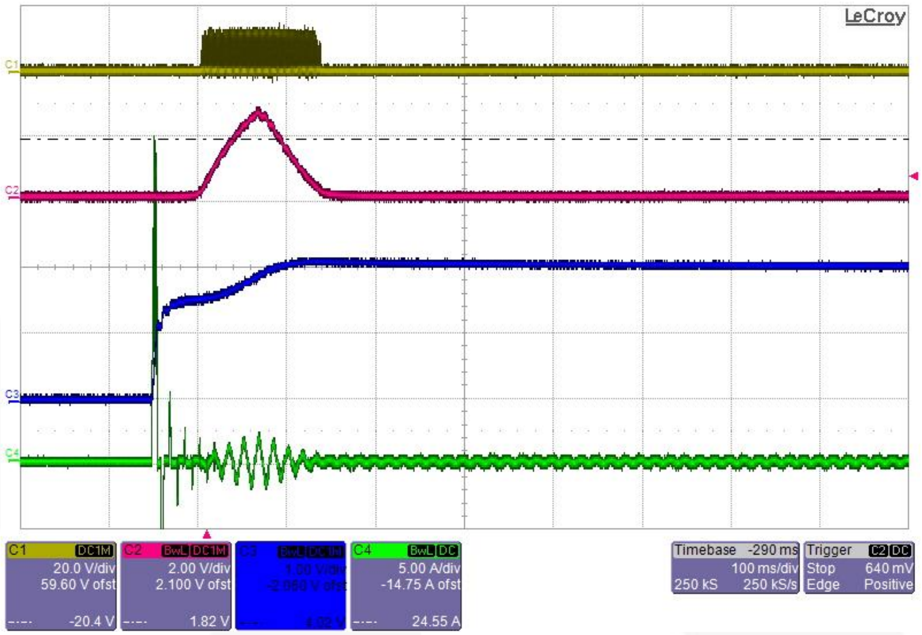
Figure 15. No-Load Startup at 115 V_{AC}



CH1: Gate Drive 1 Voltage (20 V / div), CH2: COMP Voltage (2 V / div),
CH3: Output Voltage (200 V / div), CH4: Line Current (10 A / div), Time (200 ms / div)

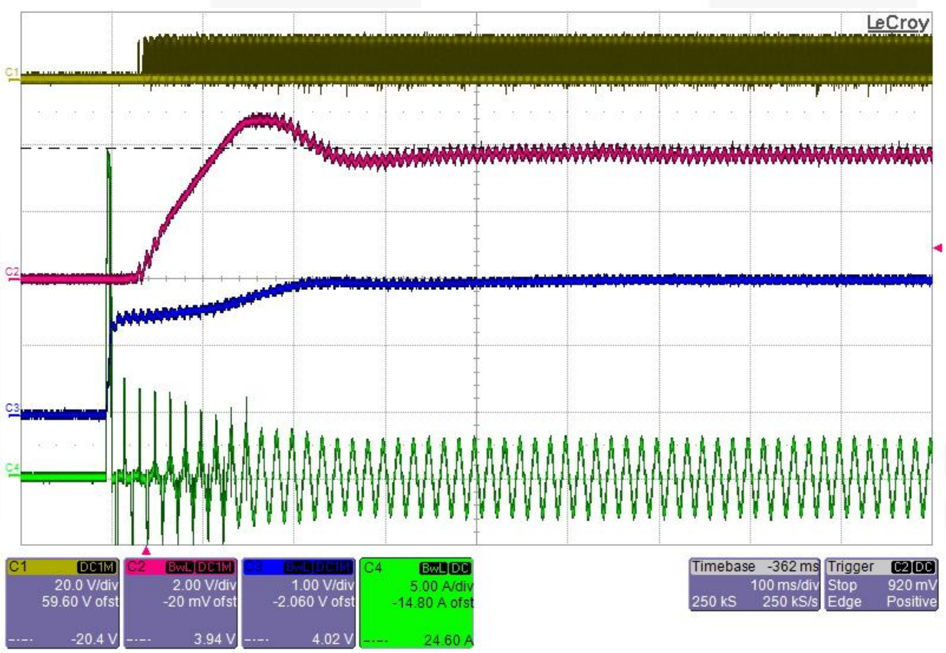
Figure 16. Full-Load Startup at 115 V_{AC}

Figure 17 and Figure 18 show the startup operation at 230 V_{AC} line voltage for no-load and full-load conditions, respectively. Due to the closed-loop soft-start, almost no overshoot is observed for no-load startup and full-load startup.



CH1: Gate Drive 1 Voltage (20 V / div), CH2: COMP Voltage (2 V / div),
CH3: Output Voltage (200 V / div), CH4: Line Current (5 A / div), Time (100 ms / div)

Figure 17. No-Load Startup at 230 V_{AC}

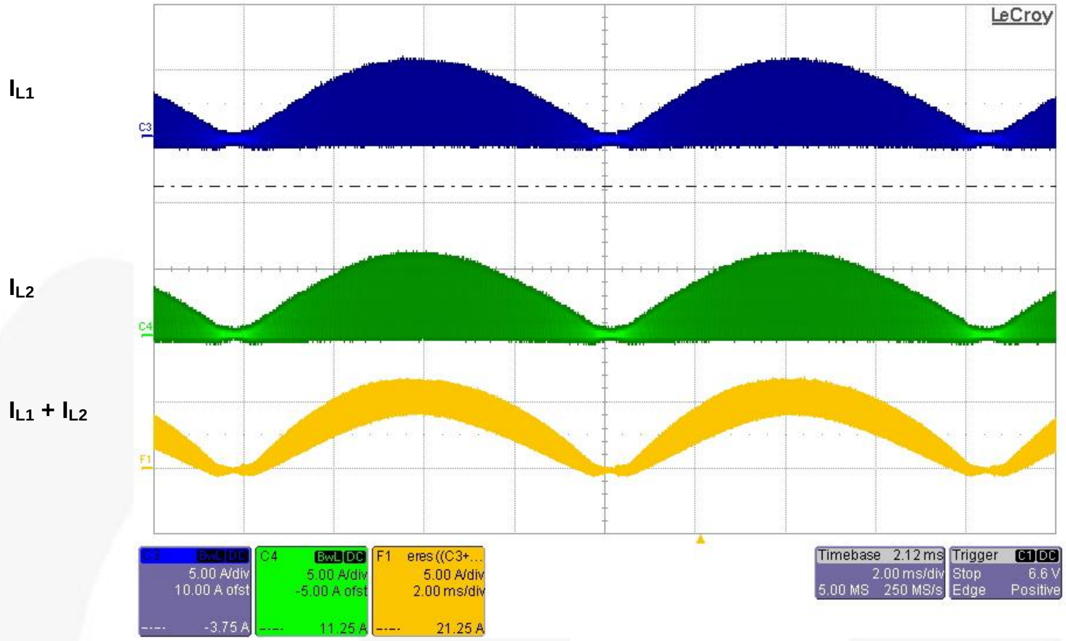


CH1: Gate Drive 1 Voltage (20 V / div), CH2: COMP Voltage (2 V / div),
CH3: Output Voltage (200 V / div), CH4: Line Current (5 A / div), Time (100 ms / div)

Figure 18. Full-Load Startup at 230 V_{AC}

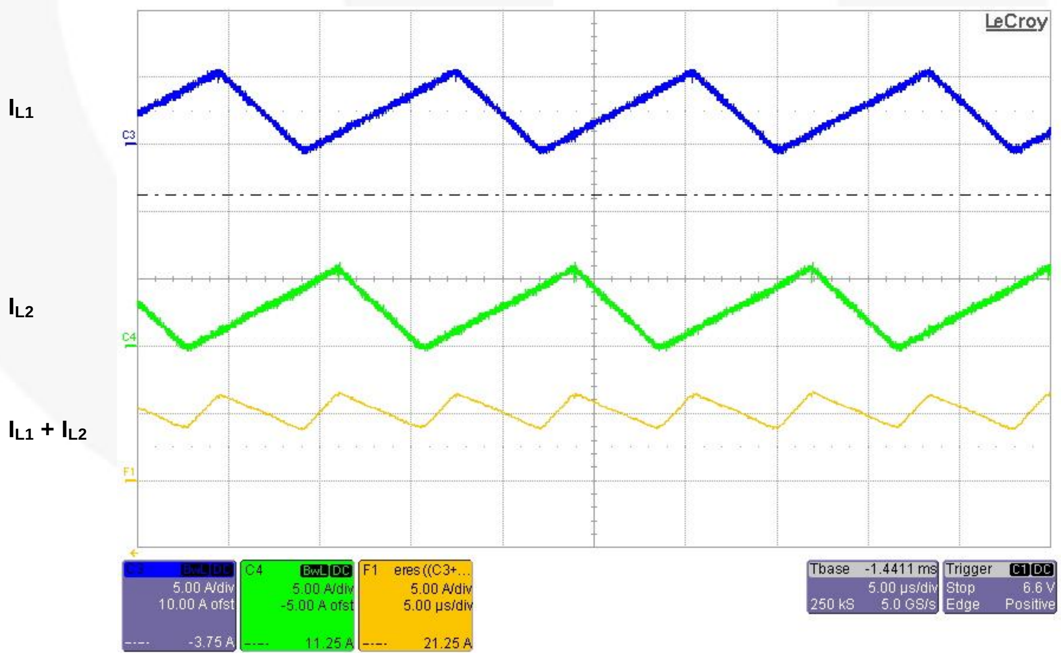
10.2. Normal Operation

Figure 19 and Figure 20 show the two inductor currents and sum of two inductor currents at 115 V_{AC} line voltage and full-load conditions. The sum of the inductor currents has relatively small ripple due to the ripple cancellation of interleaving operation.



CH3: Inductor L1 Current (5 A / div), CH4: Inductor L2 Current (5 A / div),
F1: Sum of Two Inductor Current (5 A / div), Time (2 ms / div)

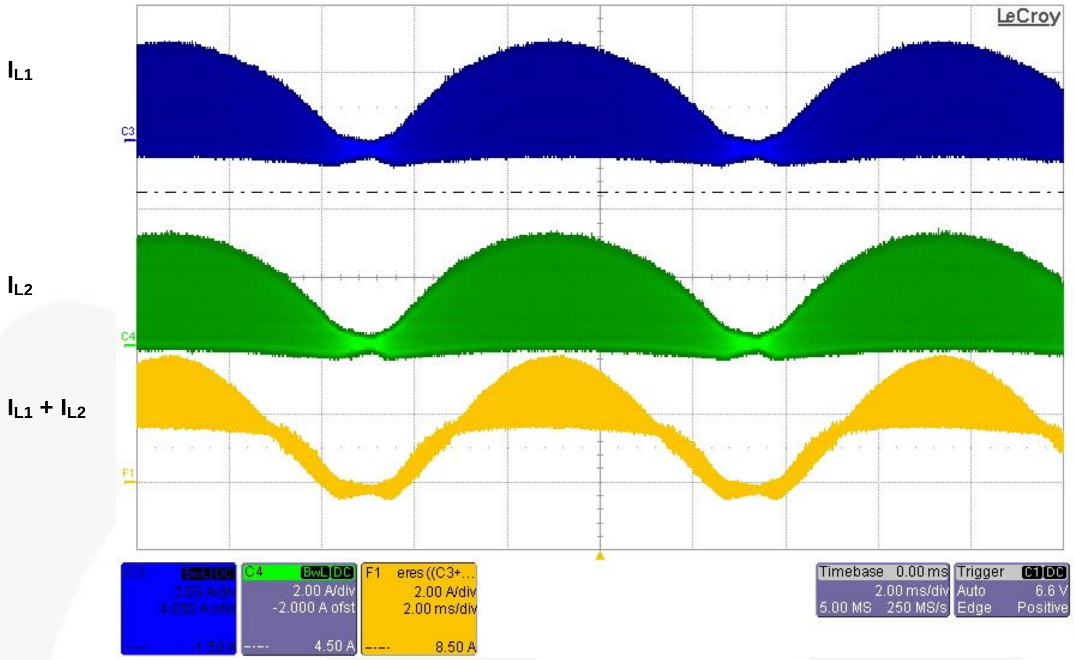
Figure 19. Inductor Current Waveforms at Full-Load and 115 V_{AC}



CH3: Inductor L1 Current (5 A / div), CH4: Inductor L2 Current (5 A / div),
F1: Sum of Two Inductor Current (5 A / div), Time (5 µs / div)

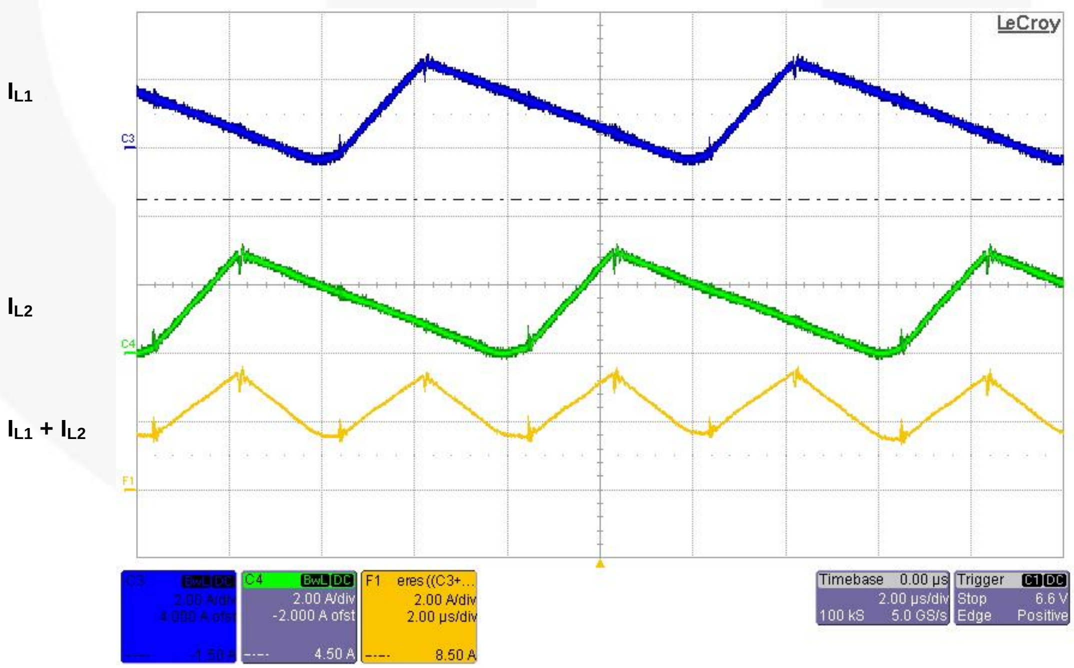
Figure 20. Zoom of Inductor Current Waveforms of Figure 19 at Peak of Line Voltage

Figure 21 and Figure 22 show the two inductor currents and sum of two inductor currents at 230 V_{AC} line voltage and full-load conditions. The sum of the inductor currents has relatively small ripple due to the ripple cancellation of interleaving operation.



CH3: Inductor L1 Current (2 A / div), CH4: Inductor L2 Current (2 A / div),
F1: Sum of Two Inductor Current (2 A / div), Time (2 ms / div)

Figure 21. Inductor Current Waveforms at Full-Load and 230 V_{AC}

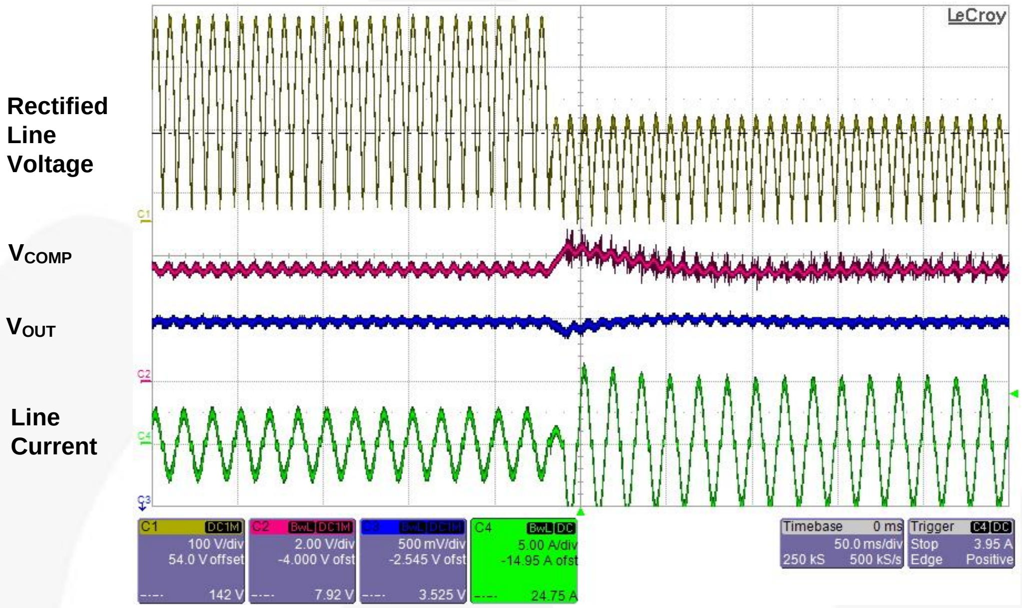


CH3: Inductor L1 Current (2 A / div), CH4: Inductor L2 Current (2 A / div),
F1: Sum of Two Inductor Current (2 A / div), Time (2 µs / div)

Figure 22. Zoom of Inductor Current Waveforms of Figure 21 at Peak of Line Voltage

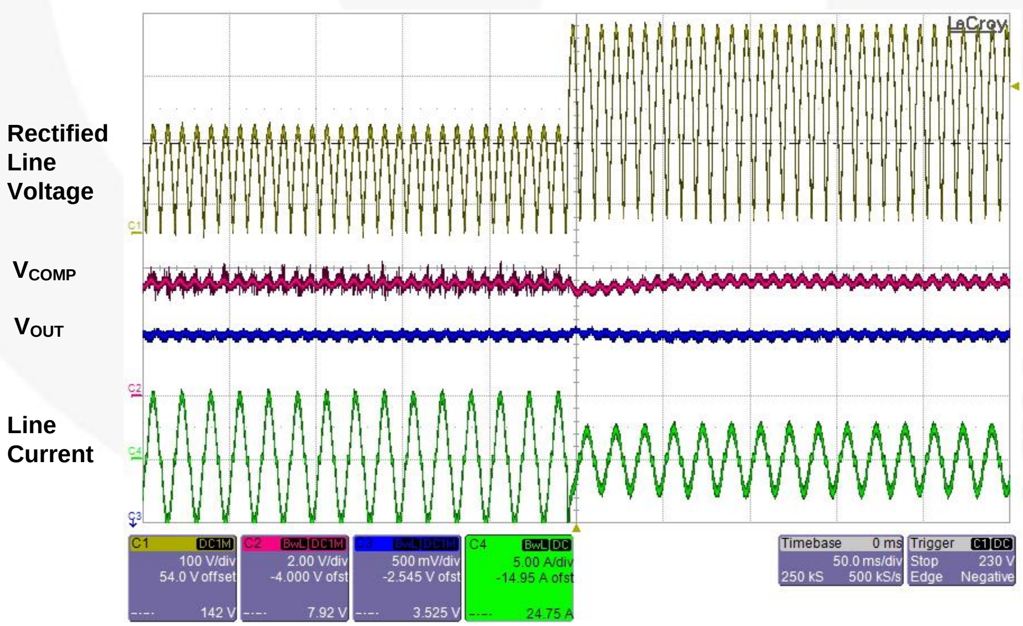
10.3. Line Transient

Figure 23 and Figure 24 show the line transient operation and minimal effect on output voltage due to the line feed-forward function. When the line voltage changes from 230 V_{AC} to 115 V_{AC}, about 20 V (5% of nominal output voltage) voltage undershoot is observed. When the line voltage changes from 115 V_{AC} to 230 V_{AC}, almost no voltage undershoot is observed.



CH1: Rectified Line Voltage (100 V / div), CH2: COMP Voltage (2 V / div),
CH3: Output Voltage (100 V / div), CH4: Line Current (5 A / div), Time (50 ms / div)

Figure 23. Line Transient Response at Full-Load Condition (230 V_{AC} →115 V_{AC})

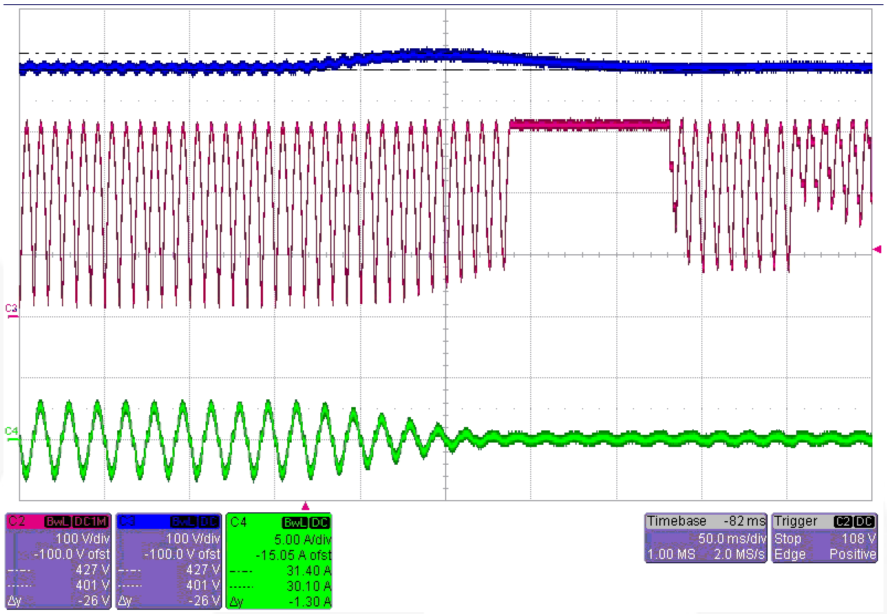


CH1: Rectified Line Voltage (100 V / div), CH2: COMP Voltage (2 V / div),
CH3: Output Voltage (100 V / div), CH4: Line Current (5 A / div), Time (50 ms / div)

Figure 24. Line Transient Response at Full-Load Condition (115 V_{AC} →230 V_{AC})

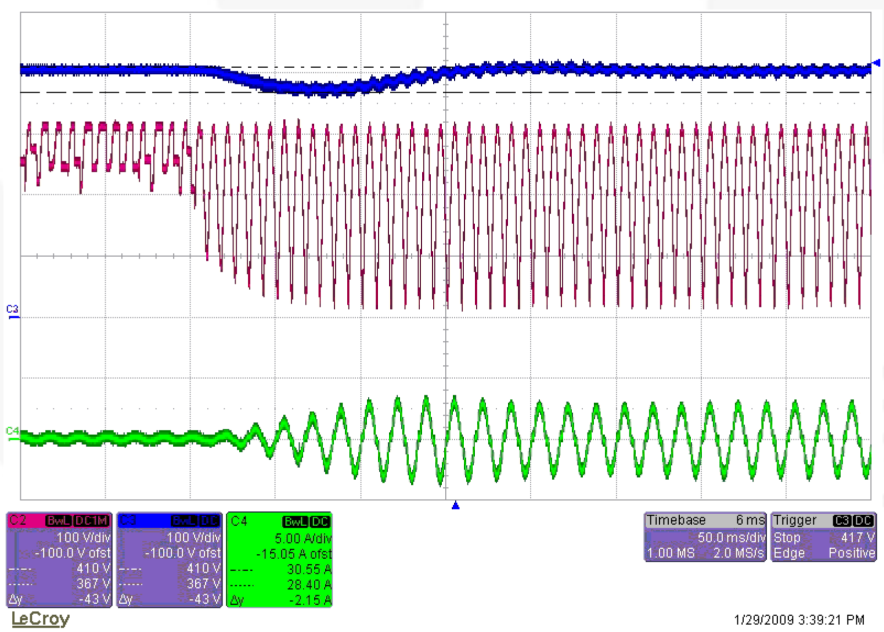
10.4. Load Transient

Figure 25 and Figure 26 show the load-transient operation. When the output load changes from 100% to 0%, 26 V (6.5% of nominal output voltage) voltage overshoot is observed. When the output load changes from 0% to 100%, 43 V (11% of nominal output voltage) voltage undershoot is observed.



CH2: Rectified line voltage (100 V / div), CH3: Output voltage (100 V / div),
CH4: Line current (5 A / div), Time (50 ms / div)

Figure 25. Load Transient Response at 230 V_{AC} (Full Load → No Load)

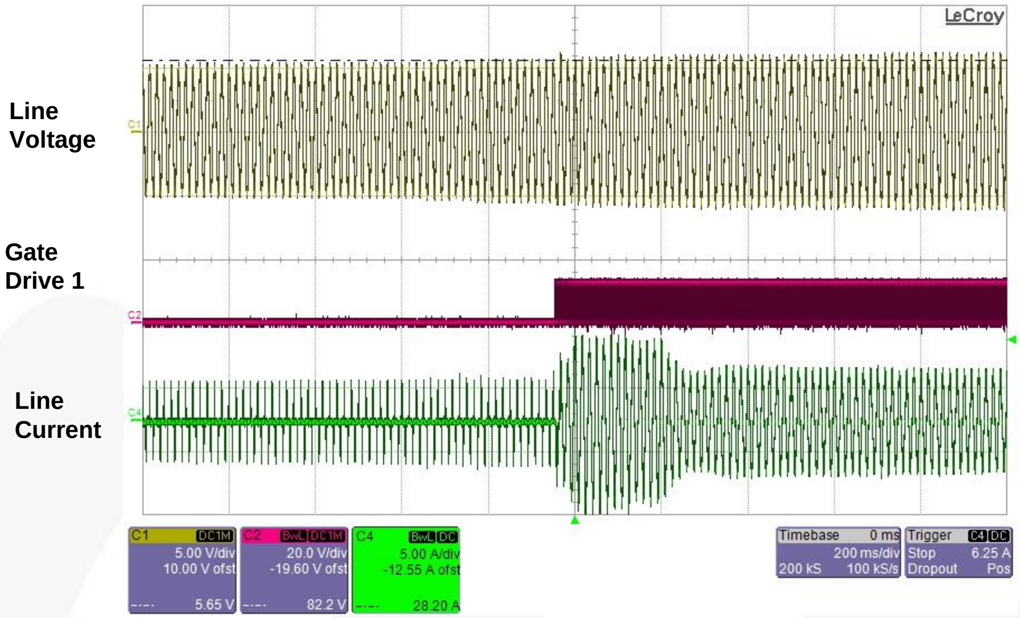


CH2: Rectified Line Voltage (100 V / div), CH3: Output Voltage (100 V / div),
CH4: Line Current (5 A / div), Time (50 ms / div)

Figure 26. Load Transient Response at 230 V_{AC} (No Load → Full Load)

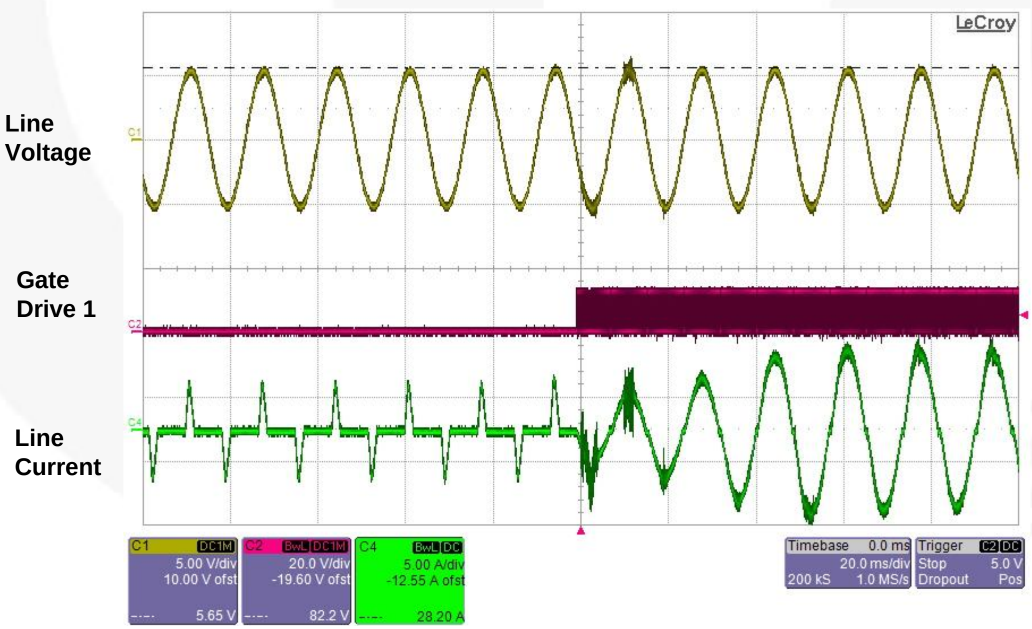
10.5. Brownout Protection

Figure 27 and Figure 28 show the startup operation at slowly increasing line voltage. The power supply starts up when the line voltage reaches around 78 V_{AC}.



CH1: Line Voltage (100 V / div), CH2: Gate Drive 1 Voltage (20 V / div),
CH4: Line Current (5 A / div), Time (200 ms / div)

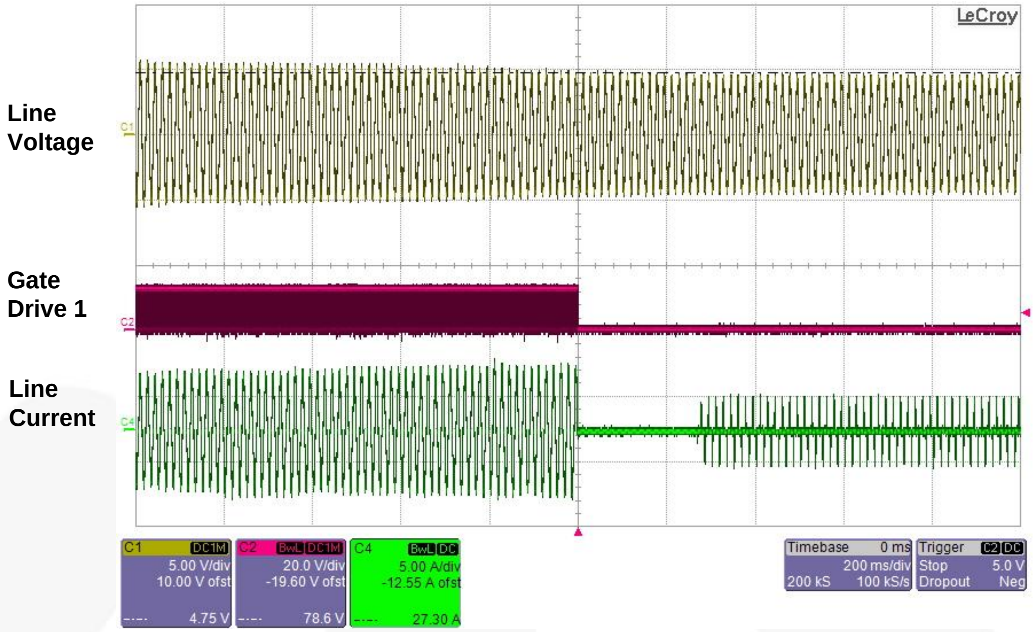
Figure 27. Startup Slowly Increasing the Line Voltage



CH1: Line Voltage (100 V / div), CH2: Gate Drive 1 Voltage (20 V / div),
CH4: Line Current (5 A / div), Time (20 ms / div)

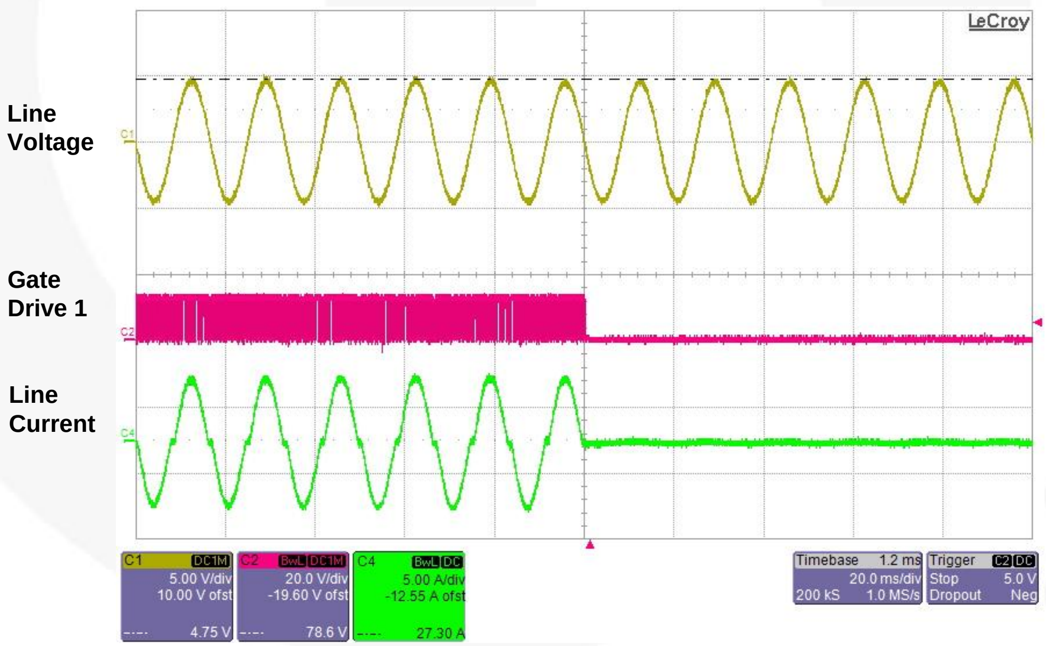
Figure 28. Shutdown Slowly Decreasing the Line Voltage

Figure 29 and Figure 30 show the shutdown operation at slowly decreasing line voltage. The power shuts down when line voltage drops below 68 V_{AC}.



CH1: Line Voltage (100 V / div), CH2: Gate Drive 1 Voltage (20 V / div),
CH4: Line Current (5 A / div), Time (200 ms / div)

Figure 29. Startup Slowly Increasing the Line Voltage

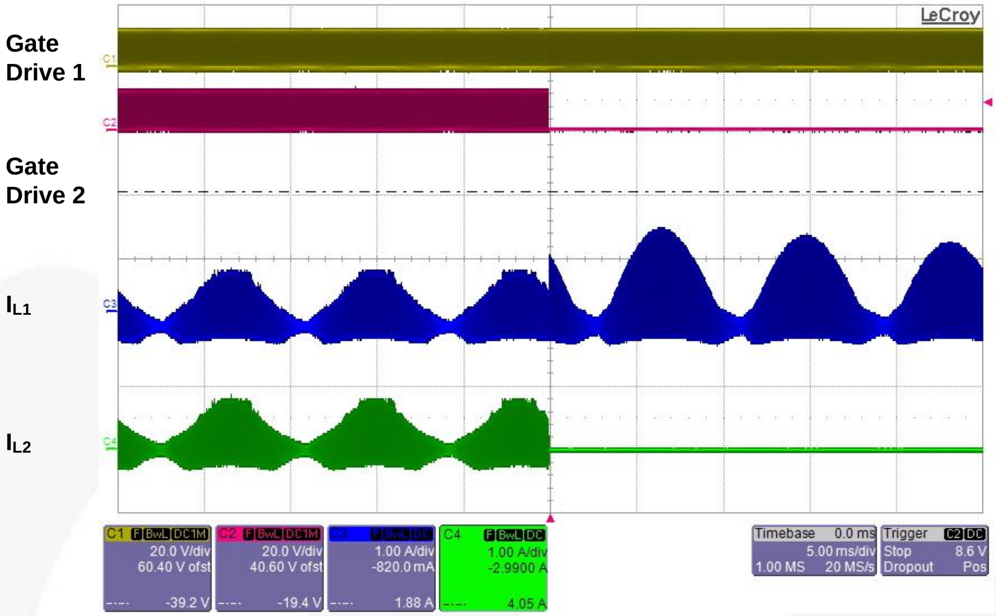


CH1: Line Voltage (100 V / div), CH2: Gate Drive 1 Voltage (20 V / div),
CH4: Line Current (5 A / div), Time (20 ms / div)

Figure 30. Shutdown Slowly Decreasing the Line Voltage

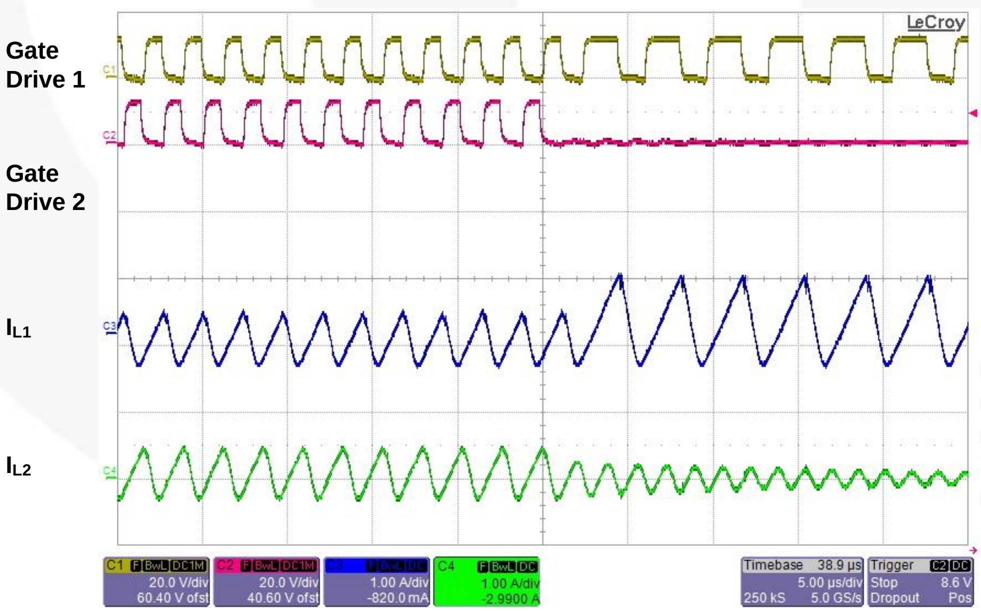
10.6. Phase Management

Figure 31 and Figure 32 show the phase-shedding waveforms. As observed, when the gate drive signal of Channel 2 is disabled, the duty cycle of Channel 1 gate drive signal is doubled to minimize the line current glitch and guarantee smooth transient.



CH1: Gate Drive 1 Voltage (20 V / div), CH2: Gate Drive 2 Voltage (20 V / div),
CH3: Inductor L1 Current (1 A / div), CH4: Inductor L2 Current (1 A / div), Time (5 ms / div)

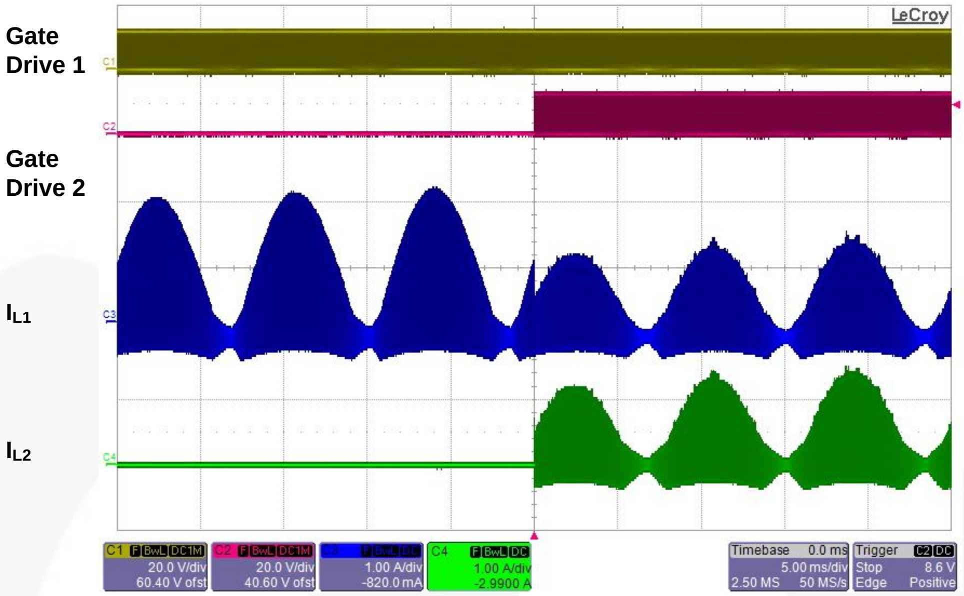
Figure 31. Phase-Shedding Operation



CH1: Gate Drive 1 Voltage (20 V / div), CH2: Gate Drive 2 Voltage (20 V / div),
CH3: Inductor L1 Current (1 A / div), CH4: Inductor L2 Current (1 A / div), Time (5 µs / div)

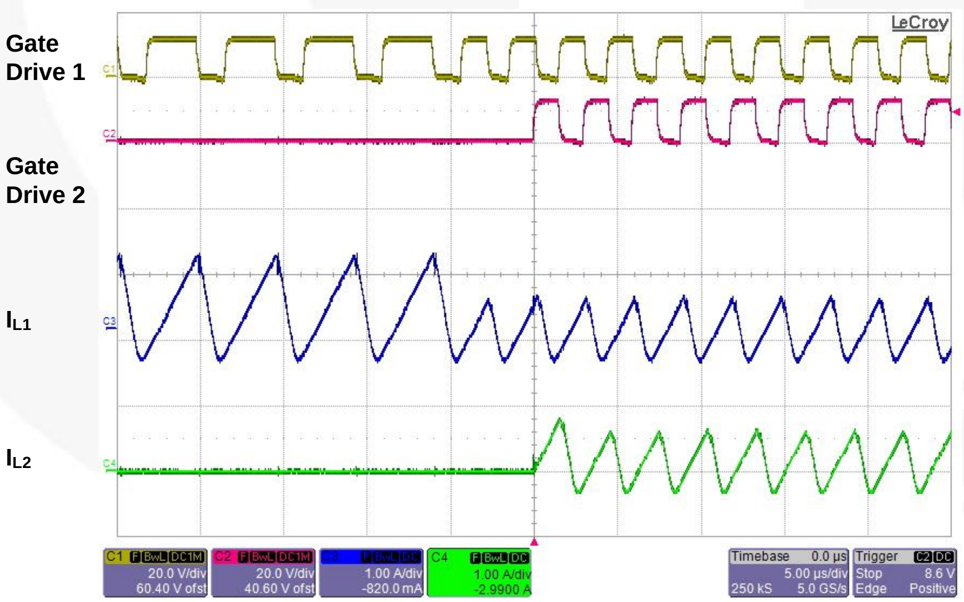
Figure 32. Phase-Shedding Operation (Zoomed-in Timescale)

Figure 33 and Figure 34 show the phase-adding waveforms. As observed, just before the Channel 2 gate drive signal is enabled, the duty cycle of Channel 1 gate drive signal is halved to minimize the line current glitch and guarantee smooth transient. In Figure 34, the first pulse of gate drive 2 during the phase-adding operation is skipped to ensure 180 degrees out-of-phase interleaving operation during transient.



CH1: Gate Drive 1 Voltage (20 V / div), CH2: Gate Drive 2 Voltage (20 V / div),
CH3: Inductor L1 Current (1 A / div), CH4: Inductor L2 Current (1 A / div), Time (5 ms / div)

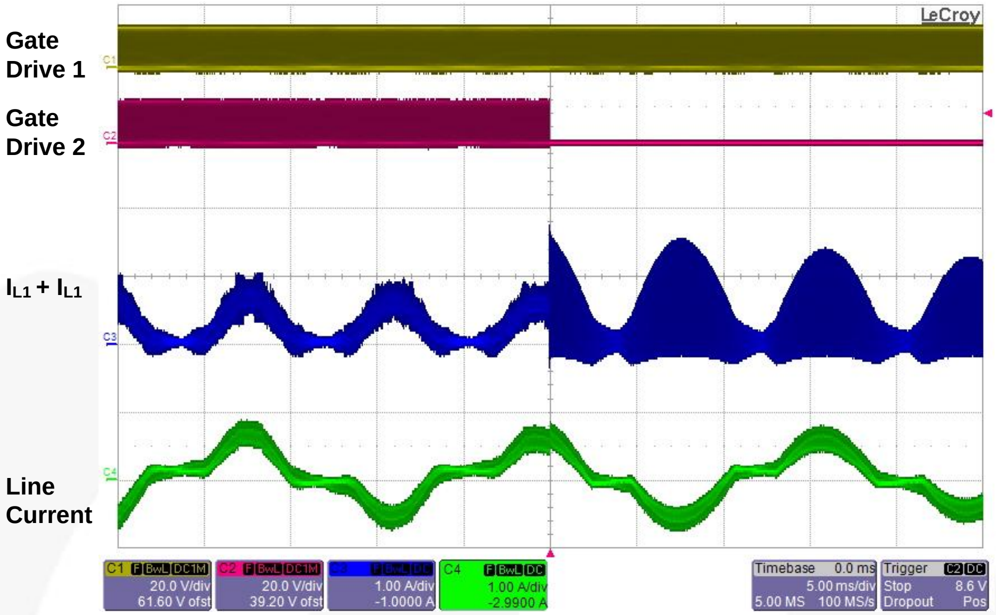
Figure 33. Phase-Adding Operation



CH1: Gate Drive 1 Voltage (20 V / div), CH2: Gate Drive 2 Voltage (20 V / div),
CH3: Inductor L1 Current (1 A / div), CH4: Inductor L2 Current (1 A / div), Time (5 µs / div)

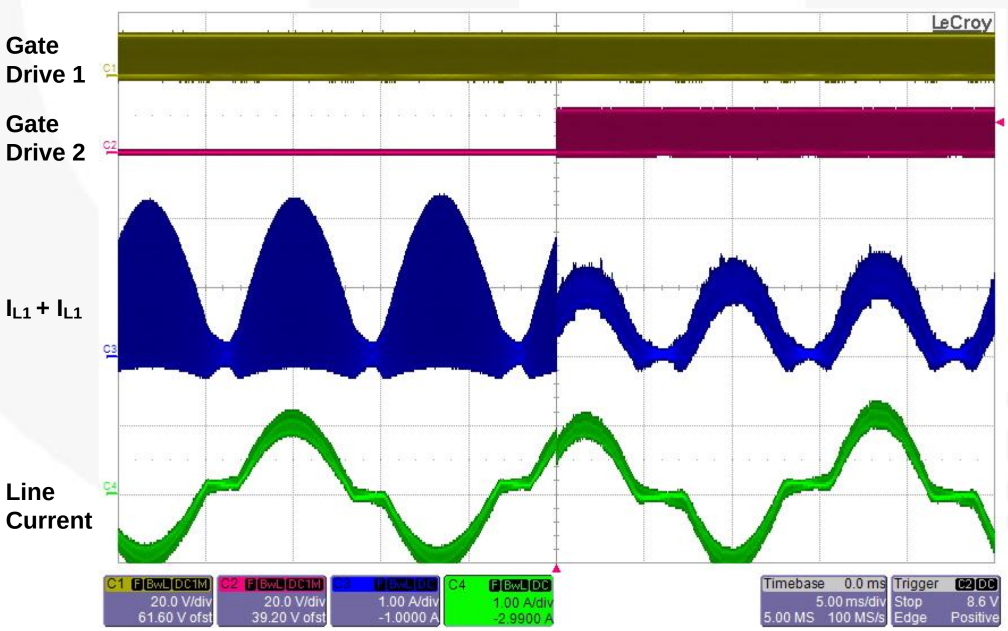
Figure 34. Phase-Adding Operation (Zoomed-in Timescale)

Figure 35 and Figure 36 show the sum of two-inductor current and line current for phase shedding and adding, respectively. The small line-current glitch during phase management exists because the actual average value of inductor current is less than half of the peak value due to the negative portion of inductor current, as shown in Figure 32 and Figure 34. However, the phase management takes place at relatively light-load condition and the effect of this phenomenon is negligible.



CH1: Gate Drive 1 Voltage (20 V / div), CH2: Gate Drive 2 Voltage (20 V / div),
CH3: Sum of Two Inductor Currents (1 A / div), CH4: Line Current (1 A / div), Time (5 ms / div)

Figure 35. Phase Shedding and Line Current



CH1: Gate Drive 1 Voltage (20 V / div), CH2: Gate Drive 2 Voltage (20 V / div),
CH3: Sum of Two Inductor Currents (1 A / div), CH4: Line Current (1 A / div), Time (5 ms / div)

Figure 36. Phase Adding Operation and Line Current

10.7. Efficiency

Figure 37 through Figure 40 show the measured efficiency of the 400 W evaluation board with and without phase management at input voltages of 115 V_{AC} and 230 V_{AC}. Phase management improves the efficiency at light load by up to 7%, depending on the line voltage and load condition. The phase management thresholds on the test evaluation board are around 15% of the nominal output power (Figure 37 and Figure 38). They can be adjusted upwards to achieve a more desirable efficiency profile (Figure 39 and Figure 40) by increasing the MOT resistor.

Since phase shedding reduces the switching loss by effectively decreasing the switching frequency at light load, a greater efficiency improvement is achieved at 230 V_{AC}, where switching losses dominate. Relatively less improvement is obtained at 115 V_{AC} since the MOSFET is turned on with zero voltage and switching losses are negligible.

The efficiency measurements include the losses in the EMI filter as well as cable loss; however, the power consumption of the control IC (<< 1 W) is not included since an external power supply is used for V_{DD}.

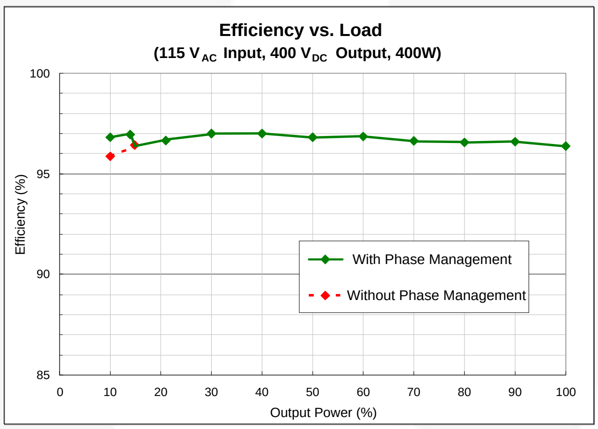


Figure 37. Measured Efficiency at 115 V_{AC} (Default Thresholds)

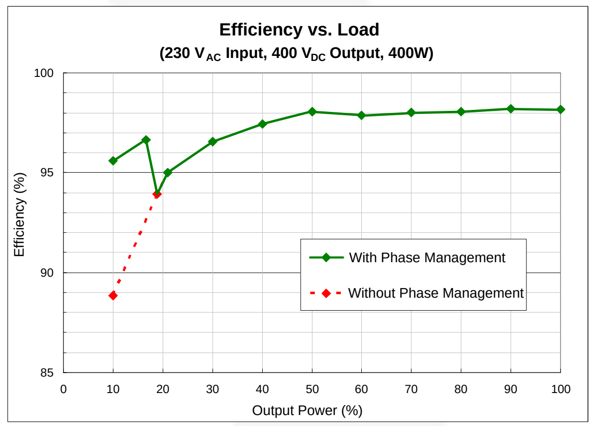


Figure 38. Measured Efficiency at 230 V_{AC} (Default Thresholds)

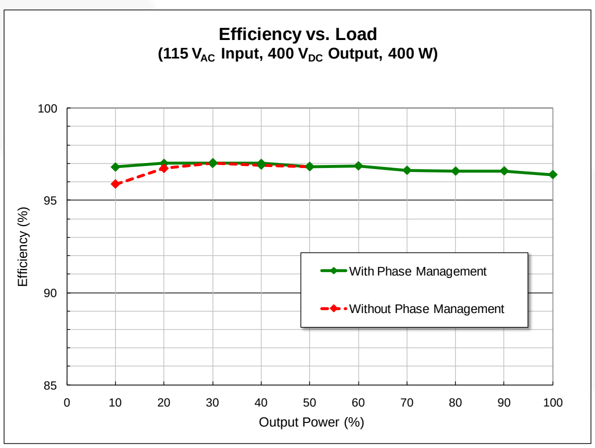


Figure 39. Measured Efficiency at 115 V_{AC} (Adjusted Thresholds)

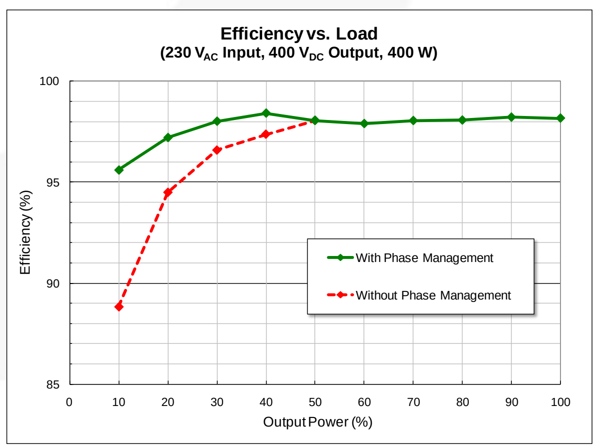


Figure 40. Measured Efficiency at 230 V_{AC} (Adjusted Thresholds)

10.8. Harmonic Distortion and Power Factor

Figure 41 and Figure 42 compare the measured harmonic current with EN61000 class D and C, respectively, at input voltages of 115 V_{AC} and 230 V_{AC}. Class D is applied to TV and PC power, while Class C is applied to lighting applications. As can be observed, both regulations are met with sufficient margin.

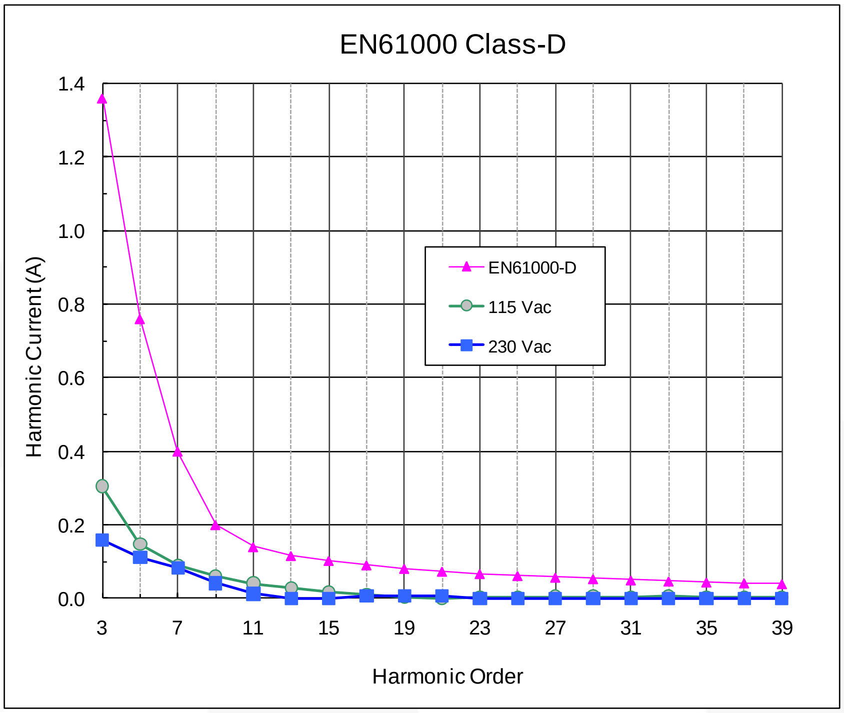


Figure 41. Measured Harmonic Current and EN61000 Class-D Regulation

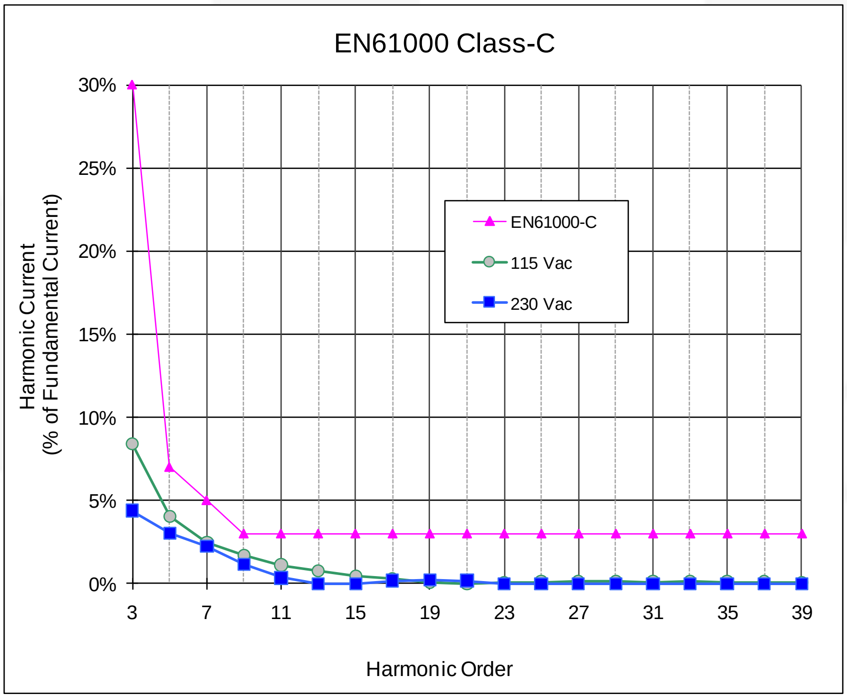


Figure 42. Measured Harmonic Current and EN61000 Class-C Regulation

Figure 43 shows the measured power factors at input voltage of 115 V_{AC} and 230 V_{AC}. As observed, high power factor above 0.98 is obtained from 100% to 50% load. Table 4 shows the total harmonic distortion at input voltages of 115 V_{AC} and 230 V_{AC}.

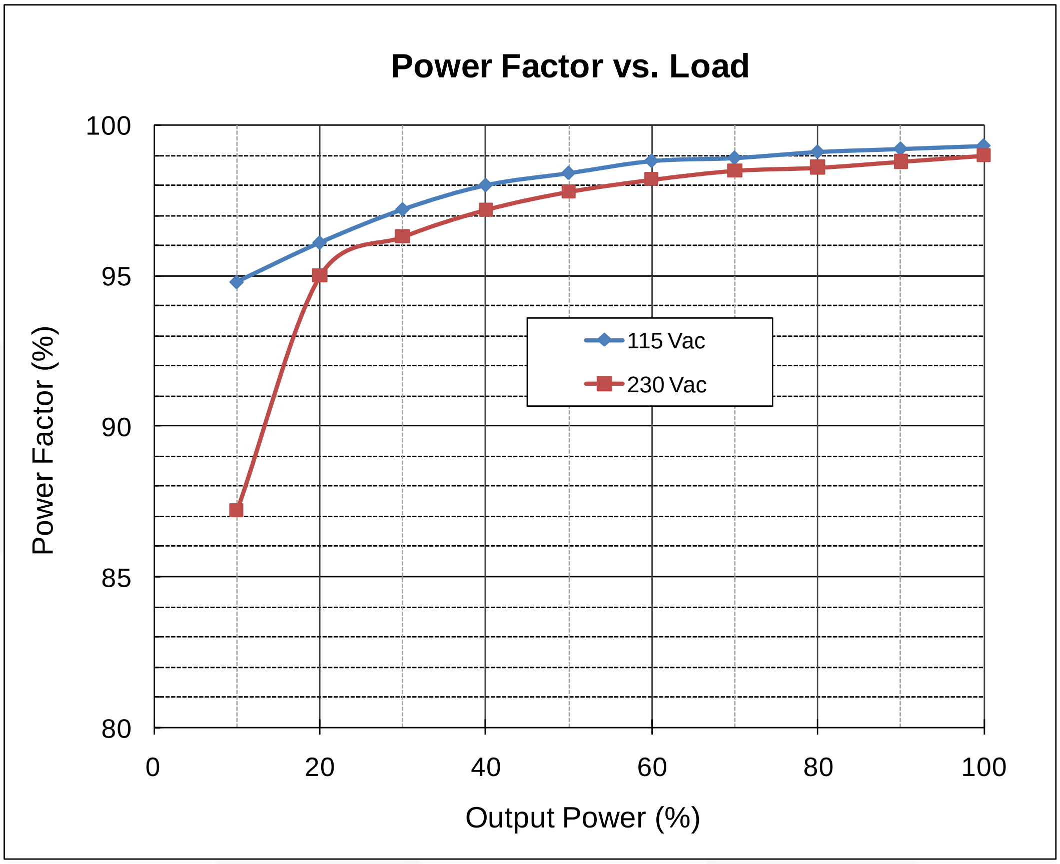


Figure 43. Measured Power Factor

Table 4. Total Harmonic Distortion (THD)

Line Voltage	100% Load	75% Load	50% Load	25% Load
115 V_{AC}	9.68%	11.82%	15.87%	24.08%
230 V_{AC}	11.36%	12.95%	15.30%	16.81%

11. References

FAN9611– Interleaved Dual BCM PFC Controller –Product Folder

FAN9612– Interleaved Dual BCM PFC Controller –Product Folder

AN-6086 – "Design Consideration for interleaved Boundary Conduction Mode (BCM) PFC Using FAN9611 / FAN9612"

12. Ordering Information

Orderable Part Number	Description
FEBFAN9611_S388V1	FAN9611 400 W Evaluation Board

13. Revision History

Date	Rev. #	Description
May 2013	0.0.5	Initial release/replacing AN-9717 (FEB388-001)
December 2014	0.0.6	Updated links

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Replace components on the Evaluation Board only with those parts shown on the parts list (or Bill of Materials) in the Users' Guide. Contact an authorized Fairchild representative with any questions.

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