



The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

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1. Go to [www.cypress.com/pcn](http://www.cypress.com/pcn).
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
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The MB9AA30N Series are highly integrated 32-bit microcontrollers that dedicated for embedded controllers with low-power consumption mode and competitive cost. The MB9AA30N Series are based on the ARM Cortex-M3 Processor with on-chip Flash memory and SRAM, and has peripheral functions such as LCD Controller, Motor Control Timers, ADCs, DACs and Communication Interfaces (UART, CSIO, I<sup>2</sup>C). The products which are described in this data sheet are placed into TYPE7 product categories in FM3 Family Peripheral Manual.

## Features

### 32-bit ARM Cortex-M3 Core

Processor version: r2p1

Up to 20 MHz Operation Frequency

Integrated Nested Vectored Interrupt Controller (NVIC): 1 channel NMI (non-maskable interrupt) and 32 channels' peripheral interrupts and 8 priority levels

24-bit System timer (Sys Tick): System timer for OS task management

### On-chip Memories

[Flash memory]

Up to 128 Kbytes

Read cycle: 0 wait-cycle

Security function for code protection

[SRAM]

This series contains a total of up to 16 Kbyte on-chip SRAM that is connected to System bus of Cortex-M3 core.

SRAM1: Up to 16 Kbytes

### LCD controller (LCDC)

Selectable from 44 SEG x 4 COM (Max) or 40 SEG x 8 COM (Max)

Internal divide resistor is contained (selectable from 10kΩ or 100kΩ for the resistor value)

LCD drive power supply (bias) pin (VV4 to VV0)

Interrupt function synchronized with the LCD module frame frequency

With blinking function

Inverted display function

### Multi-function Serial Interface (Max 8 channels)

Operation mode is selectable from the followings for each channel

UART

CSIO

I<sup>2</sup>C

[UART]

Full duplex double buffer

Selection with or without parity supported

Built-in dedicated baud rate generator

External clock available as a serial clock

Various error detection functions available (parity errors, framing errors, and overrun errors)

[CSIO]

Full duplex double buffer

Built-in dedicated baud rate generator

Overrun error detection function available

[I<sup>2</sup>C]

Standard-mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported

### A/D Converter (Max 16 channels)

[12-bit A/D Converter]

Successive Approximation type

Conversion time: Min 1.0 μs

Priority conversion available (priority at 2 levels)

Scanning conversion mode

Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

### D/A Converter (Max 2 channels)

R-2R type

10-bit resolution

### Base Timer (Max 8channels)

Operation mode is selectable from the followings for each channel.

16-bit PWM timer

16-bit PPG timer

16-/32-bit reload timer

16-/32-bit PWC timer

## General-Purpose I/O Port

This series can use its pins as general-purpose I/O ports when they are not used for peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated to.

Capable of pull-up control per pin

Capable of reading pin level directly

Built-in the port relocate function

Up to 84 high-speed general-purpose I/O Ports@100 pin Package

Some ports are 5V tolerant I/O  
See "List of Pin Functions" and "I/O Circuit Type" to confirm the corresponding pins.

## Multi-function Timer

The Multi-function timer is composed of the following blocks.

16-bit free-run timer × 3 ch.

Input capture × 4 ch.

Output compare × 6 ch.

A/D activating compare × 3 ch.

Waveform generator × 3 ch.

16-bit PPG timer × 3 ch.  
IGBT mode is contained.

The following function can be used to achieve the motor control.

PWM signal output function

DC chopper waveform output function

Dead time function

Input capture function

A/D convertor activate function

DTIF (Motor emergency stop) interrupt function

## HDMI-CEC/Remote Control Receiver (Up to 2 channels)

HDMI- CEC receiver / Remote control receiver

- Operating modes supporting the following standards can be selected
  - SIRCS
  - NEC/Association for Electric Home Appliances
  - HDMI-CEC
- Capable of adjusting detection timings for start bit and data bit
- Equipped with noise filter

HDMI-CEC transmitter

- Header block automatic transmission by judging Signal free
- Generating status interrupt by detecting Arbitration lost
- Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
- Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)

## Real-time clock (RTC)

The Real-time clock can count

Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

The interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.

Timer interrupt function after set time or each set time.

Capable of rewriting the time with continuing the time count.

Leap year automatic count is available.

## External Interrupt Controller Unit

Up to 16 external interrupt input pins

Include one non-maskable interrupt (NMI) input pin

## Watchdog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a Hardware watchdog and a Software watchdog.

The Hardware watchdog timer is clocked by the built-in Low-speed CR oscillator. Therefore, the Hardware watchdog is active in any low-power consumption mode except RTC, Stop, Deep Standby RTC and Deep Standby Stop modes.

## Clock and Reset

[Clocks]

Selectable from five clock sources (2 external oscillators, 2 built-in CR oscillators, and Main PLL).

Main Clock: 4 MHz to 20 MHz

Sub Clock: 32.768 kHz

Built-in High-speed CR Clock: 4 MHz

Built-in Low-speed CR Clock: 100 kHz

Main PLL Clock

[Resets]

Reset requests from INITX pin

Power-on reset

Software reset

Watchdog timers reset

Low-voltage detection reset

Clock Super Visor reset

## Clock Super Visor (CSV)

Clocks generated by built-in CR oscillators are used to supervise abnormality of the external clocks.

If external clock failure (clock stop) is detected, reset is asserted.

If external frequency anomaly is detected, interrupt or reset is asserted.

**Low-Voltage Detector (LVD)**

This Series includes 2-stage monitoring of voltage on the VCC. When the voltage falls below the voltage that has been set, Low-Voltage Detector generates an interrupt or reset.

LVD1: error reporting via interrupt

LVD2: auto-reset operation

**Low-Power Consumption Mode**

Six low-power consumption modes supported.

Sleep

Timer

RTC

Stop

Deep Standby RTC

Deep Standby Stop

The backup register is 16 byte

**Debug**

Serial Wire JTAG Debug Port (SWJ-DP)

**Power Supply**

Wide range voltage: VCC = 1.8 V to 5.5 V

VCC = 2.2 V to 5.5 V (when LCDC is used)

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## 1. Product Lineup

### Memory size

Product name		MB9AFA31L/M/N	MB9AFA32L/M/N
On-chip Flash memory		64 Kbytes	128 Kbytes
On-chip SRAM	SRAM1	12 Kbytes	16 Kbytes

### Function

Product name		MB9AFA31L MB9AFA32L	MB9AFA31M MB9AFA32M	MB9AFA31N MB9AFA32N
Pin count		64	80	100
CPU		Cortex-M3		
Freq.		20 MHz		
Power supply voltage range		1.8 V to 5.5 V		
LCD Controller (LCDC)		24 SEG×4 COM (Max) or 20 SEG×8 COM (Max)	37 SEG×4 COM (Max) or 33 SEG×8 COM (Max)	44 SEG×4 COM (Max) or 40 SEG×8 COM (Max)
Multi-function Serial Interface (UART/CSIO/I <sup>2</sup> C)		8 ch. (Max)		
Base Timer (PWC/ Reload timer/PWM/PPG)		8 ch. (Max)		
MF-Timer	A/D activation compare	3 ch.	1 unit (Max)	
	Input capture	4 ch.		
	Free-run timer	3 ch.		
	Output compare	6 ch.		
	Waveform generator	3 ch.		
	PPG (IGBT mode)	3 ch.		
HDMI-CEC/ Remote Control Receiver		2 ch. (Max)		
Real-time clock (RTC)		1 unit		
Watchdog timer		1 ch. (SW) + 1 ch. (HW)		
External Interrupts		8 pins (Max)+ NMI × 1	11 pins (Max) + NMI × 1	16 pins (Max) + NMI × 1
General-purpose I/O ports		52 pins (Max)	67 pins (Max)	84 pins (Max)
12-bit A/D converter		9 ch. (1 unit)	12 ch. (1 unit)	16 ch. (1 unit)
10-bit D/A converter		2 ch. (Max)		
CSV (Clock Super Visor)		Yes		
LVD (Low-Voltage Detector)		2 ch.		
Built-in CR	High-speed	4 MHz		
	Low-speed	100 kHz		
Debug Function		SWJ-DP		

### Note:

- All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.  
See Electrical Characteristics"12.4 AC Characteristics Built-in CR Oscillation Characteristics for accuracy of built-in CR.

## 2. Packages

Package \ Product name	MB9AFA31L MB9AFA32L	MB9AFA31M MB9AFA32M	MB9AFA31N MB9AFA32N
LQFP: LQD064 (0.5 mm pitch)	○	-	-
LQFP: LQG064 (0.65 mm pitch)	○	-	-
QFN: VNC064	○	-	-
LQFP: LQH080 (0.5 mm pitch)	-	○	-
LQFP: LQJ080 (0.65 mm pitch)	-	○	-
LQFP: LQI100 (0.5 mm pitch)	-	-	○
QFP: PQH100 (0.65 mm pitch)	-	-	○

○: Supported

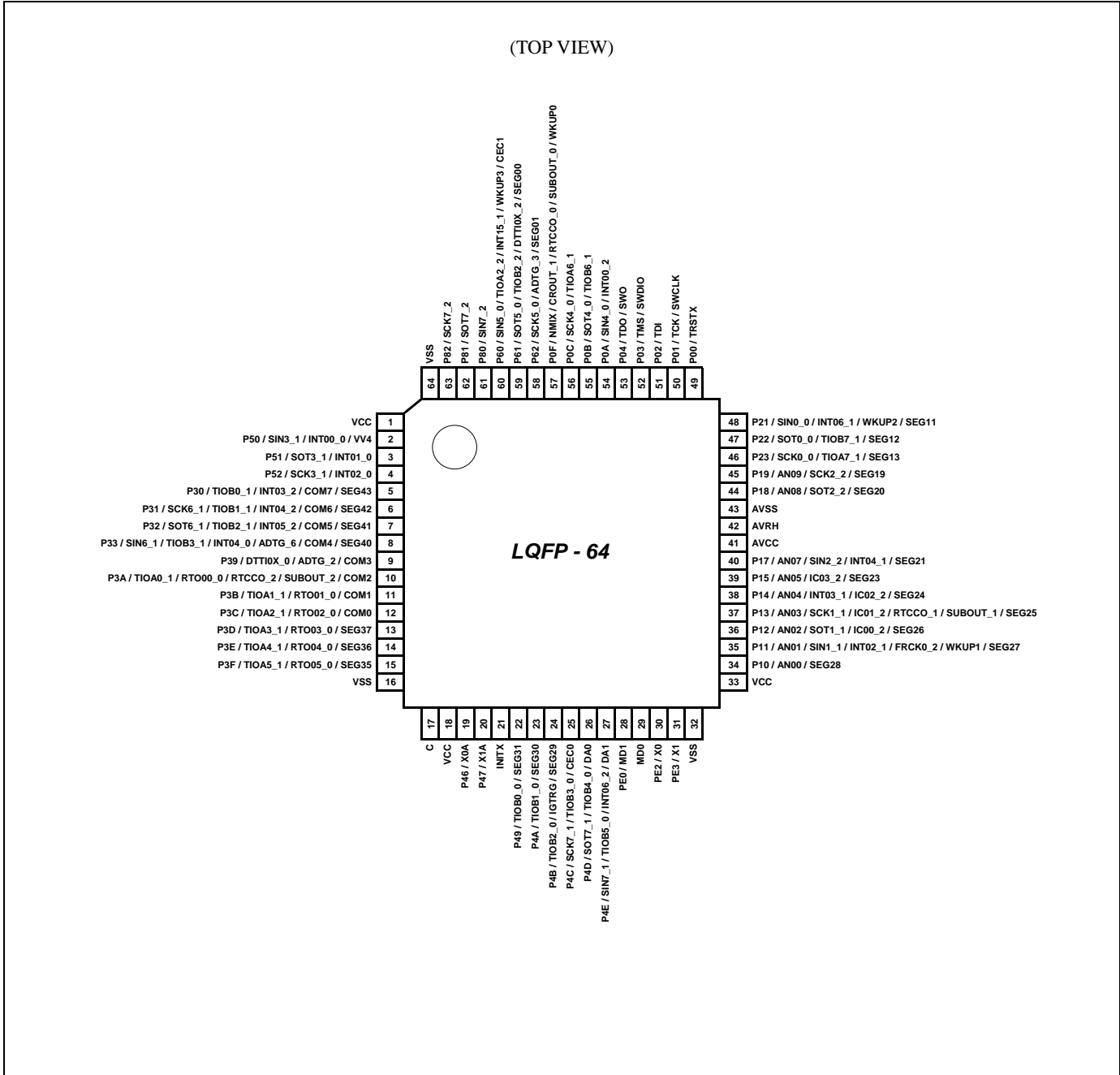
**Note:**

- See *Package Dimensions* for detailed information on each package.



## 3. Pin Assignment

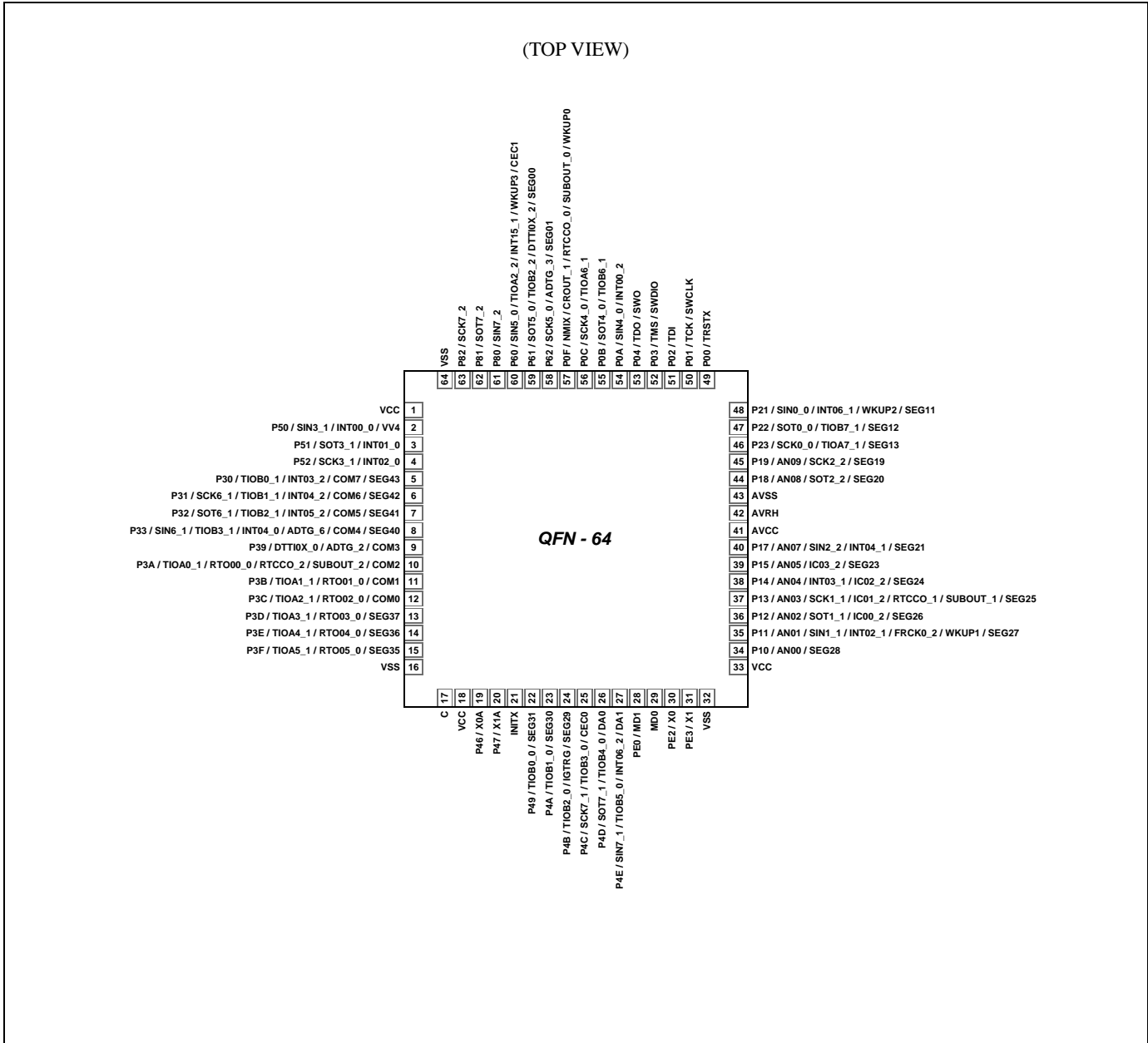
LQD064/LQG064



**Note:**

- The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPPR) to select the pin.

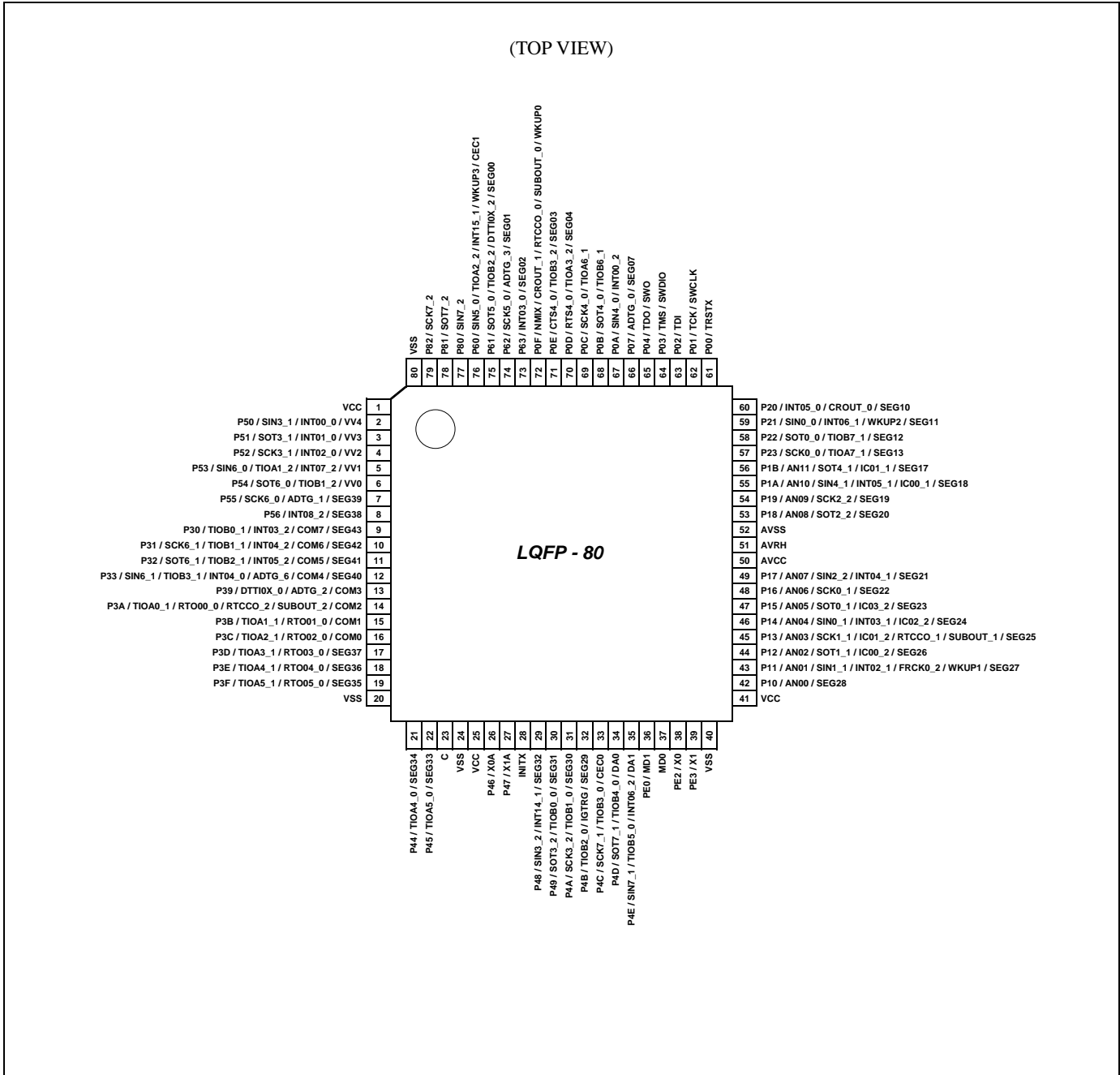
VNC064



**Note:**

- The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

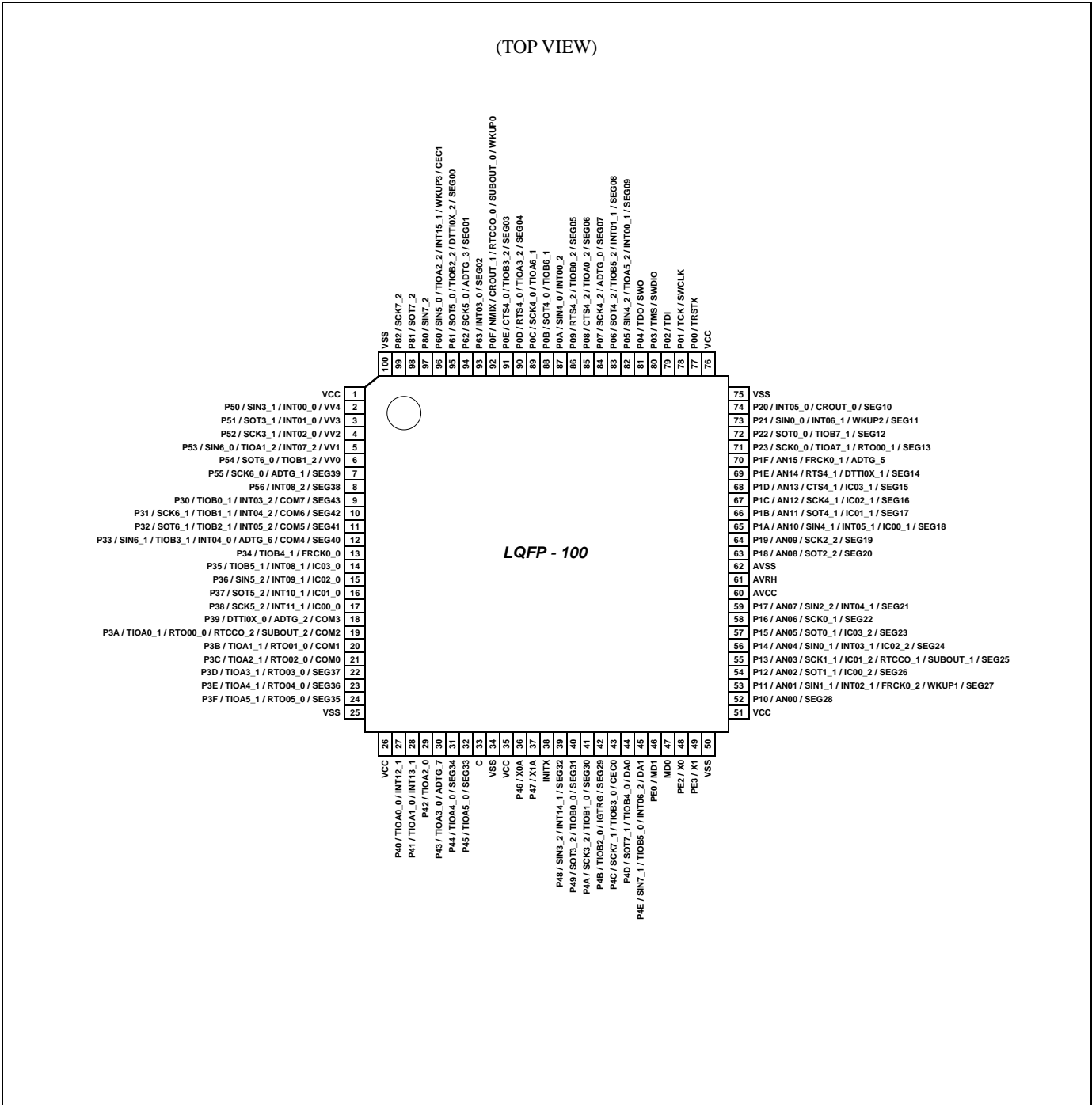
LQH080/LQJ080



**Note:**

- The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

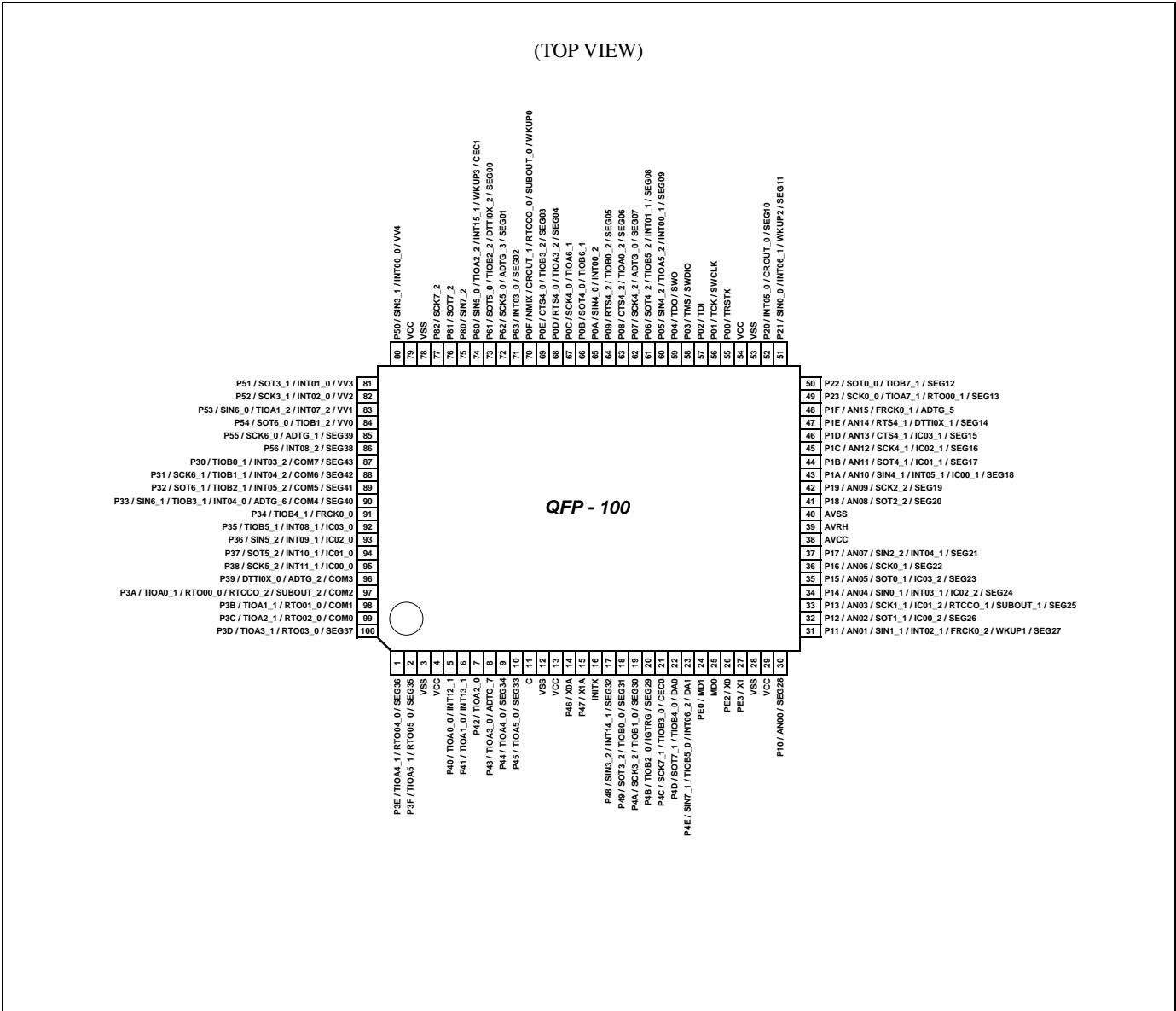
LQI100



**Note:**

- The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

PQH100


**Note:**

- The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

#### 4. List of Pin Functions

List of pin numbers

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-80	LQFP-100	QFP-100			
1	1	1	79	VCC	-	
2	2	2	80	P50	R	W
				INT00_0		
				SIN3_1		
				VV4		
-	3	3	81	P51	R	W
				INT01_0		
				SOT3_1 (SDA3_1)		
				VV3		
3	-	-	-	P51	E	F
				INT01_0		
				SOT3_1 (SDA3_1)		
-	4	4	82	P52	R	W
				INT02_0		
				SCK3_1 (SCL3_1)		
				VV2		
4	-	-	-	P52	E	F
				INT02_0		
				SCK3_1 (SCL3_1)		
-	5	5	83	P53	R	W
				SIN6_0		
				TIOA1_2		
				INT07_2		
				VV1		
-	6	6	84	P54	R	V
				SOT6_0 (SDA6_0)		
				TIOB1_2		
				VV0		
-	7	7	85	P55	J	U
				SCK6_0 (SCL6_0)		
				ADTG_1		
				SEG39		
-	8	8	86	P56	J	S
				INT08_2		
				SEG38		

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-80	LQFP-100	QFP-100			
5	9	9	87	P30	K	S
				TIOB0_1		
				INT03_2		
				COM7		
				SEG43		
6	10	10	88	P31	K	S
				TIOB1_1		
				SCK6_1 (SCL6_1)		
				INT04_2		
				COM6		
7	11	11	89	P32	K	S
				TIOB2_1		
				SOT6_1 (SDA6_1)		
				INT05_2		
				COM5		
8	12	12	90	P33	K	S
				INT04_0		
				TIOB3_1		
				SIN6_1		
				ADTG_6		
				COM4		
				SEG40		
-	-	13	91	P34	E	H
				FRCK0_0		
				TIOB4_1		
-	-	14	92	P35	E	F
				IC03_0		
				TIOB5_1		
				INT08_1		
-	-	15	93	P36	E	F
				IC02_0		
				SIN5_2		
				INT09_1		
-	-	16	94	P37	E	F
				IC01_0		
				SOT5_2 (SDA5_2)		
				INT10_1		

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-80	LQFP-100	QFP-100			
-	-	17	95	P38 IC00_0 SCK5_2 (SCL5_2) INT11_1	E	F
9	13	18	96	P39 DTTIOX_0 ADTG_2 COM3	L	U
10	14	19	97	P3A RTO00_0 (PPG00_0) TIOA0_1 RTCCO_2 SUBOUT_2 COM2	L	U
11	15	20	98	P3B RTO01_0 (PPG00_0) TIOA1_1 COM1	L	U
12	16	21	99	P3C RTO02_0 (PPG02_0) TIOA2_1 COM0	L	U
13	17	22	100	P3D RTO03_0 (PPG02_0) TIOA3_1 SEG37	J	U
14	18	23	1	P3E RTO04_0 (PPG04_0) TIOA4_1 SEG36	J	U
15	19	24	2	P3F RTO05_0 (PPG04_0) TIOA5_1 SEG35	J	U
16	20	25	3	VSS	-	
-	-	26	4	VCC	-	



Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-80	LQFP-100	QFP-100			
-	-	27	5	P40 TIOA0_0 INT12_1	E	F
-	-	28	6	P41 TIOA1_0 INT13_1	E	F
-	-	29	7	P42 TIOA2_0	E	H
-	-	30	8	P43 TIOA3_0 ADTG_7	E	H
-	21	31	9	P44 TIOA4_0 SEG34	J	U
-	22	32	10	P45 TIOA5_0 SEG33	J	U
17	23	33	11	C	-	
-	24	34	12	VSS	-	
18	25	35	13	VCC	-	
19	26	36	14	P46 X0A	D	M
20	27	37	15	P47 X1A	D	N
21	28	38	16	INITX	B	C
-	29	39	17	P48 INT14_1 SIN3_2 SEG32	J	S
22 -	30	40	18	P49 TIOB0_0 SEG31 SOT3_2 (SDA3_2)	J	U
23 -	31	41	19	P4A TIOB1_0 SEG30 SCK3_2 (SCL3_2)	J	U

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-80	LQFP-100	QFP-100			
24	32	42	20	P4B	J	U
				TIOB2_0		
				SEG29		
				IGTRG		
25	33	43	21	P4C	G	Q
				TIOB3_0		
				SCK7_1 (SCL7_1)		
				CEC0		
26	34	44	22	P4D	O	Z
				TIOB4_0		
				SOT7_1 (SDA7_1)		
				DA0		
27	35	45	23	P4E	O	Y
				TIOB5_0		
				INT06_2		
				SIN7_1 DA1		
28	36	46	24	PE0	C	P
				MD1		
29	37	47	25	MD0	H	D
30	38	48	26	PE2	A	A
				X0		
31	39	49	27	PE3	A	B
				X1		
32	40	50	28	VSS	-	
33	41	51	29	VCC	-	
34	42	52	30	P10	Q	J
				AN00		
				SEG28		
35	43	53	31	P11	Q	L
				AN01		
				SIN1_1		
				INT02_1		
				FRCK0_2		
				WKUP1		
				SEG27		
36	44	54	32	P12	Q	J
				AN02		
				SOT1_1 (SDA1_1)		
				IC00_2		
				SEG26		

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-80	LQFP-100	QFP-100			
37	45	55	33	P13	Q	J
				AN03		
				SCK1_1 (SCL1_1)		
				IC01_2		
				RTCCO_1		
				SUBOUT_1		
				SEG25		
38	46	56	34	P14	Q	K
				AN04		
				INT03_1		
				IC02_2		
				SEG24		
				SIN0_1		
-						
39	47	57	35	P15	Q	J
				AN05		
				IC03_2		
				SEG23		
				SOT0_1		
-						
-	48	58	36	P16	Q	J
				AN06		
				SCK0_1 (SCL0_1)		
				SEG22		
40	49	59	37	P17	Q	K
				AN07		
				SIN2_2		
				INT04_1		
				SEG21		
41	50	60	38	AVCC	-	
42	51	61	39	AVRH	-	
43	52	62	40	AVSS	-	
44	53	63	41	P18	Q	J
				AN08		
				SOT2_2 (SDA2_2)		
				SEG20		
45	54	64	42	P19	Q	J
				AN09		
				SCK2_2 (SCL2_2)		
				SEG19		

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-80	LQFP-100	QFP-100			
-	55	65	43	P1A AN10 SIN4_1 INT05_1 IC00_1 SEG18	Q	K
-	56	66	44	P1B AN11 SOT4_1 (SDA4_1) IC01_1 SEG17	Q	J
-	-	67	45	P1C AN12 SCK4_1 (SCL4_1) IC02_1 SEG16	Q	J
-	-	68	46	P1D AN13 CTS4_1 IC03_1 SEG15	Q	J
-	-	69	47	P1E AN14 RTS4_1 DTTIOX_1 SEG14	Q	J
-	-	70	48	P1F AN15 ADTG_5 FRCK0_1	F	X
46	57	71	49	P23 SCK0_0 (SCL0_0) TIOA7_1 SEG13 RTO00_1	J	U
-	-					
47	58	72	50	P22 SOT0_0 (SDA0_0) TIOB7_1 SEG12	J	U

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-80	LQFP-100	QFP-100			
48	59	73	51	P21	J	T
				SIN0_0		
				INT06_1		
				WKUP2		
				SEG11		
-	60	74	52	P20	J	S
				INT05_0		
				CROUT_0		
				SEG10		
-	-	75	53	VSS	-	-
-	-	76	54	VCC	-	-
49	61	77	55	P00	E	E
				TRSTX		
50	62	78	56	P01	E	E
				TCK		
				SWCLK		
51	63	79	57	P02	E	E
				TDI		
52	64	80	58	P03	E	E
				TMS		
				SWDIO		
53	65	81	59	P04	E	E
				TDO		
				SWO		
-	-	82	60	P05	J	S
				TIOA5_2		
				SIN4_2		
				INT00_1		
				SEG09		
-	-	83	61	P06	J	S
				TIOB5_2		
				SOT4_2 (SDA4_2)		
				INT01_1		
				SEG08		
-	66	84	62	P07	J	U
	-			ADTG_0		
				SEG07		
				SCK4_2 (SCL4_2)		
-	-	85	63	P08	J	U
				TIOA0_2		
				CTS4_2		
				SEG06		

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-80	LQFP-100	QFP-100			
-	-	86	64	P09 TIOB0_2 RTS4_2 SEG05	J	U
54	67	87	65	P0A SIN4_0 INT00_2	G	F
55	68	88	66	P0B SOT4_0 (SDA4_0) TIOB6_1	G	H
56	69	89	67	P0C SCK4_0 (SCL4_0) TIOA6_1	G	H
-	70	90	68	P0D RTS4_0 TIOA3_2 SEG04	J	U
-	71	91	69	P0E CTS4_0 TIOB3_2 SEG03	J	U
57	72	92	70	P0F NMIX CROUT_1 RTCCO_0 SUBOUT_0 WKUP0	E	I
-	73	93	71	P63 INT03_0 SEG02	J	S
58	74	94	72	P62 SCK5_0 (SCL5_0) ADTG_3 SEG01	J	U
59	75	95	73	P61 SOT5_0 (SDA5_0) TIOB2_2 DTTIOX_2 SEG00	J	U

Pin No				Pin name	I/O circuit type	Pin state type
LQFP-64 QFN-64	LQFP-80	LQFP-100	QFP-100			
60	76	96	74	P60	G	R
				SIN5_0		
				TIOA2_2		
				INT15_1		
				WKUP3		
CEC1						
61	77	97	75	P80	G	H
				SIN7_2		
62	78	98	76	P81	G	H
				SOT7_2		
63	79	99	77	P82	G	H
				SCK7_2		
64	80	100	78	VSS	-	

**List of pin functions**

The number after the underscore ("\_") in pin names such as XXX\_1 and XXX\_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin function	Pin name	Function description	Pin No			
			LQFP-64, QFN-64	LQFP-80	LQFP-100	QFP-100
ADC	ADTG_0	A/D converter external trigger input pin	-	66	84	62
	ADTG_1		-	7	7	85
	ADTG_2		9	13	18	96
	ADTG_3		58	74	94	72
	ADTG_4		-	-	-	-
	ADTG_5		-	-	70	48
	ADTG_6		8	12	12	90
	ADTG_7		-	-	30	8
	ADTG_8		-	-	-	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	34	42	52	30
	AN01		35	43	53	31
	AN02		36	44	54	32
	AN03		37	45	55	33
	AN04		38	46	56	34
	AN05		39	47	57	35
	AN06		-	48	58	36
	AN07		40	49	59	37
	AN08		44	53	63	41
	AN09		45	54	64	42
	AN10		-	55	65	43
	AN11		-	56	66	44
	AN12		-	-	67	45
	AN13		-	-	68	46
	AN14		-	-	69	47
	AN15	-	-	70	48	



Pin function	Pin name	Function description	Pin No			
			LQFP-64, QFN-64	LQFP-80	LQFP-100	QFP-100
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	-	-	27	5
	TIOA0_1		10	14	19	97
	TIOA0_2		-	-	85	63
	TIOB0_0	Base timer ch.0 TIOB pin	22	30	40	18
	TIOB0_1		5	9	9	87
	TIOB0_2		-	-	86	64
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	-	-	28	6
	TIOA1_1		11	15	20	98
	TIOA1_2		-	5	5	83
	TIOB1_0	Base timer ch.1 TIOB pin	23	31	41	19
	TIOB1_1		6	10	10	88
	TIOB1_2		-	6	6	84
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	-	-	29	7
	TIOA2_1		12	16	21	99
	TIOA2_2		60	76	96	74
	TIOB2_0	Base timer ch.2 TIOB pin	24	32	42	20
	TIOB2_1		7	11	11	89
	TIOB2_2		59	75	95	73
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	-	-	30	8
	TIOA3_1		13	17	22	100
	TIOA3_2		-	70	90	68
	TIOB3_0	Base timer ch.3 TIOB pin	25	33	43	21
	TIOB3_1		8	12	12	90
	TIOB3_2		-	71	91	69
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	-	21	31	9
	TIOA4_1		14	18	23	1
	TIOA4_2		-	-	-	-
	TIOB4_0	Base timer ch.4 TIOB pin	26	34	44	22
	TIOB4_1		-	-	13	91
	TIOB4_2		-	-	-	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	-	22	32	10
	TIOA5_1		15	19	24	2
	TIOA5_2		-	-	82	60
	TIOB5_0	Base timer ch.5 TIOB pin	27	35	45	23
	TIOB5_1		-	-	14	92
	TIOB5_2		-	-	83	61
Base Timer 6	TIOA6_1	Base timer ch.6 TIOA pin	56	69	89	67
	TIOB6_1	Base timer ch.6 TIOB pin	55	68	88	66
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	-	-	-	-
	TIOA7_1		46	57	71	49
	TIOA7_2		-	-	-	-
	TIOB7_0	Base timer ch.7 TIOB pin	-	-	-	-
	TIOB7_1		47	58	72	50
	TIOB7_2		-	-	-	-

Pin function	Pin name	Function description	Pin No			
			LQFP-64, QFN-64	LQFP-80	LQFP-100	QFP-100
Debugger	SWCLK	Serial wire debug interface clock input pin	50	62	78	56
	SWDIO	Serial wire debug interface data input / output pin	52	64	80	58
	SWO	Serial wire viewer output pin	53	65	81	59
	TRSTX	JTAG reset input pin	49	61	77	55
	TCK	JTAG test clock input pin	50	62	78	56
	TDI	JTAG test data input pin	51	63	79	57
	TMS	JTAG test mode state input/output pin	52	64	80	58
	TDO	JTAG debug data output pin	53	65	81	59
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2	80
	INT00_1		-	-	82	60
	INT00_2		54	67	87	65
	INT01_0	External interrupt request 01 input pin	3	3	3	81
	INT01_1		-	-	83	61
	INT02_0		4	4	4	82
	INT02_1	External interrupt request 02 input pin	35	43	53	31
	INT03_0		-	73	93	71
	INT03_1		38	46	56	34
	INT03_2	External interrupt request 03 input pin	5	9	9	87
	INT04_0		8	12	12	90
	INT04_1		40	49	59	37
	INT04_2	External interrupt request 04 input pin	6	10	10	88
	INT05_0		-	60	74	52
	INT05_1		-	55	65	43
	INT05_2	External interrupt request 05 input pin	7	11	11	89
	INT06_1		48	59	73	51
	INT06_2		27	35	45	23
	INT07_2	External interrupt request 07 input pin	-	5	5	83
	INT08_1	External interrupt request 08 input pin	-	-	14	92
	INT08_2		-	8	8	86
	INT09_1		External interrupt request 09 input pin	-	-	15
	INT10_1	External interrupt request 10 input pin	-	-	16	94
	INT11_1	External interrupt request 11 input pin	-	-	17	95
	INT12_1	External interrupt request 12 input pin	-	-	27	5
	INT13_1	External interrupt request 13 input pin	-	-	28	6
	INT14_1	External interrupt request 14 input pin	-	29	39	17
	INT15_1	External interrupt request 15 input pin	60	76	96	74
	NMIX	Non-Maskable Interrupt input pin	57	72	92	70

Pin function	Pin name	Function description	Pin No			
			LQFP-64, QFN-64	LQFP-80	LQFP-100	QFP-100
GPIO	P00	General-purpose I/O port 0	49	61	77	55
	P01		50	62	78	56
	P02		51	63	79	57
	P03		52	64	80	58
	P04		53	65	81	59
	P05		-	-	82	60
	P06		-	-	83	61
	P07		-	66	84	62
	P08		-	-	85	63
	P09		-	-	86	64
	P0A		54	67	87	65
	P0B		55	68	88	66
	P0C		56	69	89	67
	P0D		-	70	90	68
	P0E		-	71	91	69
	P0F		57	72	92	70
	P10	General-purpose I/O port 1	34	42	52	30
	P11		35	43	53	31
	P12		36	44	54	32
	P13		37	45	55	33
	P14		38	46	56	34
	P15		39	47	57	35
	P16		-	48	58	36
	P17		40	49	59	37
	P18		44	53	63	41
	P19		45	54	64	42
	P1A		-	55	65	43
	P1B		-	56	66	44
	P1C		-	-	67	45
	P1D		-	-	68	46
P1E	-	-	69	47		
P1F	-	-	70	48		
P20	General-purpose I/O port 2	-	60	74	52	
P21		48	59	73	51	
P22		47	58	72	50	
P23		46	57	71	49	

Pin function	Pin name	Function description	Pin No					
			LQFP-64, QFN-64	LQFP-80	LQFP-100	QFP-100		
GPIO	P30	General-purpose I/O port 3	5	9	9	87		
	P31		6	10	10	88		
	P32		7	11	11	89		
	P33		8	12	12	90		
	P34		-	-	13	91		
	P35		-	-	14	92		
	P36		-	-	15	93		
	P37		-	-	16	94		
	P38		-	-	17	95		
	P39		9	13	18	96		
	P3A		10	14	19	97		
	P3B		11	15	20	98		
	P3C		12	16	21	99		
	P3D		13	17	22	100		
	P3E		14	18	23	1		
	P3F		15	19	24	2		
	P40		-	General-purpose I/O port 4	-	-	27	5
	P41	-	-		-	28	6	
	P42	-	-		-	29	7	
	P43	-	-		-	30	8	
	P44	-	21		31	9		
	P45	-	22		32	10		
	P46	19	26		36	14		
	P47	20	27		37	15		
	P48	-	29		39	17		
	P49	22	30		40	18		
	P4A	23	31		41	19		
	P4B	24	32		42	20		
	P4C	25	33		43	21		
	P4D	26	34		44	22		
	P4E	27	35		45	23		
	P50	2	General-purpose I/O port 5		2	2	2	80
	P51	3			3	3	3	81
	P52	4		4	4	4	82	
	P53	-		5	5	5	83	
	P54	-		6	6	6	84	
	P55	-		7	7	7	85	
	P56	-		8	8	8	86	
	P60	60	General-purpose I/O port 6	76	96	74		
	P61	59		75	95	73		
	P62	58		74	94	72		
	P63	-		73	93	71		
	P80	61	General-purpose I/O port 8	77	97	75		
	P81	62		78	98	76		
	P82	63		79	99	77		
	PE0	28	General-purpose I/O port E	36	46	24		
	PE2	30		38	48	26		
PE3	31	39		49	27			

Pin function	Pin name	Function description	Pin No			
			LQFP-64, QFN-64	LQFP-80	LQFP-100	QFP-100
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	48	59	73	51
	SIN0_1		-	46	56	34
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA0 when it is used in an I <sup>2</sup> C (operation mode 4).	47	58	72	50
	SOT0_1 (SDA0_1)		-	47	57	35
	SCK0_0 (SCL0_0)		Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL0 when it is used in an I <sup>2</sup> C (operation mode 4).	46	57	71
SCK0_1 (SCL0_1)	-	48		58	36	
Multi-function Serial 1	SIN1_1	Multi-function serial interface ch.1 input pin	35	43	53	31
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA1 when it is used in an I <sup>2</sup> C (operation mode 4).	36	44	54	32
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL1 when it is used in an I <sup>2</sup> C (operation mode 4).	37	45	55	33
Multi-function Serial 2	SIN2_2	Multi-function serial interface ch.2 input pin	40	49	59	37
	SOT2_2 (SDA2_2)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA2 when it is used in an I <sup>2</sup> C (operation mode 4).	44	53	63	41
	SCK2_2 (SCL2_2)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL2 when it is used in an I <sup>2</sup> C (operation mode 4).	45	54	64	42

Pin function	Pin name	Function description	Pin No			
			LQFP-64, QFN-64	LQFP-80	LQFP-100	QFP-100
Multi-function Serial 3	SIN3_1	Multi-function serial interface ch.3 input pin	2	2	2	80
	SIN3_2		-	29	39	17
	SOT3_1 (SDA3_1)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA3 when it is used in an I <sup>2</sup> C (operation mode 4).	3	3	3	81
	SOT3_2 (SDA3_2)		-	30	40	18
	SCK3_1 (SCL3_1)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL3 when it is used in an I <sup>2</sup> C (operation mode 4).	4	4	4	82
	SCK3_2 (SCL3_2)		-	31	41	19
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	54	67	87	65
	SIN4_1		-	55	65	43
	SIN4_2		-	-	82	60
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4 when it is used in an I <sup>2</sup> C (operation mode 4).	55	68	88	66
	SOT4_1 (SDA4_1)		-	56	66	44
	SOT4_2 (SDA4_2)		-	-	83	61
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL4 when it is used in an I <sup>2</sup> C (operation mode 4).	56	69	89	67
	SCK4_1 (SCL4_1)		-	-	67	45
	SCK4_2 (SCL4_2)		-	-	84	62
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	-	70	90	68
	RTS4_1		-	-	69	47
	RTS4_2		-	-	86	64
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	-	71	91	69
	CTS4_1		-	-	68	46
	CTS4_2		-	-	85	63

Pin function	Pin name	Function description	Pin No			
			LQFP-64, QFN-64	LQFP-80	LQFP-100	QFP-100
Multi-function Serial 5	SIN5_0	Multi-function serial interface ch.5 input pin	60	76	96	74
	SIN5_2		-	-	15	93
	SOT5_0 (SDA5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA5 when it is used in an I <sup>2</sup> C (operation mode 4).	59	75	95	73
	SOT5_2 (SDA5_2)		-	-	16	94
	SCK5_0 (SCL5_0)		Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL5 when it is used in an I <sup>2</sup> C (operation mode 4).	58	74	94
SCK5_2 (SCL5_2)	-	-		17	95	
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	-	5	5	83
	SIN6_1		8	12	12	90
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA6 when it is used in an I <sup>2</sup> C (operation mode 4).	-	6	6	84
	SOT6_1 (SDA6_1)		7	11	11	89
	SCK6_0 (SCL6_0)		Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL6 when it is used in an I <sup>2</sup> C (operation mode 4).	-	7	7
SCK6_1 (SCL6_1)	6	10		10	88	
Multi-function Serial 7	SIN7_1	Multi-function serial interface ch.7 input pin	27	35	45	23
	SIN7_2		61	77	97	75
	SOT7_1 (SDA7_1)	Multi-function serial interface ch.7 output pin. This pin operates as SOT7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA7 when it is used in an I <sup>2</sup> C (operation mode 4).	26	34	44	22
	SOT7_2 (SDA7_2)		62	78	98	76
	SCK7_1 (SCL7_1)		Multi-function serial interface ch.7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/CSIO (operation modes 0 to 2) and as SCL7 when it is used in an I <sup>2</sup> C (operation mode 4).	25	33	43
SCK7_2 (SCL7_2)	63	79		99	77	

Pin function	Pin name	Function description	Pin No				
			LQFP-64, QFN-64	LQFP-80	LQFP-100	QFP-100	
Multi-function Timer 0	DTTI0X_0	Input signal of waveform generator to control outputs RTO00 to RTO05 of Multi-function timer 0	9	13	18	96	
	DTTI0X_1		-	-	69	47	
	DTTI0X_2		59	75	95	73	
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	-	-	13	91	
	FRCK0_1		-	-	70	48	
	FRCK0_2		35	43	53	31	
	IC00_0	16-bit input capture input pin of Multi-function timer 0. ICxx describes a channel number.	-	-	17	95	
	IC00_1		-	55	65	43	
	IC00_2		36	44	54	32	
	IC01_0		-	-	16	94	
	IC01_1		-	56	66	44	
	IC01_2		37	45	55	33	
	IC02_0		-	-	15	93	
	IC02_1		-	-	67	45	
	IC02_2		38	46	56	34	
	IC03_0		-	-	14	92	
	IC03_1		-	-	68	46	
	IC03_2		39	47	57	35	
	RTO00_0 (PPG00_0)		Waveform generator output pin of Multi-function timer 0.	10	14	19	97
	RTO00_1 (PPG00_1)		This pin operates as PPG00 when it is used in PPG0 output mode.	-	-	71	49
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output mode.	11	15	20	98	
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	12	16	21	99	
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output mode.	13	17	22	100	
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	14	18	23	1	
RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output mode.	15	19	24	2		
IGTRG	PPG IGBT mode external trigger input pin	24	32	42	20		



Pin function	Pin name	Function description	Pin No			
			LQFP-64, QFN-64	LQFP-80	LQFP-100	QFP-100
LCD Controller	VV0	LCD controller power supply I/O pin	-	6	6	84
	VV1		-	5	5	83
	VV2		-	4	4	82
	VV3		-	3	3	81
	VV4		2	2	2	80
	COM0	LCD controller common output pin	12	16	21	99
	COM1		11	15	20	98
	COM2		10	14	19	97
	COM3		9	13	18	96
	COM4		8	12	12	90
	COM5		7	11	11	89
	COM6		6	10	10	88
	COM7		5	9	9	87
	SEG00	LCD controller segment output pin	59	75	95	73
	SEG01		58	74	94	72
	SEG02		-	73	93	71
	SEG03		-	71	91	69
	SEG04		-	70	90	68
	SEG05		-	-	86	64
	SEG06		-	-	85	63
	SEG07		-	66	84	62
	SEG08		-	-	83	61
	SEG09		-	-	82	60
	SEG10		-	60	74	52
	SEG11		48	59	73	51
	SEG12		47	58	72	50
	SEG13		46	57	71	49
	SEG14		-	-	69	47
	SEG15		-	-	68	46
	SEG16		-	-	67	45
	SEG17		-	56	66	44
	SEG18		-	55	65	43
	SEG19		45	54	64	42
	SEG20		44	53	63	41
	SEG21		40	49	59	37
SEG22	-		48	58	36	
SEG23	39		47	57	35	
SEG24	38		46	56	34	
SEG25	37		45	55	33	
SEG26	36		44	54	32	
SEG27	35		43	53	31	
SEG28	34		42	52	30	
SEG29	24		32	42	20	
SEG30	23		31	41	19	
SEG31	22		30	40	18	
SEG32	-		29	39	17	
SEG33	-		22	32	10	
SEG34	-		21	31	9	
SEG35	15	19	24	2		

Pin function	Pin name	Function description	Pin No			
			LQFP-64, QFN-64	LQFP-80	LQFP-100	QFP-100
LCD Controller	SEG36	LCD controller segment output pin	14	18	23	1
	SEG37		13	17	22	100
	SEG38		-	8	8	86
	SEG39		-	7	7	85
	SEG40		8	12	12	90
	SEG41		7	11	11	89
	SEG42		6	10	10	88
	SEG43		5	9	9	87
Real-time clock	RTCCO_0	Pulse output pin of Real-time clock	57	72	92	70
	RTCCO_1		37	45	55	33
	RTCCO_2		10	14	19	97
	SUBOUT_0	Sub clock output pin	57	72	92	70
	SUBOUT_1		37	45	55	33
	SUBOUT_2		10	14	19	97
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	57	72	92	70
	WKUP1	Deep standby mode return signal input pin 1	35	43	53	31
	WKUP2	Deep standby mode return signal input pin 2	48	59	73	51
	WKUP3	Deep standby mode return signal input pin 3	60	76	96	74
DAC	DA0	D/A converter ch.0 analog output pin	26	34	44	22
	DA1	D/A converter ch.1 analog output pin	27	35	45	23
HDMI-CEC/Remote Control Reception	CEC0	HDMI-CEC/Remote Control Reception ch.0 input/output pin	25	33	43	21
	CEC1	HDMI-CEC/Remote Control Reception ch.1 input/output pin	60	76	96	74

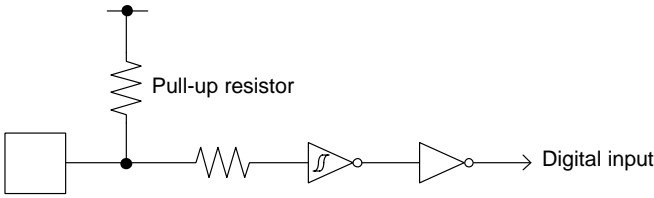
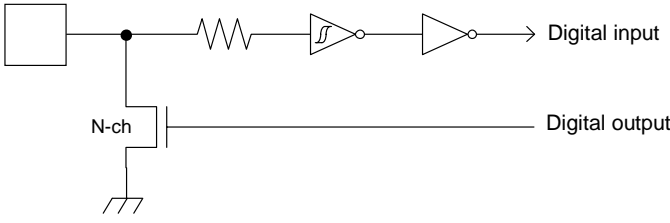
Pin function	Pin name	Function description	Pin No			
			LQFP-64, QFN-64	LQFP-80	LQFP-100	QFP-100
Reset	INITX	External Reset Input Pin. A reset is valid when INITX = L.	21	28	38	16
Mode	MD0	Mode 0 pin. During normal operation, MD0 = L must be input. During serial programming to Flash memory, MD0 = H must be input.	29	37	47	25
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = L must be input.	28	36	46	24
Power	VCC	Power supply pin	1	1	1	79
	VCC		-	-	26	4
	VCC		18	25	35	13
	VCC		33	41	51	29
	VCC		-	-	76	54
GND	VSS	GND pin	16	20	25	3
	VSS		-	24	34	12
	VSS		32	40	50	28
	VSS		-	-	75	53
	VSS		64	80	100	78
Clock	X0	Main clock (oscillation) input pin	30	38	48	26
	X0A	Sub clock (oscillation) input pin	19	26	36	14
	X1	Main clock (oscillation) I/O pin	31	39	49	27
	X1A	Sub clock (oscillation) I/O pin	20	27	37	15
	CROUT_0	Built-in High-speed CR-osc clock output port	-	60	74	52
	CROUT_1		57	72	92	70
Analog Power	AVCC	A/D converter and D/A converter analog power supply pin	41	50	60	38
	AVRH	A/D converter analog reference voltage input pin	42	51	61	39
Analog GND	AVSS	A/D converter and D/A converter GND pin	43	52	62	40
C pin	C	Power supply stabilization capacity pin	17	23	33	11

**Note:**

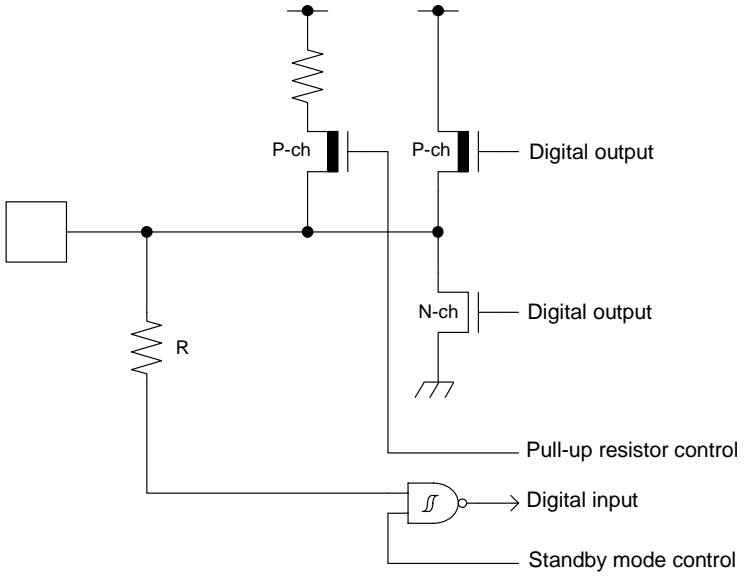
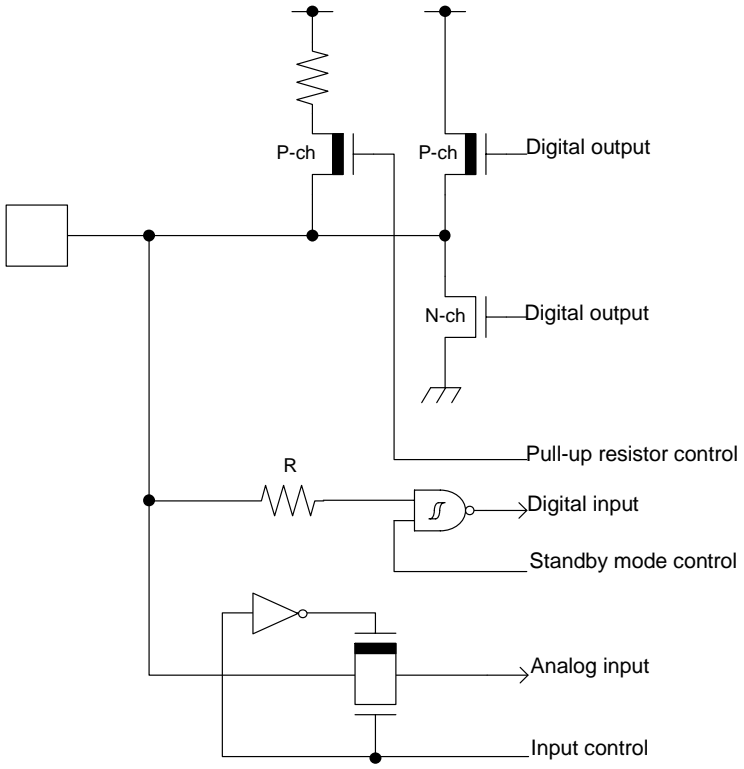
- While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.

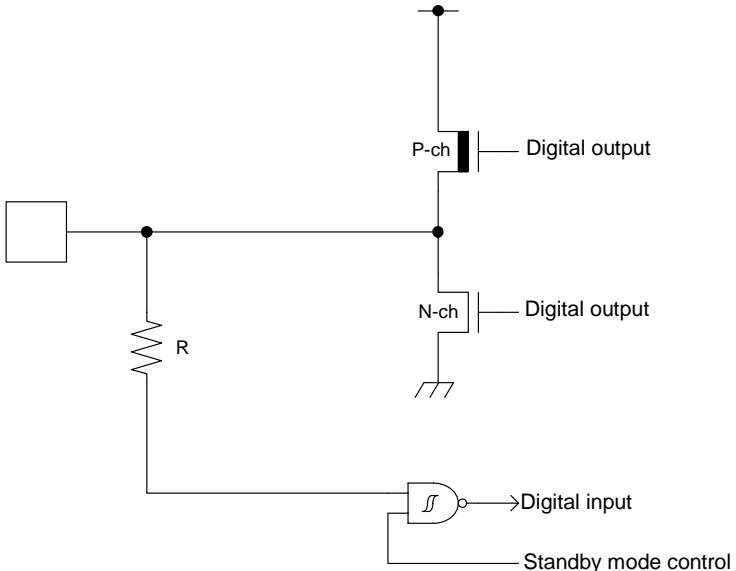
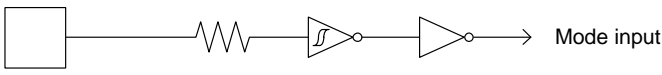
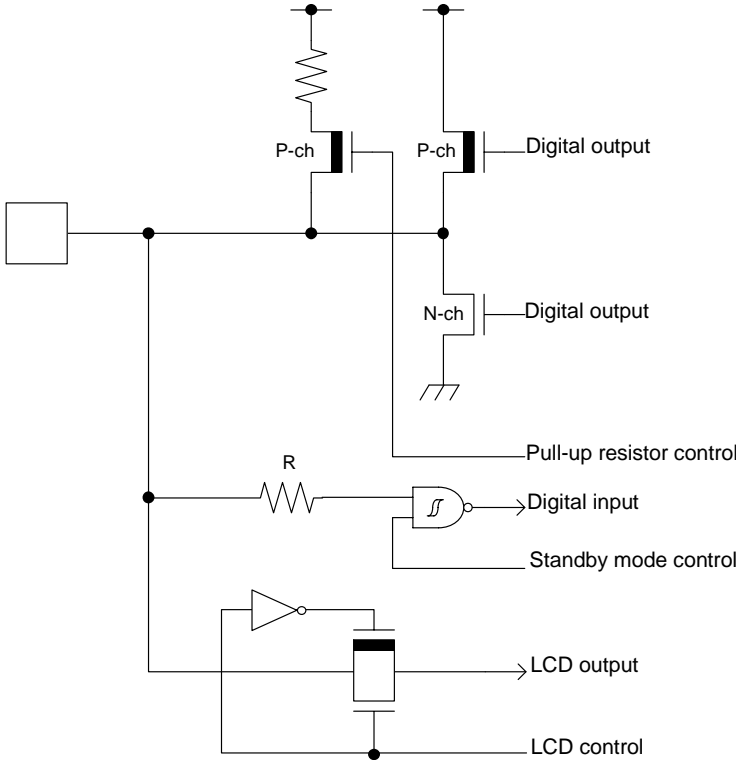
5. I/O Circuit Type

Type	Circuit	Remarks
A	<p>The diagram illustrates the internal circuitry for I/O Type A. It features two external oscillators, X1 and X0. X1 is connected to a pull-up resistor R and a P-channel MOSFET (P-ch). X0 is connected to a pull-up resistor R, a P-channel MOSFET (P-ch), and an N-channel MOSFET (N-ch). The circuit includes several digital I/O pins: Digital output (P-ch), Digital output (N-ch), Digital input, and Clock input. It also includes a Feedback resistor, a Standby mode control signal, and a Pull-up resistor control signal. The circuit is designed to support both main oscillation and GPIO functions.</p>	<p>It is possible to select the main oscillation / GPIO function.</p> <p>When the main oscillation is selected.</p> <p>Oscillation feedback resistor : Approximately 1 MΩ</p> <p>With standby mode control</p> <p>When the GPIO is selected.</p> <p>CMOS level output.</p> <p>CMOS level hysteresis input</p> <p>With pull-up resistor control</p> <p>With standby mode control</p> <p>Pull-up resistor : Approximately 50 kΩ</p> <p><math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></p>

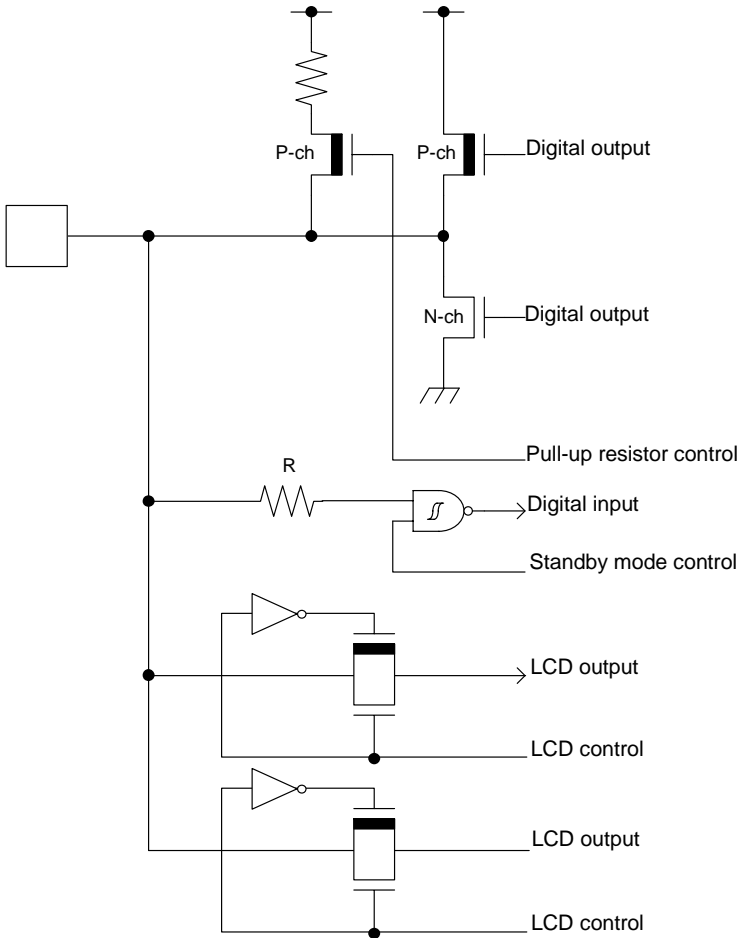
Type	Circuit	Remarks
B	 <p style="text-align: center;">Pull-up resistor</p> <p style="text-align: right;">Digital input</p>	CMOS level hysteresis input Pull-up resistor : Approximately 50 kΩ
C	 <p style="text-align: right;">Digital input</p> <p style="text-align: center;">N-ch</p> <p style="text-align: right;">Digital output</p>	Open drain output CMOS level hysteresis input

Type	Circuit	Remarks
D	<p>The diagram illustrates two identical circuit blocks, X1A and X0A. Each block features a pull-up resistor connected to a supply line. Below this resistor are two P-channel MOSFETs (P-ch) and one N-channel MOSFET (N-ch). The P-ch transistors are configured as digital outputs, while the N-ch transistor is also a digital output connected to ground. A feedback resistor is connected to a clock input through an inverter. Standby mode control signals are connected to digital inputs and clock inputs via logic gates. The circuit is controlled by pull-up resistor control signals.</p>	<p>It is possible to select the sub oscillation / GPIO function</p> <p>When the sub oscillation is selected.</p> <p>Oscillation feedback resistor : Approximately 5 MΩ</p> <p>With standby mode control</p> <p>When the GPIO is selected.</p> <p>CMOS level output.</p> <p>CMOS level hysteresis input</p> <p>With pull-up resistor control</p> <p>With standby mode control</p> <p>Pull-up resistor : Approximately 50 kΩ</p> <p><math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></p>

Type	Circuit	Remarks
E		<p>CMOS level output            CMOS level hysteresis input            With pull-up resistor control            With standby mode control            Pull-up resistor            : Approximately 50 kΩ  <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math>            When this pin is used as an I<sup>2</sup>C pin,            the digital output P-ch transistor is            always off</p>
F		<p>CMOS level output            CMOS level hysteresis input            With input control            Analog input            With pull-up resistor control            With standby mode control            Pull-up resistor            : Approximately 50 kΩ  <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></p>

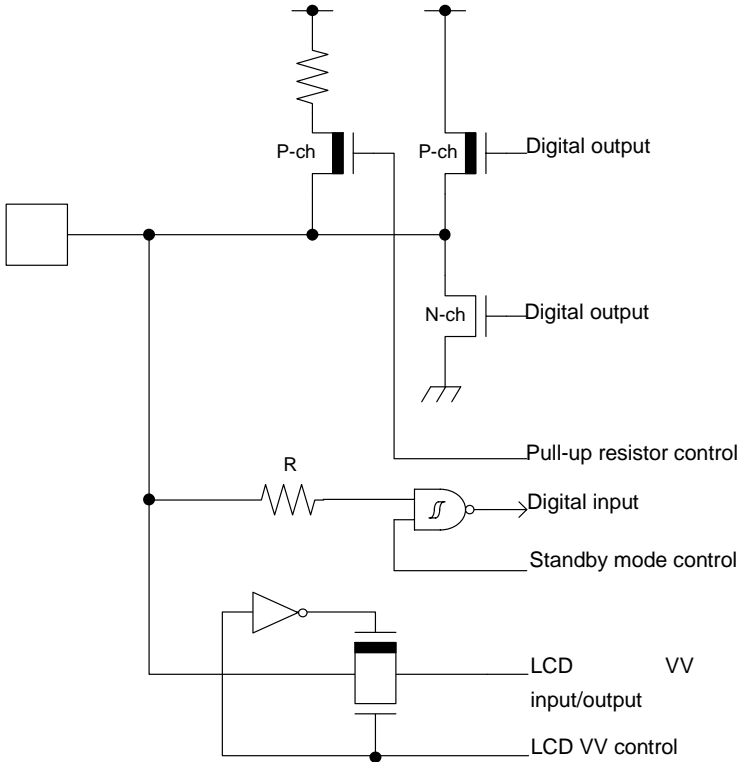
Type	Circuit	Remarks
G		<p>CMOS level output</p> <p>CMOS level hysteresis input</p> <p>With standby mode control</p> <p>5 V tolerant input</p> <p><math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></p> <p>Available to control PZR registers. P0B, P0C, P4C, P60, P81, P82 only.</p> <p>When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</p>
H		<p>CMOS level hysteresis input</p>
J		<p>CMOS level output</p> <p>CMOS level hysteresis input</p> <p>With input control</p> <p>LCD segment output</p> <p>With pull-up resistor control</p> <p>With standby mode control</p> <p>Pull-up resistor : Approximately 50 k<math>\Omega</math></p> <p><math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></p> <p>When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</p>



Type	Circuit	Remarks
K	 <p>The circuit diagram for pin K shows a central vertical bus connected to several functional blocks:</p> <ul style="list-style-type: none"> <li><b>Top Section:</b> A pull-up resistor is connected to the bus. Below it, a P-channel MOSFET (P-ch) is connected to the bus and ground. To its right, another P-channel MOSFET (P-ch) is connected to the bus and a "Digital output" terminal.</li> <li><b>Middle Section:</b> An N-channel MOSFET (N-ch) is connected to the bus and ground, with its "Digital output" terminal.</li> <li><b>Below Middle:</b> A resistor labeled 'R' is connected to the bus and an AND gate. The AND gate has two inputs: one from the bus and one from "Standby mode control". Its output is labeled "Digital input".</li> <li><b>Bottom Section:</b> Two identical LCD driver stages are shown. Each stage consists of an inverter connected to the bus, followed by a P-channel MOSFET (LCD control) and an N-channel MOSFET (LCD output) connected to ground.</li> </ul>	<p>CMOS level output          CMOS level hysteresis input          With input control          LCD common output          LCD segment output          With pull-up resistor control          With standby mode control          Pull-up resistor          : Approximately 50 kΩ  <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math>          When this pin is used as an I<sup>2</sup>C pin,          the digital output P-ch transistor is          always off</p>

Type	Circuit	Remarks
L		<p>CMOS level output            CMOS level hysteresis input            With input control            LCD common output            With pull-up resistor control            With standby mode control            Pull-up resistor            : Approximately 50 kΩ  <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></p>
O		<p>CMOS level output            CMOS level hysteresis input            With input control            Analog output            With pull-up resistor control            With standby mode control            Pull-up resistor            : Approximately 50 kΩ  <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math>            When this pin is used as an I<sup>2</sup>C pin,            the digital output P-ch transistor is            always off</p>

Type	Circuit	Remarks
Q	<p>The circuit diagram for pin Q shows a central vertical bus connected to several functional blocks:</p> <ul style="list-style-type: none"> <li><b>Top section:</b> A pull-up resistor is connected to the bus. Below it, a P-channel MOSFET (P-ch) is connected to the bus. To the right, another P-channel MOSFET (P-ch) is connected to the bus and labeled "Digital output". Below that, an N-channel MOSFET (N-ch) is connected to the bus and labeled "Digital output". A "Pull-up resistor control" line is connected to the bus.</li> <li><b>Middle section:</b> A resistor labeled "R" is connected to the bus. Below it, an AND gate has one input connected to the bus (labeled "Digital input") and another input connected to the "Pull-up resistor control" line (labeled "Standby mode control").</li> <li><b>Bottom section:</b> An inverter is connected to the bus. Below it, a MOSFET is connected to the bus and labeled "Analog input". Below that, another MOSFET is connected to the bus and labeled "Input control". At the bottom, a third MOSFET is connected to the bus and labeled "LCD output". Below that, a fourth MOSFET is connected to the bus and labeled "LCD control".</li> </ul>	<p>CMOS level output            CMOS level hysteresis input            With input control            Analog input            LCD segment output            With pull-up resistor control            With standby mode control            Pull-up resistor            : Approximately 50 kΩ  <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math>            When this pin is used as an I<sup>2</sup>C pin,            the digital output P-ch transistor is            always off</p>

Type	Circuit	Remarks
R	 <p>The circuit diagram for pin R shows a multi-functional pin configuration. At the top, a pull-up resistor is connected to the pin. The pin is connected to the gates of two transistors: a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET's drain is connected to the pin, and its source is connected to ground. The N-ch MOSFET's drain is connected to the pin, and its source is connected to ground. The P-ch MOSFET is labeled 'Digital output'. The N-ch MOSFET is labeled 'Digital output'. Below this, a resistor 'R' is connected to the pin, which is also connected to the input of an AND gate. The output of the AND gate is labeled 'Digital input'. The other input of the AND gate is labeled 'Standby mode control'. Below the AND gate, there is an inverter connected to the pin, which is also connected to the gate of a third P-channel MOSFET. The drain of this MOSFET is connected to the pin, and its source is connected to ground. This MOSFET is labeled 'LCD VV control'. The pin is also connected to the gate of a fourth P-channel MOSFET, which is labeled 'LCD VV input/output'. The drain of this MOSFET is connected to the pin, and its source is connected to ground.</p>	<p>CMOS level output          CMOS level hysteresis input          With input control          LCD VV input/output          With pull-up resistor control          With standby mode control          Pull-up resistor          : Approximately 50 k<math>\Omega</math>  <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math>          When this pin is used as an I<sup>2</sup>C pin,          the digital output P-ch transistor is          always off</p>

## 6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

### 6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

#### Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

#### Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

#### Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

##### 1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

##### 2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

##### 3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

#### Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

**CAUTION:** The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

#### Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

#### Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

#### Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

**CAUTION:** Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

## 6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress' recommended conditions. For detailed information about mount conditions, contact your sales representative.

### Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

### Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

#### Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

#### Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.  
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

#### Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

#### Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

### 6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

**CAUTION:** Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.



## 7. Handling Devices

### Power supply pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1  $\mu\text{F}$  be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin near this device.

### Stabilizing power supply voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/ $\mu\text{s}$  when there is a momentary fluctuation on switching the power supply.

### Crystal oscillator circuit

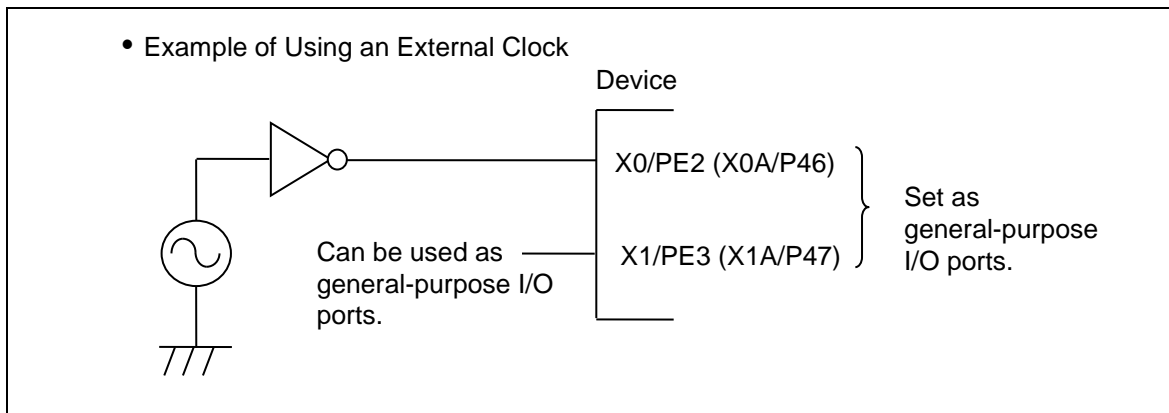
Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

### Using an external clock

To use the external clock, set general-purpose I/O ports to input the clock to X0/PE2 and X0A/P46 pin.

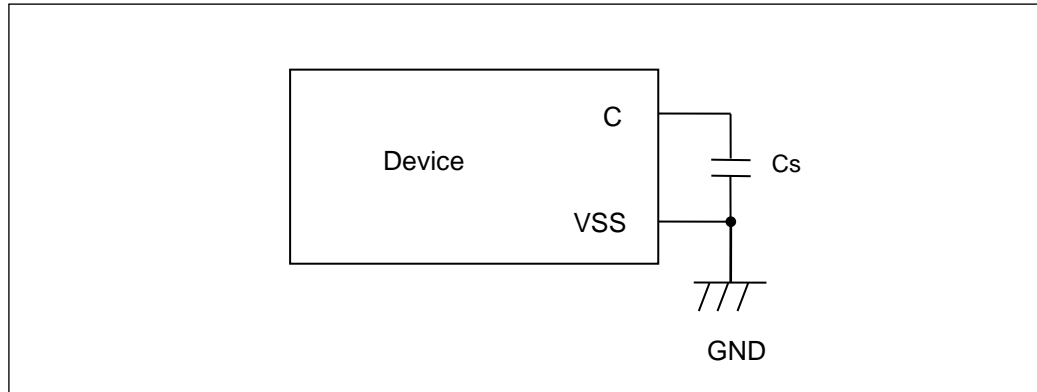


### Handling when using Multi-function serial pin as I<sup>2</sup>C pin

If it is using the multi-function serial pin as I<sup>2</sup>C pins, P-ch transistor of digital output is always disable. However, I<sup>2</sup>C pins need to keep the electrical characteristic like other pins and not to connect to the external I<sup>2</sup>C bus system with power OFF.

## C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor ( $C_s$ ) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor. A smoothing capacitor of about 4.7  $\mu\text{F}$  would be recommended for this series.



## Mode pins (MD0, MD1)

Connect the MD pin (MD0, MD1) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

## Notes on power-on

Turn power on/off in the following order or at the same time.

If not using the A/D converter, connect AVCC = VCC and AVSS = VSS.

Turning on : VCC → AVCC → AVRH

Turning off : AVRH → AVCC → VCC

## Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise; perform error detection such as by applying a checksum of data at the end.

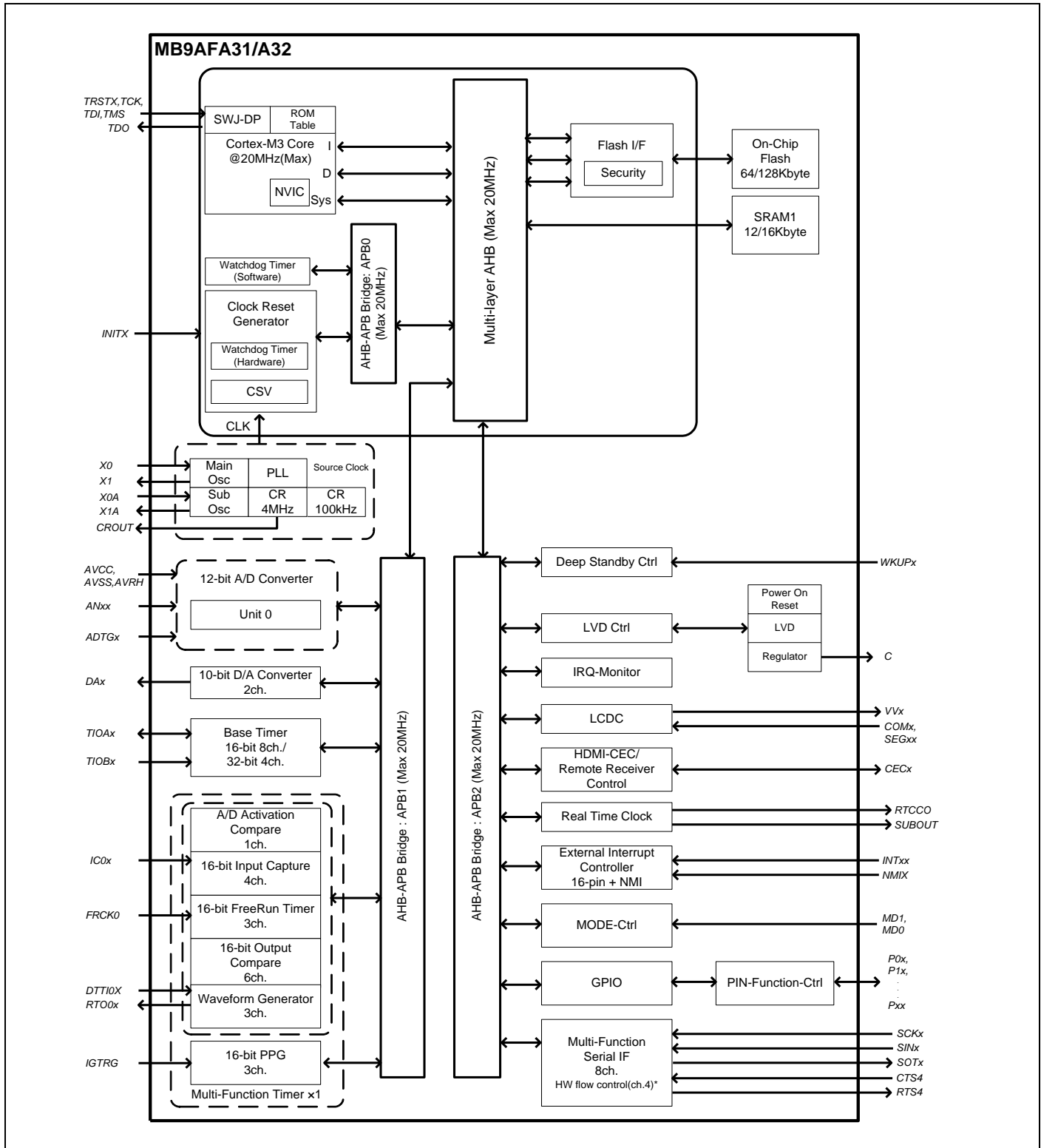
If an error is detected, retransmit the data.

Differences in features among the products with different memory sizes and between Flash memory products and MASK products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

**8. Block Diagram**



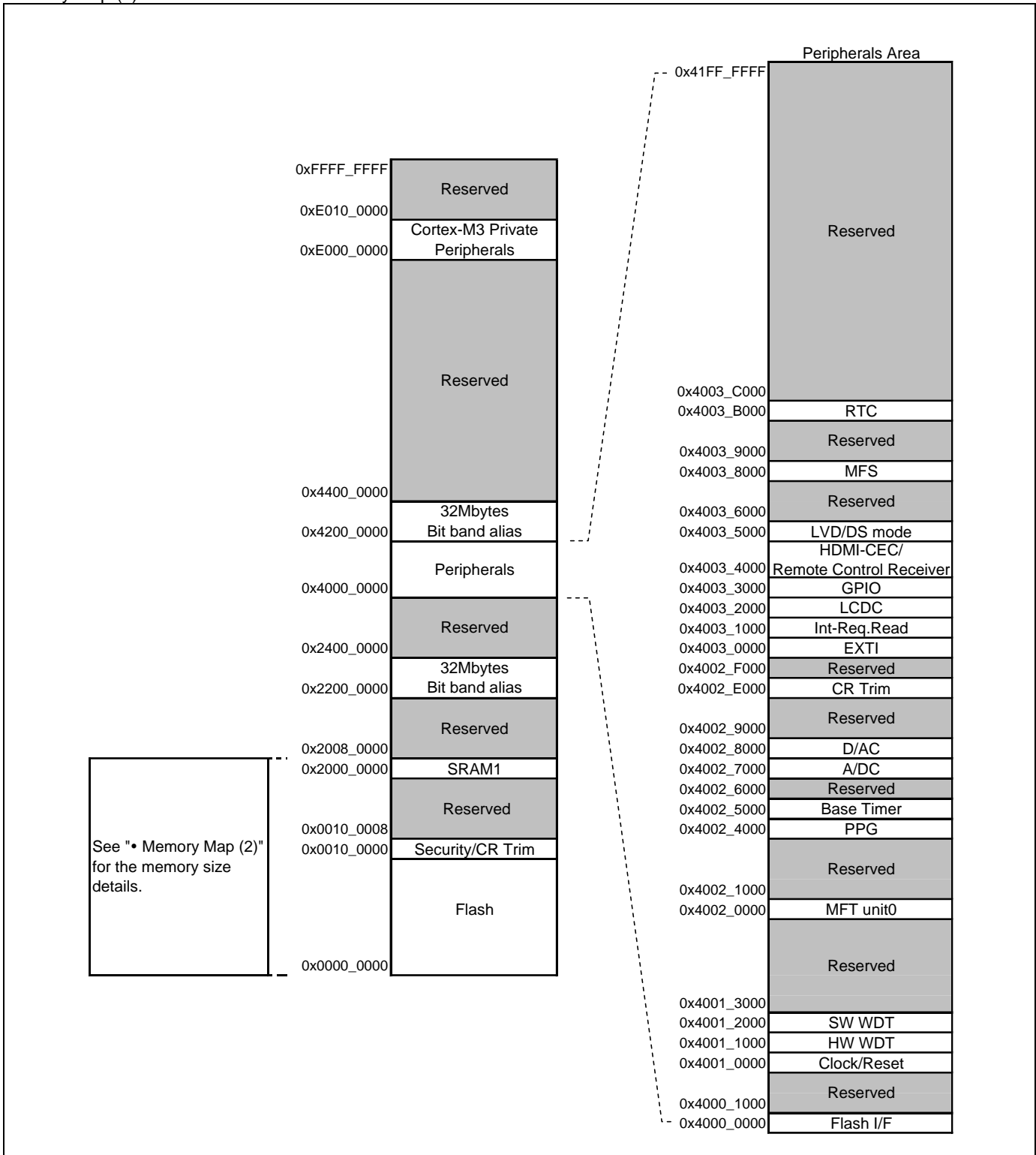
\*: For the MB9AFA31L and MB9AFA32L, Multi-function Serial Interface does not support hardware flow control in these products.

## 9. Memory Size

See Memory size in Product Lineup to confirm the memory size.

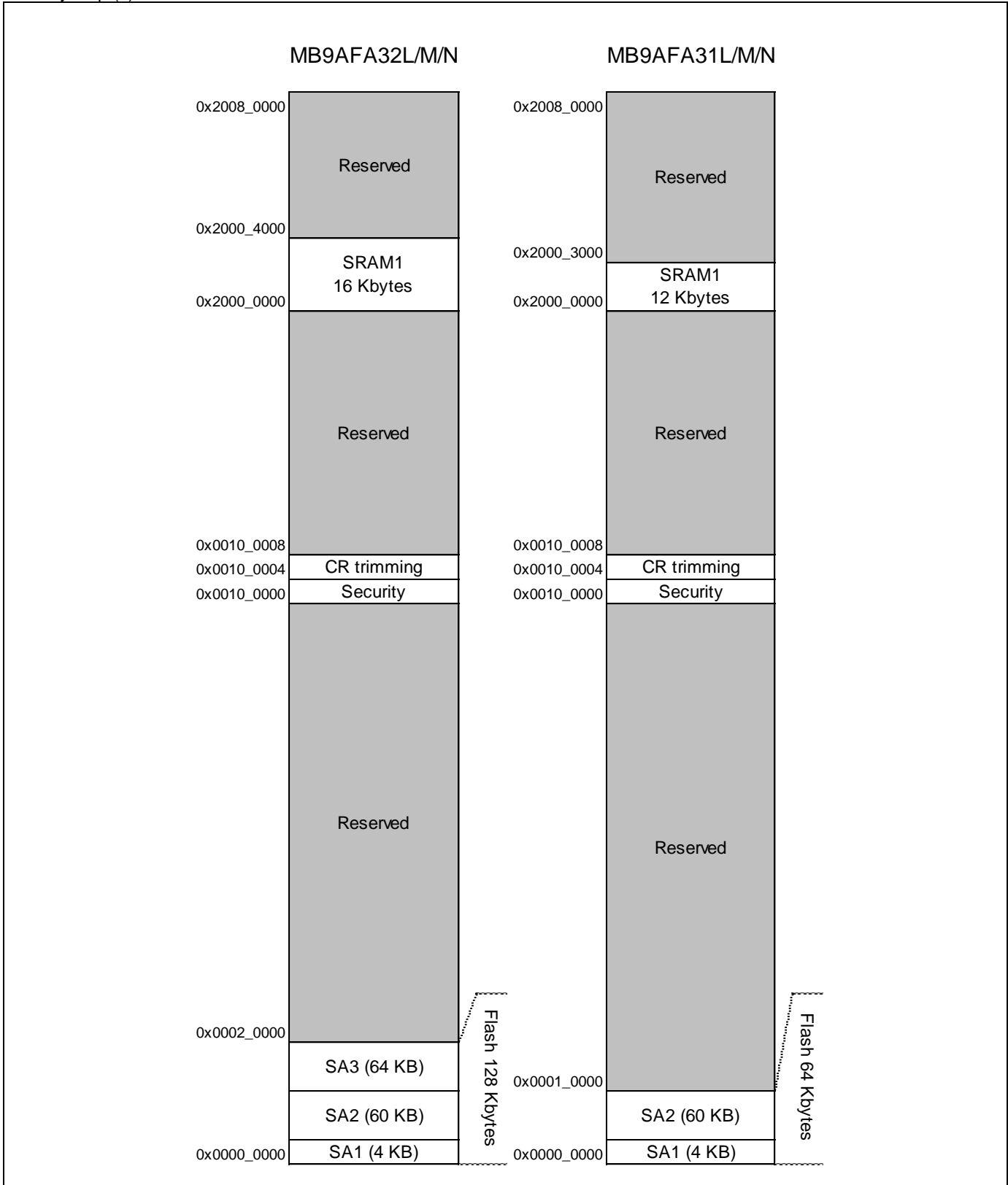
## 10. Memory Map

Memory Map (1)



See "• Memory Map (2)" for the memory size details.

## Memory Map (2)



\*: See MB9AAA0N/1A0N/A30N/130N/130L Series Flash Programming Manual to confirm the detail of Flash memory.

## Peripheral Address Map

Start address	End address	Bus	Peripherals	
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register	
0x4000_1000	0x4000_FFFF		Reserved	
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control	
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer	
0x4001_2000	0x4001_2FFF		Software Watchdog timer	
0x4001_3000	0x4001_4FFF		Reserved	
0x4001_5000	0x4001_5FFF		Reserved	
0x4001_6000	0x4001_FFFF		Reserved	
0x4002_0000	0x4002_0FFF		APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF	Reserved		
0x4002_2000	0x4002_3FFF	Reserved		
0x4002_4000	0x4002_4FFF	PPG		
0x4002_5000	0x4002_5FFF	Base Timer		
0x4002_6000	0x4002_6FFF	Reserved		
0x4002_7000	0x4002_7FFF	A/D Converter		
0x4002_8000	0x4002_8FFF	D/A Converter		
0x4002_9000	0x4002_DFFF	Reserved		
0x4002_E000	0x4002_EFFF	Built-in CR trimming		
0x4002_F000	0x4002_FFFF	Reserved		
0x4003_0000	0x4003_0FFF	APB2		External Interrupt
0x4003_1000	0x4003_1FFF			Interrupt Source Check Register
0x4003_2000	0x4003_2FFF		LCD Controller	
0x4003_3000	0x4003_3FFF		GPIO	
0x4003_4000	0x4003_4FFF		HDMI-CEC/ Remote Control Receiver	
0x4003_5000	0x4003_50FF		Low-Voltage Detector	
0x4003_5100	0x4003_5FFF		Deep standby mode Controller	
0x4003_6000	0x4003_6FFF		Reserved	
0x4003_7000	0x4003_7FFF		Reserved	
0x4003_8000	0x4003_8FFF		Multi-function serial	
0x4003_9000	0x4003_9FFF		Reserved	
0x4003_A000	0x4003_AFFF		Reserved	
0x4003_B000	0x4003_BFFF		Real-time clock	
0x4003_C000	0x4003_FFFF		Reserved	
0x4004_0000	0x4004_FFFF		AHB	Reserved
0x4005_0000	0x4005_FFFF	Reserved		
0x4006_0000	0x4006_0FFF	Reserved		
0x4006_1000	0x4006_1FFF	Reserved		
0x4006_2000	0x4006_2FFF	Reserved		
0x4006_3000	0x4006_3FFF	Reserved		
0x4006_4000	0x41FF_FFFF	Reserved		

## 11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

INITX = 0

This is the period when the INITX pin is the L level.

INITX = 1

This is the period when the INITX pin is the H level.

SPL = 0

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB\_CTL) is set to 0.

SPL = 1

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB\_CTL) is set to 1.

Input enabled

Indicates that the input function can be used.

Internal input fixed at 0

This is the status that the input function cannot be used. Internal input is fixed at L.

Hi-Z

Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

Setting disabled

Indicates that the setting is disabled.

Maintain previous state

Maintains the state that was immediately prior to entering the current mode.  
If a built-in peripheral function is operating, the output follows the peripheral function.  
If the pin is being used as a port, that output is maintained.

Analog input is enabled

Indicates that the analog input is enabled.

Trace output

Indicates that the trace function can be used.

GPIO selected

In Deep Standby mode, pins switch to the general-purpose I/O port.



List of Pin Status

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
A	Main crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state / When oscillation stops*1, output maintains previous state / Internal input fixed at 0	Hi-Z / Input enabled / When oscillation stops*1, Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state
B	Main crystal oscillator output pin	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z output / Internal input fixed at 0
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
E	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	Output maintain previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
F	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		
G	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled			Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected							Output maintains previous state / Internal input fixed at 0		

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state								
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable								
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1								
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-								
H	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected	Hi-Z / Internal input fixed at 0	GPIO selected								
	Internal input fixed at 0							Maintain previous state / Internal input fixed at 0										
I	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled								
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled				Maintain previous state			Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected			
	GPIO selected														Maintain previous state			
J	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled								
	Resource other than above selected										Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected	GPIO selected
	GPIO selected																Internal input fixed at 0	Internal input fixed at 0

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state		
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable		
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1		
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-		
K	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled		
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0		
	Resource other than above selected						Hi-Z / Internal input fixed at 0				Output maintains previous state / Internal input fixed at 0	
	GPIO selected						Output maintains previous state / Internal input fixed at 0					
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled		
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected Internal input fixed at 0		
	External interrupt enabled selected						Maintain previous state				Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0
	Resource other than above selected						Hi-Z / Internal input fixed at 0					
GPIO selected	Output maintains previous state / Internal input fixed at 0											

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
M	Sub crystal oscillator input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state / When oscillation stops*2, output maintains previous state / Internal input fixed at 0	Hi-Z / Input enabled / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, output maintains previous state / Internal input fixed at 0	Hi-Z / Input enabled / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When Return from Deep Standby STOP mode, GPIO is selected
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state
N	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
O	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0		Maintain previous state
P	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	Maintain previous state	Hi-Z / Input enabled	Maintain previous state
Q	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected							Output maintains previous state / Internal input fixed at 0		Maintain previous state

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-	
R	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected	
	External interrupt enabled selected						Maintain previous state	GPIO selected	Hi-Z / Internal input fixed at 0		
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0			
GPIO selected	Maintain previous state										
S	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected	Hi-Z / Internal input fixed at 0	GPIO selected	
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Hi-Z / Internal input fixed at 0				Output maintains previous state / Internal input fixed at 0
	GPIO selected										

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
T	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected Internal input fixed at 0
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled			Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0		Output maintains previous state / Internal input fixed at 0
	GPIO selected									
U	Resource selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0
	GPIO selected									
V	Resource selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0
	GPIO selected									



Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state	
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable	
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1	
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-	
W	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Hi-Z / Internal input fixed at 0				Output maintains previous state / Internal input fixed at 0
	GPIO selected						Hi-Z / Internal input fixed at 0				
X	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected	
	GPIO selected									Maintain previous state	

Pin status type	Function group	Power-on reset or low-voltage detection state	INITX input state	Device internal reset state	Run mode or Sleep mode state	Timer mode, RTC mode, or Stop mode state		Deep Standby RTC mode or Deep Standby Stop mode state		Return from Deep Standby mode state
		Power supply unstable	Power supply stable		Power supply stable	Power supply stable		Power supply stable		Power supply stable
		-	INITX = 0	INITX = 1	INITX = 1	INITX = 1		INITX = 1		INITX = 1
		-	-	-	-	SPL = 0	SPL = 1	SPL = 0	SPL = 1	-
Y	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*3	*4	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled		Maintain previous state				
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled		Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0			
	GPIO selected									
Z	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*3	*4	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled		Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0			
	GPIO selected									

\*1: Oscillation is stopped at Sub Run mode, Low-speed CR Run mode, Sub Sleep mode, Low-speed CR Sleep mode, Sub Timer mode, Low-speed CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

\*2: Oscillation is stopped at Stop mode and Deep Standby Stop mode.

\*3: Maintain previous state at Timer mode. GPIO selected Internal input fixed at 0 at RTC mode, Stop mode.

\*4: Maintain previous state at Timer mode. Hi-Z/Internal input fixed at 0 at RTC mode, Stop mode.

## 12. Electrical Characteristics

### 12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	V <sub>CC</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Analog power supply voltage*1,*3	AV <sub>CC</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Analog reference voltage*1,*3	AV <sub>RH</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
LCD input voltage*1,*3	V <sub>V4</sub> to V <sub>V0</sub>	V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	
Input voltage*1	V <sub>I</sub>	V <sub>SS</sub> - 0.5	V <sub>CC</sub> + 0.5 (≤ 6.5 V)	V	
		V <sub>SS</sub> - 0.5	V <sub>SS</sub> + 6.5	V	5 V tolerant
Analog pin input voltage*1	V <sub>IA</sub>	V <sub>SS</sub> - 0.5	AV <sub>CC</sub> + 0.5 (≤ 6.5 V)	V	
Output voltage*1	V <sub>O</sub>	V <sub>SS</sub> - 0.5	V <sub>CC</sub> + 0.5 (≤ 6.5 V)	V	
L level maximum output current*4	I <sub>OL</sub>	-	10	mA	
L level average output current*5	I <sub>OLAV</sub>	-	4	mA	
L level total maximum output current	∑I <sub>OL</sub>	-	100	mA	
L level total average output current*6	∑I <sub>OLAV</sub>	-	50	mA	
H level maximum output current*4	I <sub>OH</sub>	-	-10	mA	
H level average output current*5	I <sub>OHAV</sub>	-	-4	mA	
H level total maximum output current	∑I <sub>OH</sub>	-	-100	mA	
H level total average output current*6	∑I <sub>OHAV</sub>	-	-50	mA	
Power consumption	P <sub>D</sub>	-	400	mW	
Storage temperature	T <sub>STG</sub>	- 55	+ 150	°C	

\*1: These parameters are based on the condition that V<sub>SS</sub> = AV<sub>SS</sub> = 0 V.

\*2: V<sub>CC</sub> must not drop below V<sub>SS</sub> - 0.5 V.

\*3: Be careful not to exceed V<sub>CC</sub> + 0.5 V, for example, when the power is turned on.

\*4: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

\*5: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100 ms period.

\*6: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100 ms.

#### **WARNING:**

- Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.  
Do not exceed any of these ratings.

**12.2 Recommended Operating Conditions**

 (V<sub>SS</sub> = AV<sub>SS</sub> = 0.0V)

Parameter	Symbol	Conditions	Value		Unit	Remarks	
			Min	Max			
Power supply voltage	V <sub>CC</sub>	-	1.8	5.5	V	*1	
			2.2	5.5		*2	
LCD input voltage	V <sub>V4</sub>	-	2.2	V <sub>CC</sub>	V		
Analog power supply voltage	AV <sub>CC</sub>	-	1.8	5.5	V	AV <sub>CC</sub> = V <sub>CC</sub>	
Analog reference voltage	AV <sub>RH</sub>	-	2.7	AV <sub>CC</sub>	V	AV <sub>CC</sub> ≥ 2.7 V	
			AV <sub>CC</sub>			AV <sub>CC</sub> < 2.7 V	
Smoothing capacitor	C <sub>S</sub>	-	1	10	μF	For built-in Regulator *3	
Operating Temperature	LQD064, LQG064, VNC064, LQH080, LQJ080, LQI100, PQH100	T <sub>A</sub>	-	- 40	+ 85	°C	

\*1: When LCD is not used

\*2: When LCD is used

\*3: See "C Pin" in Handling Devices for the smoothing capacitor.

**WARNING:**

- The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions. Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

**12.3 DC Characteristics**
**12.3.1 Current Rating**

 (V<sub>CC</sub> = AV<sub>CC</sub> = 1.8V to 5.5V, V<sub>SS</sub> = AV<sub>SS</sub> = 0V, T<sub>A</sub> = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks	
				Typ* <sup>3</sup>	Max* <sup>4</sup>			
Power supply current	I <sub>CC</sub>	VCC	PLL Run mode	CPU: 20 MHz, Peripheral: 20 MHz, Flash memory 0 Wait, FRWTR.RWT = 00, FSYNDN.SD = 000	19	24	mA	*1, *5
				CPU: 20 MHz, Peripheral: clock stopped, NOP operation	9.5	12.5	mA	*1, *5
			High-speed CR Run mode	CPU/Peripheral: 4 MHz* <sup>2</sup> Flash memory 0 Wait FRWTR.RWT = 00 FSYNDN.SD = 000	4.5	5.5	mA	*1
			Sub Run mode	CPU/Peripheral: 32 kHz, Flash memory 0 Wait, FRWTR.RWT = 00, FSYNDN.SD = 000	0.25	0.55	mA	*1, *6
			Low-speed CR Run mode	CPU/Peripheral: 100 kHz, Flash memory 0 Wait, FRWTR.RWT = 00, FSYNDN.SD = 000	0.3	0.95	mA	*1
	I <sub>CCS</sub>		PLL Sleep mode	Peripheral: 20 MHz	8	10.5	mA	*1, *5
			High-speed CR Sleep mode	Peripheral: 4 MHz* <sup>2</sup>	2	2.5	mA	*1
			Sub Sleep mode	Peripheral: 32 kHz	0.2	0.45	mA	*1, *6
			Low-speed CR Sleep mode	Peripheral: 100 kHz	0.25	0.65	mA	*1

\*1: When all ports are fixed.

\*2: When setting it to 4 MHz by trimming.

 \*3: T<sub>A</sub>=+25°C, V<sub>CC</sub>=3.3 V

 \*4: T<sub>A</sub>=+85°C, V<sub>CC</sub>=5.5 V

\*5: When using the crystal oscillator of 4 MHz (Including the current consumption of the oscillation circuit)

\*6: When using the crystal oscillator of 32 kHz (Including the current consumption of the oscillation circuit)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks	
				Typ <sup>*2</sup>	Max <sup>*3</sup>			
Power supply current	I <sub>CC</sub> T	VCC	Main Timer mode	T <sub>A</sub> = + 25°C, When LVD is off	0.9	3.3	mA	*1, *4
				T <sub>A</sub> = + 85°C, When LVD is off	1.5	3.5	mA	*1, *4
			Sub Timer mode	T <sub>A</sub> = + 25°C, When LVD is off	7.5	60	μA	*1, *5
				T <sub>A</sub> = + 85°C, When LVD is off	16	150	μA	*1, *5
	I <sub>CC</sub> R		RTC mode	T <sub>A</sub> = + 25°C, When LVD is off	1.5	6.5	μA	*1, *5
				T <sub>A</sub> = + 85°C, When LVD is off	6	89	μA	*1, *5
	I <sub>CC</sub> H		Stop mode	T <sub>A</sub> = + 25°C, When LVD is off	0.6	5	μA	*1
				T <sub>A</sub> = + 85°C, When LVD is off	4.2	87	μA	*1
	I <sub>CC</sub> RD		Deep Standby RTC mode	T <sub>A</sub> = + 25°C, When LVD is off	1.3	4.5	μA	*1, *5
				T <sub>A</sub> = + 85°C, When LVD is off	3	32	μA	*1, *5
	I <sub>CC</sub> HD		Deep Standby Stop mode	T <sub>A</sub> = + 25°C, When LVD is off	0.4	3	μA	*1
				T <sub>A</sub> = + 85°C, When LVD is off	1.4	30	μA	*1

\*1: When all ports are fixed.

\*2: V<sub>CC</sub>=3.3 V

\*3: V<sub>CC</sub>=5.5 V

\*4: When using the crystal oscillator of 4 MHz(Including the current consumption of the oscillation circuit)

\*5: When using the crystal oscillator of 32 kHz(Including the current consumption of the oscillation circuit)

## Low Voltage Detection Current

 ( $V_{CC} = AV_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ*	Max		
Low-voltage detection circuit (LVD) power supply current	I <sub>CC</sub> LVD	VCC	For occurrence of reset or for occurrence of interrupt in normal mode operation	10	20	μA	When not detected
			For occurrence of reset and for occurrence of interrupt in normal mode operation	14	30	μA	
			For occurrence of interrupt in low-power mode operation	0.3	2	μA	When not detected

 \*: When  $V_{CC}=3.3 \text{ V}$ 

## Flash Memory Current

 ( $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	I <sub>CC</sub> FLASH	VCC	At Write/Erase	10.8	11.9	mA	

## A/D Converter Current

 ( $V_{CC} = AV_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I <sub>CC</sub> AD	AVCC	At 1unit operation	1.4	2.5	mA	
			At stop	0.1	0.35	μA	
Reference power supply current	I <sub>CC</sub> AVRH	AVRH	At 1unit operation AVRH=5.5 V	0.5	1.5	mA	
			At stop	0.1	0.3	μA	

## D/A Converter Current

 ( $V_{CC} = AV_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I <sub>DDA</sub>	AVCC	At D/A 1ch. operation AV <sub>CC</sub> =3.3 V	314	440	μA	*1, *2
			At D/A 1ch. operation AV <sub>CC</sub> =5.0 V	476	670	μA	*1, *2
	I <sub>DSA</sub>		At D/A stop	-	1.0	μA	*1

\*1: No-load

\*2: Generates the max current by the CODE about 0x200

**12.3.2 Pin Characteristics**
 $(V_{CC} = AV_{CC} = 1.8V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +85^{\circ}C)$ 

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	$V_{IHS}$	MD0, MD1 PE0, PE2, PE3, P46, P47, P3A, P3B, P3C, P3D, P3E, P3F, INITX	-	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
		P0A, P0B, P0C, P4C, P60, P80, P81, P82	-	$V_{CC} \times 0.7$	-	$V_{SS} + 5.5$	V	5V tolerant
		CMOS hysteresis input pins other than the above	-	$V_{CC} \times 0.7$	-	$V_{CC} + 0.3$	V	
L level input voltage (hysteresis input)	$V_{ILS}$	MD0, MD1 PE0, PE2, PE3, P46, P47, INITX	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
		CMOS hysteresis input pins other than the above	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.3$	V	
H level output voltage	$V_{OH}$	Pxx	$V_{CC} \geq 4.5 V,$ $I_{OH} = -4 \text{ mA}$ $V_{CC} < 4.5 V,$ $I_{OH} = -1 \text{ mA}$	$V_{CC} - 0.5$	-	$V_{CC}$	V	
L level output voltage	$V_{OL}$	Pxx	$V_{CC} \geq 4.5 V,$ $I_{OL} = 4 \text{ mA}$ $V_{CC} < 4.5 V,$ $I_{OL} = 2 \text{ mA}$	$V_{SS}$	-	0.4	V	
Input leak current	$I_{IL}$	-	-	-5	-	+5	$\mu A$	
		CEC0, CEC1	$V_{CC} = AV_{CC} =$ $AVRH = V_{SS}$ $= AV_{SS} = 0.0$ V	-	-	+1.8		
Pull-up resistor value	$R_{PU}$	Pull-up pin	$V_{CC} \geq 4.5 V$	25	50	100	k $\Omega$	
			$V_{CC} < 4.5 V$	40	100	400		
Input capacitance	$C_{IN}$	Other than VCC, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	



**12.3.3 LCD Characteristics**
 $(V_{CC} = 2.2V \text{ to } 5.5V, V_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +85^{\circ}C)$ 

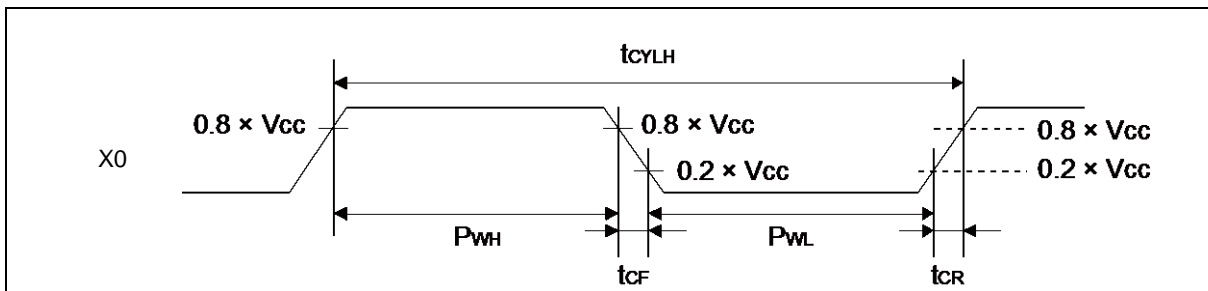
Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
VV0 to VV3 Output voltage (1/4 bias)	V <sub>V0</sub>	VV0	When using internal dividing register	0	-	V <sub>V4</sub> × 5%	V	
	V <sub>V1</sub>	VV1		V <sub>V4</sub> × 1/4 -10%	-	V <sub>V4</sub> × 1/4 +10%		
	V <sub>V2</sub>	VV2		V <sub>V4</sub> × 1/2 -10%	-	V <sub>V4</sub> × 1/2 +10%		
	V <sub>V3</sub>	VV3		V <sub>V4</sub> × 3/4 -10%	-	V <sub>V4</sub> × 3/4 +10%		
VV0 to VV3 Output voltage (1/3 bias)	V <sub>V0</sub>	VV0	When using internal dividing register	0	-	V <sub>V4</sub> × 5%	V	
	V <sub>V1</sub>	VV1		V <sub>V4</sub> × 1/3 -10%	-	V <sub>V4</sub> × 1/3 +10%		
	V <sub>V2</sub>	VV2		V <sub>V4</sub> × 2/3 -10%	-	V <sub>V4</sub> × 2/3 +10%		
	V <sub>V3</sub>	VV3		V <sub>V4</sub> × 2/3 -10%	-	V <sub>V4</sub> × 2/3 +10%		
VV0 to VV3 Output voltage (1/2 bias)	V <sub>V0</sub>	VV0	When using internal dividing register	0	-	V <sub>V4</sub> × 5%	V	
	V <sub>V1</sub>	VV1		V <sub>V4</sub> × 1/2 -10%	-	V <sub>V4</sub> × 1/2 +10%		
	V <sub>V2</sub>	VV2		V <sub>V4</sub> × 1/2 -10%	-	V <sub>V4</sub> × 1/2 +10%		
	V <sub>V3</sub>	VV3		V <sub>V4</sub> × 1/2 -10%	-	V <sub>V4</sub> × 1/2 +10%		
VV4 Active current (1/4 bias)	I <sub>R100K</sub>	VV4	When using 100 kΩ internal dividing register	-	15	35	μA	
	I <sub>R10K</sub>	VV4	When using 10 kΩ internal dividing register	-	130	250	μA	
VV4 Active current (1/3 bias)	I <sub>R100K</sub>	VV4	When using 100 kΩ internal dividing register	-	18	45	μA	
	I <sub>R10K</sub>	VV4	When using 10 kΩ internal dividing register	-	170	350	μA	
VV4 Active current (1/2 bias)	I <sub>R100K</sub>	VV4	When using 100 kΩ internal dividing register	-	27	75	μA	
	I <sub>R10K</sub>	VV4	When using 10 kΩ internal dividing register	-	250	500	μA	
VV4 Static current	I <sub>off_vv4</sub>	VV4	When LCD stops	-	-	0.5	μA	
VV0 Output Voltage in using external resistor	V <sub>V0E</sub>	VV0	I <sub>OL</sub> =1mA	-	-	1.0	V	

**12.4 AC Characteristics**
**12.4.1 Main Clock Input Characteristics**
 $(V_{CC} = 1.8V \text{ to } 5.5V, V_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +85^{\circ}C)$ 

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks	
				Min	Max			
Input frequency	$f_{CH}$	X0, X1	$V_{CC} \geq 2.0 V$	4	20	MHz	When crystal oscillator is connected	
			$V_{CC} < 2.0 V$	4	4	MHz		
			$V_{CC} \geq 4.5 V$	4	20	MHz	When using external clock	
			$V_{CC} < 4.5 V$	4	16	MHz		
Input clock cycle	$t_{CYLH}$		$V_{CC} \geq 4.5 V$	50	250	ns	When using external clock	
			$V_{CC} < 4.5 V$	62.5	250	ns		
Input clock pulse width	-			$P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}$	45	55	%	When using external clock
Input clock rising time and falling time	$t_{CF}, t_{CR}$			-	-	5	ns	When using external clock
	$f_{CM}$	-	-	-	20	MHz	Master clock	
	$f_{CC}$	-	-	-	20	MHz	Base clock (HCLK/FCLK)	
	$f_{CP0}$	-	-	-	20	MHz	APB0 bus clock*2	
	$f_{CP1}$	-	-	-	20	MHz	APB1 bus clock*2	
	$f_{CP2}$	-	-	-	20	MHz	APB2 bus clock*2	
Internal operating clock*1 cycle time	$t_{CYCC}$	-	-	50	-	ns	Base clock (HCLK/FCLK)	
	$t_{CYCP0}$	-	-	50	-	ns	APB0 bus clock*2	
	$t_{CYCP1}$	-	-	50	-	ns	APB1 bus clock*2	
	$t_{CYCP2}$	-	-	50	-	ns	APB2 bus clock*2	

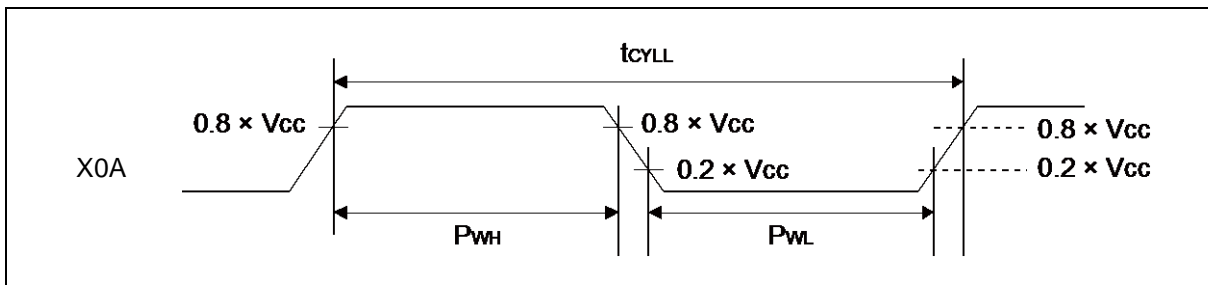
\*1: For more information about each internal operating clock, see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

\*2: For about each APB bus which each peripheral is connected to, see Block Diagram in this data sheet.



**12.4.2 Sub Clock Input Characteristics**
 $(V_{CC} = 1.8V \text{ to } 5.5V, V_{SS} = 0V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$f_{CL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100		kHz
Input clock cycle	$t_{CYLL}$		-	10	-	31.25	$\mu s$	When using external clock
Input clock pulse width	-		$P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}$	45	-	55	%	When using external clock


**12.4.3 Built-in CR Oscillation Characteristics**

Built-in High-speed CR

 $(V_{CC} = 1.8V \text{ to } 5.5V, V_{SS} = 0V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Conditions	Value			Unit	Remarks	
			Min	Typ	Max			
Clock frequency	$f_{CRH}$	$V_{CC} \geq 2.2V$	$T_A = +25^\circ C$	3.92	4	4.08	MHz	When trimming*1
			$T_A = -40^\circ C \text{ to } +85^\circ C$	3.8	4	4.2		
			$T_A = -40^\circ C \text{ to } +85^\circ C$	2.3	-	7.03		When not trimming
		$V_{CC} < 2.2V$	$T_A = +25^\circ C$	3.4	4	4.6	MHz	When trimming*1
			$T_A = -40^\circ C \text{ to } +85^\circ C$	3.16	4	4.84		
			$T_A = -40^\circ C \text{ to } +85^\circ C$	2.3	-	7.03		When not trimming
Frequency stabilization time	$t_{CRWT}$	-	-	-	10	$\mu s$	*2	

\*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming.

\*2: This is the time to stabilize the frequency of High-speed CR clock after setting trimming value. This period is able to use High-speed CR clock as source clock.

Built-in Low-speed CR

 $(V_{CC} = 1.8V \text{ to } 5.5V, V_{SS} = 0V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_{CRL}$	-	50	100	150	kHz	

**12.4.4 Operating Conditions of Main PLL (In the case of using main clock for input of PLL)**
*(V<sub>CC</sub> = 1.8V to 5.5V, V<sub>SS</sub> = 0V, T<sub>A</sub> = - 40°C to + 85°C)*

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* <sup>1</sup> (LOCK UP time)	t <sub>LOCK</sub>	200	-	-	μs	
PLL input clock frequency	f <sub>PLLI</sub>	4	-	20	MHz	
PLL multiplication rate	-	1	-	5	multiplier	
PLL macro oscillation clock frequency	f <sub>PLLO</sub>	10	-	20	MHz	
Main PLL clock frequency* <sup>2</sup>	f <sub>CLKPLL</sub>	-	-	20	MHz	

\*1: Time from when the PLL starts operating until the oscillation stabilizes.

\*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

**12.4.5 Operating Conditions of Main PLL (In the case of using the built-in High-speed CR for the input clock of the Main PLL)**
*(V<sub>CC</sub> = 2.2V to 5.5V, V<sub>SS</sub> = 0V, T<sub>A</sub> = - 40°C to + 85°C)*

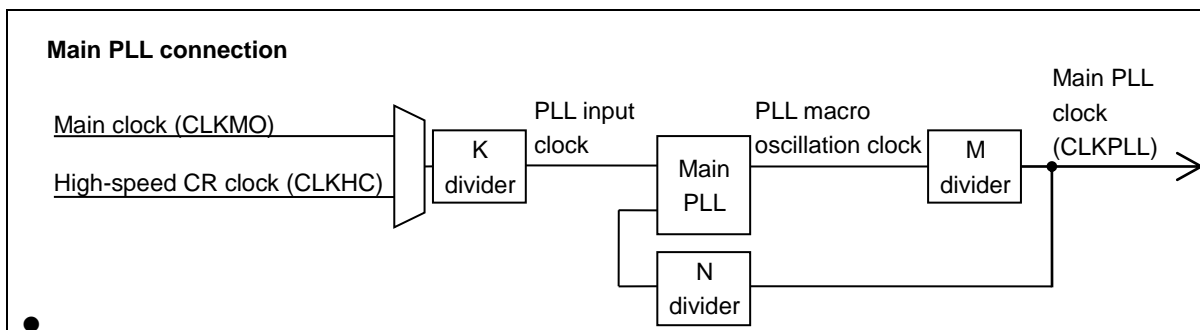
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* <sup>1</sup> (LOCK UP time)	t <sub>LOCK</sub>	200	-	-	μs	
PLL input clock frequency	f <sub>PLLI</sub>	3.8	4	4.2	MHz	
PLL multiplication rate	-	3	-	4	multiplier	
PLL macro oscillation clock frequency	f <sub>PLLO</sub>	11.4	-	16.8	MHz	
Main PLL clock frequency* <sup>2</sup>	f <sub>CLKPLL</sub>	-	-	16.8	MHz	

\*1: Time from when the PLL starts operating until the oscillation stabilizes.

\*2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM3 Family Peripheral Manual.

**Note:**

- Make sure to input to the Main PLL source clock, the High-speed CR clock (CLKHC) that the frequency has been trimmed. When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

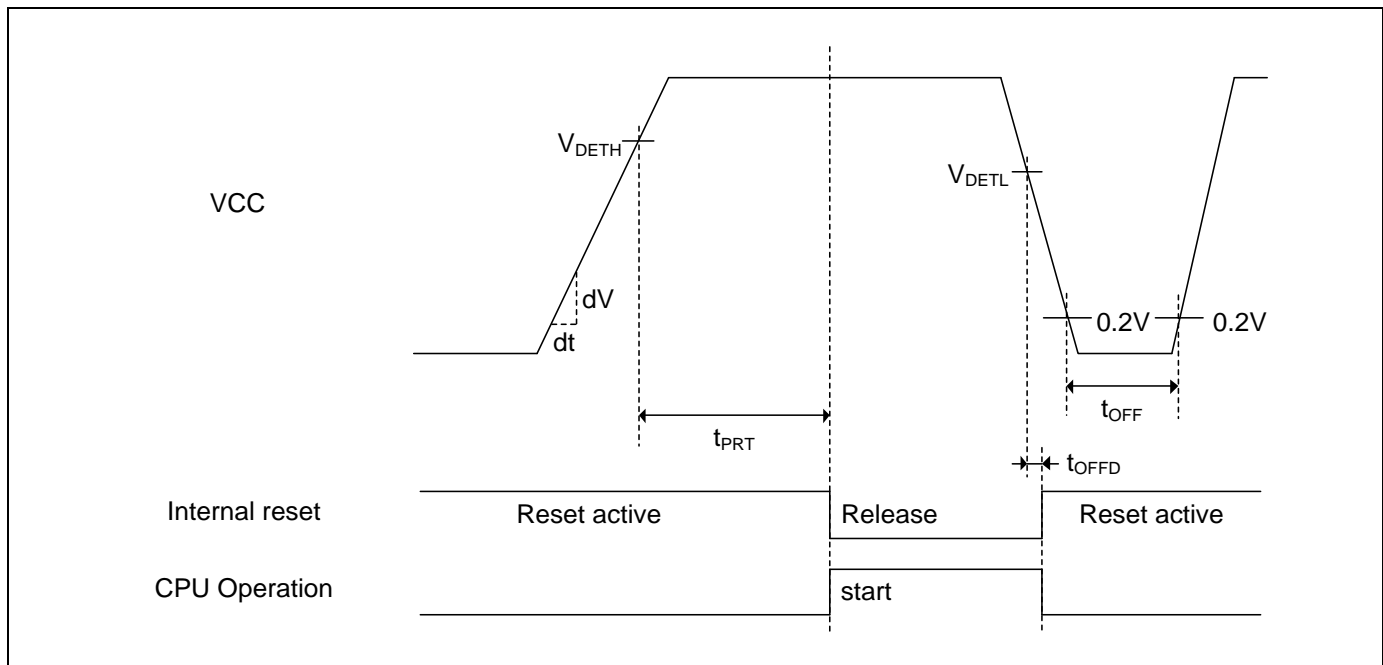


**12.4.6 Reset Input Characteristics**
 $(V_{CC} = 1.8V \text{ to } 5.5V, V_{SS} = 0V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	$t_{INITX}$	INITX	-	500	-	ns	
				1.5	-	ms	When RTC mode or Stop mode
				1.5	-	ms	When Deep Standby mode

**12.4.7 Power-on Reset Timing**
 $(V_{CC} = 1.8V \text{ to } 5.5V, V_{SS} = 0V, T_A = -40^\circ C \text{ to } +85^\circ C)$ 

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply rising time	$dV/dt$	VCC	0.1	-	-	V/ms	
Power supply shut down time	$t_{OFF}$		1	-	-	ms	
Reset release voltage	$V_{DETH}$		1.44	1.60	1.76	V	When voltage rises
Reset detection voltage	$V_{DETL}$		1.39	1.55	1.71	V	When voltage drops
Time until releasing Power-on reset	$t_{PRT}$		0.46	-	11.4	ms	$dV/dt \geq 0.1 \text{ mV}/\mu\text{s}$
Reset detection delay time	$t_{OFFD}$		-	-	0.4	ms	$dV/dt \geq -0.04 \text{ mV}/\mu\text{s}$

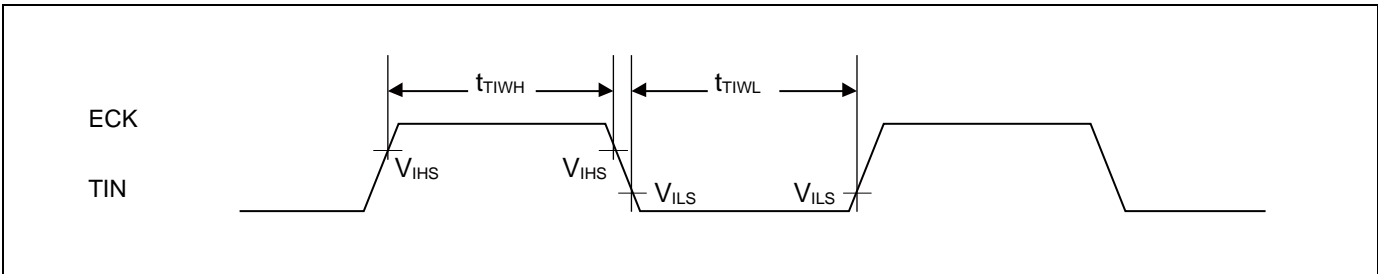


### 12.4.8 Base Timer Input Timing

Timer input timing

( $V_{CC} = 1.8V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

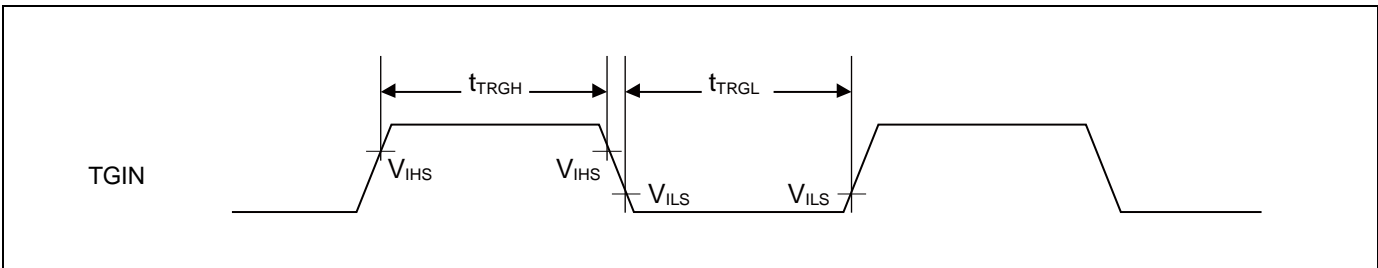
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$ , $t_{TIWL}$	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger input timing

( $V_{CC} = 1.8V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$ , $t_{TRGL}$	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



**Note:**

- $t_{CYCP}$  indicates the APB bus clock cycle time.
- About the APB bus number which the Base Timer is connected to, see Block Diagram in this data sheet.

**12.4.9 CSIO/UART Timing**

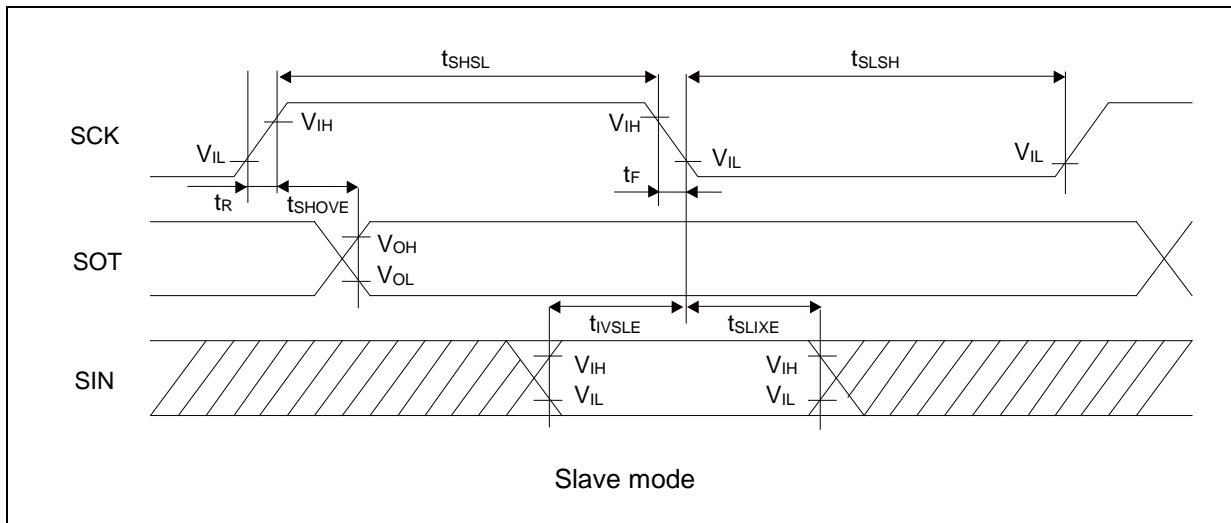
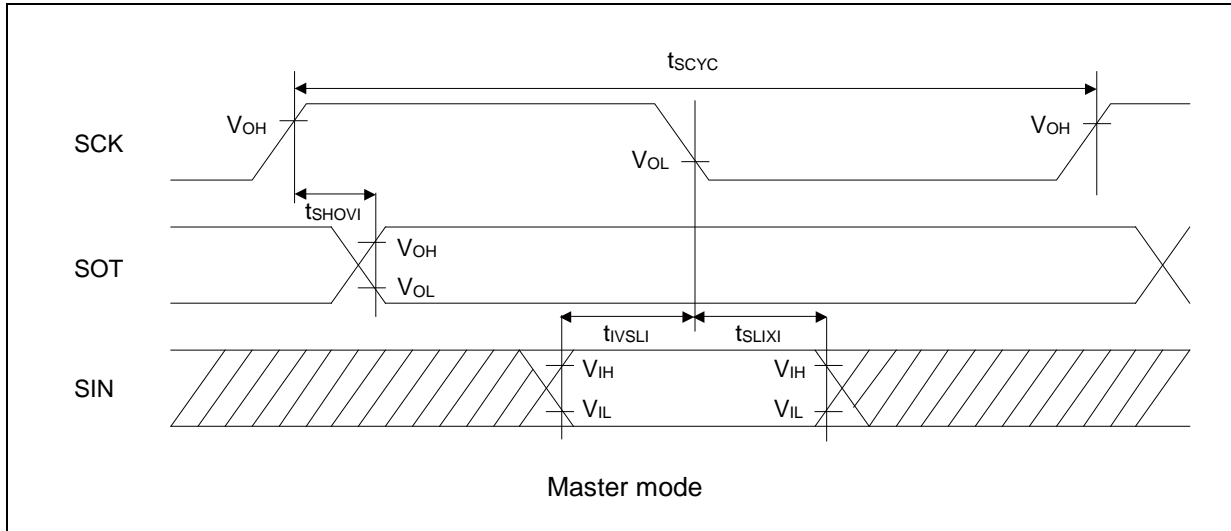
CSIO (SPI = 0, SCINV = 0)

 ( $V_{CC} = 1.8V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	$V_{CC} < 2.7 V$		$2.7 V \leq V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
				Min	Max	Min	Max	Min	Max	
Baud rate	-	-	-	-	5	-	5	-	5	Mbps
Serial clock cycle time	$t_{SCYC}$	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCKx , SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	$t_{IVSHI}$	SCKx , SINx		75	-	50	-	30	-	ns
SCK ↑ → SIN hold time	$t_{SHIXI}$	SCKx , SINx		0	-	0	-	0	-	ns
Serial clock L pulse width	$t_{LSLH}$	SCKx	Slave mode	$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	ns
Serial clock H pulse width	$t_{SHSL}$	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCKx , SOTx		-	75	-	50	-	30	ns
SIN → SCK ↑ setup time	$t_{IVSHE}$	SCKx , SINx		10	-	10	-	10	-	ns
SCK ↑ → SIN hold time	$t_{SHIXE}$	SCKx , SINx		20	-	20	-	20	-	ns
SCK falling time	$t_F$	SCKx		-	5	-	5	-	5	ns
SCK rising time	$t_R$	SCKx		-	5	-	5	-	5	ns

**Notes:**

- The above characteristics apply to clock synchronous mode.
- $t_{CYCP}$  indicates the APB bus clock cycle time.  
About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance  $C_L = 50 pF$ .





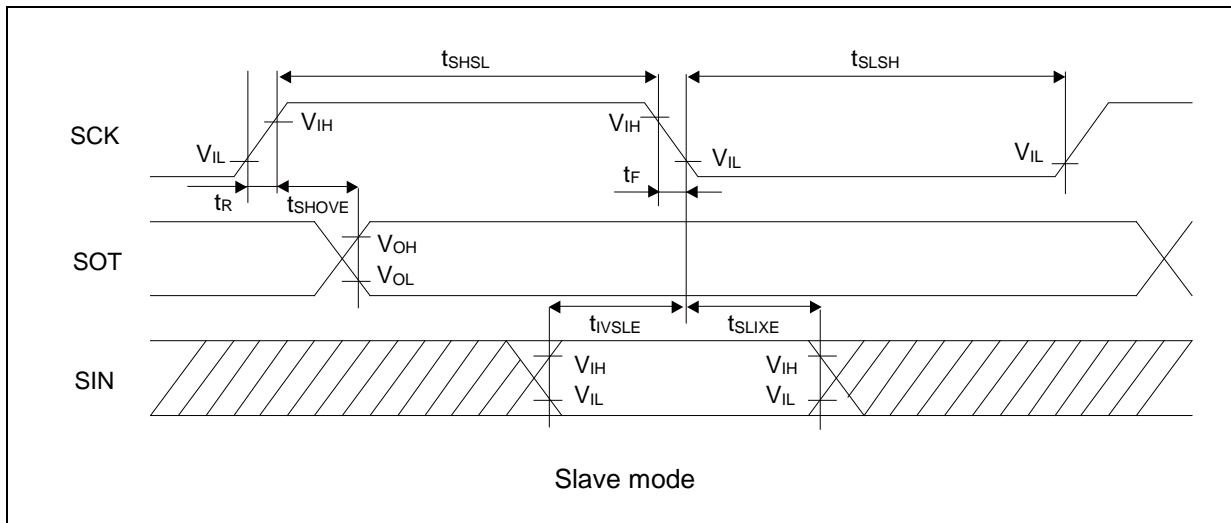
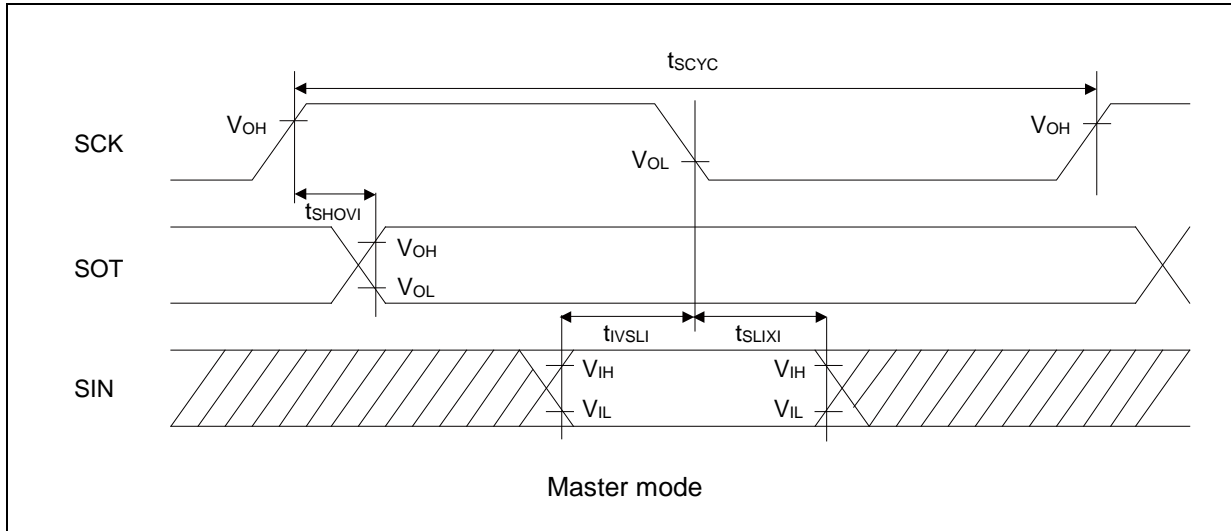
CSIO (SPI = 0, SCINV = 1)

 ( $V_{CC} = 1.8V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	$V_{CC} < 2.7 V$		$2.7 V \leq V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
				Min	Max	Min	Max	Min	Max	
Baud rate	-	-	-	-	5	-	5	-	5	Mbps
Serial clock cycle time	$t_{SCYC}$	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLI}$	SCKx, SINx		75	-	50	-	30	-	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXI}$	SCKx, SINx		0	-	0	-	0	-	ns
Serial clock L pulse width	$t_{SLSH}$	SCKx	Slave mode	$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	ns
Serial clock H pulse width	$t_{SHSL}$	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVE}$	SCKx, SOTx		-	75	-	50	-	30	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLE}$	SCKx, SINx		10	-	10	-	10	-	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXE}$	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	$t_F$	SCKx		-	5	-	5	-	5	ns
SCK rising time	$t_R$	SCKx	-	5	-	5	-	5	ns	

**Notes:**

- The above characteristics apply to clock synchronous mode.
- $t_{CYCP}$  indicates the APB bus clock cycle time.  
About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance  $C_L = 50$  pF.



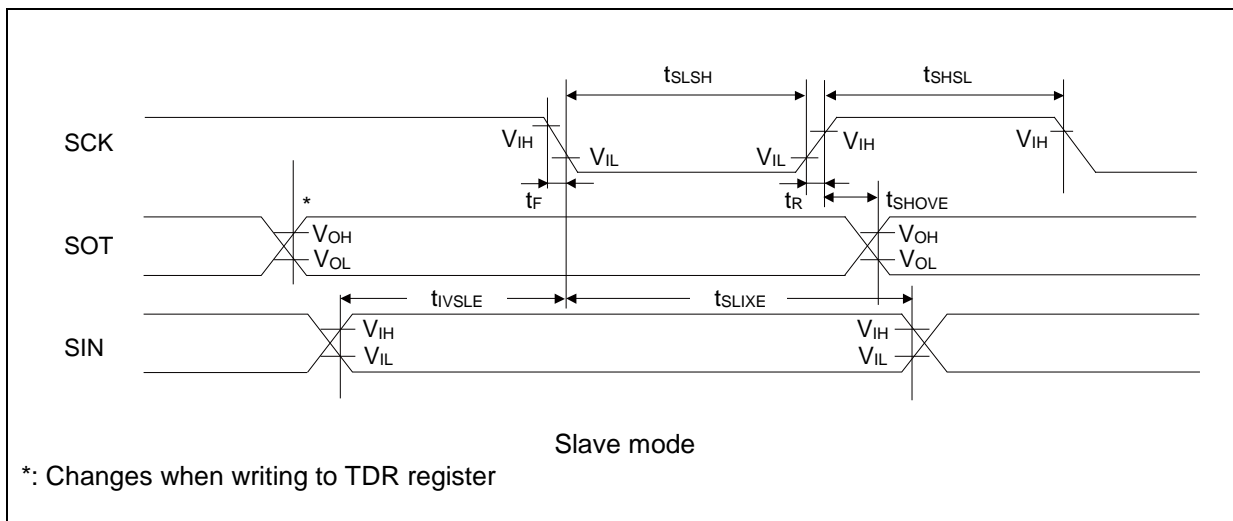
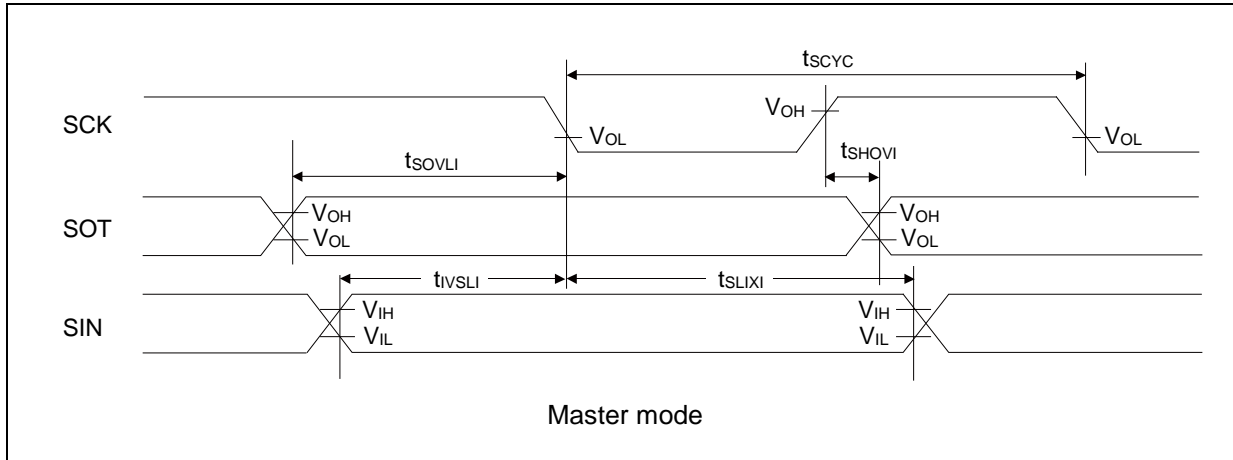
CSIO (SPI = 1, SCINV = 0)

 ( $V_{CC} = 1.8V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	$V_{CC} < 2.7 V$		$2.7 V \leq V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
				Min	Max	Min	Max	Min	Max	
Baud rate	-	-	-	-	5	-	5	-	5	Mbps
Serial clock cycle time	$t_{SCYC}$	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLI}$	SCKx, SINx		75	-	50	-	30	-	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXI}$	SCKx, SINx		0	-	0	-	0	-	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	$t_{SOVLI}$	SCKx, SOTx		$2t_{CYCP} - 30$	-	$2t_{CYCP} - 30$	-	$2t_{CYCP} - 30$	-	ns
Serial clock L pulse width	$t_{LSLH}$	SCKx		$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	ns
Serial clock H pulse width	$t_{SHSL}$	SCKx	$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns	
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVE}$	SCKx, SOTx	Slave mode	-	75	-	50	-	30	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLE}$	SCKx, SINx		10	-	10	-	10	-	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXE}$	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	$t_F$	SCKx		-	5	-	5	-	5	ns
SCK rising time	$t_R$	SCKx		-	5	-	5	-	5	ns

**Notes:**

- The above characteristics apply to clock synchronous mode.
- $t_{CYCP}$  indicates the APB bus clock cycle time.  
About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance  $C_L = 50$  pF.



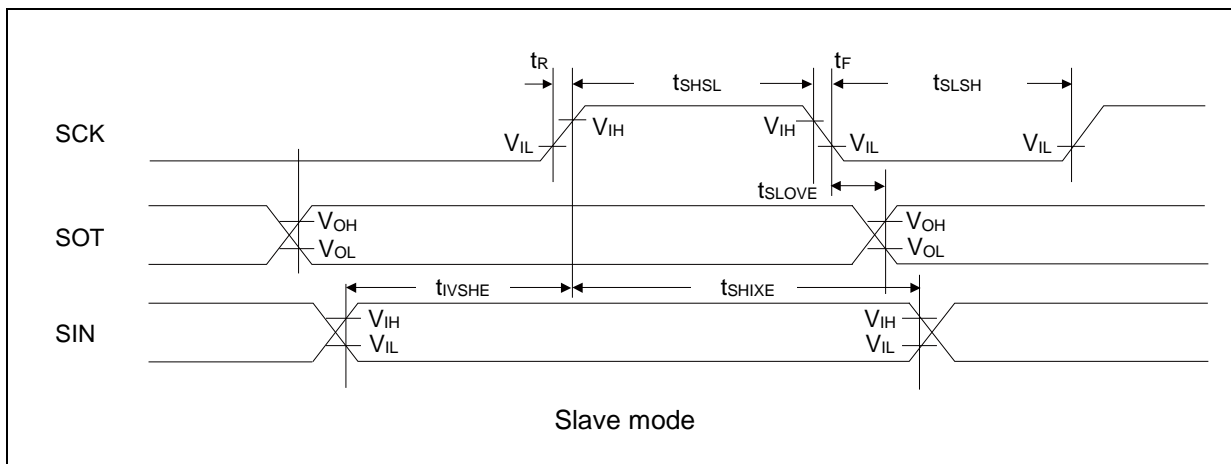
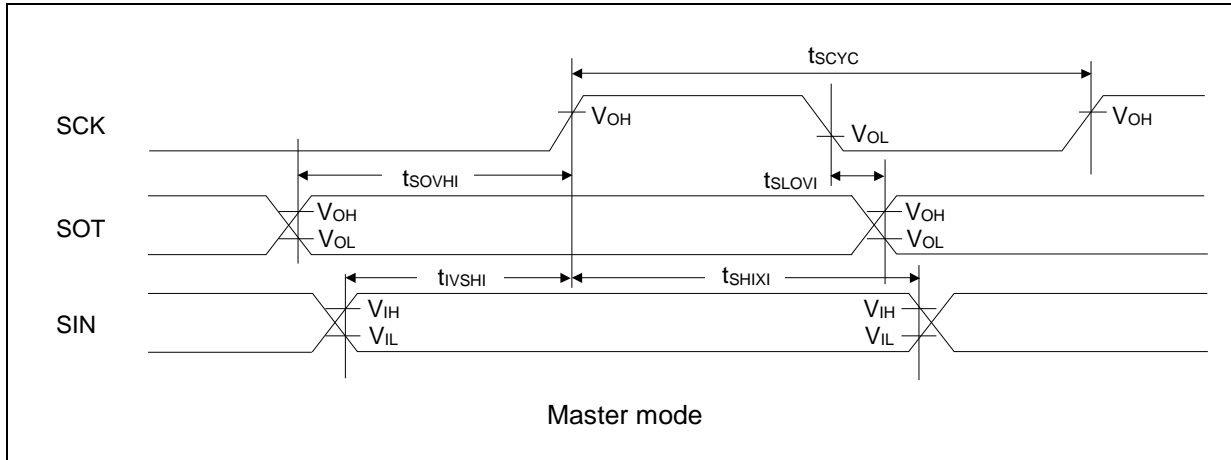
CSIO (SPI = 1, SCINV = 1)

 ( $V_{CC} = 1.8V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Parameter	Symbol	Pin name	Conditions	$V_{CC} < 2.7 V$		$2.7 V \leq V_{CC} < 4.5 V$		$V_{CC} \geq 4.5 V$		Unit
				Min	Max	Min	Max	Min	Max	
Baud rate	-	-	-	-	5	-	5	-	5	Mbps
Serial clock cycle time	$t_{SCYC}$	SCKx	Master mode	$4t_{CYCP}$	-	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCKx, SOTx		-40	+40	-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	$t_{IVSHI}$	SCKx, SINx		75	-	50	-	30	-	ns
SCK ↑ → SIN hold time	$t_{SHIXI}$	SCKx, SINx		0	-	0	-	0	-	ns
SOT → SCK ↑ delay time	$t_{SOVHI}$	SCKx, SOTx		$2t_{CYCP} - 30$	-	$2t_{CYCP} - 30$	-	$2t_{CYCP} - 30$	-	ns
Serial clock L pulse width	$t_{LSLH}$	SCKx		$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	$2t_{CYCP} - 10$	-	ns
Serial clock H pulse width	$t_{HSLH}$	SCKx	$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns	
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCKx, SOTx	Slave mode	-	75	-	50	-	30	ns
SIN → SCK ↑ setup time	$t_{IVSHE}$	SCKx, SINx		10	-	10	-	10	-	ns
SCK ↑ → SIN hold time	$t_{SHIXE}$	SCKx, SINx		20	-	20	-	20	-	ns
SCK falling time	$t_F$	SCKx		-	5	-	5	-	5	ns
SCK rising time	$t_R$	SCKx		-	5	-	5	-	5	ns

**Notes:**

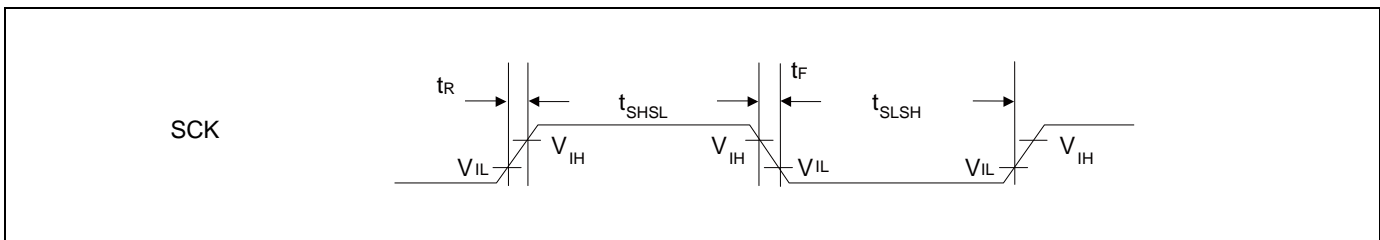
- The above characteristics apply to clock synchronous mode.
- $t_{CYCP}$  indicates the APB bus clock cycle time.  
About the APB bus number which Multi-function serial is connected to, see Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SOTx\_1 is not guaranteed.
- When the external load capacitance  $C_L = 50$  pF.



UART external clock input (EXT = 1)

( $V_{CC} = 1.8V$  to  $5.5V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	$t_{SLSH}$	$C_L = 50\text{ pF}$	$t_{CYCP} + 10$	-	ns	
Serial clock H pulse width	$t_{SHSL}$		$t_{CYCP} + 10$	-	ns	
SCK falling time	$t_F$		-	5	ns	
SCK rising time	$t_R$		-	5	ns	



**12.4.10 External Input Timing**

 (V<sub>CC</sub> = 1.8V to 5.5V, V<sub>SS</sub> = 0V, T<sub>A</sub> = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t <sub>INH</sub> , t <sub>INL</sub>	ADTG	-	2t <sub>CYCP</sub> *1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTixX	-	2t <sub>CYCP</sub> *1	-	ns	Waveform generator
		IGTRG	-	2t <sub>CYCP</sub> *1	-	ns	PPG IGBT mode
		INTxx, NMIX	*2	2t <sub>CYCP</sub> + 100*1	-	ns	External interrupt, NMI
			*3	500	-	ns	
WKUPx	*4	500	-	ns	Deep standby wake up		

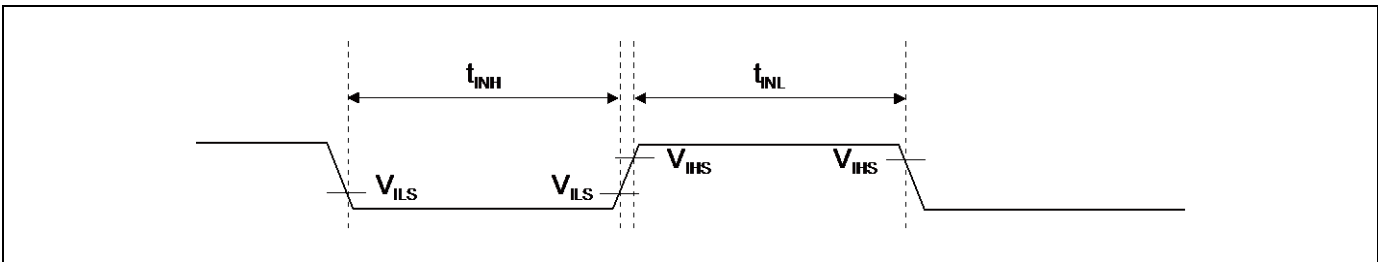
 \*1: t<sub>CYCP</sub> indicates the APB bus clock cycle time.

About the APB bus number which the A/D converter, Multi-function Timer, PPG, External interrupt, Deep Standby mode Controller are connected to, see Block Diagram in this data sheet.

\*2: When in Run mode, in Sleep mode.

\*3: When in Timer mode, in RTC mode, in Stop mode.

\*4: When in Deep Standby RTC mode, in Deep Standby Stop mode.



**12.4.11 PC Timing**
 $(V_{CC} = 1.8V \text{ to } 5.5V, V_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +85^{\circ}C)$ 

Parameter	Symbol	Conditions	Standard-mode		Fast-mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	$f_{SCL}$		0	100	0	400	kH z	
(Repeated) START condition hold time SDA $\downarrow \rightarrow$ SCL $\downarrow$	$t_{HDSTA}$	$C_L = 50 \text{ pF},$ $R = (V_P/I_{OL})^{*1}$	4.0	-	0.6	-	$\mu$ s	
SCL clock L width	$t_{LOW}$		4.7	-	1.3	-	$\mu$ s	
SCL clock H width	$t_{HIGH}$		4.0	-	0.6	-	$\mu$ s	
(Repeated) START condition setup time SCL $\uparrow \rightarrow$ SDA $\downarrow$	$t_{SUSTA}$		4.7	-	0.6	-	$\mu$ s	
Data hold time SCL $\downarrow \rightarrow$ SDA $\downarrow \uparrow$	$t_{HDDAT}$		0	$3.45^{*2}$	0	$0.9^{*3}$	$\mu$ s	
Data setup time SDA $\downarrow \uparrow \rightarrow$ SCL $\uparrow$	$t_{SUDAT}$		250	-	100	-	ns	
STOP condition setup time SCL $\uparrow \rightarrow$ SDA $\uparrow$	$t_{SUSTO}$		4.0	-	0.6	-	$\mu$ s	
Bus free time between STOP condition and START condition	$t_{BUF}$		4.7	-	1.3	-	$\mu$ s	
Noise filter	$t_{SP}$		-	$2 t_{CYCP}^{*4}$	-	$2 t_{CYCP}^{*4}$	-	ns

\*1: R and  $C_L$  represent the pull-up resistor and load capacitance of the SCL and SDA lines, respectively.  
 $V_P$  indicates the power supply voltage of the pull-up resistor and  $I_{OL}$  indicates  $V_{OL}$  guaranteed current.

\*2: The maximum  $t_{HDDAT}$  must satisfy that it does not extend at least L period ( $t_{LOW}$ ) of device's SCL signal.

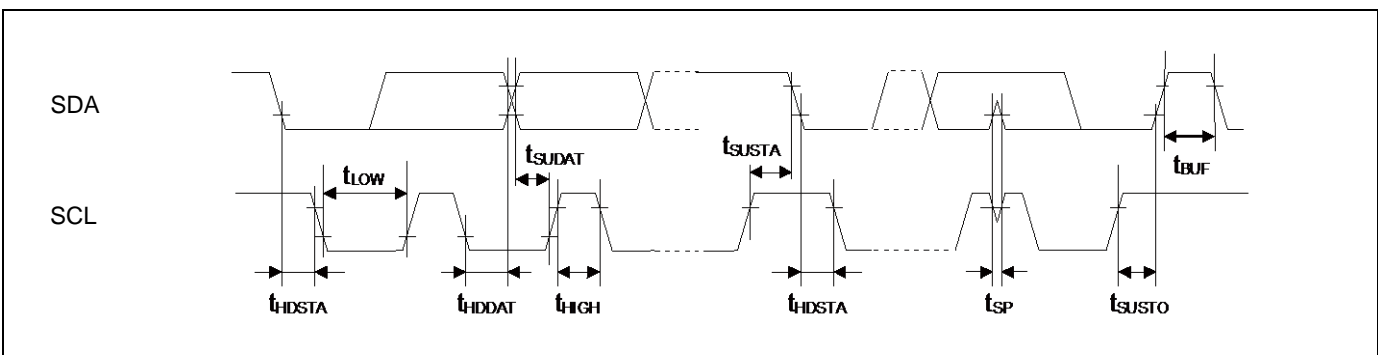
\*3: A Fast-mode I<sup>2</sup>C bus device can be used on a Standard-mode I<sup>2</sup>C bus system as long as the device satisfies the requirement of  $t_{SUDAT} \geq 250$  ns.

\*4:  $t_{CYCP}$  is the APB bus clock cycle time.

About the APB bus number which I<sup>2</sup>C is connected to, see Block Diagram in this data sheet.

To use Standard-mode, set the APB bus clock at 2 MHz or more.

To use Fast-mode, set the APB bus clock at 8 MHz or more.



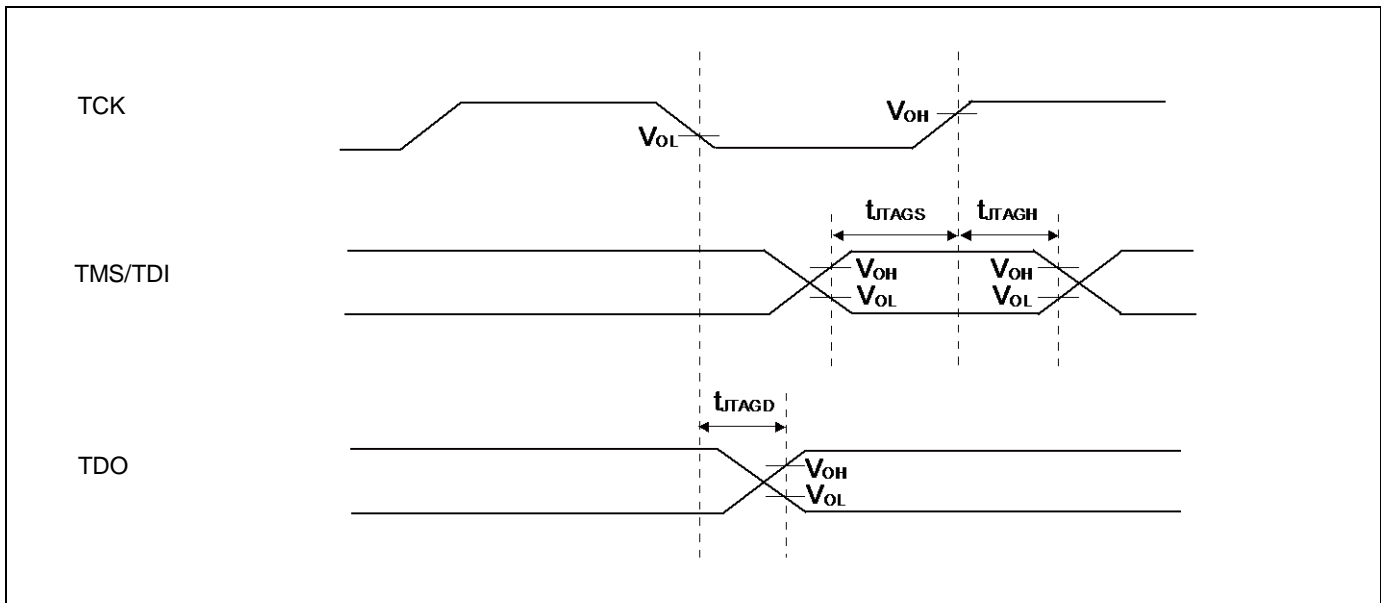


**12.4.12 JTAG Timing**

 (V<sub>CC</sub> = 1.8V to 5.5V, V<sub>SS</sub> = 0V, T<sub>A</sub> = - 40°C to + 85°C)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS,TDI setup time	t <sub>JTAGS</sub>	TCK, TMS, TDI	V <sub>CC</sub> ≥ 4.5 V	15	-	ns	
			V <sub>CC</sub> < 4.5 V				
TMS,TDI hold time	t <sub>JTAGH</sub>	TCK, TMS, TDI	V <sub>CC</sub> ≥ 4.5 V	15	-	ns	
			V <sub>CC</sub> < 4.5 V				
TDO delay time	t <sub>JTAGD</sub>	TCK, TDO	V <sub>CC</sub> ≥ 4.5 V	-	30	ns	
			2.7 V ≤ V <sub>CC</sub> < 4.5 V	-	45		
			V <sub>CC</sub> < 2.7 V	-	60		

**Note:**

 - When the external load capacitance C<sub>L</sub> = 50 pF.


## 12.5 12-bit A/D Converter

### 12.5.1 Electrical Characteristics for the A/D Converter

( $V_{CC} = AV_{CC} = 1.8V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	INL	-	-	$\pm 2.5$	$\pm 3.0$	LSB	$AV_{CC} \geq 2.7 V$
			-	$\pm 3.5$	$\pm 4.0$	LSB	$AV_{CC} < 2.7 V$
Differential Nonlinearity	DNL	-	-	$\pm 1.8$	$\pm 1.9$	LSB	$AV_{CC} \geq 2.7 V$
			-	$\pm 2.7$	$\pm 2.9$	LSB	$AV_{CC} < 2.7 V$
Zero transition voltage	$V_{ZT}$	ANxx	-	$\pm 9$	$\pm 20$	mV	
Full-scale transition voltage	$V_{FST}$	ANxx	-	$AVRH \pm 9$	$AVRH \pm 20$	mV	
Conversion time*1	-	-	1.0	-	-	$\mu s$	$AV_{CC} \geq 2.7 V$
			4.0				$AV_{CC} < 2.7 V$
Sampling time*2	$t_s$	-	0.3	-	10	$\mu s$	$AV_{CC} \geq 2.7 V$
			1.2				$AV_{CC} < 2.7 V$
Compare clock cycle*3	$t_{CCK}$	-	50	-	1000	ns	$AV_{CC} \geq 2.7 V$
			200				$AV_{CC} < 2.7 V$
Period of operation enable state transitions	$t_{STT}$	-	-	-	1	$\mu s$	
Analog input capacity	$C_{AIN}$	-	-	-	15	pF	
Analog input resistor	$R_{AIN}$	-	-	-	0.9	k $\Omega$	$AV_{CC} \geq 4.5 V$
					1.6		$2.7 V \leq AV_{CC} < 4.5 V$
					4.0		$AV_{CC} < 2.7 V$
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	0.3	$\mu A$	
Analog input voltage	-	ANxx	$AV_{SS}$	-	$AVRH$	V	
Reference voltage	-	AVRH	2.7	-	$AV_{CC}$	V	$AV_{CC} \geq 2.7 V$
			$AV_{CC}$				$AV_{CC} < 2.7 V$

\*1: The conversion time is the value of sampling time ( $t_s$ ) + compare time ( $t_c$ ).

The condition of the minimum conversion time is the following.

$AV_{CC} \geq 2.7 V$ , HCLK=20 MHz      sampling time: 0.3  $\mu s$ , compare time: 0.7  $\mu s$

$AV_{CC} < 2.7 V$ , HCLK=20 MHz      sampling time: 1.2  $\mu s$ , compare time: 2.8  $\mu s$

Ensure that it satisfies the value of the sampling time ( $t_s$ ) and compare clock cycle ( $t_{CCK}$ ).

For setting\*4 of the sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM3 Family Peripheral Manual Analog Macro Part.

The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.

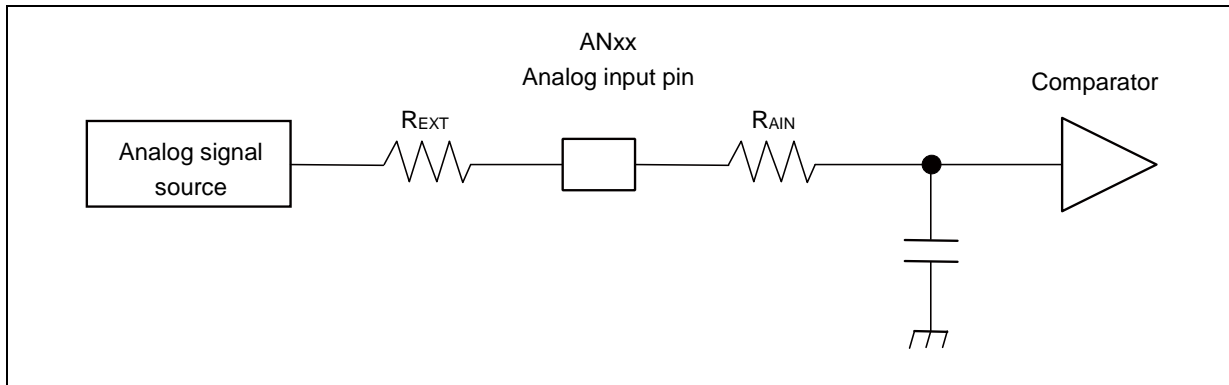
For the number of the APB bus to which the A/D Converter is connected, see Block Diagram.

The Base clock (HCLK) is used to generate the sampling time and the compare clock cycle.

\*2: A necessary sampling time changes by external impedance.

Ensure to set the sampling time to satisfy (Equation 1).

\*3: The compare time ( $t_c$ ) is the value of (Equation 2).



(Equation 1)  $t_s \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

$t_s$ : Sampling time

$R_{AIN}$ : Input resistor of A/D = 0.9 k $\Omega$  at 4.5 V  $\leq$  AV<sub>CC</sub>  $\leq$  5.5 V

Input resistor of A/D = 1.6 k $\Omega$  at 2.7 V  $\leq$  AV<sub>CC</sub> < 4.5 V

Input resistor of A/D = 4.0 k $\Omega$  at 1.8 V  $\leq$  AV<sub>CC</sub> < 2.7 V

$C_{AIN}$ : Input capacity of A/D = 15 pF at 1.8 V  $\leq$  AV<sub>CC</sub>  $\leq$  5.5 V

$R_{EXT}$ : Output impedance of external circuit

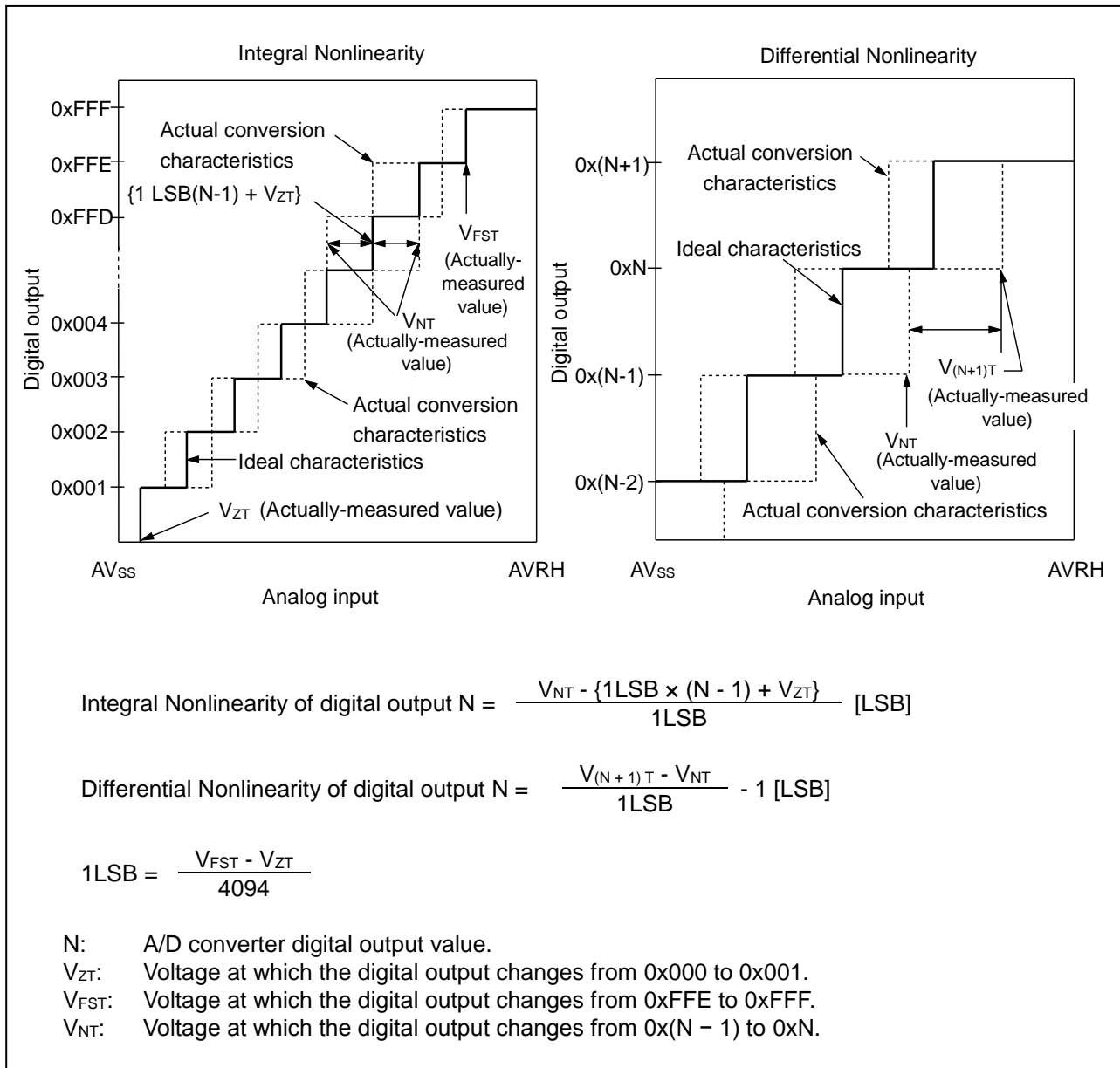
(Equation 2)  $t_c = t_{cck} \times 14$

$t_c$ : Compare time

$t_{cck}$ : Compare clock cycle

**Definition of 12-bit A/D Converter Terms**

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000←→0b000000000001) and the full-scale transition point (0b111111111110←→0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



## 12.6 10-bit D/A Converter

Electrical Characteristics for the D/A Converter

( $V_{CC} = AV_{CC} = 1.8V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	10	bit	
Conversion time	$t_{C20}$		0.37	0.53	0.69	$\mu s$	Load 20 pF
	$t_{C100}$		1.87	2.67	3.47	$\mu s$	Load 100 pF
Integral Nonlinearity	INL		-4.0	-	+4.0	LSB	*
Differential Nonlinearity	DNL		-0.9	-	+0.9	LSB	*
Output Voltage offset	$V_{OFF}$		-	-	10.0	mV	Code is 0x000
			-50.0	-	+5.5	mV	Code is 0x3FF
Analog output impedance	$R_o$		2.45	3.50	4.55	k $\Omega$	D/A operation
			5.0	9.0	-	M $\Omega$	D/A stop
Output undefined period	$t_R$	-	-	250	ns		

\*: No-load

## 12.7 Low-Voltage Detection Characteristics

### 12.7.1 Low-Voltage Detection Reset

(T<sub>A</sub> = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V <sub>DLR</sub>	SVHR = 0001	1.43	1.53	1.63	V	When voltage drops
Released voltage	V <sub>DHR</sub>		1.53	1.63	1.73	V	When voltage rises
Detected voltage	V <sub>DLR</sub>	SVHR = 0100	1.80	1.93	2.06	V	When voltage drops
Released voltage	V <sub>DHR</sub>		1.90	2.03	2.16	V	When voltage rises
LVD stabilization wait time	t <sub>LVD<sub>RW</sub></sub>	-	-	-	633 × t <sub>CYCP</sub> *	μs	
Detection delay time	t <sub>LVD<sub>RD</sub></sub>	dV/dt ≥ -4 mV/μs	-	-	60	μs	

\*: t<sub>CYCP</sub> indicates the APB2 bus clock cycle time.

**12.7.2 Interrupt of Low-Voltage Detection**

Normal mode

 (T<sub>A</sub> = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V <sub>DLI</sub>	SVHI = 0000	1.87	2.00	2.13	V	When voltage drops
Released voltage	V <sub>DHI</sub>		1.97	2.10	2.23	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 0001	1.96	2.10	2.24	V	When voltage drops
Released voltage	V <sub>DHI</sub>		2.06	2.20	2.34	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 0010	2.05	2.20	2.35	V	When voltage drops
Released voltage	V <sub>DHI</sub>		2.15	2.30	2.45	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 0011	2.15	2.30	2.45	V	When voltage drops
Released voltage	V <sub>DHI</sub>		2.25	2.40	2.55	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 0100	2.24	2.40	2.56	V	When voltage drops
Released voltage	V <sub>DHI</sub>		2.34	2.50	2.66	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 0101	2.33	2.50	2.67	V	When voltage drops
Released voltage	V <sub>DHI</sub>		2.43	2.60	2.77	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 0110	2.43	2.60	2.77	V	When voltage drops
Released voltage	V <sub>DHI</sub>		2.53	2.70	2.87	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 0111	2.61	2.80	2.99	V	When voltage drops
Released voltage	V <sub>DHI</sub>		2.71	2.90	3.09	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 1000	2.80	3.00	3.20	V	When voltage drops
Released voltage	V <sub>DHI</sub>		2.90	3.10	3.30	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 1001	2.99	3.20	3.41	V	When voltage drops
Released voltage	V <sub>DHI</sub>		3.09	3.30	3.51	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 1010	3.36	3.60	3.84	V	When voltage drops
Released voltage	V <sub>DHI</sub>		3.46	3.70	3.94	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 1011	3.45	3.70	3.95	V	When voltage drops
Released voltage	V <sub>DHI</sub>		3.55	3.80	4.05	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 1100	3.73	4.00	4.27	V	When voltage drops
Released voltage	V <sub>DHI</sub>		3.83	4.10	4.37	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 1101	3.83	4.10	4.37	V	When voltage drops
Released voltage	V <sub>DHI</sub>		3.93	4.20	4.47	V	When voltage rises
Detected voltage	V <sub>DLI</sub>	SVHI = 1110	3.92	4.20	4.48	V	When voltage drops
Released voltage	V <sub>DHI</sub>		4.02	4.30	4.58	V	When voltage rises
LVD stabilization wait time	t <sub>LVDIW</sub>	-	-	-	633 × t <sub>CYCP</sub> *	μs	
Detection delay time	t <sub>LVDID</sub>	dV/dt ≥ - 4 mV/μs	-	-	60	μs	

 \*: t<sub>CYCP</sub> indicates the APB2 bus clock cycle time.

Low-power mode

 (T<sub>A</sub> = - 40°C to + 85°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V <sub>DLIL</sub>	SVHI = 0000	1.80	2.00	2.20	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		1.90	2.10	2.30	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 0001	1.89	2.10	2.31	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		1.99	2.20	2.41	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 0010	1.98	2.20	2.42	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		2.08	2.30	2.52	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 0011	2.07	2.30	2.53	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		2.17	2.40	2.63	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 0100	2.16	2.40	2.64	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		2.26	2.50	2.74	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 0101	2.25	2.50	2.75	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		2.35	2.60	2.85	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 0110	2.34	2.60	2.86	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		2.44	2.70	2.96	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 0111	2.52	2.80	3.08	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		2.62	2.90	3.18	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 1000	2.70	3.00	3.30	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		2.80	3.10	3.40	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 1001	2.88	3.20	3.52	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		2.98	3.30	3.62	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 1010	3.24	3.60	3.96	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		3.34	3.70	4.06	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 1011	3.33	3.70	4.07	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		3.43	3.80	4.17	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 1100	3.60	4.00	4.40	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		3.70	4.10	4.50	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 1101	3.69	4.10	4.51	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		3.79	4.20	4.61	V	When voltage rises
Detected voltage	V <sub>DLIL</sub>	SVHI = 1110	3.78	4.20	4.62	V	When voltage drops
Released voltage	V <sub>DHIL</sub>		3.88	4.30	4.72	V	When voltage rises
LVD stabilization wait time	t <sub>LVDILW</sub>	-	-	-	8039 × t <sub>CYCP</sub> *	μs	
Detection delay time	t <sub>LVDILD</sub>	dV/dt ≥ - 0.4 mV/μs	-	-	800	μs	

 \*: t<sub>CYCP</sub> indicates the APB2 bus clock cycle time.



## 12.8 Flash Memory Write/Erase Characteristics

### 12.8.1 Write / Erase time

( $V_{CC} = 2.0V$  to  $5.5V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Parameter		Value		Unit	Remarks
		Typ*	Max*		
Sector erase time	Large Sector	1.6	7.5	s	Includes write time prior to internal erase
	Small Sector	0.4	2.1		
Half word (16-bit) write time		25	400	$\mu s$	Not including system-level overhead time.
Chip erase time		4	19.2	s	Includes write time prior to internal erase

\*: The typical value is immediately after shipment, the maximum value is guarantee value under 100,000 cycle of erase/write.

### 12.8.2 Write cycles and data hold time

Erase/write cycles (cycle)	Data hold time (year)	Remarks
1,000	20 *	
10,000	10 *	
100,000	5*	

\*: At average  $+85^{\circ}C$

## 12.9 Return Time from Low-Power Consumption Mode

### 12.9.1 Return Factor: Interrupt/WKUP

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

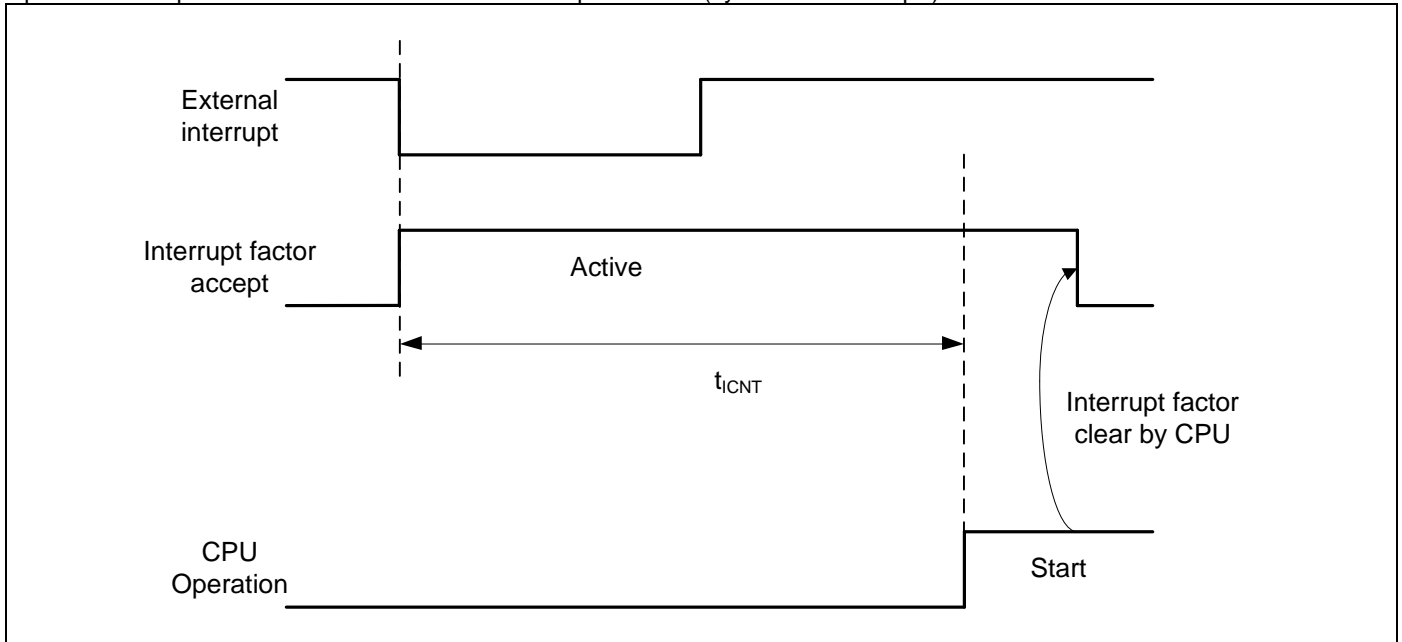
Return Count Time

( $V_{CC} = 1.65V$  to  $3.6V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t <sub>ICNT</sub>	t <sub>cycc</sub>		μs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		40	80	μs	
Low-speed CR Timer mode		630	1260	μs	
Sub Timer mode		630	1260	μs	
RTC mode, Stop mode		1083	2100	μs	
Deep Standby RTC mode Deep Standby Stop mode		1099	2127	μs	

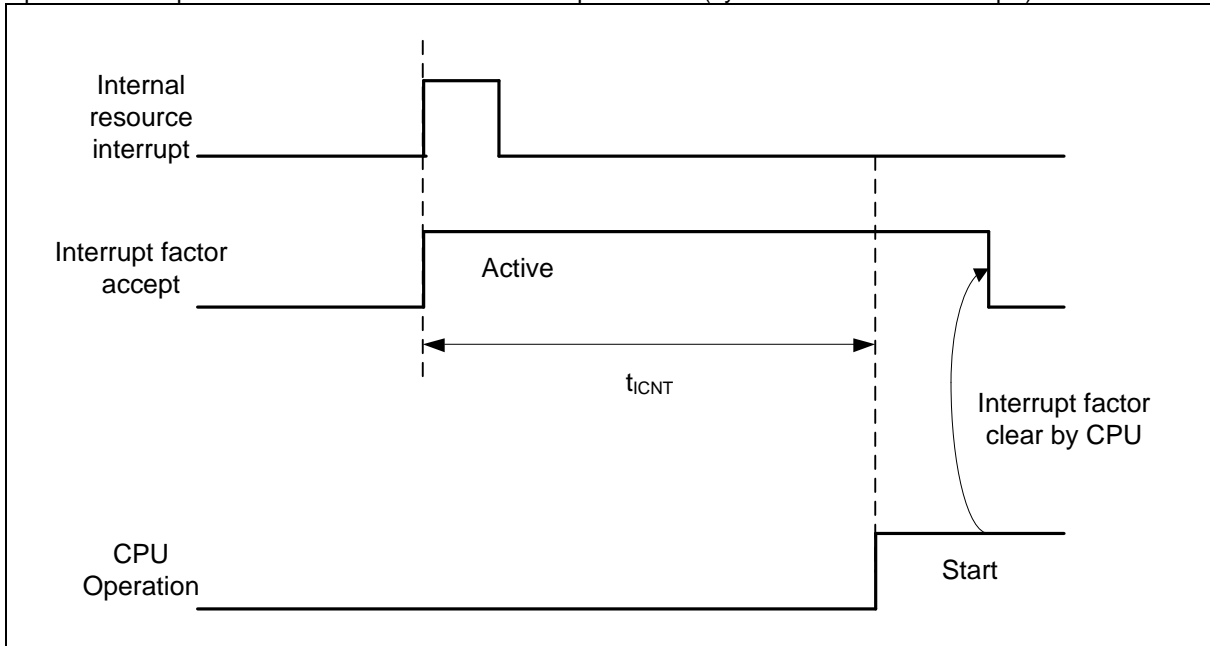
\*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by external interrupt\*)



\*: External interrupt is set to detecting fall edge.

Operation example of return from Low-Power consumption mode (by internal resource interrupt\*)



\*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

- Notes:**
- The return factor is different in each Low-Power consumption modes.  
See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.
  - When interrupt recovers, the operation mode that CPU recovers depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.

**12.9.2 Return Factor: Reset**

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

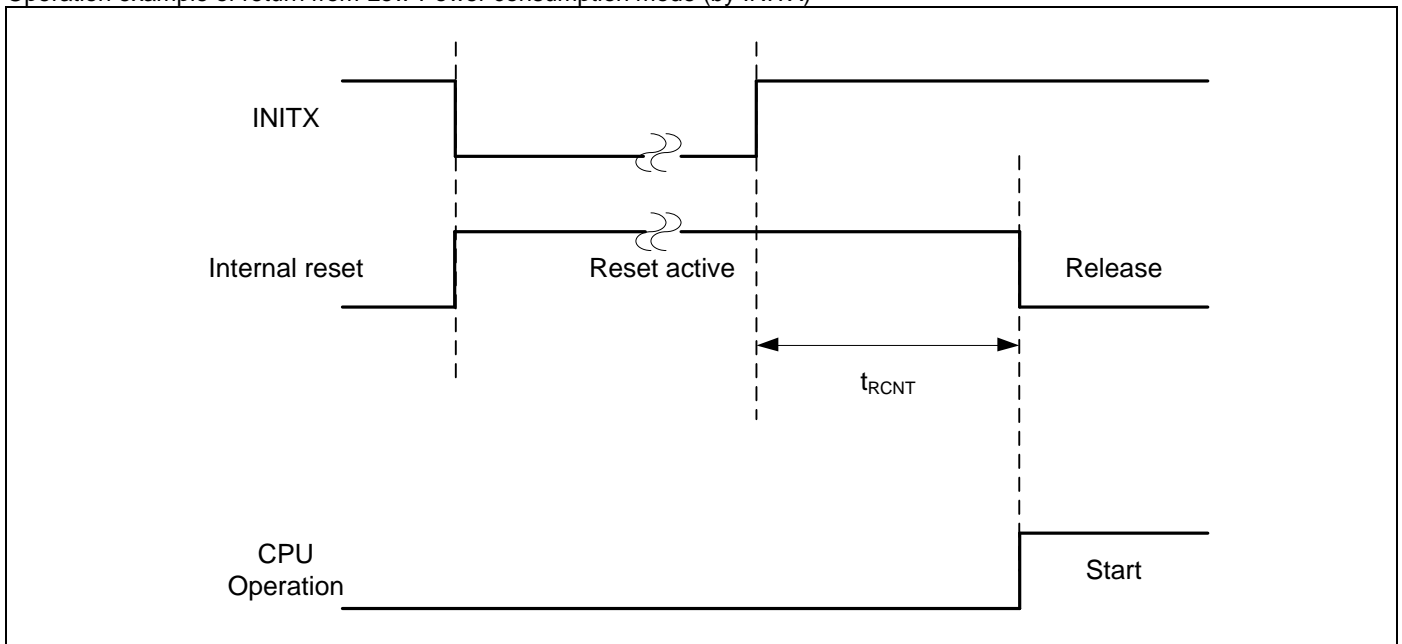
Return Count Time

( $V_{CC} = 1.65V$  to  $3.6V$ ,  $V_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

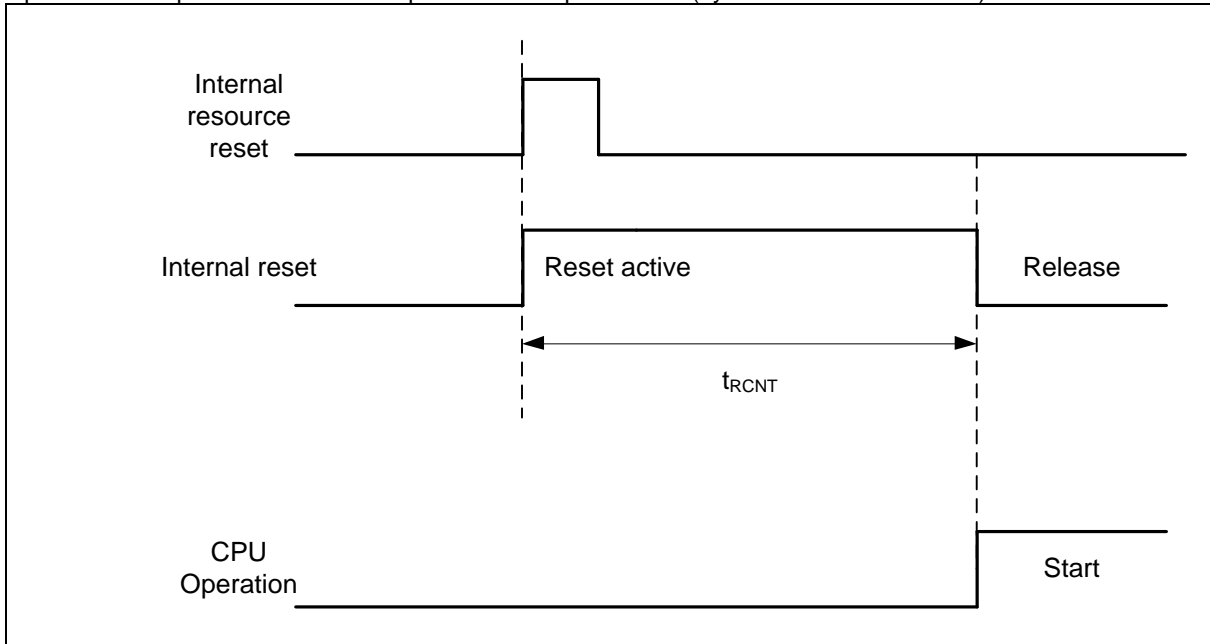
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t <sub>RCNT</sub>	359	647	μs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		359	647	μs	
Low-speed CR Timer mode		929	1787	μs	
Sub Timer mode		929	1787	μs	
RTC/Stop mode		1099	2127	μs	
Deep Standby RTC mode Deep Standby Stop mode		1099	2127	μs	

\*: The maximum value depends on the accuracy of built-in CR.

Operation example of return from Low-Power consumption mode (by INITX)



Operation example of return from low power consumption mode (by internal resource reset\*)



\*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

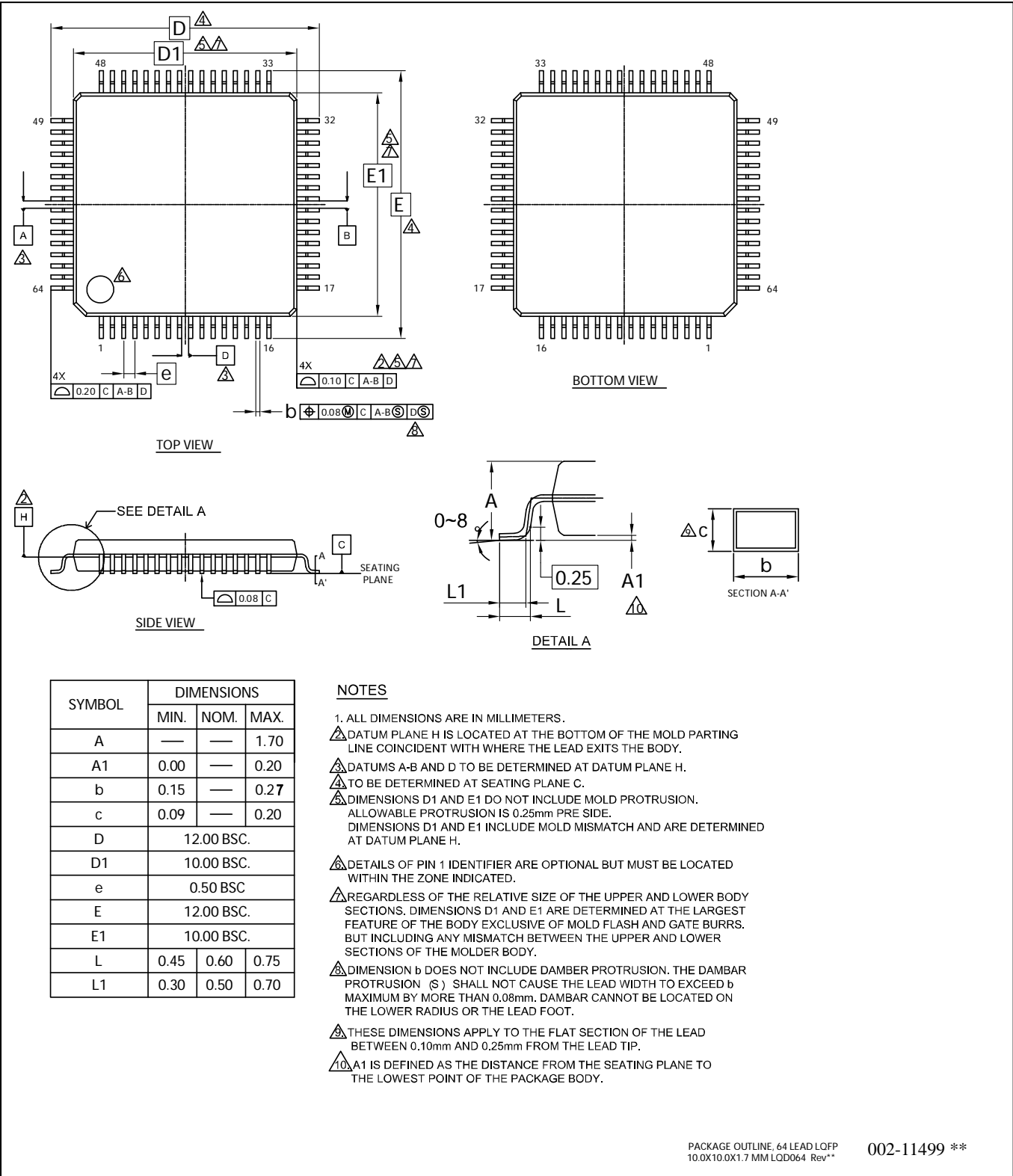
- Notes:**
- The return factor is different in each Low-Power consumption modes. See Chapter 6: Low Power Consumption Mode and Operations of Standby Modes in FM3 Family Peripheral Manual.
  - When interrupt recovers, the operation mode that CPU recovers depend on the state before the Low-Power consumption mode transition. See Chapter 6: Low Power Consumption Mode in FM3 Family Peripheral Manual.
  - The time during the power-on reset/low-voltage detection reset is excluded. See Power-on Reset Timing in AC Characteristics in Electrical Characteristics for the detail on the time during the power-on reset/low-voltage detection reset.
  - When in recovery from reset, CPU changes to the High-speed CR Run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the Main PLL clock stabilization wait time.
  - The internal resource reset means the watchdog reset and the CSV reset.

**13. Ordering Information**

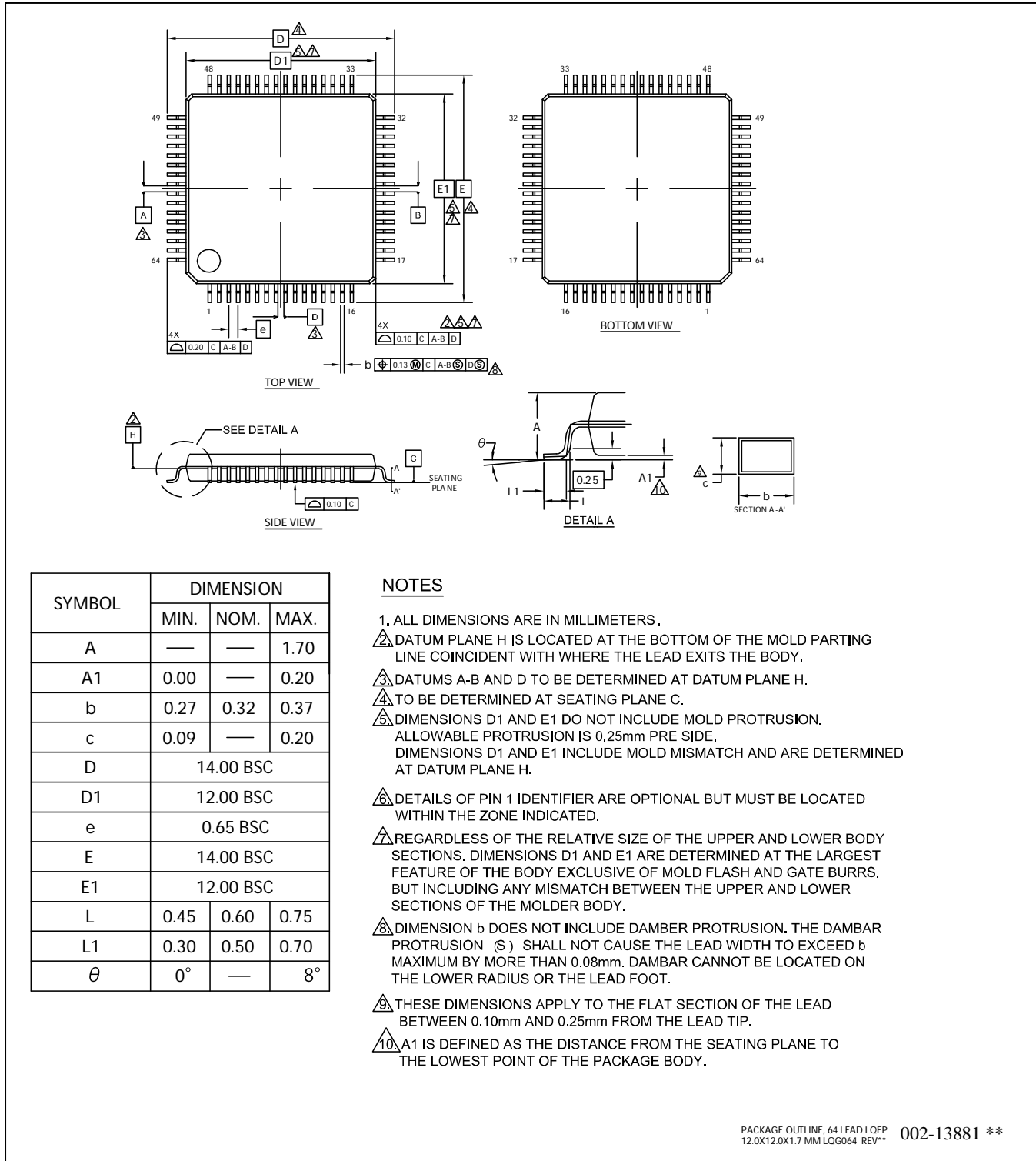
Part number	On-chip Flash memory	On-chip SRAM	Package	Packing
MB9AFA31LPMC1-G-SNE2	64 Kbyte	12 Kbyte	Plastic • LQFP (0.5mm pitch), 64-pin (LQD064)	Tray
MB9AFA32LPMC1-G-SNE2	128 Kbyte	16 Kbyte		
MB9AFA31LPMC-G-SNE2	64 Kbyte	12 Kbyte	Plastic • LQFP (0.65mm pitch), 64-pin (LQG064)	
MB9AFA32LPMC-G-SNE2	128 Kbyte	16 Kbyte		
MB9AFA31LQN-G-AVE2	64 Kbyte	12 Kbyte	Plastic • QFN (0.5mm pitch), 64-pin (VNC064)	
MB9AFA32LQN-G-AVE2	128 Kbyte	16 Kbyte		
MB9AFA31MPMC-G-SNE2	64 Kbyte	12 Kbyte	Plastic • LQFP (0.5mm pitch), 80-pin (LQH080)	
MB9AFA32MPMC-G-SNE2	128 Kbyte	16 Kbyte		
MB9AFA31MPMC1-G-SNE2	64 Kbyte	12 Kbyte	Plastic • LQFP (0.65mm pitch), 80-pin (LQJ080)	
MB9AFA32MPMC1-G-SNE2	128 Kbyte	16 Kbyte		
MB9AFA31NPMC-G-SNE2	64 Kbyte	12 Kbyte	Plastic • LQFP (0.5mm pitch), 100-pin (LQI100)	
MB9AFA32NPMC-G-SNE2	128 Kbyte	16 Kbyte		
MB9AFA31NPF-G-SNE1	64 Kbyte	12 Kbyte	Plastic • QFP (0.65mm pitch), 100-pin (PQH100)	
MB9AFA32NPF-G-SNE1	128 Kbyte	16 Kbyte		

14. Package Dimensions

Package Type	Package Code
LQFP 64 (0.5mm pitch)	LQD064



<b>Package Type</b>	<b>Package Code</b>
LQFP 64 (0.65mm pitch)	LQG064



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.27	0.32	0.37
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.65 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
$\theta$	0°	—	8°

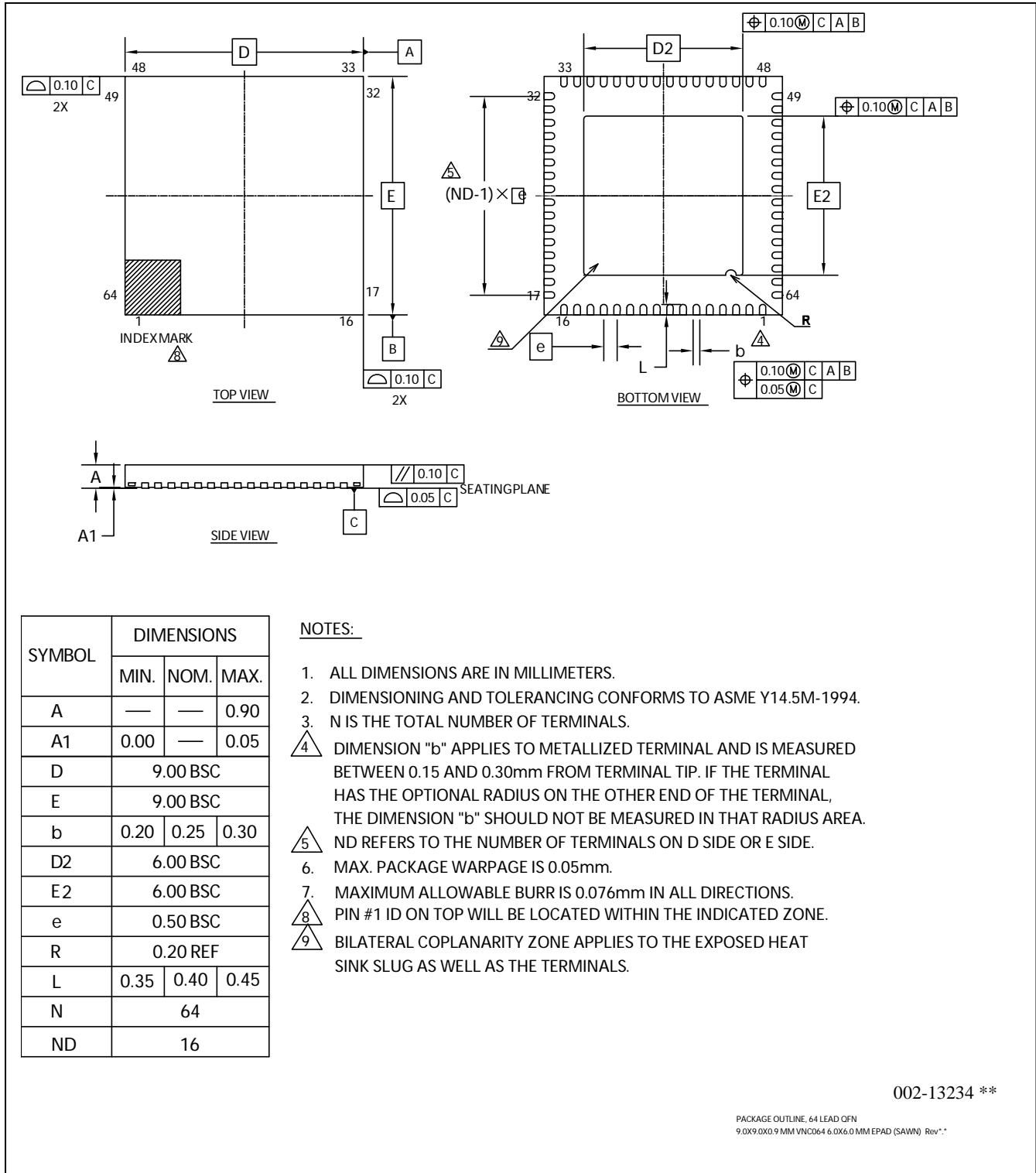
**NOTES**

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 64 LEAD LQFP  
12.0X12.0X1.7 MM LQG064 REV\*\* 002-13881 \*\*



<b>Package Type</b>	<b>Package Code</b>
QFN 64	VNC064



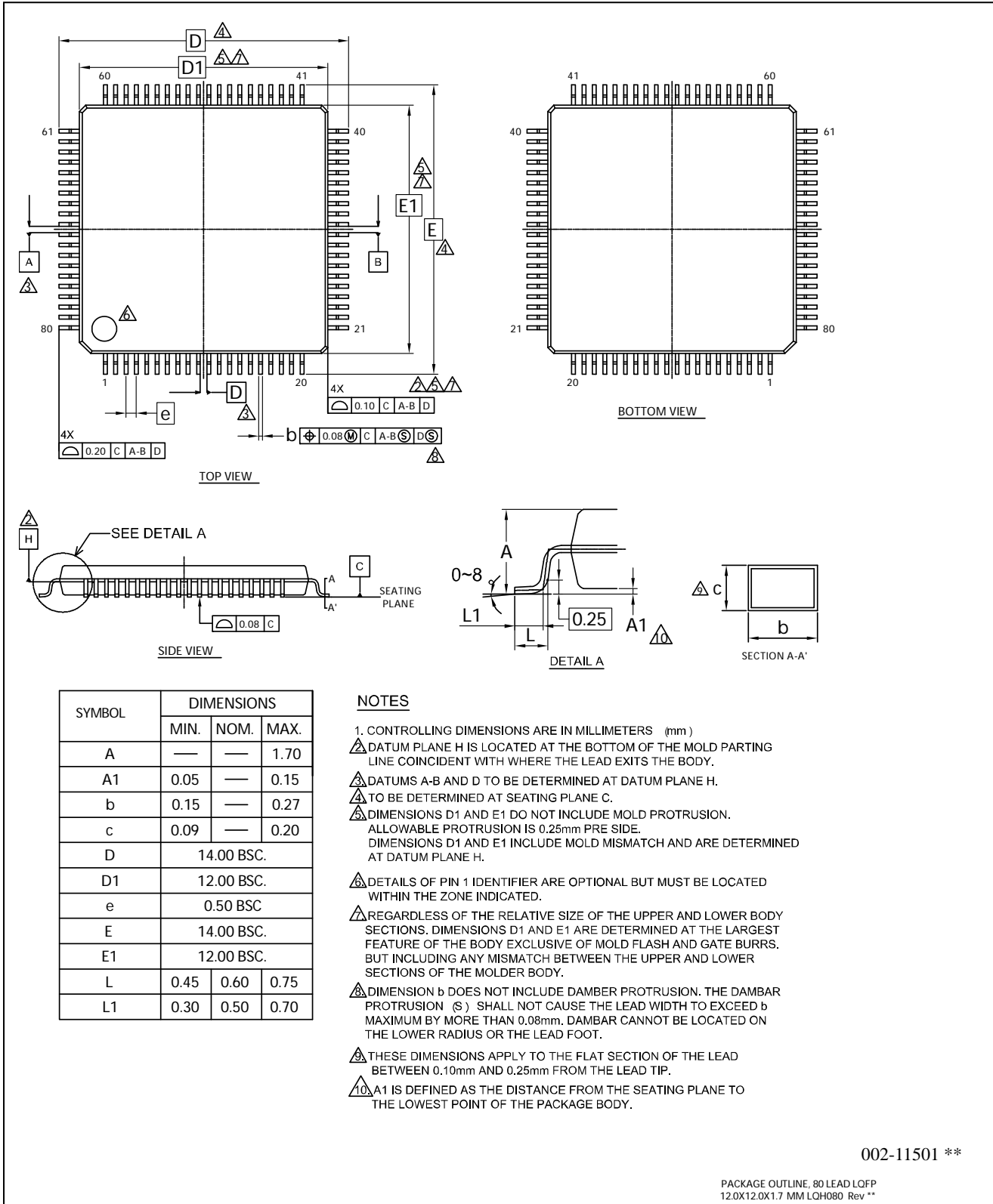
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.90
A1	0.00	—	0.05
D	9.00 BSC		
E	9.00 BSC		
b	0.20	0.25	0.30
D2	6.00 BSC		
E2	6.00 BSC		
e	0.50 BSC		
R	0.20 REF		
L	0.35	0.40	0.45
N	64		
ND	16		

- NOTES:**
- ALL DIMENSIONS ARE IN MILLIMETERS.
  - DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5M-1994.
  - N IS THE TOTAL NUMBER OF TERMINALS.
  - $\triangle$  DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
  - $\triangle$  ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE OR E SIDE.
  - MAX. PACKAGE WARPAGE IS 0.05mm.
  - MAXIMUM ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
  - $\triangle$  PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
  - $\triangle$  BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

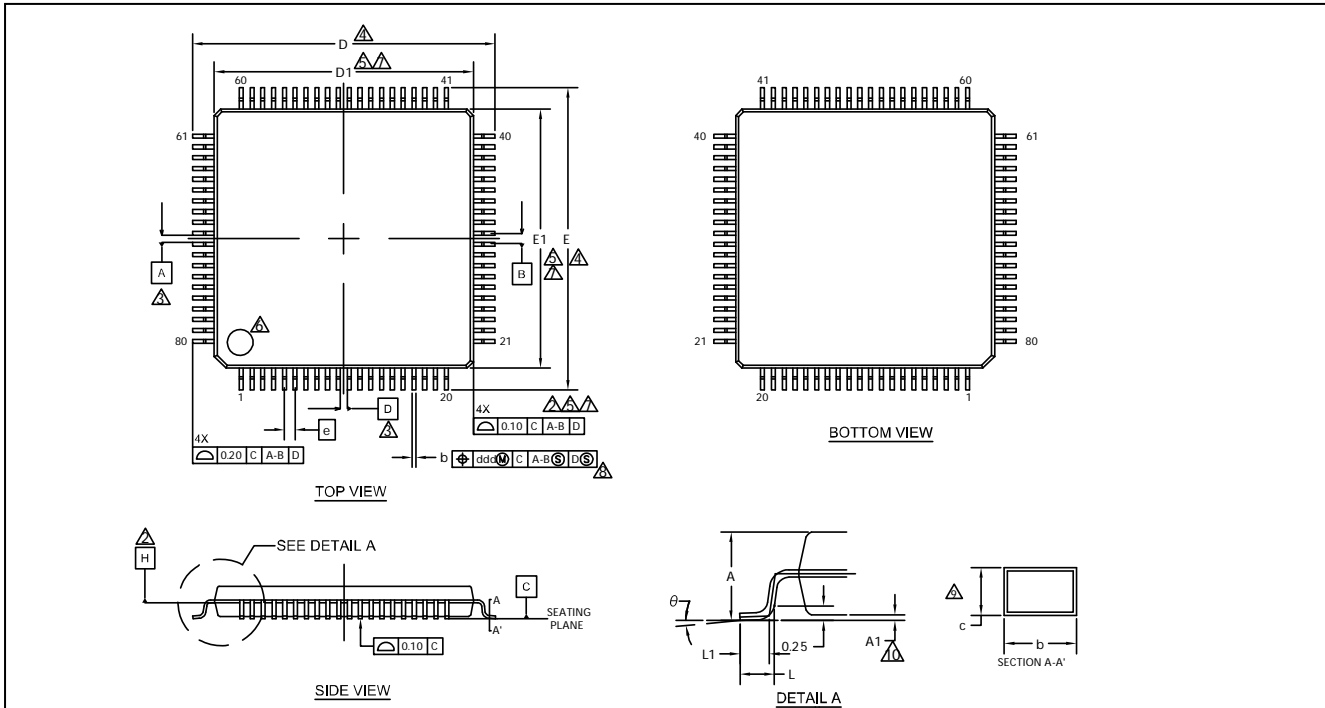
002-13234 \*\*

PACKAGE OUTLINE, 64 LEAD QFN  
9.0X9.0X0.9 MM VNC064 6.0X6.0 MM EPAD (SAWN) Rev\*\*

Package Type	Package Code
LQFP 80 (0.5mm pitch)	LQH080



<b>Package Type</b>	<b>Package Code</b>
LQFP 80 (0.65mm pitch)	LQJ080



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.16	0.32	0.38
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.65 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
$\theta$	0°	—	8°

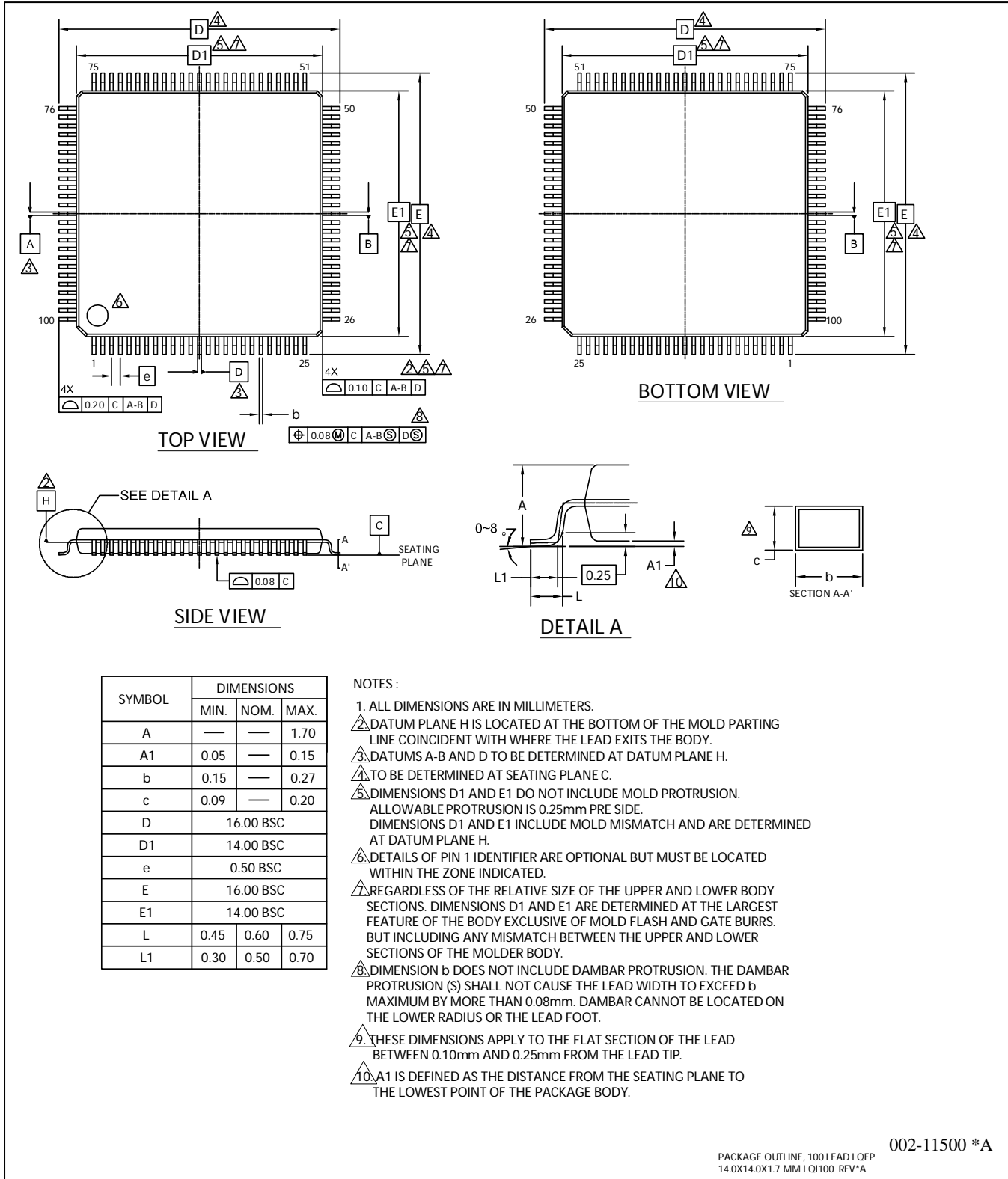
### NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
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- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

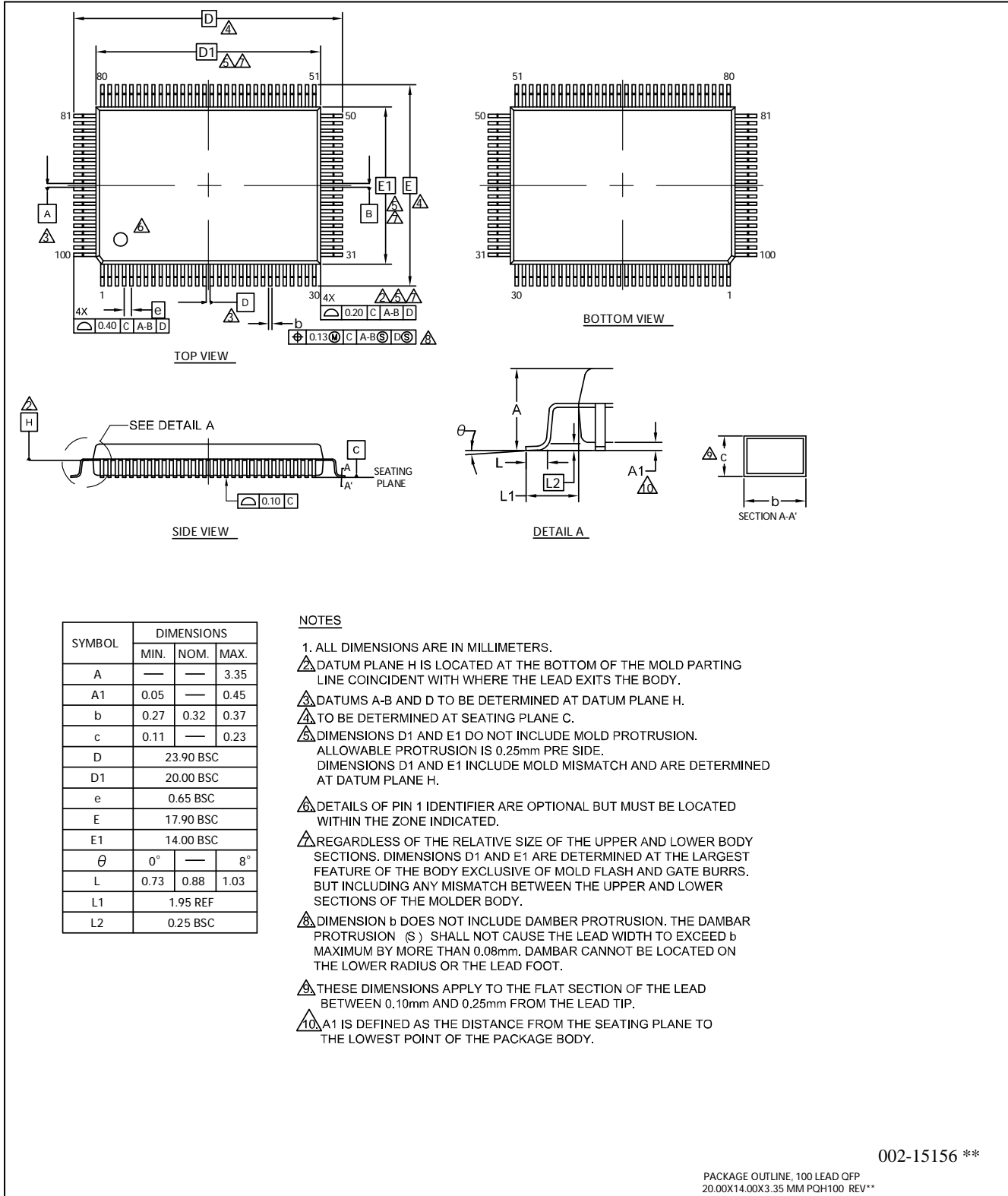
002-14043 \*\*

PACKAGE OUTLINE, 80 LEAD LQFP  
14.0X14.0X1.7 MM LQJ080 REV\*\*

Package Type	Package Code
LQFP 100	LQ100



<b>Package Type</b>	<b>Package Code</b>
QFP 100	PQH100



## 15. Major Changes

Spanion Publication Number: DS706-00041

Page	Section	Change Results
Revision 3.0		
18	list of pin functions • List of pin numbers	Revised the Pin state type.
26	• List of pin functions	Revised the pin name of "External Interrupt". INIT15_1 → INT15_1
63	pin status in each cpu state • List of pin status	• Added "Y" and "Z" type to the Pin status type. • Added the footnote.
Revision 3.1		
-	-	Company name and layout design change
Revision 4.0		
2	Features • On-chip Memories	Changed the description of on-chip SRAM
7 - 34	Packages Pin Assignment List of Pin Functions	Deleted BGA package
46	Handling Devices	Added ". Stabilizing power supply voltage"
46	Handling Devices Crystal oscillator circuit	Added the following description "Evaluate oscillation of your using crystal oscillator by your mount board."
48	Block Diagram	Modified the block diagram
50	Memory Map • Memory map(2)	Added the summary of Flash memory sector and the note
65 - 67	Electrical Characteristics DC Characteristics Current rating	• Changed the table format • Added Main Timer mode current • Added Flash Memory Current • Moved A/D Converter Current • Moved D/A Converter Current
68	Electrical Characteristics DC Characteristics Pin Characteristics	Added the input leak current of CEC port at power off
72	Electrical Characteristics AC Characteristics Operating Conditions of Main PLL Operating Conditions of Main PLL	• Added the figure of Main PLL connection
73	Electrical Characteristics AC Characteristics Power-on Reset Timing	• Changed the figure of timing • Changed from Reset release delay time( $t_{OND}$ ) to Time until releasing Power-on reset( $t_{PRT}$ )
75 - 82	Electrical Characteristics AC Characteristics CSIO/UART Timing	• Modified from UART Timing to CSIO/UART Timing • Changed from Internal shift clock operation to Master mode • Changed from External shift clock operation to Slave mode
86	Electrical Characteristics 12bit A/D Converter	• Added the typical value of Integral Nonlinearity, Differential Nonlinearity, Zero transition voltage and Full-scale transition voltage • Added Conversion time at $AV_{CC} < 2.7 V$ • Changed from Non linearity error to Integral Nonlinearity • Changed from Differential linearity error to Differential Nonlinearity
89	Electrical Characteristics 10bit D/A Converter	• Changed from Non linearity error to Integral Nonlinearity • Changed from Differential linearity error to Differential Nonlinearity
90	Electrical Characteristics Low-voltage Detection Characteristics	Deleted the figure

Page	Section	Change Results
93	Electrical Characteristics Flash Memory Write/Erase Characteristics	Change to the erase time of include write time prior to internal erase
94 - 97	Electrical Characteristics 9. Return Time from Low-Power Consumption Mode	Added Return Time from Low-Power Consumption Mode
98	Ordering Information	Changed notation of part number
99	Package Dimensions	Deleted BGA-112P-M04

**NOTE: Please see “Document History” about later revised information.**

## Document History

**Document Title: MB9AA30N Series 32-bit ARM® Cortex®-M3 FM3 Microcontroller**

**Document Number: 002-05640**

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	AKIH	06/19/2015	Migrated to Cypress and assigned document number 002-05640. No change to document contents or format.
*A	5189010	AKIH	04/18/2016	Migrated to Cypress format
*B	5742352	YSKA	05/23/2017	<p>Adapted new Cypress logo</p> <p>Modified RTC description in “<a href="#">Features, Real-Time Clock(RTC)</a>”. Changed starting count value from 01 to 00. Deleted “second, or day of the week” in the Interrupt function.</p> <p>Changed package code as the following in chapter :</p> <p><a href="#">2. Packages</a></p> <p><a href="#">3. Pin Assignment</a></p> <p><a href="#">13. Ordering Information</a></p> <p><a href="#">14. Package Dimensions.</a></p> <p>FTP-64P-M38 -&gt; LQD064, FPT-64P-M39 -&gt; LQG064, LCC-64P-M24 -&gt; VNC064, FPT-80P-M37 -&gt; LQH080, FPT-80P-M40 -&gt; LQJ080, FPT-100P-M23 -&gt; LQI100, FPT-100P-M06 -&gt; PQH100</p> <p>Corrected “J-TAG” to “JTAG” in <a href="#">4. List of Pin Functions</a>.</p> <p>Added Note for JTAG pin in <a href="#">4. List of Pin Functions</a>.</p> <p>Added the Baud rate spec in <a href="#">12.4.9 CSIO/UART Timing</a>.</p>

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