12-Bit, 1.25Msps Sampling A/D Converter with Shutdown

FEATURES

- **1.25Msps Sample Rate**
- **Power Dissipation: 160mW**
- **71dB S/(N + D) and 82dB THD at Nyquist**
- No Pipeline Delay
- Nap (7mW) and Sleep (10µW) Shutdown Modes
- Operates with Internal 15ppm/°C Reference or External Reference
- True Differential Inputs Reject Common Mode Noise
- 20MHz Full Power Bandwidth Sampling
- ±2.5V Bipolar Input Range
- 28-Pin SO Wide Package

APPLICATIONS

- Telecommunications
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition
- Spectrum Analysis
- Imaging Systems

DESCRIPTION

The LTC®1410 is a 0.65µs, 1.25Msps, 12-bit sampling A/D converter that draws only 160mW from ±5V supplies. This easy-to-use device includes a high dynamic range sample-and-hold, a precision reference and requires no external components. Two digitally selectable power shutdown modes provide flexibility for low power systems.

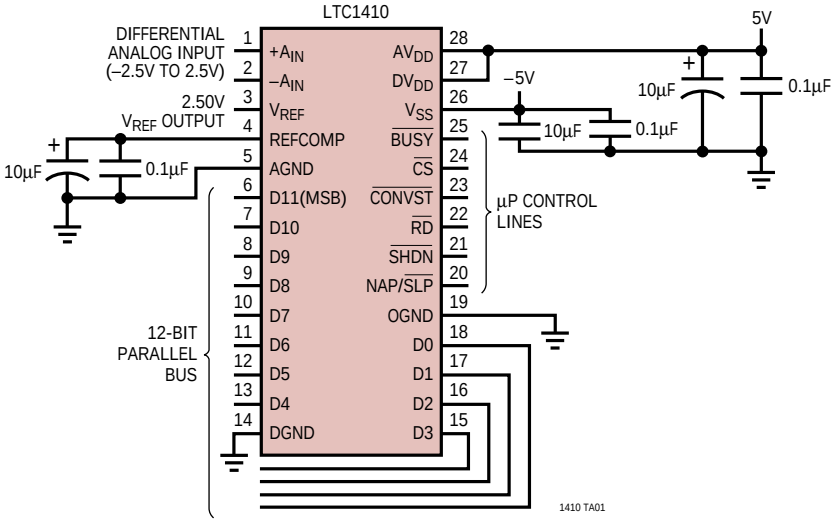
The LTC1410's full-scale input range is ±2.5V. Maximum DC specifications include ±1LSB INL and ±1LSB DNL over temperature. Outstanding AC performance includes 71dB S/(N + D) and 82dB THD at the Nyquist input frequency of 625kHz.

The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 20MHz bandwidth. The 60dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source.

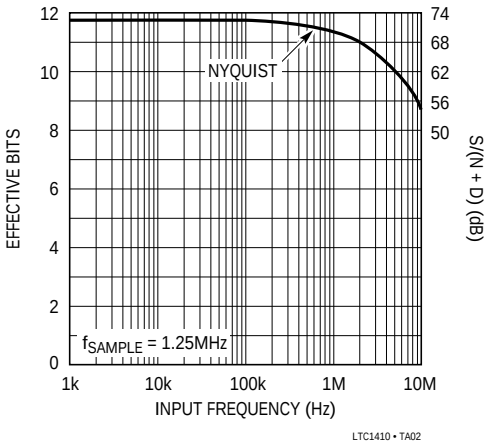
The ADC has a µP compatible, 12-bit parallel output port. There is no pipeline delay in the conversion results. A separate convert start input and a data ready signal (BUSY) ease connections to FIFOs, DSPs and microprocessors.

TYPICAL APPLICATION

Complete 1.25MHz, 12-Bit Sampling A/D Converter



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency

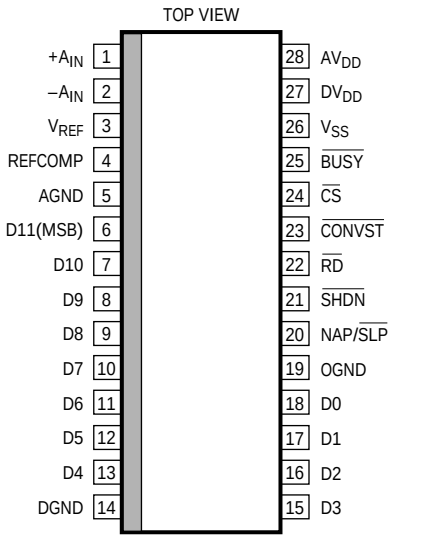


ABSOLUTE MAXIMUM RATINGS

AV_{DD} = DV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) ..... –6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4) ..... V_{SS} – 0.3V to 10V
Digital Output Voltage ..... – 0.3V to V_{DD} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
LTC1410C ..... 0°C to 70°C
LTC1410I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

SW PACKAGE
28-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 90°C/W (SW)
T_{JMAX} = 110°C, θ_{JA} = 95°C/W (G)

ORDER PART NUMBER

LTC1410CG
LTC1410CSW
LTC1410IG
LTC1410ISW

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 7)	●		±0.3	±1	LSB
Differential Linearity Error		●		±0.3	±1	LSB
Offset Error	(Note 8)	 ●		±2	±6 ±8	LSB LSB
Full-Scale Error					±15	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0	●		±15		ppm/°C

ANALOG INPUT

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –4.75V	●		±2.5		V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			17 5		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time		●		50	100	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				–1.5		ns
t_{jitter}	Sample-and-Hold Aperture Delay Time Jitter				5		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	–2.5V < (–A_{IN} = A_{IN}) < 2.5V			60		dB

DYNAMIC ACCURACY

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-(Noise + Distortion) Ratio	100kHz Input Signal (Note 12) 600kHz Input Signal (Note 12)	● ●	70 68	72.5 71.0		dB dB
THD	Total Harmonic Distortion	100kHz Input Signal, First 5 Harmonics 600kHz Input Signal, First 5 Harmonics	 ●		–85 –82	 –74	dB dB
	Peak Harmonic or Spurious Noise	600kHz Input Signal	●		–84	–74	dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz			–84		dB
	Full Power Bandwidth				20		MHz
	Full Linear Bandwidth	(S/(N + D) ≥ 68dB)			2.5		MHz

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.480	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0			±15		ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ –4.75V			0.01 0.01		LSB/V LSB/V
V_{REF} Output Resistance	$\lvert I_{OUT} \rvert$ ≤ 0.1mA			2		kΩ
COMP Output Voltage	I_{OUT} = 0			4.06		V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V I_O = –10µA I_O = –200µA	 ●	 4.0	 4.5 	 	 V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V I_O = 160µA I_O = 1.6mA	 ●		 0.05 0.10	 0.4	 V V
I_{OZ}	High-Z Output Leakage D11 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High-Z Output Capacitance D11 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Notes 10, 11)		4.75		5.25	V
V_{SS}	Negative Supply Voltage	(Note 10)		–4.75		–5.25	V
I_{DD}	Positive Supply Current Nap Mode Sleep Mode	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = 5V $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V	●		12 1.5 1	16 2.3 100	mA mA µA
I_{SS}	Negative Supply Current Nap Mode Sleep Mode	$\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = 5V $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V	●		20 10 1	30 200 100	mA µA µA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
P_D	Power Dissipation				160	230	mW
	Nap Mode	$\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V			7.5	12	mW
	Sleep Mode	SHDN = 0V, NAP/SLP = 0V			0.01	1	mW

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	1.25			MHz
t_{CONV}	Conversion Time		●		650	750	ns
t_{ACQ}	Acquisition Time		●		50	100	ns
$t_{ACQ+CONV}$	Throughput Time (Acquisition + Conversion)		●			800	ns
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time	(Notes 9, 10)	●	0			ns
t_2	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Notes 9, 10)	●	10			ns
t_3	NAP/$\overline{SLP}\downarrow$ to $\overline{SHDN}\downarrow$ Setup Time	(Notes 9, 10)	●	10			ns
t_4	$\overline{SHDN}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time	(Note 10)			200		ns
t_5	$\overline{CONVST}$ Low Time	(Notes 10, 11)	●	40			ns
t_6	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	C_L = 25pF	 ●		10	 50	ns ns
t_7	Data Ready Before $\overline{BUSY}\uparrow$		 ●	20 15	35		ns ns
t_8	Delay Between Conversions	(Note 10)	●	40			ns
t_9	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$	(Note 10)	●	–5			ns
t_{10}	Data Access Time After $\overline{RD}\downarrow$	C_L = 25pF C_L = 100pF	 ● ●		15 20	25 35 35 50	ns ns ns ns
t_{11}	Bus Relinquish Time	 Commercial Industrial	 ● ●		8	20 25 30	ns ns ns
t_{12}	$\overline{RD}$ Low Time		●	t_{10}			ns
t_{13}	$\overline{CONVST}$ High Time		●	40			ns
t_{14}	Aperture Delay of Sample-and-Hold				–1.5		ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, OGND and AGND wired together unless otherwise noted.

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below V_{SS}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, V_{SS} = –5V, f_{SAMPLE} = 1.25MHz, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended $+A_{IN}$ input with $-A_{IN}$ grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

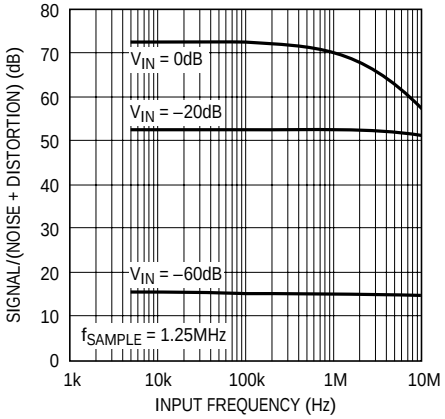
Note 10: Recommended operating conditions.

Note 11: The falling $\overline{CONVST}$ edge starts a conversion. If $\overline{CONVST}$ returns high at a critical point during the conversion it can create small errors. For best results ensure that $\overline{CONVST}$ returns high either within 425ns after the start of the conversion or after $\overline{BUSY}$ rises.

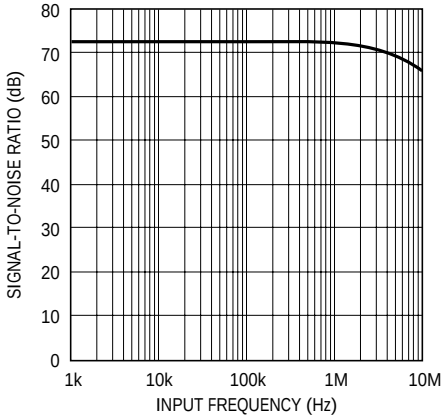
Note 12: Signal-to-noise ratio (SNR) is measured at 100kHz and distortion is measured at 600kHz. These results are used to calculate signal-to-noise plus distortion (SINAD).

TYPICAL PERFORMANCE CHARACTERISTICS

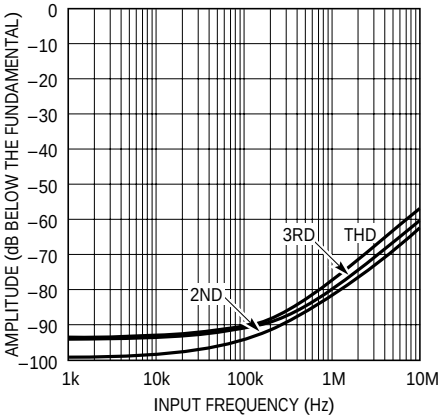
S/(N + D) vs Input Frequency and Amplitude



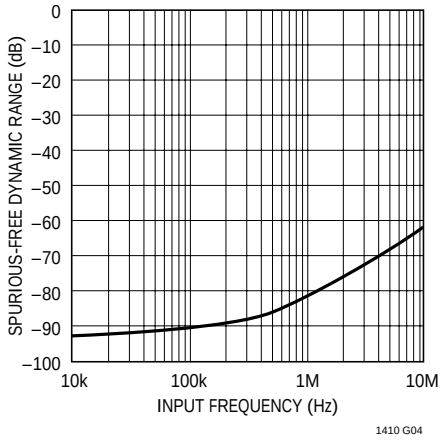
Signal-to-Noise Ratio vs Input Frequency



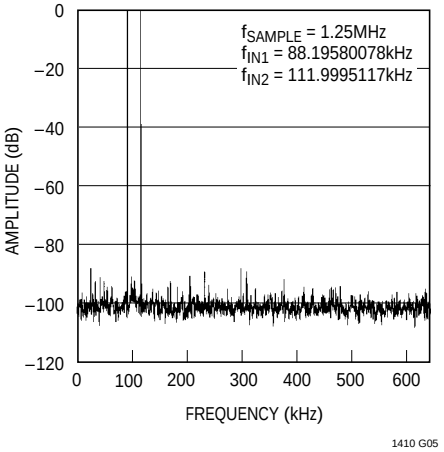
Distortion vs Input Frequency



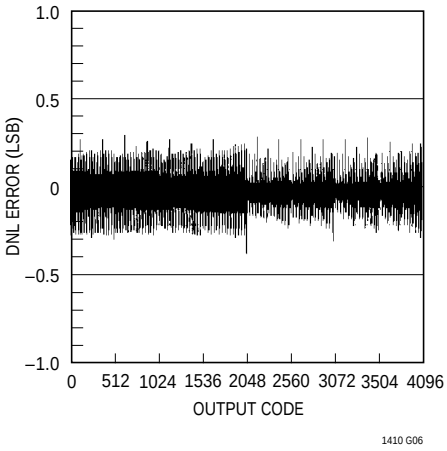
Spurious-Free Dynamic Range vs Input Frequency



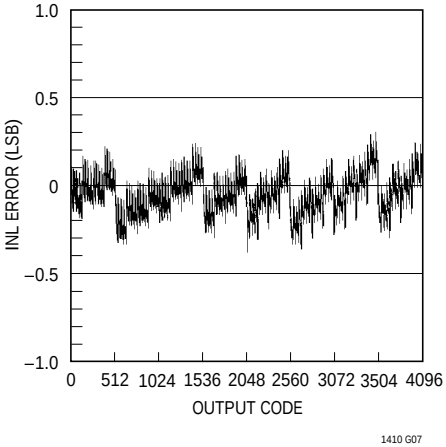
Intermodulation Distortion Plot



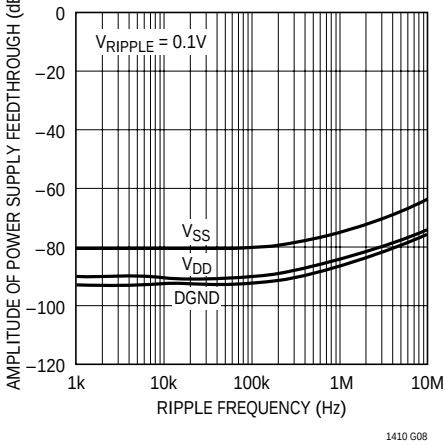
Differential Nonlinearity vs Output Code



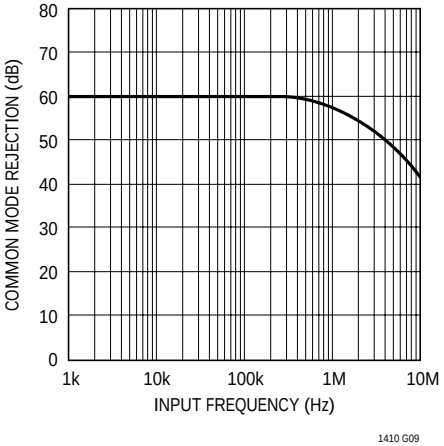
Integral Nonlinearity vs Output Code



Power Supply Feedthrough vs Ripple Frequency



Input Common Mode Rejection vs Input Frequency



PIN FUNCTIONS

+A_{IN} (Pin 1): Positive Analog Input, ±2.5V.

–A_{IN} (Pin 2): Negative Analog Input, ±2.5V.

V_{REF} (Pin 3): 2.50V Reference Output.

REFCOMP (Pin 4): 4.06V Reference Bypass Pin. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic.

AGND (Pin 5): Analog Ground.

D11 to D4 (Pins 6 to 13): Three-State Data Outputs.

DGND (Pin 14): Digital Ground for Internal Logic. Tie to AGND.

D3 to D0 (Pins 15 to 18): Three-State Data Outputs.

OGND (Pin 19): Digital Ground for Output Drivers. Tie to AGND.

NAP/$\overline{SLP}$ (Pin 20): Power Shutdown Mode. Selects the mode invoked by the $\overline{SHDN}$ pin. Low selects Sleep mode and high selects quick wake-up Nap mode.

$\overline{SHDN}$ (Pin 21): Power Shutdown Input. A low logic level will invoke the Shutdown mode selected by the NAP/$\overline{SLP}$ pin.

$\overline{RD}$ (Pin 22): Read Input. This enables the output drivers when $\overline{CS}$ is low.

$\overline{CONVST}$ (Pin 23): Conversion Start Signal. This active low signal starts a conversion on its falling edge.

$\overline{CS}$ (Pin 24): The Chip Select input must be low for the ADC to recognize $\overline{CONVST}$ and $\overline{RD}$ inputs.

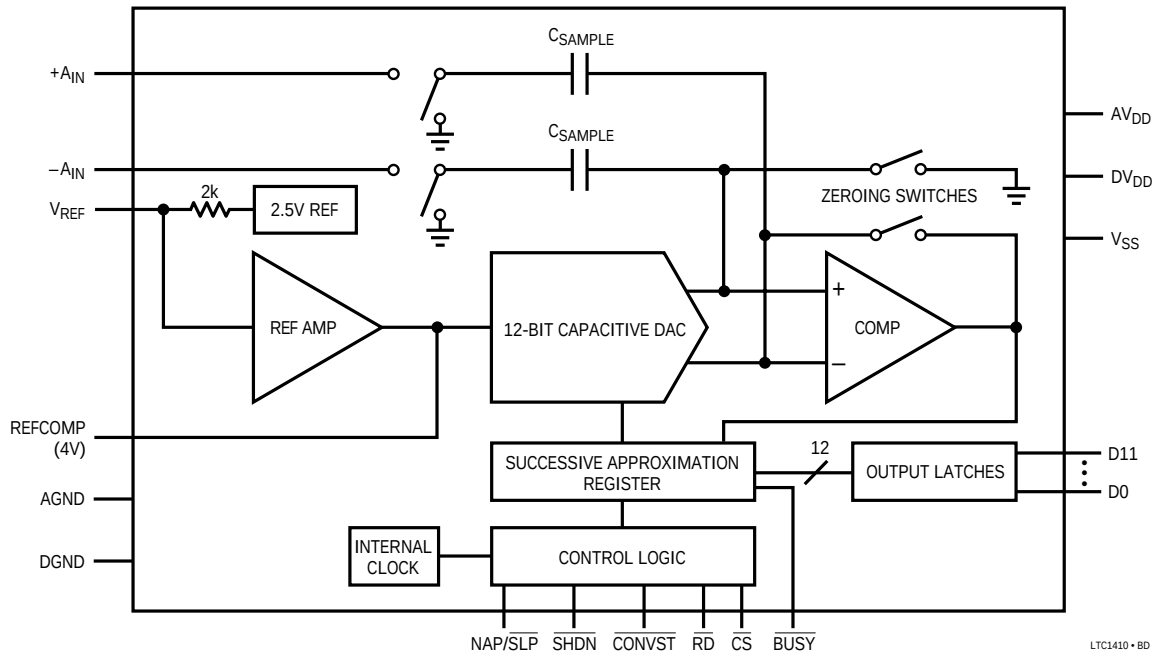
$\overline{BUSY}$ (Pin 25): The $\overline{BUSY}$ output shows the converter status. It is low when a conversion is in progress. Data valid on the rising edge of $\overline{BUSY}$.

V_{SS} (Pin 26): –5V Negative Supply. Bypass to AGND with 10µF tantalum in parallel 0.1µF ceramic.

DV_{DD} (Pin 27): 5V Positive Supply. Short to Pin 28.

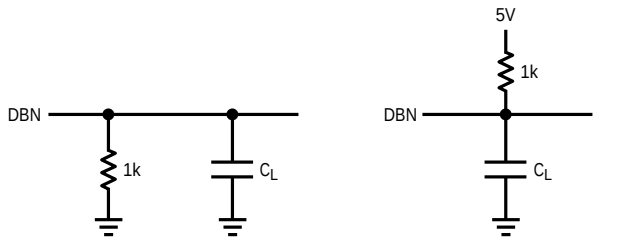
AV_{DD} (Pin 28): 5V Positive Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic.

FUNCTIONAL BLOCK DIAGRAM

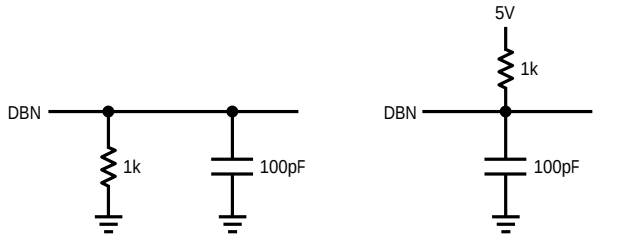


TEST CIRCUITS

Load Circuits for Access Timing



Load Circuits for Output Float Delay



APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1410 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of the conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During the conversion, the internal differential 12-bit capacitive DAC output is sequenced by the SAR from the Most Significant Bit (MSB) to the Least Significant Bit (LSB). Referring to Figure 1, the $+A_{IN}$ and $-A_{IN}$ inputs are connected to the sample-and-hold capacitors (C_{SAMPLE}) during the acquire phase and the comparator offset is nulled by the zeroing switches. In this acquire phase, a minimum duration of 100ns will provide enough time for the sample-and-hold capacitors to acquire the analog signal. During the convert phase the comparator zeroing switches open, putting the comparator into compare mode. The input switches connect the C_{SAMPLE} capacitors to ground, transferring the differential analog input charge onto the summing junctions. This input charge is successively compared with the binarily-weighted charges supplied by the differential capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the differential DAC output balances the $+A_{IN}$ and $-A_{IN}$ input charges. The SAR contents (a 12-bit data word) which represent the difference of $+A_{IN}$ and $-A_{IN}$ are loaded into the 12-bit output latches.

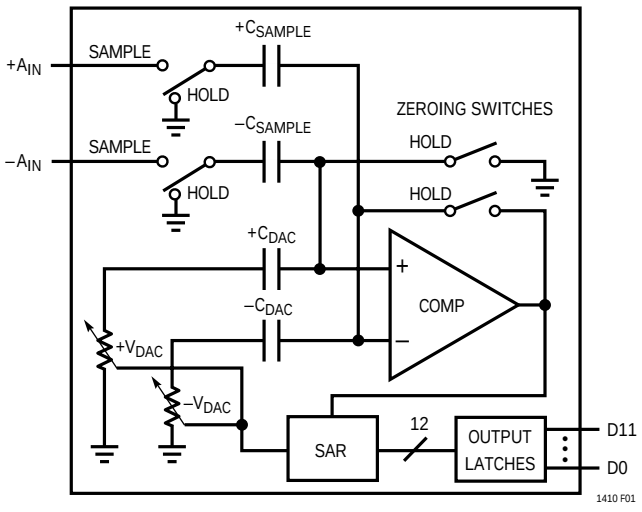


Figure 1. Simplified Block Diagram

APPLICATIONS INFORMATION

DYNAMIC PERFORMANCE

The LTC1410 has excellent high speed sampling capability. Fast Four Transform (FFT) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental.

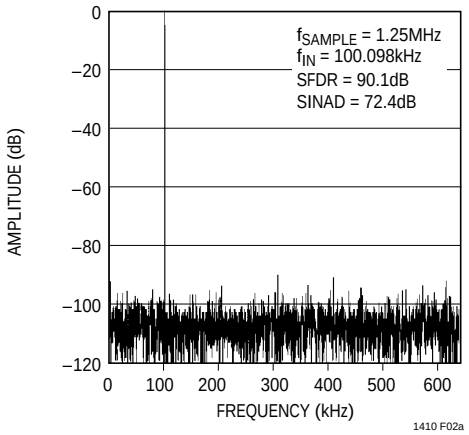


Figure 2a. LTC1410 Nonaveraged 4096 Point FFT, 100kHz Input

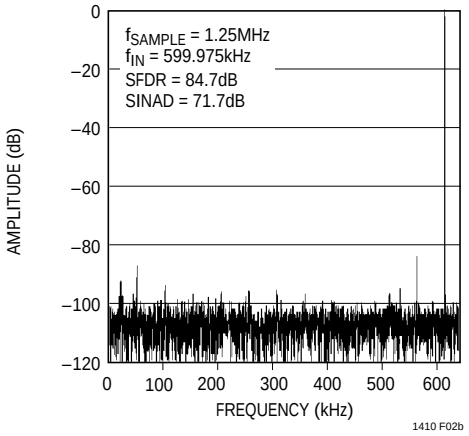


Figure 2b. LTC1410 Nonaveraged 4096 Point FFT, 600kHz Input

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figures 2a and 2b shows a typical spectral content with a 1.25MHz sampling rate for 100kHz and 600kHz inputs. The dynamic performance is excellent for input frequencies up to the Nyquist limit of 625kHz and beyond.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) – 1.76]/6.02$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 1.25MHz the LTC1410 maintains very good ENOBs up to the Nyquist input frequency of 625kHz and beyond. Refer to Figure 3.

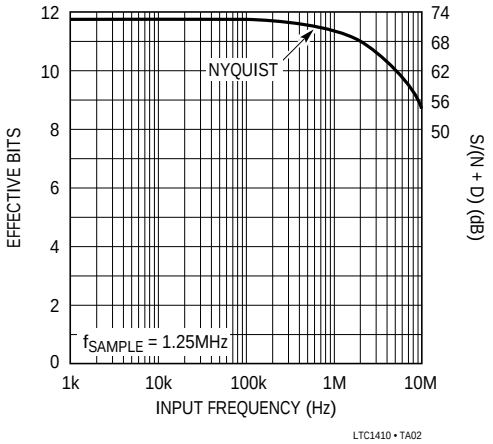


Figure 3. Effective Bits and Signal/(Noise + Distortion) vs Input Frequency

Total Harmonic Distortion (THD)

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots V_n^2}}{V_1}$$

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where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_n are the amplitudes of the second through nth harmonics. THD vs Input Frequency is shown in Figure 4. The LTC1410 has good distortion performance up to the Nyquist frequency and beyond.

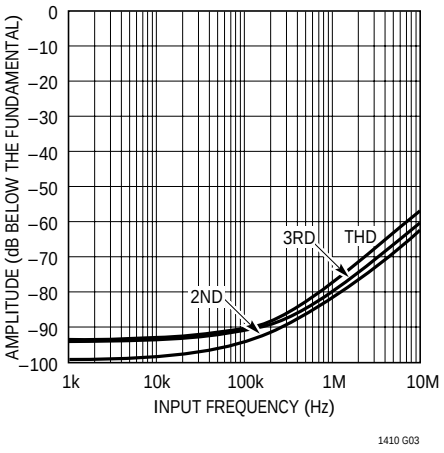

Figure 4. Distortion vs Input Frequency

Intermodulation Distortion (IMD)

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce Intermodulation Distortion in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of $mf_a \pm nf_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include $(f_a + f_b)$. If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\left(f_a + f_b\right) = 20 \log \frac{\text{Amplitude at } \left(f_a \pm f_b\right)}{\text{Amplitude at } f_a}$$

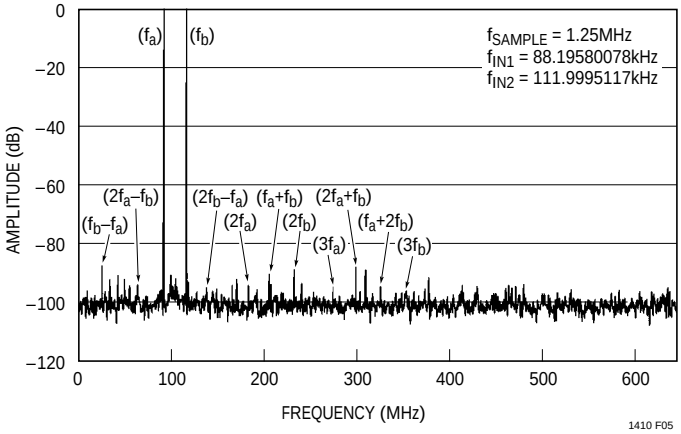

Figure 5. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibel relative to the RMS value of a full-scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1410 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist frequency. The noise floor stays very low at high frequencies; S/(N + D) does not become dominated by distortion until frequencies far beyond Nyquist.

Driving the Analog Input

The differential analog inputs of the LTC1410 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the $–A_{IN}$ input is grounded). The $+A_{IN}$ and $–A_{IN}$ inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold

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capacitors at the end of conversion. During conversion the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low then the LTC1410 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 6). For minimum acquisition time with high source impedance, a buffer amplifier should be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 100ns for full throughput rate).

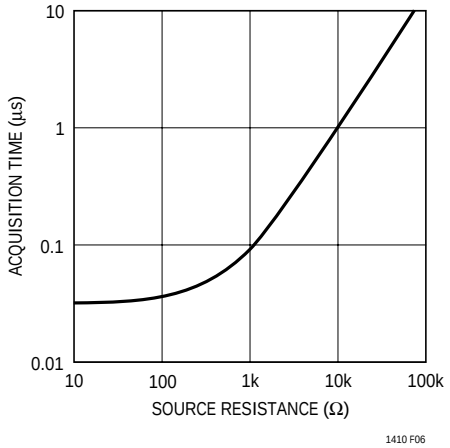

Figure 6. Acquisition Time vs Source Resistance

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, choose an amplifier that has a low output impedance (< 100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of +1 and has a closed-loop bandwidth of 50MHz, then the output impedance at 50MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 20MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's inputs include the LT®1360, LT1220, LT1223, LT1224 and LT1227 op amps.

The noise and the distortion of the input amplifier must also be considered since they will add to the LTC1410 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 20MHz. Any noise that is present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is usually sufficient. For example, Figure 7 shows a 1000pF capacitor from $+A_{IN}$ to ground and a 100Ω source resistor will limit the input bandwidth to 1.6MHz. Simple RC filters work well for AC applications, but they will limit the transient response. For full speed operation, amplifiers with fast settling and low noise should be chosen.

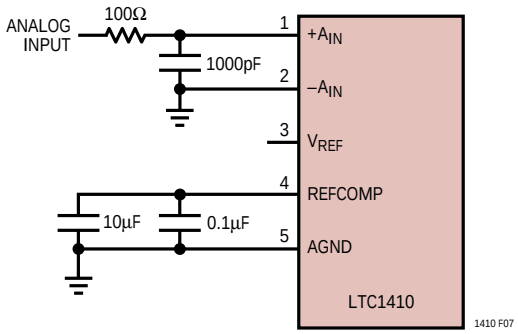

Figure 7. RC Input Filter

Internal Reference

The LTC1410 has an on-chip, temperature compensated, curvature corrected, bandgap reference which is factory trimmed to 2.500V. It is connected internally to a reference amplifier and is available at V_{REF} (Pin 3). See Figure 8a. A 2k resistor is in series with the output so that it can be

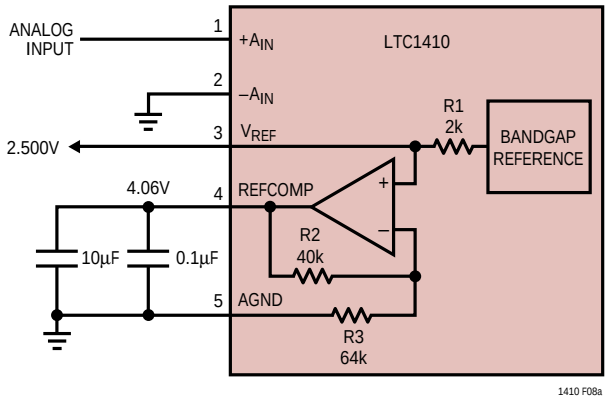

Figure 8a. LTC1410 Reference Circuit

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easily overdriven in applications where an external reference is required. The reference amplifier provides buffering between the internal reference and the capacitive DAC. The reference amplifier compensation pin REFCOMP (Pin 4), must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 1µF or greater. For the best noise performance, a 10µF tantalum in parallel with 0.1µF ceramic is recommended.

The V_{REF} pin can be driven with an external reference (Figure 8b), a DAC or other means to provide input span adjustment. The V_{REF} should be kept in the range of 2.25V to 2.75V for specified linearity.

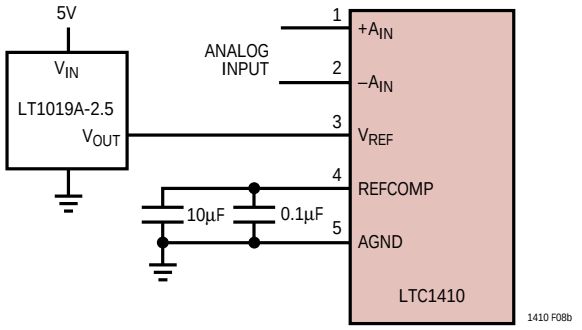

Figure 8b. Using the LT1019-2.5 as an External Reference

Full-Scale and Offset Adjustment

Figure 9 shows the ideal input/output characteristics for the LTC1410. The code transitions occur midway between successive integer LSB values (i.e., –FS + 0.5LSB, –FS + 1.5LSB, –FS + 2.5LSB, . . . FS – 1.5LSB, FS – 0.5LSB).The output is two's complement binary with 1LSB = [(+FS) – (–FS)]/4096 = 5V/4096 = 1.22mV.

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 10 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the $-A_{IN}$ input. For zero offset error apply –0.61mV (i.e., –0.5LSB) at $+A_{IN}$ and adjust the offset at the $-A_{IN}$ input until the output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 2.49817V (FS – 1.5LSBs) is applied to A_{IN} and R2 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

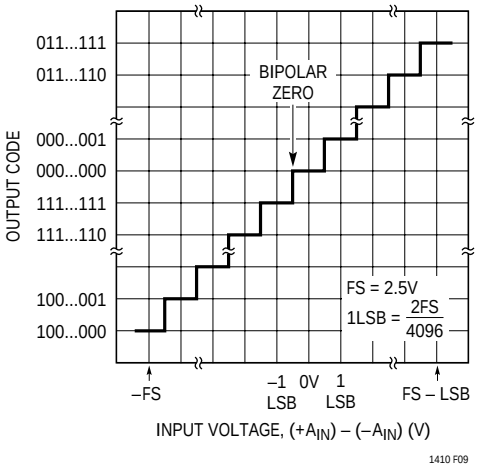

Figure 9. LTC1410 Transfer Characteristics

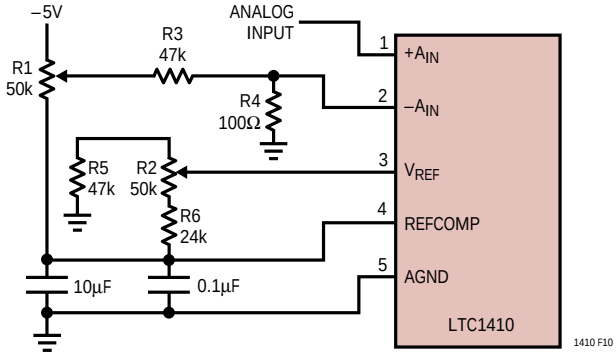

Figure 10. Offset and Full-Scale Adjust Circuit

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1410, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. Particular care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

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High quality tantalum and ceramic bypass capacitors should be used at the V_{DD}, V_{SS} and REFCOMP pins as shown in the Typical Application on the first page of this data sheet. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1410 has differential inputs to minimize noise coupling. Common mode noise on the $+A_{IN}$ and $-A_{IN}$ leads will be rejected by the input CMRR. The $-A_{IN}$ input can be used as a ground sense for the $+A_{IN}$ input; the LTC1410 will hold and convert the difference voltage between $+A_{IN}$ and $-A_{IN}$. The leads to $+A_{IN}$ (Pin 1) and $-A_{IN}$ (Pin 2) should be kept as short as possible. In applications where this is not possible, the $+A_{IN}$ and $-A_{IN}$ traces should be run side by side to equalize coupling.

A single point analog ground separate from the logic system ground should be established with an analog ground plane at Pin 5 (AGND) or as close as possible to the ADC. Pin 14 and Pin 19 (ADC's DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a wait state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion.

Internal Clock

The A/D converter has an internal clock that eliminates the need of synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 0.65µs and a maximum conversion time over the full operating temperature range of 0.75µs. No external adjustments are required. The guaranteed maximum acquisition time is 100ns. In addition, throughput time of 800ns and a minimum sampling rate of 1.25Msps is guaranteed.

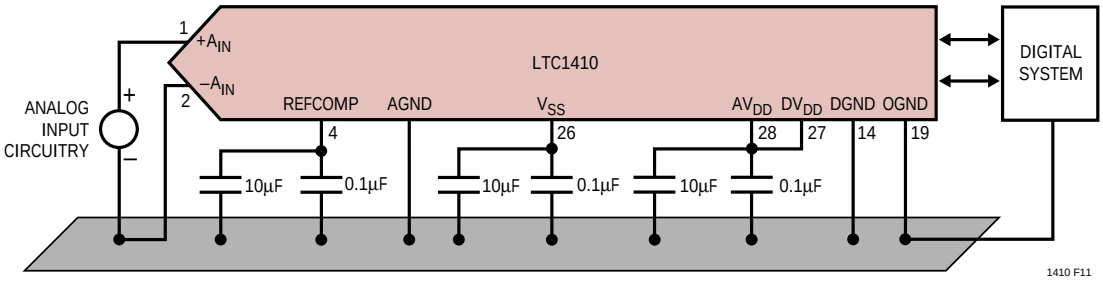

Figure 11. Power Supply Grounding Practice

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Power Shutdown

The LTC1410 provides two power shutdown modes, Nap and Sleep, to save power during inactive periods. The Nap mode reduces the power by 95% and leaves only the digital logic and reference powered up. The wake-up time from Nap to active is 200ns. In Sleep mode all bias currents are shut down and only leakage current remains — about 1µA. Wake-up time from Sleep mode is much slower since the reference circuit must power up and settle to 0.01% for full 12-bit accuracy. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (Pin 4). The wake-up time is 10ms with the recommended 10µF capacitor.

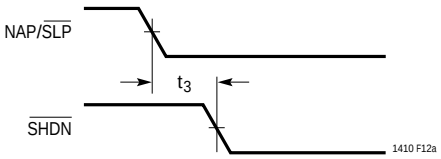

Figure 12a. NAP/SLP to SHDN Timing

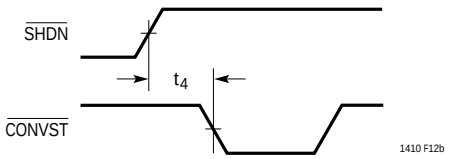

Figure 12b. SHDN to CONVST Wake-Up Timing

Shutdown is controlled by Pin 21 (SHDN), the ADC is in shutdown when it is low. The shutdown mode is selected with Pin 20 (NAP/SLP); high selects Nap.

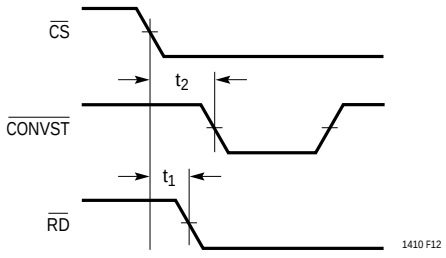

Figure 13. CS to CONVST Setup Timing

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: CONVST, CS and RD. A logic "0" applied to the CONVST pin will start a conversion after the ADC has been selected (i.e., CS is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the BUSY output. BUSY is low during a conversion.

Figures 14 through 18 show several different modes of operation. In modes 1a and 1b (Figures 14 and 15) CS and RD are both tied low. The falling edge of CONVST starts the conversion. The data outputs are always enabled and data can be latched with the BUSY rising edge. Mode 1a shows operation with a narrow logic low CONVST pulse. Mode 1b shows a narrow logic high CONVST pulse.

In mode 2 (Figure 16) CS is tied low. The falling edge of CONVST signal again starts the conversion. Data outputs are in three-state until read by the MPU with the RD signal. Mode 2 can be used for operation with a shared MPU databus.

In slow memory and ROM modes (Figures 17 and 18) CS is tied low and CONVST and RD are tied together. The MPU starts the conversion and reads the output with the RD signal. Conversions are started by the MPU or DSP (no external sample clock).

In slow memory mode the processor applies a logic low to RD (= CONVST), starting the conversion. BUSY goes low forcing the processor into a wait state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; BUSY goes high releasing the processor and the processor takes RD (= CONVST) back high and reads the new conversion data.

In ROM mode, the processor takes RD (= CONVST) low, starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

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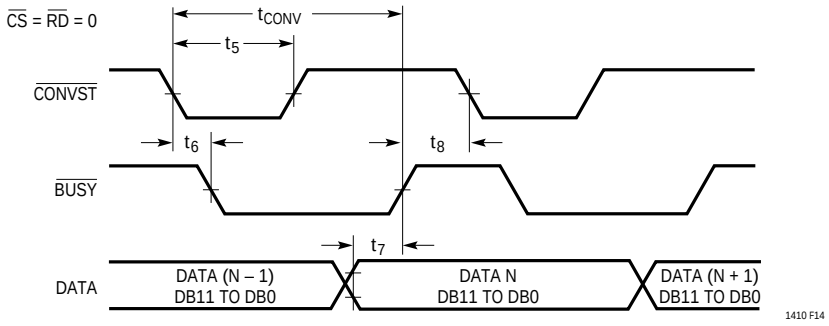


Figure 14. Mode 1a. $\overline{\text{CONVST}}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{\text{CONVST}}$ = ⊓⊓⊓)

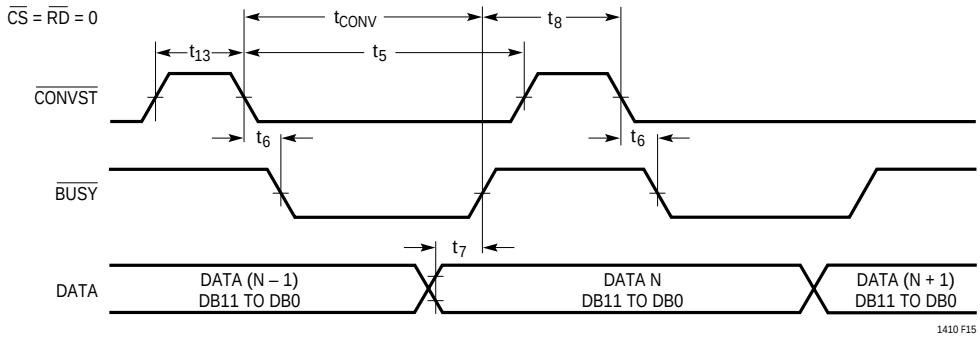


Figure 15. Mode 1b. $\overline{\text{CONVST}}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{\text{CONVST}}$ = ⊓⊓⊓)

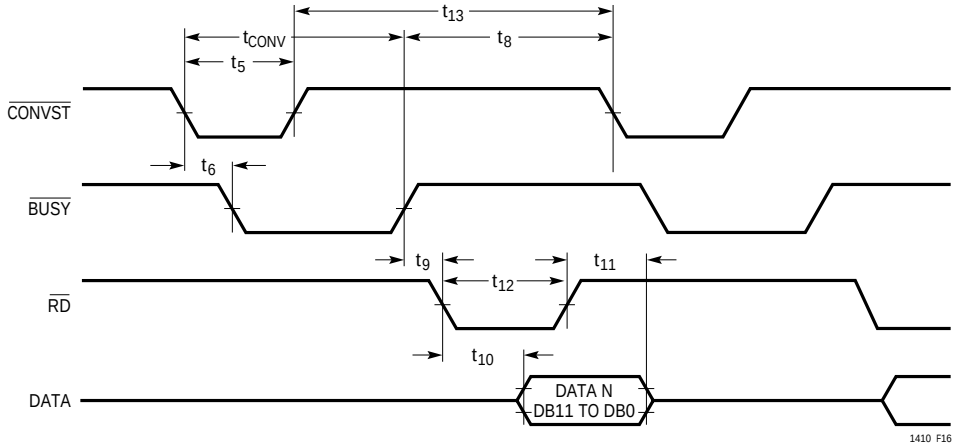


Figure 16. Mode 2. $\overline{\text{CONVST}}$ Starts a Conversion. Data is Read by $\overline{\text{RD}}$

APPLICATIONS INFORMATION

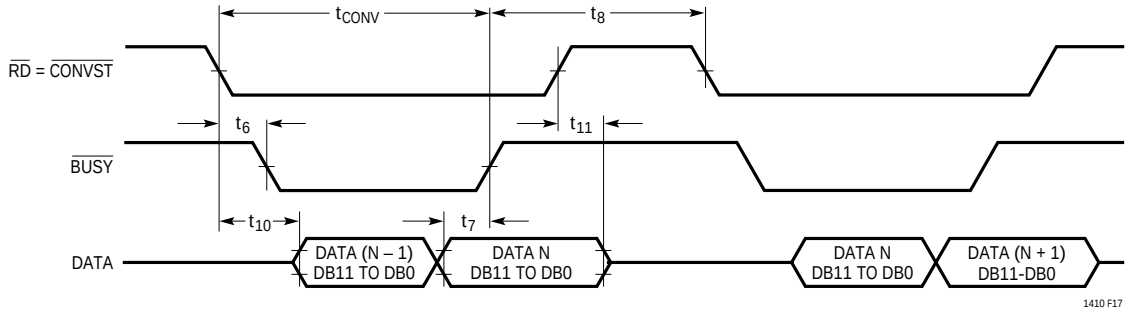


Figure 17. Slow Memory Mode Timing

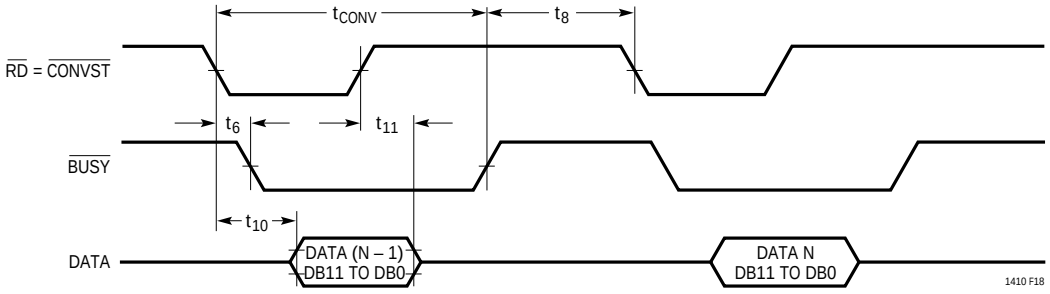
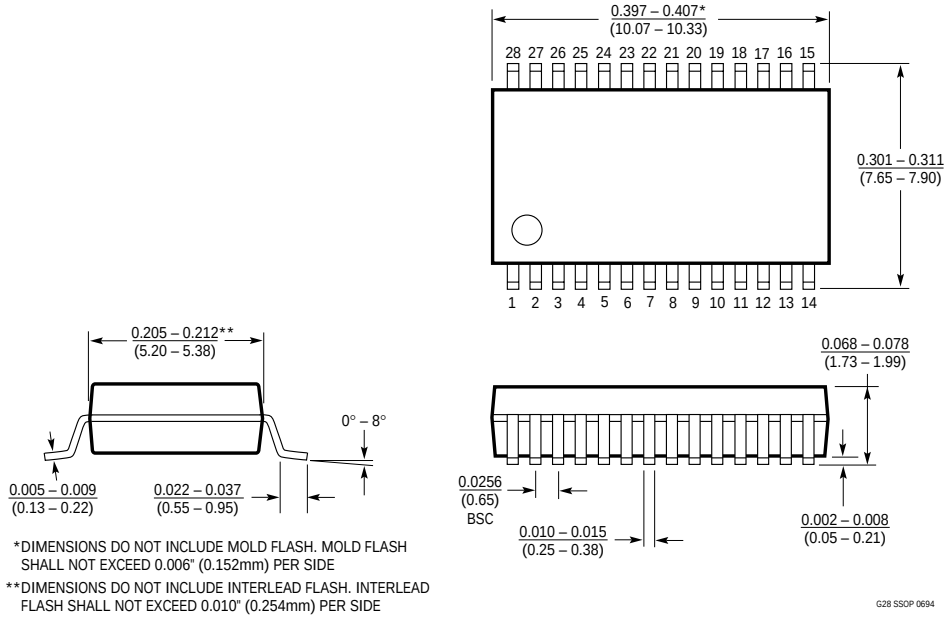


Figure 18. ROM Mode Timing

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



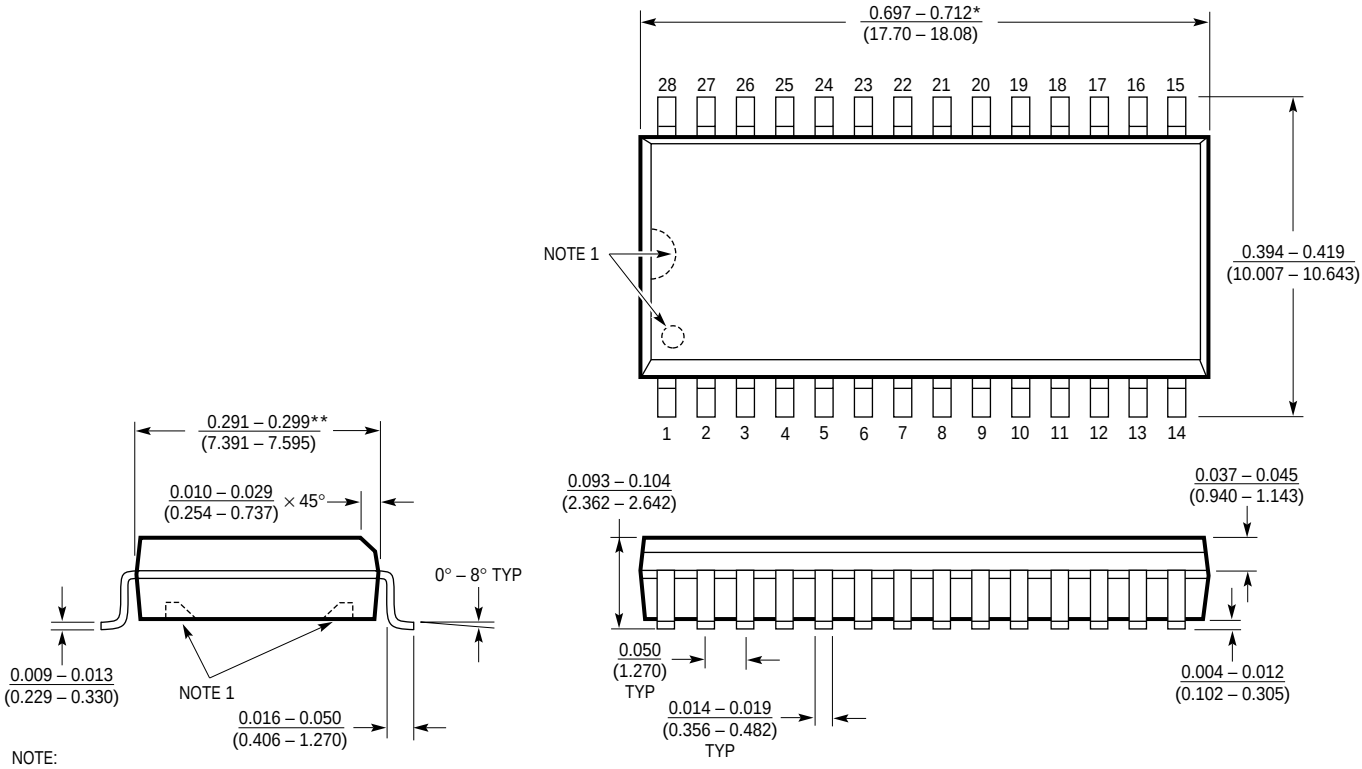
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

SW Package
28-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S28 (WIDE) 0996

RELATED PARTS

12-Bit Sampling A/D Converters

PART NUMBER	DESCRIPTION	COMMENTS
LTC1273/75/76	Complete 5V Sampling 12-Bit ADCs with 70dB SINAD at Nyquist	Lower Power and Cost Effective for $f_{SAMPLE} \leq 300$ksps
LTC1274/77	Low Power 12-Bit ADCs with Nap and Sleep Mode Shutdown	Lowest Power for $f_{SAMPLE} \leq 100$ksps
LTC1278/79	High Speed Sampling 12-Bit ADCs with Shutdown	Cost Effective 12-Bit ADCs — Best for 2-Pair HDSL, $f_{SAMPLE} \leq 500$ksps/600ksps
LTC1282	Complete 3V 12-Bit ADCs with 12mW Power Dissipation	Fully Specified for 3V-Powered Applications, $f_{SAMPLE} \leq 140$ksps

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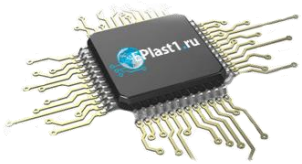
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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