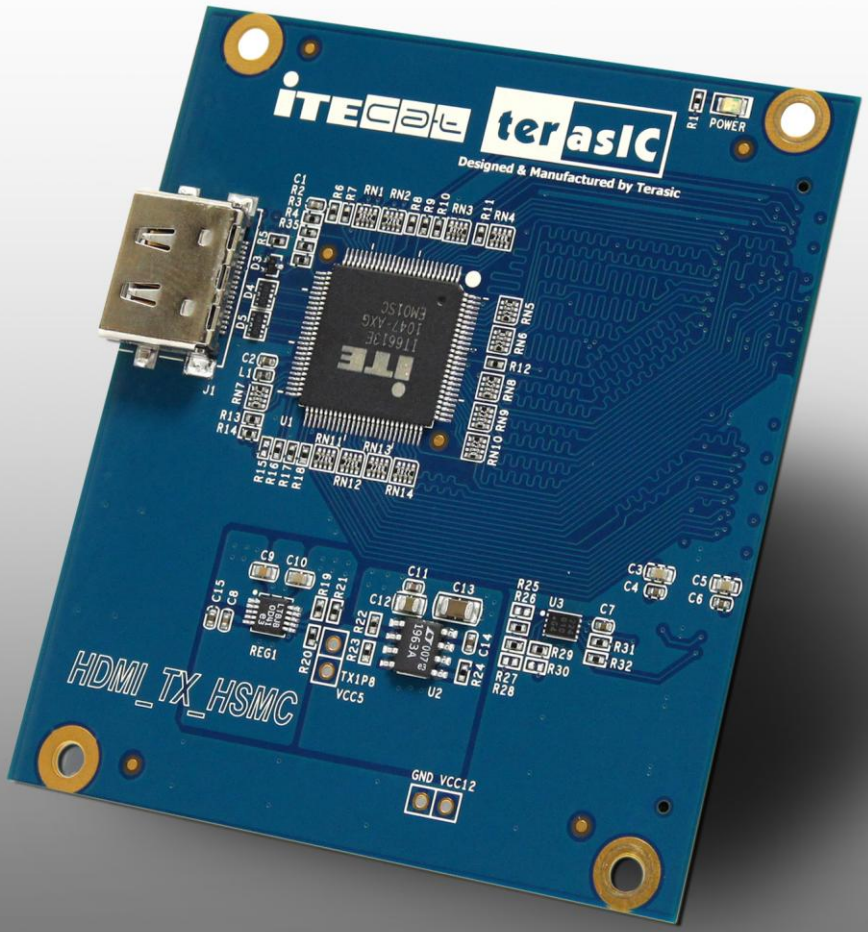
# HDMI_TX_HSMC

## Terasic HDMI Video Transmitter Daughter Board

## User Manual



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# Chapter 1

# Introduction

HDMI_TX_HSMC is a HDMI transmitter daughter board with HSMC (High Speed Mezzanine Connector) interface. Host boards, supporting HSMC-compliant connectors, can control the HDMI_TX_HSMC daughter board through the HSMC interface.

This HDMI_TX_HSMC kit contains complete reference design with source code written in Verilog and C, for HDMI signal transmitting. Based on reference designs, users can easily and quickly develop their applications.

## 1.1 About the KIT

This section describes the package content.

The HDMI_TX_HSMC package, as shown in **Figure 1-1**, contains:

- HDMI_TX_HSMC board x 1
- System CD-ROM x 1

The CD contains technical documents of the HDMI transmitter, and one reference design for DE4 HDMI transmitting with source code.

**Figure 1-1 HDMI_TX_HSMC Package**

## 1.2 Assemble the HDMI_TX_HSMC Board

This section describes how to connect the HDMI_TX_HSMC daughter board to a main board, and uses DE4 as an example.

The HDMI_TX_HSMC board connects to main boards through the HSMC interface. For DE4, the HDMI daughter board can be connected to any one of two HSMC connectors on DE4.

Figure 1-2 shows a HDMI_TX_HSMC daughter board connected to the HSMC connector of DE4. Due to high speed data rate in between, users are strongly recommended to screw the two boards together.

Note. Do not attempt to connect/remove the HDMI_TX_HSMC daughter board to/from the main board when the power is on, or the hardware could be damaged.

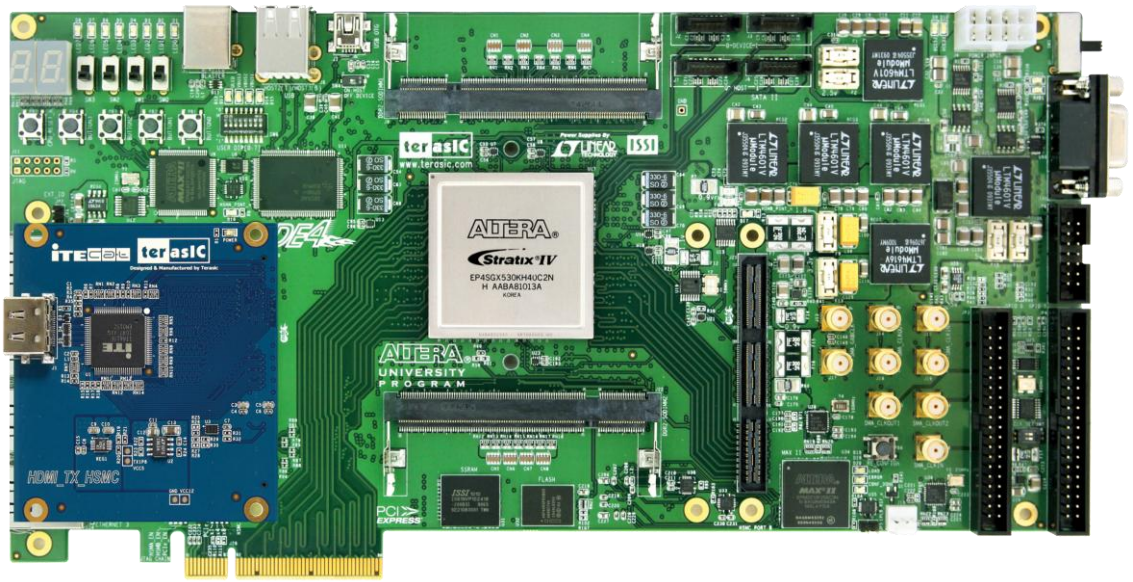


**Figure 1-2 Connect HDMI_TX_HSMC daughter board to DE4 board**

## 1.3 Getting Help

Here are some places to get help if you encounter any problem:

- Email to support@terasic.com
- Taiwan : +886-3-550-8800
- China : +0086-13971483508
- Korea : +82-2-512-7661
- English Support Line: +1-408-512-12336

# Chapter 2

# HDMI_TX_HSMC Board

This chapter will illustrate technical details of HDMI_TX_HSMC board.

## 2.1 Features

This section describes the major features of the HDMI board.

Board Features:

- One HSMC interface for connection purpose
- One HDMI transmitter with single transmitting port
- Powered from 3.3V and 12V pins of HSMC connector

HDMI Transmitter Features:

1. HDMI 1.4 transmitter
2. Compliant with HDMI 1.3, HDMI 1.4a 3D, HDCP 1.4 and DVI 1.0 specifications
3. Supporting link speeds of up to 2.25 Gbps (link clock rate of 225MHZ)
4. Various video input interface supporting digital video standards such as:
   - 24/30/36-bit RGB/YCbCr 4:4:4
   - 16/20/24-bit YCbCr 4:2:2
   - 8/10/12-bit YCbCr 4:2:2 (CCIR-656)
5. Bi-direction Color Space Conversion (CSC) between RGB and YCbCr color space with programmable coefficients
6. Up/down sampling between YCbCr 4:4:4 and YCbCr 4:2:2
7. Dither for conversion from 12-bit/10-bit to component to 8-bit

8. Support Gammat Metadata packet
9. Digital audio input interface supporting:
    - Up to four I2S interface supporting 8-channel audio, with sample rates of 32~192 kHz and sample sizes of 16~24 bits
    - S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio at up to 192kHz frame rate
    - Support for high-bit-rate (HBR) audio such as DTS-HD and Dolby TrueHD through the four I2S interface or the S/PDIF interface, with frame rates as high as 768kHz
    - Support for 8-channel DSD audio through dedicated inputs
    - Compatible with IEC 60958 and IEC 61937
    - Audio down-sampling of 2X and 4X
10. Software programmable, auto-calibrated TMDS source terminations provide for optimal source signal quality
11. Software programmable HDMI output current level
12. MCLK input is optional for audio operation. Users could opt to implement audio input interface with or without MCLK
13. Integrated pre-programmed HDCP keys
14. Purely hardware HDCP engine increasing the robustness and security of HDCP operation
15. Monitor detection through Hot Plug Detection and Receiver Termination Detection
16. Embedded full-function pattern generator
17. Intelligent, programmable power management

**Table** 2-1 lists the supported output video formats:

**Table 2-1 Output video formats supported by the HDMI_TX_HSMC board**

| | | | | *Output Pixel Clock Frequency(MHz)* | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| *Color Space* | *Video Format* | *Bus Width* | *Hsync/ Vsync* | *480i* | *480p* | *XGA* | *720p* | *1080i* | *SXGA* | *1080p* | *UXGA* |
| RGB | 4:4:4 | 24 | Separate | 13.5 | 27 | 65 | 74.25 | 74.25 | 108 | 148.5 | 162 |
| | | 30/36 | | 13.5 | 27 | 65 | 74.25 | 74.25 | 108 | 148.5 | |
| | | 12/15/18 | Separate | 13.5 | 27 | 65 | 74.25 | 74.25 | | | |
| YCbCr | 4:4:4 | 24 | Separate | 13.5 | 27 | 65 | 74.25 | 74.25 | 108 | 148.5 | 162 |
| | | 30/36 | | 13.5 | 27 | 65 | 74.25 | 74.25 | 108 | 148.5 | |
| | | 12/15/18 | Separate | 13.5 | 27 | 65 | 74.25 | 74.25 | | | |
| | 4:2:2 | 16/20/24 | Separate | 13.5 | 27 | | 74.25 | 74.25 | | 148.5 | |
| | | | Embedded | 13.5 | 27 | | 74.25 | 74.25 | | 148.5 | |
| | | 8/10/12 | Separate | 27 | 54 | | 148.5 | 148.5 | | | |
| | | | Embedded | 27 | 54 | | 148.5 | 148.5 | | | |

## 2.2 Layout and Components

The photos of the HDMI_TX_HSMC board are shown in **Figure 2-1** and **Figure 2-2**. They indicate the location of the connectors and key components.

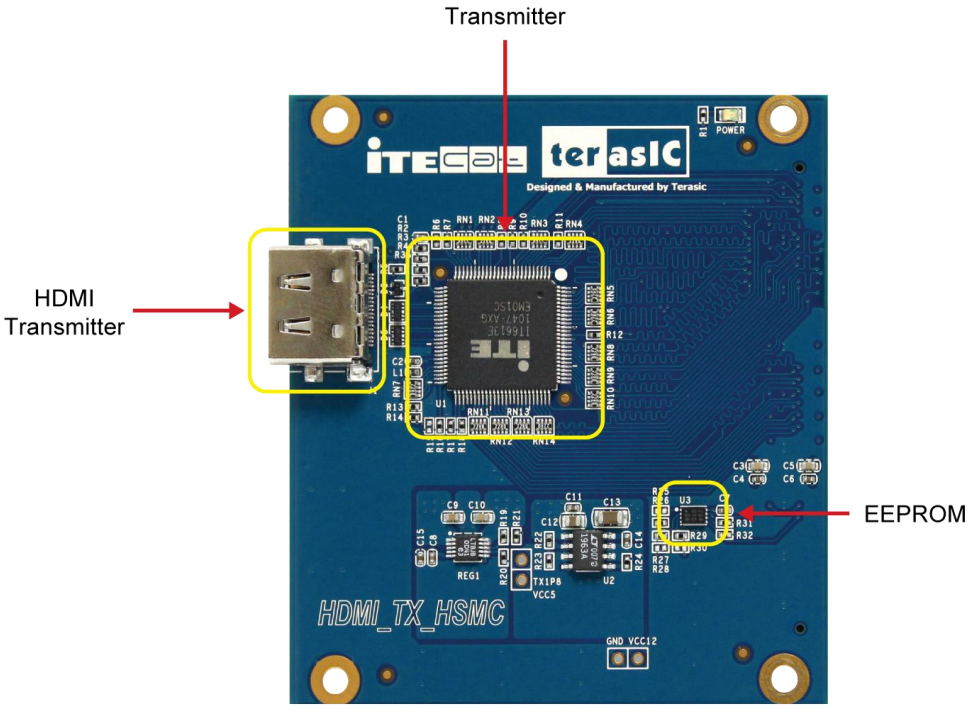



**Figure 2-1 HDMI transmitter on the front of the HDMI_TX_HSMC board**

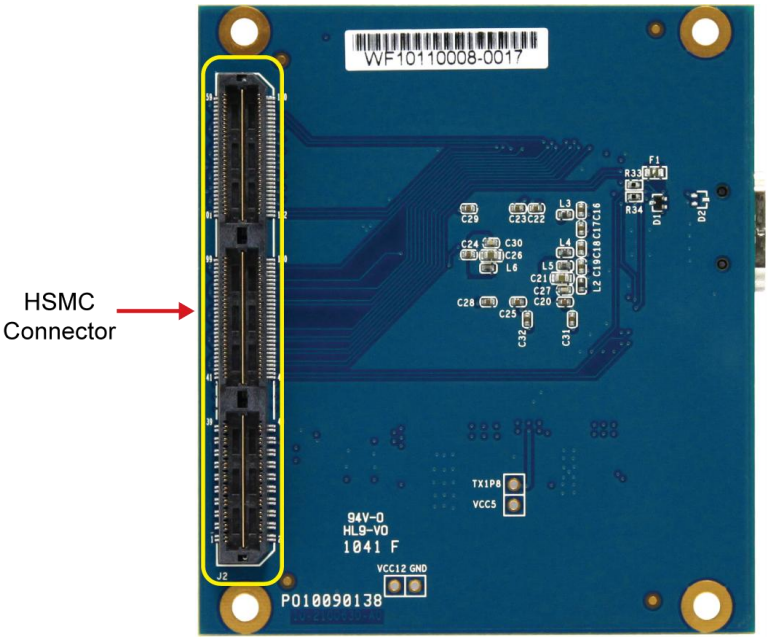



**Figure 2-2 On the back of the HDMI_TX_HSMC board with HSMC connector**

## ■ The HDMI_TX_HSMC board includes the following key components:

- Transmitter (U1)
- Transmitter port (J1)
- HSMC expansion connector (J2)
- TX Regulator (REG1)
- TX Regulator (U2)

## 2.3 Block Diagram of HDMI Signal Transmission

This section describes the block diagram of HDMI signal transmission.

Figure 2-3 shows the block diagram of HDMI signal transmission. Please refer to the schematic included in the CD for more details. The HDMI transmitter is controlled through I2C interface, where the host works as master and the transmitter works as a slave. Because the pin PCADR is pulled low, the transmitter I2C device address is set to 0x98. Through the I2C interface, the host board can access the internal registers of transmitter to control its behavior.

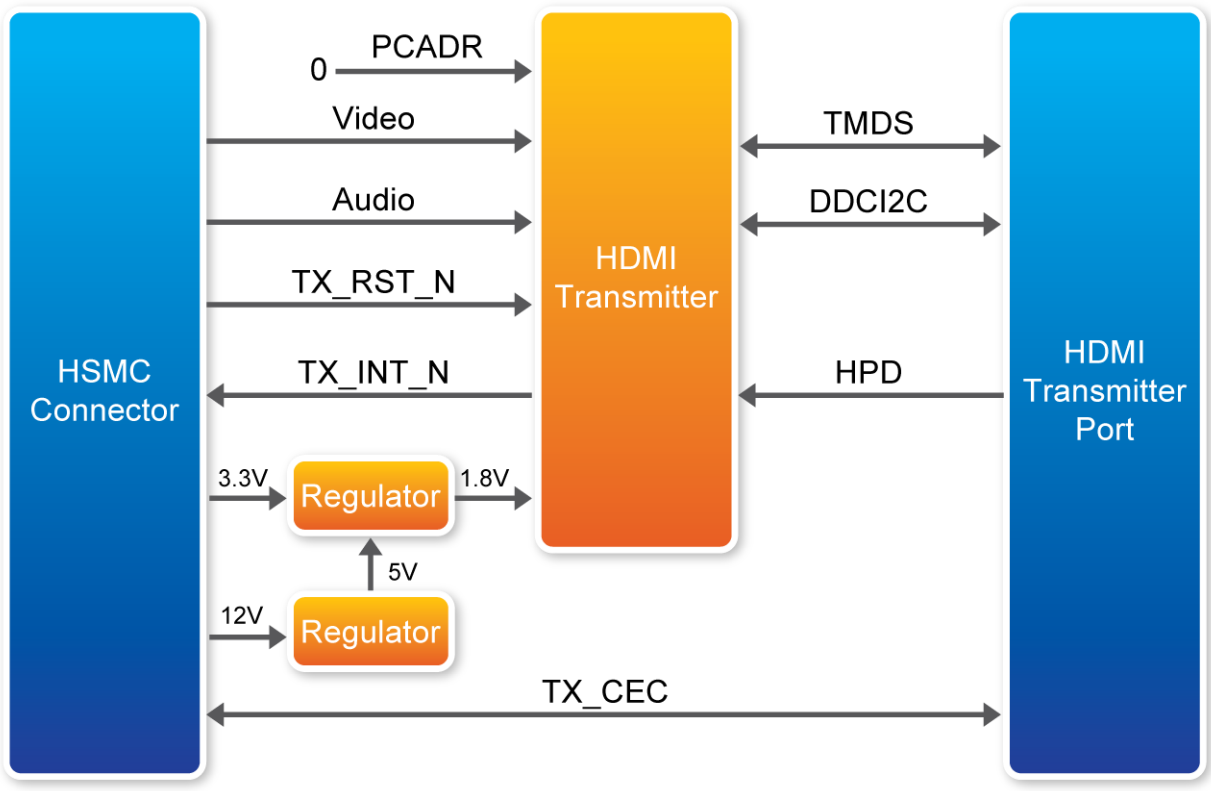



**Figure 2-3 The block diagram of the HDMI signal transmission**

The host can use reset pin TX_RST_N to reset the transmitter, and listen to the interrupt pin TX_INT_N to detect change of the transmitter status. When interrupt happens, the host needs to

read the internal register to find out which event is triggered and perform proper actions for the interrupt.

Here are the 3 steps to control the transmitter:

1. Reset the transmitter from the TX_RST_N pin
2. Initialize the transmitter through the I2C interface
3. Polling the interrupt pin INT_N continuously

- If a HDMI sink device is detected (HDP flag is on):
  - Read and parse EDID to determine the capacity of the attached HDMI sink device
  - Configure desired output video/audio, including color space and color depth
  - Perform HDCP authentication
  - Output video/audio signals to the Video/Audio bus
- Stop video output if a video sink device is removed (HPD flag is off)
- Perform proper actions according to various interrupt events

## 2.4 Generate Pin Assignments

This section describes how to automatically generate a top-level project, including HDMI pin assignments.

Users can easily create the HDMI_TX_HSMC board pin assignments by utilizing the Terasic System Builder (Please visit http://www.terasic.com.tw/en/ to download the latest version of System Builder). Here are the procedures to generate a top-level project for HDMI_TX_HSMC.

- Launch Terasic System Builder(from the following path on the HDMI_TX system CD:HDMI_TX_Tool\DE4_SystemBuilder.exe)
- Select CLOCK, LED x 8, Button x 4, as shown in **Figure 2-4**
- Select HDMI TX on the HSMC Expansion options
- Input desired pin Prefix Name in the dialog of DE4 Configuration

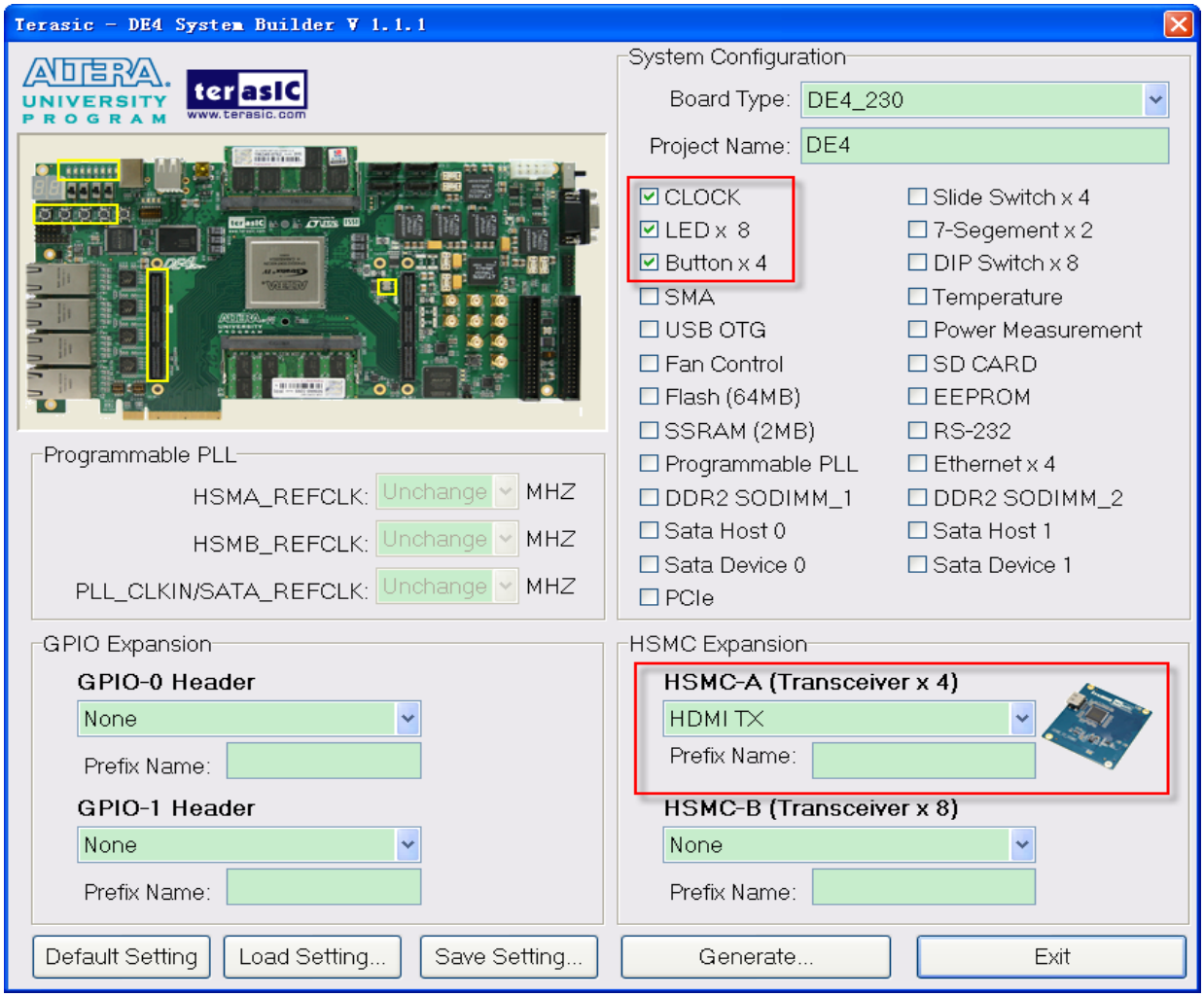


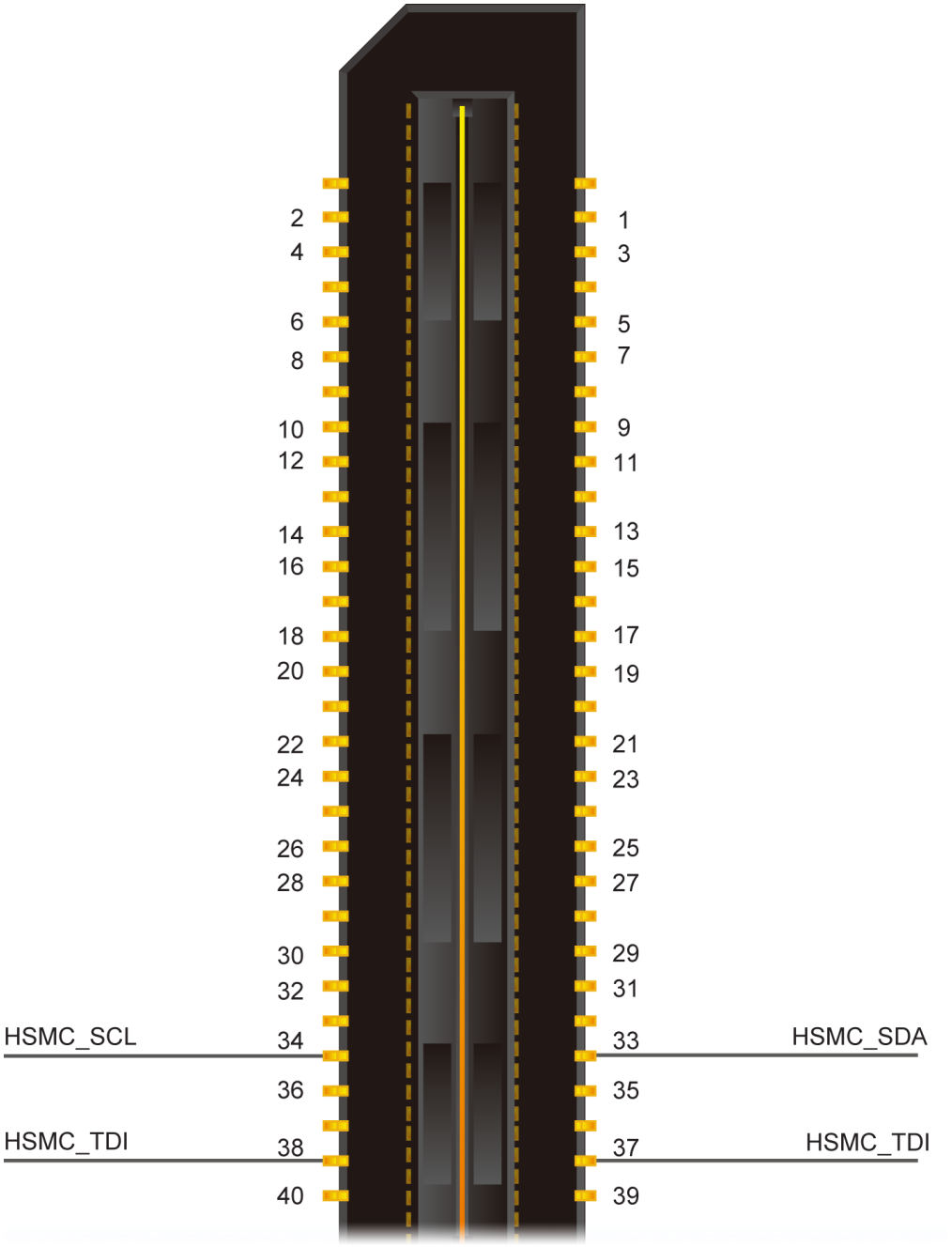

**Figure 2-4 Select the HDMI TX board**

Click “Generate” to generate the desired top-level and pin assignments for a HDMI project.

## 2.5 Pin Definition of HSMC Connector

This section describes pin definition of the HSMC interface onboard.

All the control and data signals of HDMI transmitter are connected to the HSMC connector, so users can fully control the HDMI_TX_HSMC daughter board through the HSMC interface. Power is derived from 3.3V and 12V pins of the HSMC connector. **Figure 2-5** shows the physical pin location and signal name on the HSMC connector.


2
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22
24
26
28
30
32
HSMC_SCL
34
36
HSMC_TDI
38
40
1
3
5
7
9
11
13
15
17
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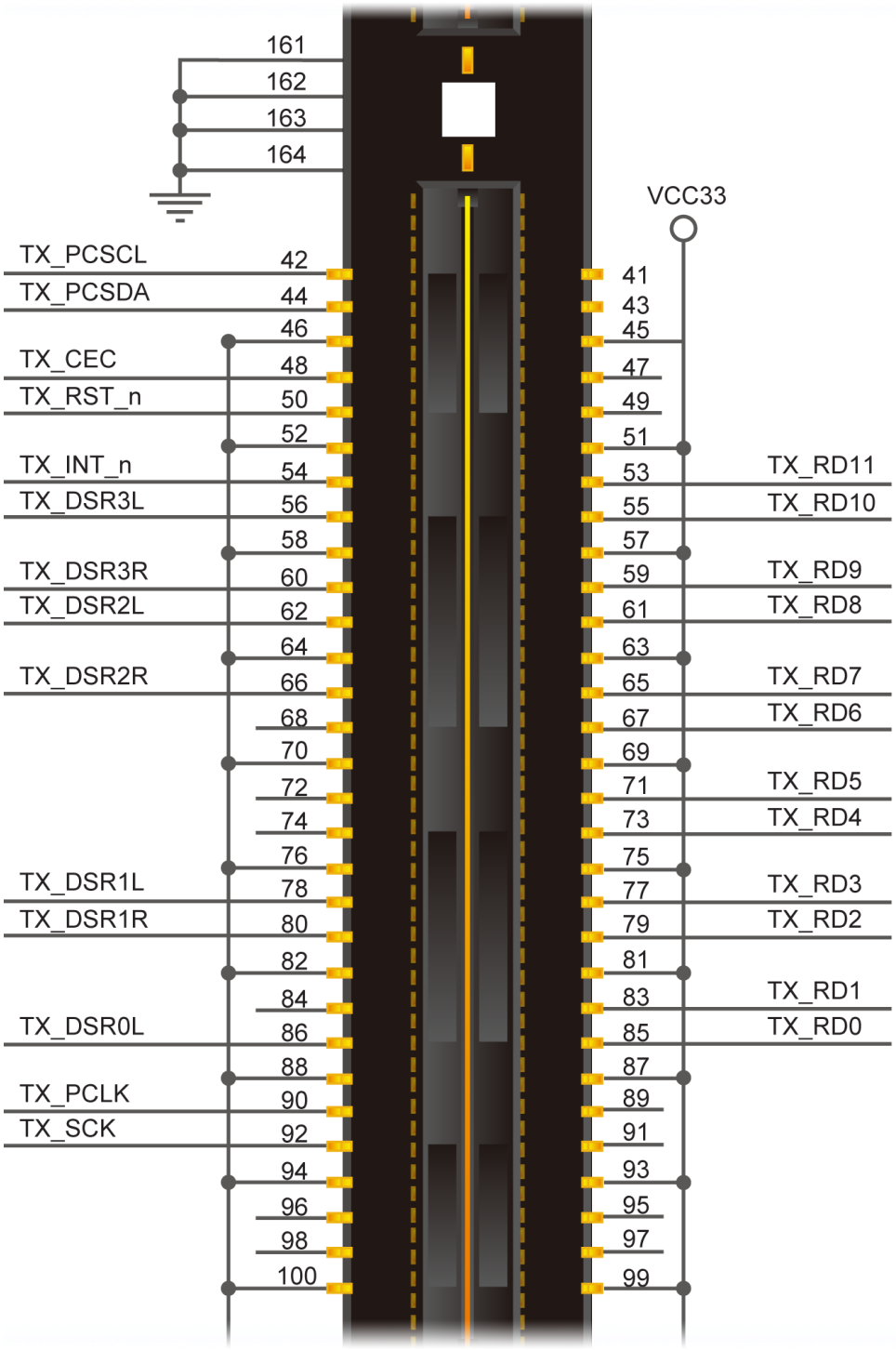
23
25
27
29
31
33
HSMC_SDA
35
37
HSMC_TDI
39


161
162
163
164
VCC33
TX_PCSCL
TX_PCSDA
TX_CEC
TX_RST_n
TX_INT_n
TX_DSR3L
TX_DSR3R
TX_DSR2L
TX_DSR2R
TX_DSR1L
TX_DSR1R
TX_DSR0L
TX_PCLK
TX_SCK
TX_RD11
TX_RD10
TX_RD9
TX_RD8
TX_RD7
TX_RD6
TX_RD5
TX_RD4
TX_RD3
TX_RD2
TX_RD1
TX_RD0
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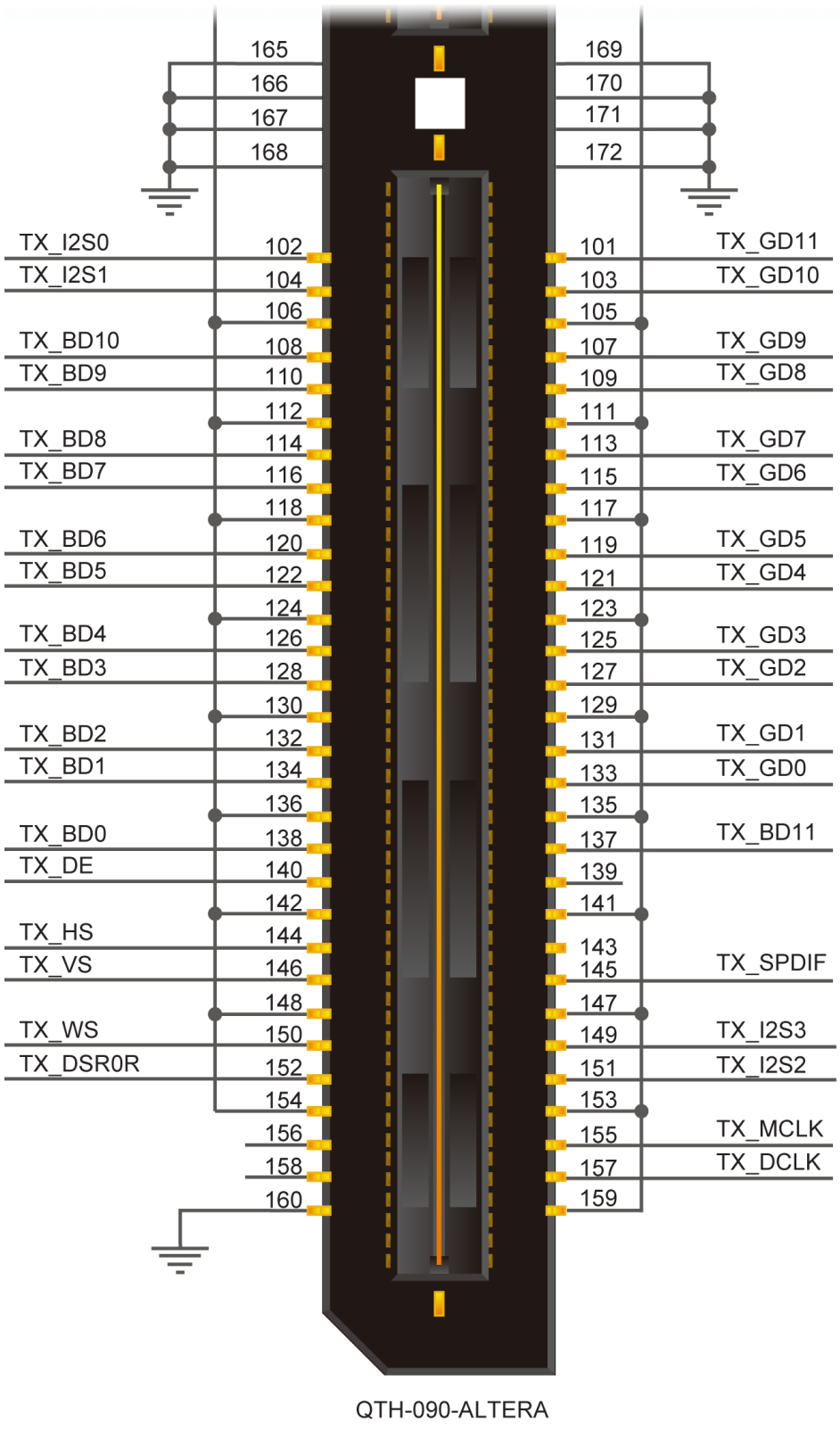


**Figure 2-5 HSMC Connector of HDMI_TX_HSMC board**

Table 2-2 below lists the HSMC signal direction and description.

*Note. The power pins are not shown in the table.*

**Table 2-2 The HSMC pin definition of the HDMI_TX_HSMC board**

| *Signal Name* | *Pin NO.* | *Direction (FPGA View)* | *Description* |
|---|---|---|---|
| HSMC_SDA | 33 | inout | $I^2C$ serial data for on-board EEPROM |
| HSMC_SCL | 34 | output | $I^2C$ serial clock for onboard EEPROM |
| TX_PCSCL | 42 | output | $I^2C$ Clock for DDC |
| TX_PCSDA | 44 | inout | $I^2C$ Data for DDC |
| TX_CEC | 48 | inout | CEC (Consumer Electronics Control) |
| TX_RST_n | 50 | output | Hardware reset pin. Active LOW |
| TX_RD11 | 53 | output | Digital video output pins |
| TX_INT_n | 54 | input | Interrupt output. Default active-low |
| TX_RD10 | 55 | output | Digital video output pins |
| TX_DSR3L | 56 | output | DSD Serial Left CH3 data input |
| TX_RD9 | 59 | output | Digital video output pins |
| TX_DSR3R | 60 | output | DSD Serial Right CH3 data input |
| TX_RD8 | 61 | output | Digital video output pins |
| TX_DSR2L | 62 | output | DSD Serial Left CH2 data input |
| TX_RD7 | 65 | output | Digital video input pins |
| TX_DSR2R | 66 | output | DSD Serial Right CH2 data input |
| TX_RD6 | 67 | output | Digital video output pins |
| TX_RD5 | 71 | output | Digital video output pins |
| TX_RD4 | 73 | output | Digital video output pins |
| TX_RD3 | 77 | output | Digital video output pins |
| TX_DSR1L | 78 | output | DSD Serial Left CH1 data input |
| TX_RD2 | 79 | output | Digital video output pins |
| TX_DSR1R | 80 | output | DSD Serial Right CH1 data input |
| TX_RD1 | 83 | output | Digital video output pins |
| TX_RD0 | 85 | output | Digital video output pins |
| TX_DSR0L | 86 | output | DSD Serial Left CH0 data input |
| TX_PCLK | 90 | output | Input data clock |
| TX_SCK | 92 | output | I2S serial clock input |
| TX_GD11 | 101 | output | Digital video output pins |
| TX_I2S0 | 102 | output | I2S serial data input |
| TX_GD10 | 103 | output | Digital video output pins |
| TX_I2S1 | 104 | output | I2S serial data input |
| TX_GD9 | 107 | output | Digital video output pins |
| TX_BD10 | 108 | output | Digital video output pins |
| TX_GD8 | 109 | output | Digital video output pins |
| TX_BD9 | 110 | output | Digital video output pins |
| TX_GD7 | 113 | output | Digital video output pins |
| TX_BD8 | 114 | output | Digital video output pins |
| TX_GD6 | 115 | output | Digital video output pins |
| TX_BD7 | 116 | output | Digital video output pins |
| TX_GD5 | 119 | output | Digital video output pins |
| TX_BD6 | 120 | output | Digital video output pins |

| | | | |
|---|---|---|---|
| TX_GD4 | 121 | output | Digital video output pins |
| TX_BD5 | 122 | output | Digital video output pins |
| TX_GD3 | 125 | output | Digital video output pins |
| TX_BD4 | 126 | output | Digital video output pins |
| TX_GD2 | 127 | output | Digital video output pins |
| TX_BD3 | 128 | output | Digital video output pins |
| TX_GD1 | 131 | output | Digital video output pins |
| TX_BD2 | 132 | output | Digital video output pins |
| TX_GD0 | 133 | output | Digital video output pins |
| TX_BD1 | 134 | output | Digital video output pins |
| TX_BD11 | 137 | output | Digital video output pins |
| TX_BD0 | 138 | output | Digital video output pins |
| TX_DE | 140 | output | Data enable |
| TX_HS | 144 | output | Horizontal sync. signal |
| TX_SPDIF | 145 | output | S/PDIF audio input |
| TX_VS | 146 | output | Vertical sync. signal |
| TX_I2S3 | 149 | output | I2S serial data input |
| TX_WS | 150 | output | I2S word select input |
| TX_I2S2 | 151 | output | I2S serial data input |
| TX_DSR0R | 152 | output | Digital video output pins |
| TX_MCLK | 155 | output | Audio master clock input |
| TX_DCLK | 157 | output | DSD Serial audio clock input |

# Chapter 3

# Demonstration

This chapter illustrates the video/audio demonstration for the HDMI_TX_HSMC board. There are three versions of source code available for connecting to different main boards, DE4, A2GX and DE2-115. Users may modify the reference designs for various purposes accordingly.

## 3.1 Introduction

■ **This section describes the functionality of the demonstration briefly**

This demonstration shows how to use DE4 (or A2GX, DE2-115) to control the HDMI_TX_HSMC board. The demonstration includes Transmission-Only:

Generate HDMI Video signal for transmission, including various video formats and color space. There are 11 video formats available. The color space includes RGB444, YUV422, and YUV444.

## 3.2 System Requirements

The following items are required for transmission-only demonstration.

Transmission-Only

- HDMI_TX_HSMC x 1
- DE4 Board x 1
- LCD monitor with at least one HDMI input x 1
- HDMI Cable x 1
- THCB-HMF2 x1

## 3.3 Setup the Demonstration

**Figure 3-1** shows the THCB-HMF2 card.

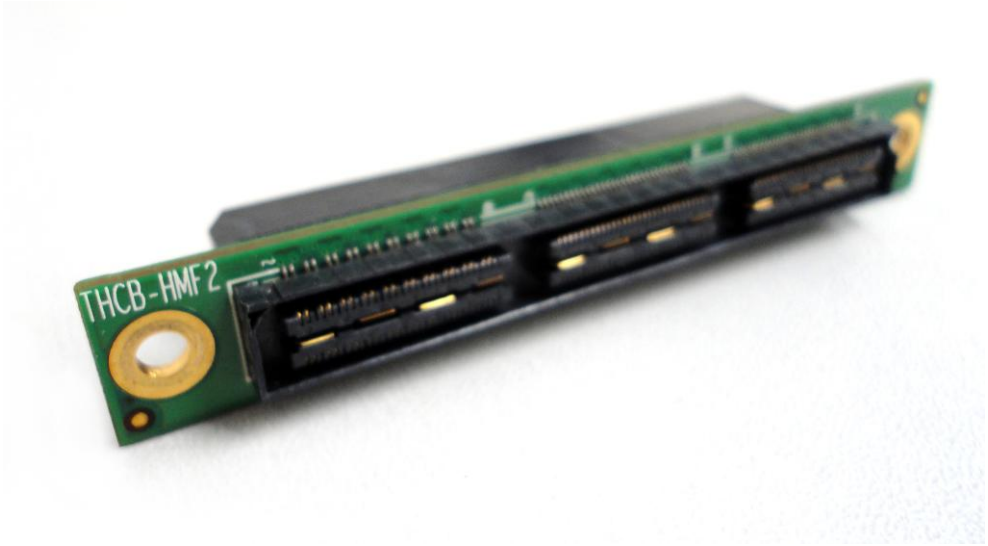


**Figure 3-1 THCB-HMF2 card**

Note that we need to use the THCB-HMF2 card in between to make the HDMI_TX_HSMC daughter board connected to the HSMC connector of DE4.

**Figure 3-2**, **Figure 3-3** and **Figure 3-4** show how to setup hardware for transmission demonstration.

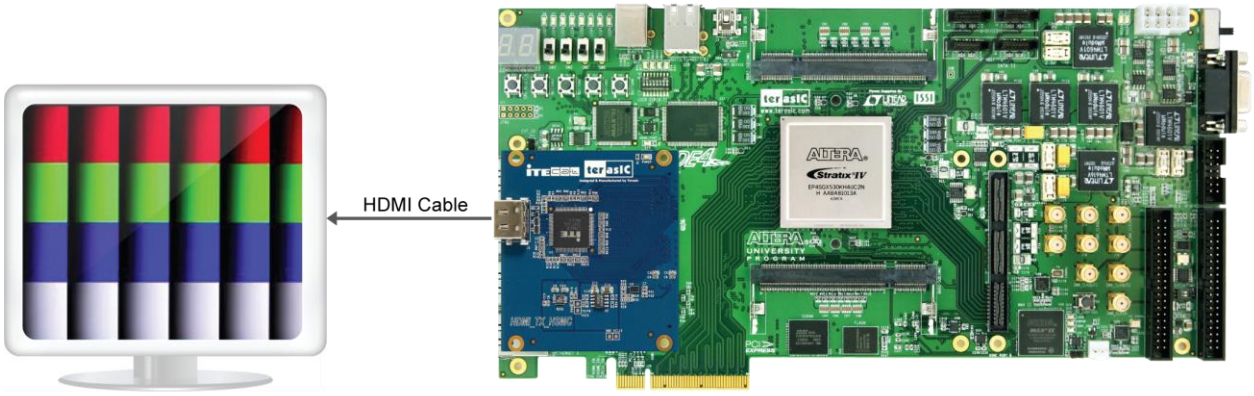


**Figure 3-2 HDMI Transmission-Only Demonstration Setup**

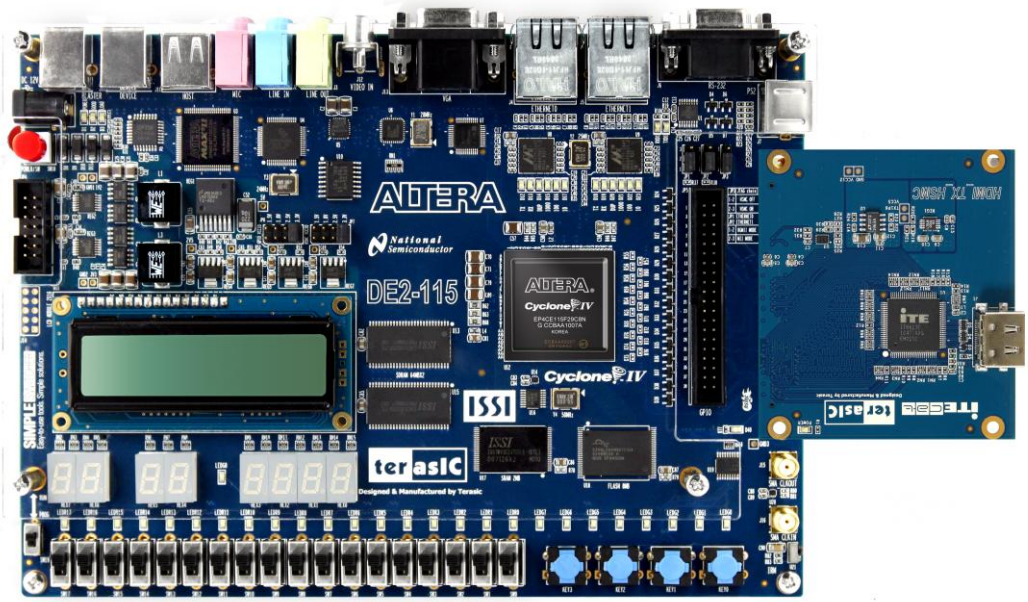


**Figure 3-3 Connecting HDMI_TX_HSMC to DE2-115**

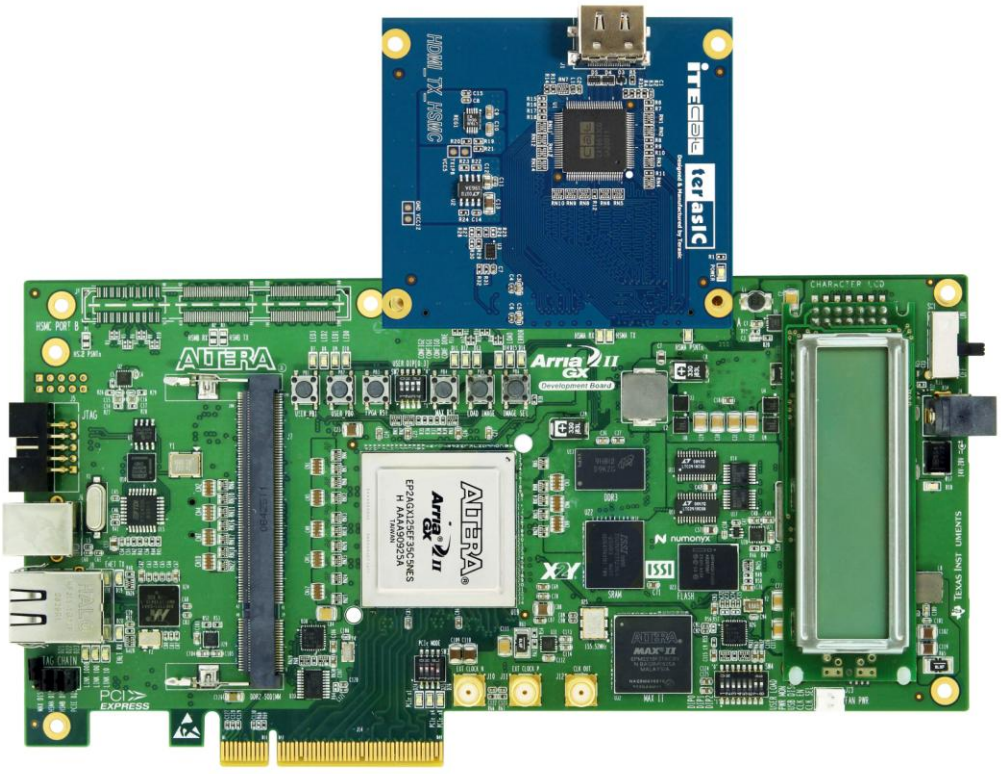


**Figure 3-4 Connecting HDMI_TX_HSMC to A2GX**

## 3.4 Operation

This section describes the procedures of running the demonstration.

### ■ FPGA Configuration

Please follow the steps below to configure the FPGA.

- Make sure hardware setup is completed
- Connect PC with DE4 via a USB cable
- Power on the DE4
- Make sure Quartus II is installed on your PC
- Execute the batch file hdmi_demo.bat under the folder "\HDMI_TX_Demonstration\DE4_230_HDMI_TX\demo batch" from the HDMI_TX_HSMC system CD

### ■ HDMI Transmission-Only

After FPGA is configured, please follow the steps below to run the HDMI transmission-only demonstration.

- Connect the HDMI LCD monitor and the HDMI transmitting port with a HDMI cable
- Power on the LCD monitor and make sure the LCD monitor is set to the mode where HDMI input is the source. Please refer to the user manual of your HDMI Display for more details
- When LCD monitor is detected, the LED2 of DE4 will be turned on
- After approximately 10 seconds, a test pattern will be displayed on the LCD monitor. The first displayed pattern is 480p (720x480p60) pattern
- Press "BUTTON0" to change test patterns. Please refer to Table 4-3 for built-in test patterns. There are eleven built-in test patterns available in this demonstration. You will not be able to see all the test patterns if your LCD monitor doesn't support such resolution
- Press "BUTTON1" to change the color space of pattern source. The color space includes

RGB444, YUV422, and YUV444

Figure 3-5 and Figure 3-6 show the test patterns of FULL HD (1920x1080p60) in RGB and YUV color space, respectively.

It will take approximately 10 seconds to display a new pattern on the LCD when users change test pattern or color space.

**Figure 3-5 FULL HD in RGB444 Color Space**

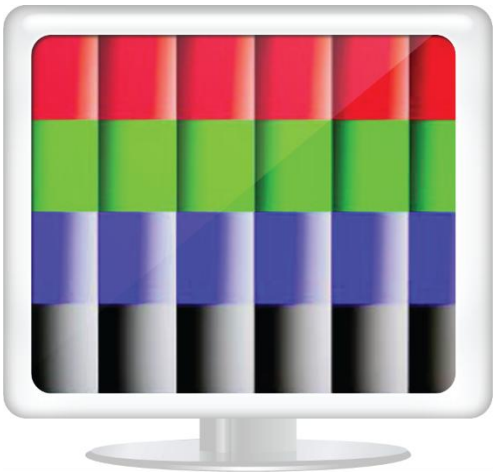

**Figure 3-6 FULL HD in YUV Color Space**

Figure 3-7 shows the Nios II program trace log when a HDMI LCD monitor is detected. It indicates that the LCD monitor in use supports color space YUV444 and YUV422, but not RGB444. Various video formats supported are listed according to Video Identify Code (VIC). The format of input and output color of the transmitter is RGB444 and RGB444, respectively. It implies there is no change of color format in between.

```
[TERASIC-00000.001]
======== HDMI Demo ==============
[TERASIC-00000.002]TX hardware Reset
TX Chip Revision ID: 1
[TERASIC-00000.755][I2S]register callback success
[TERASIC-00000.756][I2S]register button callback success
[TERASIC-00000.758]RX hardware Reset
[TERASIC-00003.111]RX hardware Reset
[TERASIC-00004.541]RX Chip Revision ID: A1h
[TERASIC-00004.543]++++++++++ RX HW Reset +++++++++
[TERASIC-00004.546]RX hardware Reset
[TERASIC-00007.694][RX]Active Port: A
[TERASIC-00007.808]HPDChange
[TERASIC-00007.809]HPD=ON
[TERASIC-00010.577]Support Color: YUV444
[TERASIC-00010.578]Support Color: YUV422
[TERASIC-00010.581]HDMI Sink VIC(Video Identify Code)=3
[TERASIC-00010.583]HDMI Sink VIC(Video Identify Code)=18
[TERASIC-00010.585]HDMI Sink VIC(Video Identify Code)=4
[TERASIC-00010.588]HDMI Sink VIC(Video Identify Code)=19
[TERASIC-00010.590]HDMI Sink VIC(Video Identify Code)=5
[TERASIC-00010.592]HDMI Sink VIC(Video Identify Code)=20
[TERASIC-00010.595]HDMI Sink VIC(Video Identify Code)=16
[TERASIC-00010.597]HDMI Sink VIC(Video Identify Code)=31
[TERASIC-00010.599]HDMI Sink VIC(Video Identify Code)=9
[TERASIC-00010.601]HDMI Sink VIC(Video Identify Code)=1
[TERASIC-00010.604]HDMI Display found
[TERASIC-00010.605]HDMITX_SetOutput
[TERASIC-00010.653]===> Pattern Generator Mode: 0 (720x480p60 VIC=3)
[TERASIC-00010.702]Set Tx Color Depth: 24 bits
[TERASIC-00010.704]Set Tx Color Convert:RGB444->RGB444
[TERASIC-00011.441]ConfigAVIInfoFrame, VIC=3
```

**Figure 3-7 Nios II program trace log of transmitting-only demonstration**

# Chapter 4

# Case Study

This chapter describes the design concepts for the HDMI demonstration mentioned in the previous chapter.

## 4.1 Overview

This section describes the overview of the reference design.

This reference design shows how to use DE4 to control the HDMI_TX_HSMC board. Please refer to the previous chapter for the demonstration of this reference design.

The source code of the reference design can be found under the directory of Example folder in the CD of the HDMI_TX_HSMC board. The demonstration includes the following major function:

Transmission only:

Generate HDMI Video/Audio signal for transmission, including various video formats and color space. There are 11 video formats available. The color space includes RGB444, YUV422, and YUV444.

## 4.2 System Function Block

This section will describe the system behavior in function blocks.

Figure 4-1 shows the system function block diagram of this demonstration. In the design, SOPC is included because Nios II processor is used to control the transmitter through I2C interface. The Nios II program is designed to run on the on-chip memory. A customized I2S controller is designed to generate I2S 48K stereo audio for the HDMI transmitting-only mode. The audio data is stored in the on-chip memory and sent to the HDMI transmitter by Nios II processor.

The video pattern generator is designed to generate test patterns for HDMI transmitter-only mode. It provides eleven video formats in RGB color spaces. The source selector circuit is designed to select the desired video source from the video pattern generator. Four LEDs and two BUTTONs on DE4 are used for human interface. BUTTONs are designed to change the test pattern and associated

color space for transmission. LEDs are designed to indicate the HDMI status, which is illustrated in Table 4-1. BUTTONs are designed to change the video format and color space of the build-in video pattern generator, which is illustrated in Table 4-2.

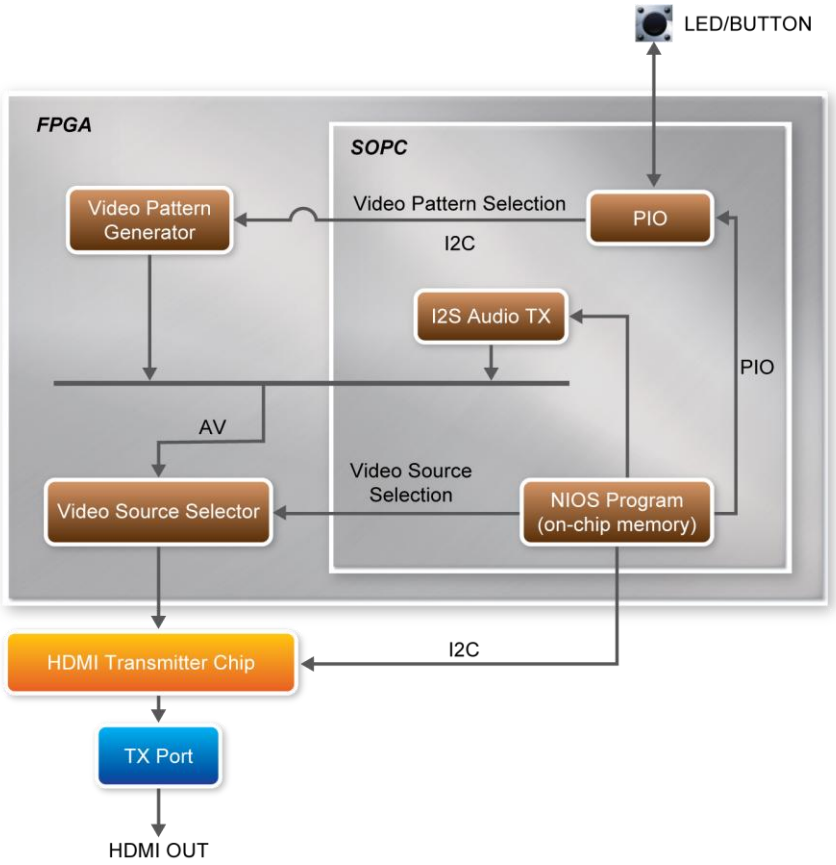


**Figure 4-1 System Function Block Diagram**

**Table 4-1 LED Indications**

| *LED* | *Description* |
|---|---|
| | **System is running.** |
| | **HDMI sink device is detected and synchronized.** |

**Table 4-2 Button Operation Definition**

| *BUTTON* | *Description* |
|---|---|
| | **Press to change active video format of the built-in video pattern generator.** |
| | **Press to change active video color space of the built-in video pattern generator.** |

## ■ Transmitter Controlled by Nios II Processor

The transmitter is controlled by Nios II program through I2C interface. Based on I2C protocol, the Nios II program can read/write the internal registers of the transmitter, and control the behavior of the transmitter. The NIOS program controls the transmitter to perform the following procedures step by step:

- Initialize the HDMI chip
- Detect if a HDMI sink device is attached or detached, e.g. LCD Display
- Read and parse the EDID content to find the capability of the HDMI sink device. The capability includes supported color space, video format (VIC code), and color depth etc.
- Perform HDCP authentication
- Configure the color space of input and output. The transmitter offers color space transformation and outputs RGB444, YUV422, or YUV444
- Configure the color depth of output video
- Send VIC to the video sink device
- Configure the audio interface and format of output video

## ■ Video Pattern Generator

The video pattern generator is designed to generate test pattern for HDMI transmitting-only mode. The supported video formats are listed in **Table 4-3.**

**Table 4-3 Built-in video formats**

| *Video Format* | *VIC* | *PCLK (MHZ)* |
|---|---|---|
| 720x480p60 | 3 | 27 |
| 1024x768pP60 | - | 65 |
| 1280x720p50 | 19 | 74.25 |
| 1280x720p60 | 4 | 74.25 |
| 1280x1024 | - | 108 |
| 1920x1080i60 | 5 | 74.25 |
| 1920x1080i50 | 20 | 74.25 |
| 1920x1080p60 | 16 | 148.5 |
| 1920x1080p50 | 31 | 148.5 |
| 1600x1200p5 | - | 162 |
| 1920x1080i120 | 46 | 148.5 |

It also supports three color spaces, which are RGB444, YUV422, and YUV444.

The required PCLK is generated from Megafunction ALTPLL and ALTPLL_RECONFIG IP. The required PLL-reconfigure data is stored in on-chip ROMs.

## 4.3 Nios II Program

This section describes the design flow and how Nios II processor controls transmitter.

Figure 4-2 shows the software stack of the Nios II program. The I2C block implements the I2C read/write functions based on GPIO system call. The HDMI transmitter block is referred as the HDMI driver. The HDMI transmitter chip is managed and controlled through the I2C protocol. The I2S driver block is in charge of sending audio data to the transmitter.

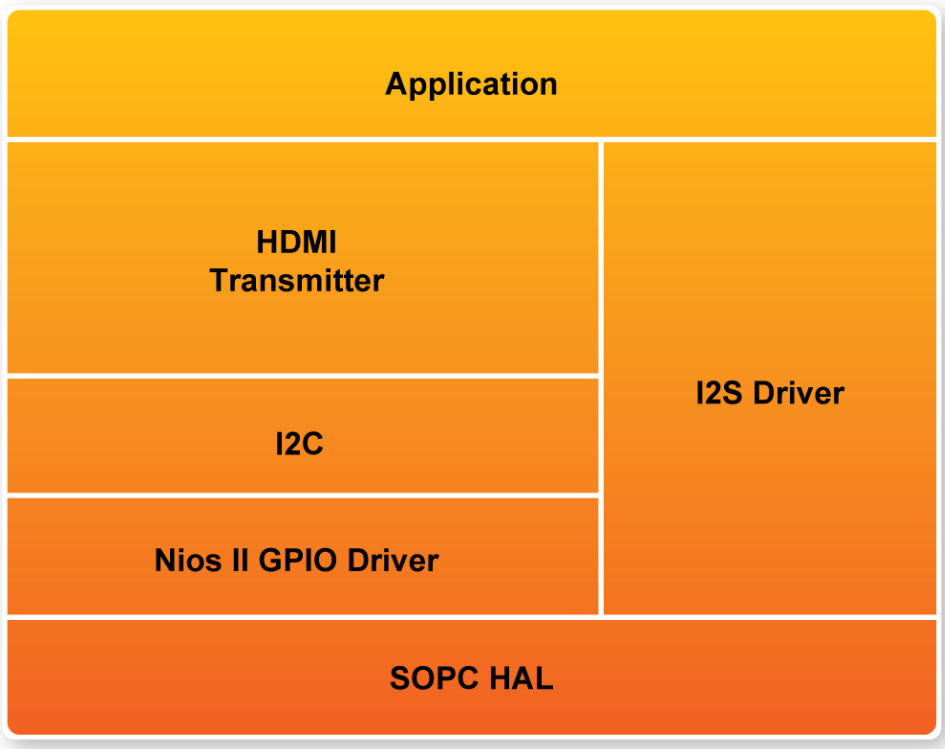


**Figure 4-2 Software Stack**

Figure 4-3 shows the file list of the Nios II program. The control center is located in main.c. The beep.c includes audio raw data for generating a tone sound. The folder named terasic_lib includes the I2C driver. The folder named HDMI_Lib includes transmitter drivers. The platform-dependent functions are located in mcu.c under HDMI_Lib.

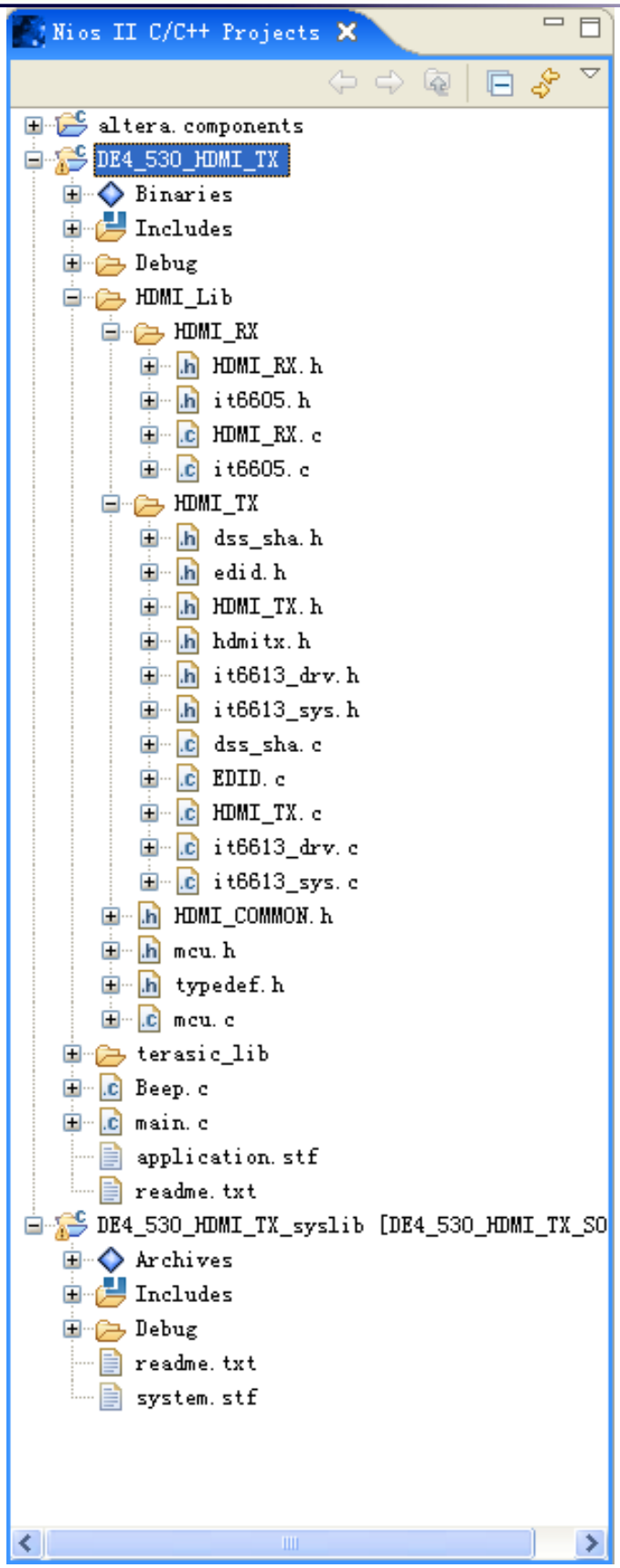


**Figure 4-3 Nios II Program File List**

## ■ System Configuration

To use the HDMI library in Nios II, the const _MCU_ should be defined in the configuration settings, as shown in Figure 4-4. Two on-chip memories are created to store the Nios II program and data separately. The size of each on-chip memory is 128 K bytes. One on-chip memory is used to store program and the other one is used to store data. The option “Small C Library” must be enabled to reduce the size of the program. The associated configuration is shown in Figure 4-5

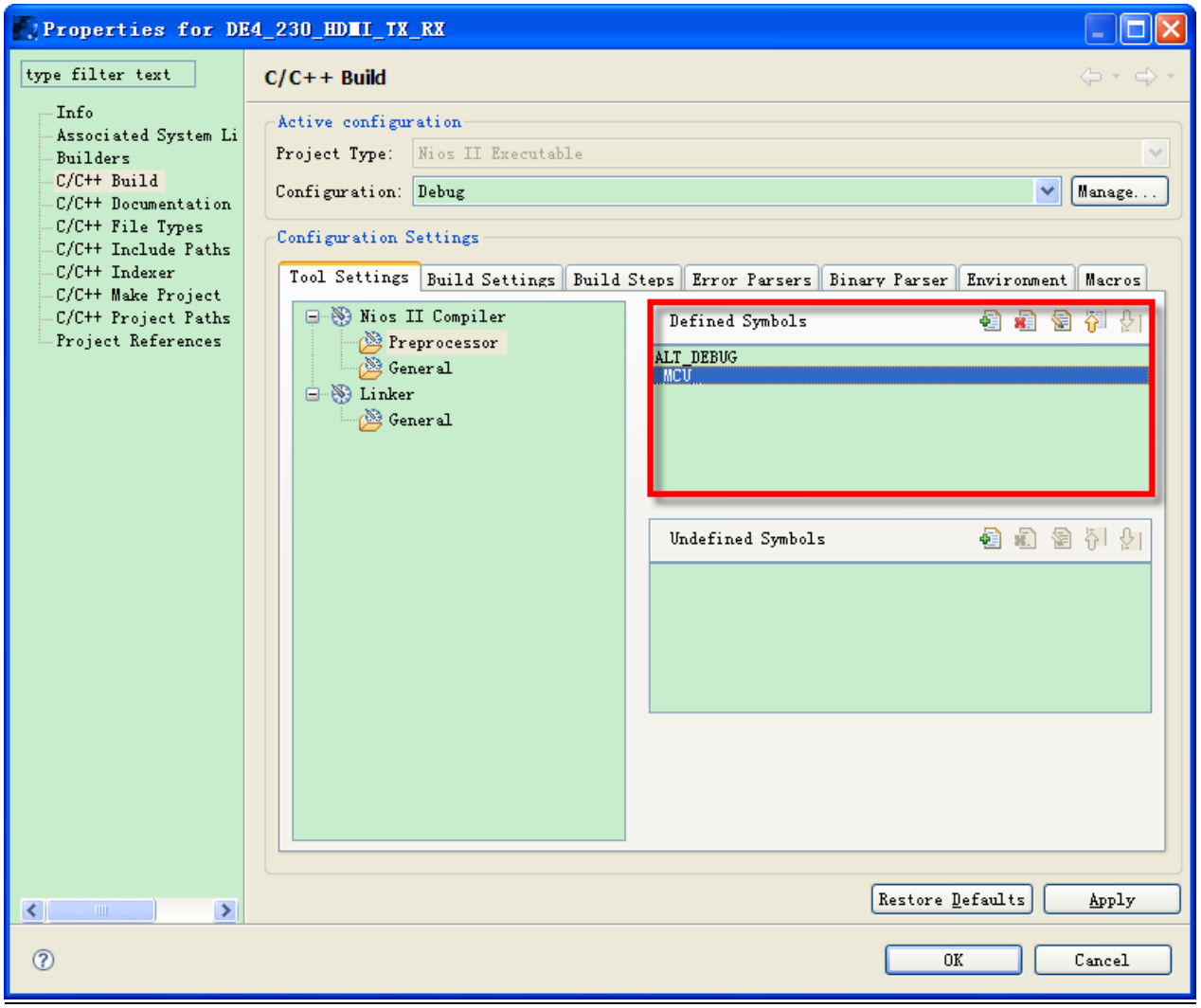


**Figure 4-4 Define _MCU_ constant**

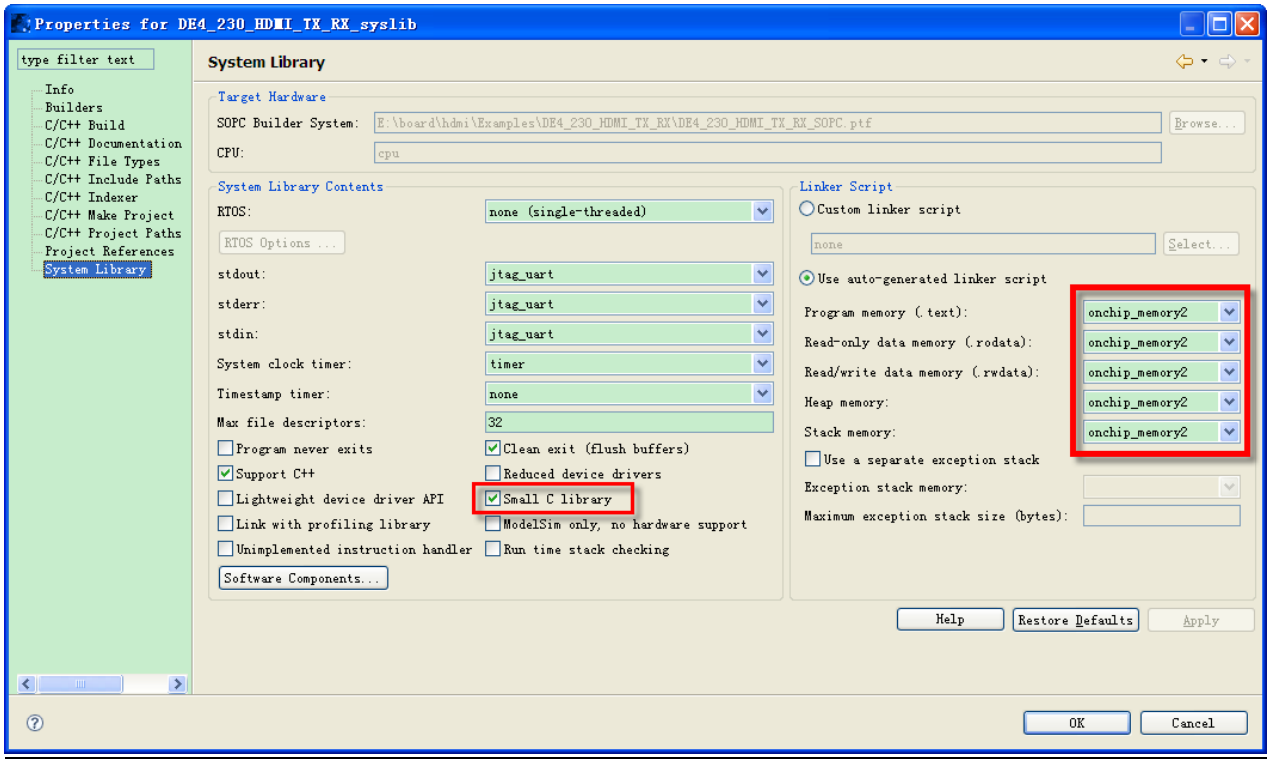


**Figure 4-5 Configuration of System Library**

## ■ Audio Test

If users would like to test audio during HDMI transmitting-only mode, please remove the constant definition TX_VPG_COLOR_CTRL_DISABLED from main.c. Users will hear a tone sound from the built-in speaker of HDMI LCD monitor when pressing BUTTON1 of DE4 board.

# Chapter 5

# Appendix

## 5.1 Revision History

| Revision | Date | Change Log |
|---|---|---|
| 1.0 | NOV 02 2010 | Initial Version |
| 1.1 | MAR 09 2011 | Support to HDMI 1.4 |

## 5.2 Always Visit HDMI_TX_HSMC Webpage for Update

We will be continuing providing interesting examples and labs on our HDMI_TX_HSMC web page. Please visit www.altera.com or hdmi_1.4_tx_.terasic.com for more information.

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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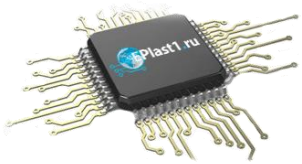


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