

SN54ABT162825, SN74ABT162825 18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS474C – JUNE 1994 – REVISED MAY 1997

- Members of the Texas Instruments *Widebus™* Family
- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

description

The 'ABT162825 are 18-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices provide true data, and can be used as two 9-bit buffers or one 18-bit buffer.

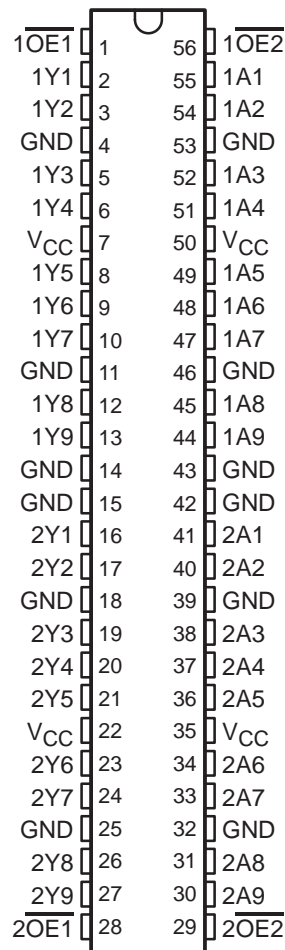
The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all nine affected outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT162825 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT162825 is characterized for operation from -40°C to 85°C .

SN54ABT162825 . . . WD PACKAGE
SN74ABT162825 . . . DL PACKAGE
(TOP VIEW)



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**TEXAS
INSTRUMENTS**

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SN54ABT162825, SN74ABT162825
18-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

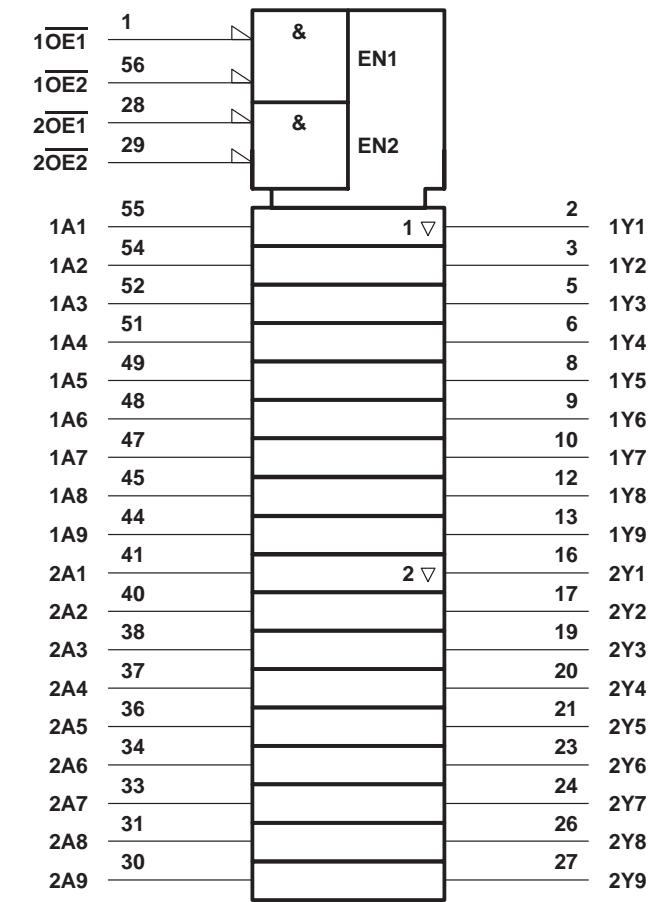
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FUNCTION TABLE

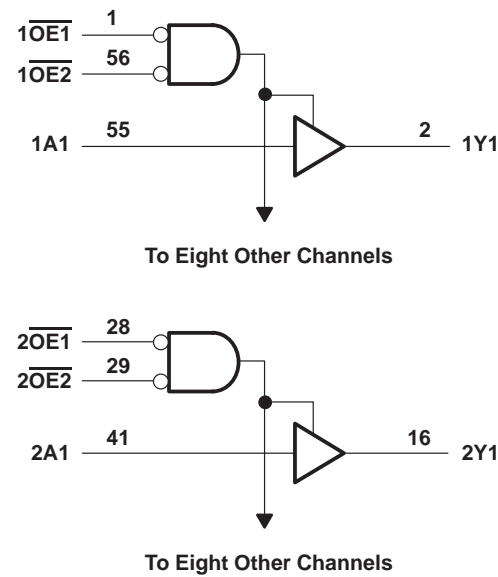
(each 9-bit buffer)

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O	30 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): DL package	74°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABT162825		SN74ABT162825		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage		2		2		V
V _{IL}	Low-level input voltage			0.8		0.8	V
V _I	Input voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current			−12		−12	mA
I _{OL}	Low-level output current			12		12	mA
Δt/Δv	Input transition rise or fall rate		Control inputs		9		ns/V
			Data inputs		10		
Δt/ΔV _{CC}	Power-up ramp rate		200		200		μs/V
T _A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT162825		SN74ABT162825		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = –18 mA			–1.2		–1.2		–1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = –1 mA		2.5			2.5		2.5	V
	V _{CC} = 5 V, I _{OH} = –1 mA		3			3		3	
	V _{CC} = 4.5 V		2.4			2.4		2.4	
			2			2		2	
V _{OL}	V _{CC} = 4.5 V		0.4	0.8		0.8		0.65	V
								0.8	
V _{hys}			100						mV
I _I	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{OZPU} ‡	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, \overline{OE} = X			±50		±50		±50	μA
I _{OZPD} ‡	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, \overline{OE} = X			±50		±50		±50	μA
I _{OZH} §	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, \overline{OE} ≥ 2 V			10		10		10	μA
I _{OZL} §	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, \overline{OE} ≥ 2 V			–10		–10		–10	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEx}	Outputs high			50		50		50	μA
I _O ¶	V _{CC} = 5.5 V, V _O = 2.5 V	–25	–75	–100	–25	–100	–25	–100	mA
I _{CC}	Outputs high			2		2		2	mA
	Outputs low			32		32		32	
	Outputs disabled			2		2		2	
ΔI _{CC} #	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled	1		1.5		1	mA
			Outputs disabled	0.05		1		0.05	
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		1.5		1.5		1.5	
C _i	V _I = 2.5 V or 0.5 V			3.5					pF
C _O	V _O = 2.5 V or 0.5 V			8					pF

† All typical values are at V_{CC} = 5 V.

‡ This parameter is characterized, but not production tested.

§ The parameters I_{OZH} and I_{OZL} include the input leakage current.

¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

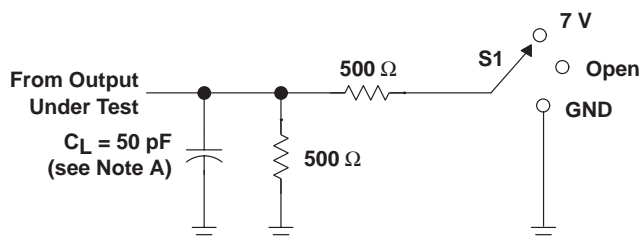
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABT162825		SN74ABT162825		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.1	3.6	1	4.1	1	3.9	ns
t_{PHL}			1.1	2.8	4.2	1.1	5	1.1	4.7	
t_{PZH}	\overline{OE}	Y	1.5	3.4	6.3	1.5	7.2	1.5	6.9	ns
t_{PZL}			1.6	3.5	7.3	1.6	6.6	1.6	6.3	
t_{PHZ}	\overline{OE}	Y	2.1	4.1	6.5	2.1	6.8	2.1	6.6	ns
t_{PLZ}			1.5	3.5	5.9	1.5	7.3	1.5	6.3	

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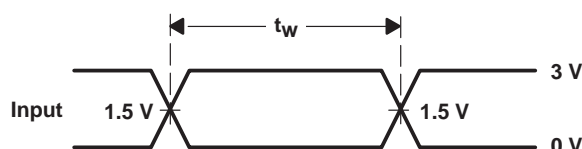
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PARAMETER MEASUREMENT INFORMATION

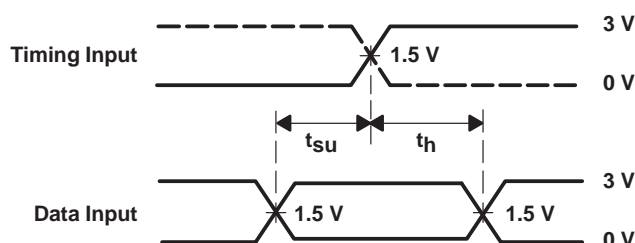


LOAD CIRCUIT

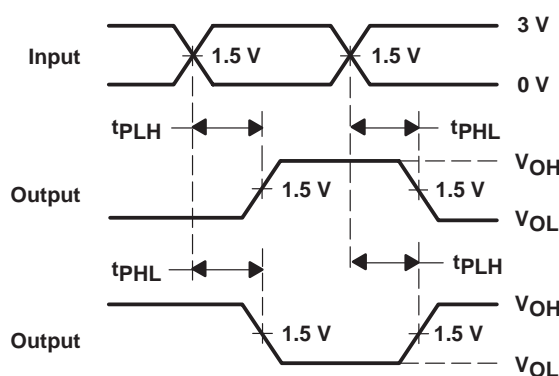
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



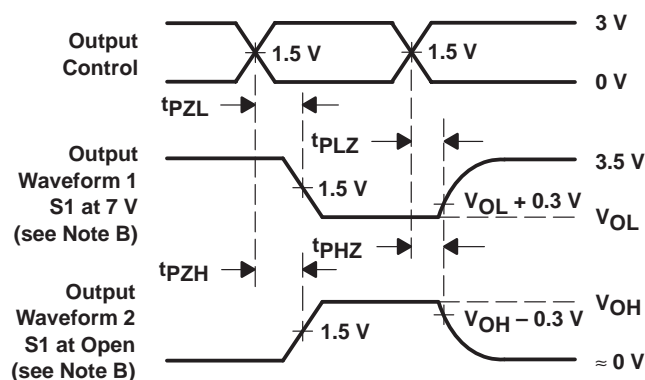
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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