PESD5V0U2BT

Ultra low capacitance bidirectional double ESD protection diode

Rev. 01 — 27 March 2007 Product data sheet

1. Product profile

1.1 General description

Ultra low capacitance bidirectional double ElectroStatic Discharge (ESD) protection diode in a SOT23 (TO-236AB) small Surface-Mounted Device (SMD) plastic package designed to protect two data lines from the damage caused by ESD.

1.2 Features

- Bidirectional ESD protection of two lines
- Ultra low diode capacitance: C_d = 2.9 pF
- IEC 61000-4-2; level 4 (ESD)
- Ultra low leakage current: I_{RM} = 5 nA
- ESD protection of up to 10 kV

1.3 Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- 10/100/1000 Ethernet
- Local Area Network (LAN) equipment
- Communication systems
- Portable electronics
- Subscriber Identity Module (SIM) card protection
- FireWire
- High-speed data lines

1.4 Quick reference data

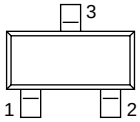
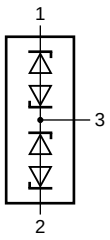
Table 1. Quick reference data

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per diode						
V_{RWM}	reverse standoff voltage		-	-	5	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	-	2.9	3.5	pF

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
1	cathode 1		
2	cathode 2		
3	common cathode		

006aaa155

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0U2BT	-	plastic surface-mounted package; 3 leads	SOT23

4. Marking

Table 4. Marking codes

Type number	Marking code[1]
PESD5V0U2BT	1U*

[1] * = -: made in Hong Kong
* = p: made in Hong Kong
* = t: made in Malaysia
* = W: made in China

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per device					
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		–65	+150	°C
T_{stg}	storage temperature		–65	+150	°C

Table 6. ESD maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
Per diode					
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge) [1][2]	-	10	kV
		MIL-STD-883 (human body model)	-	8	kV

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1 to pin 2.

Table 7. ESD standards compliance

Standard	Conditions
Per diode	
IEC 61000-4-2; level 4 (ESD)	> 15 kV (air); > 8 kV (contact)
MIL-STD-883; class 3 (human body model)	> 4 kV

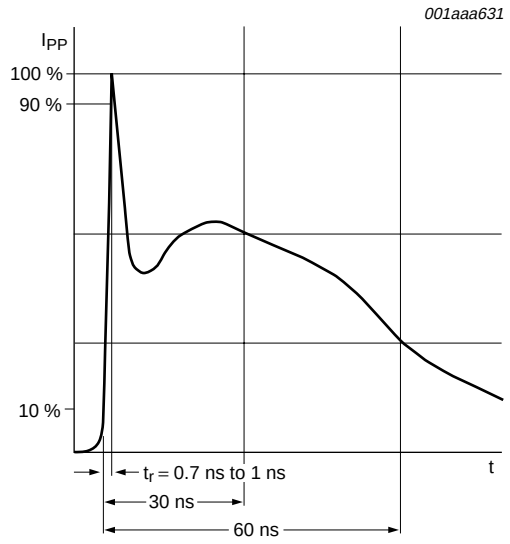


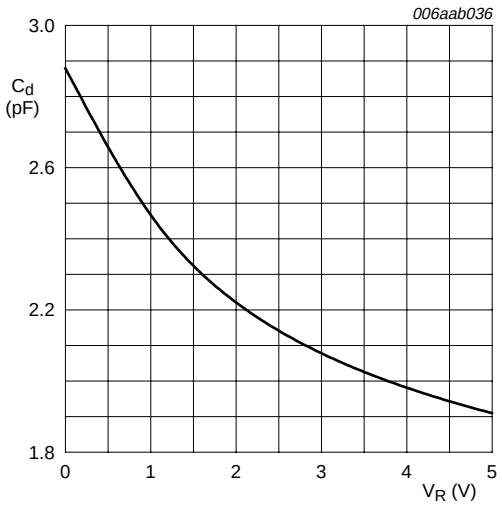
Fig 1. ESD pulse waveform according to IEC 61000-4-2

6. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per diode						
V_{RWM}	reverse standoff voltage		-	-	5	V
I_{RM}	reverse leakage current	V_{RWM} = 5 V	-	5	100	nA
V_{BR}	breakdown voltage	I_R = 5 mA	5.5	7	9.5	V
C_d	diode capacitance	f = 1 MHz				
		V_R = 0 V	-	2.9	3.5	pF
		V_R = 5 V	-	1.9	-	pF
r_{dif}	differential resistance	I_R = 1 mA	-	-	100	Ω



f = 1 MHz; T_{amb} = 25 °C

Fig 2. Diode capacitance as a function of reverse voltage; typical values

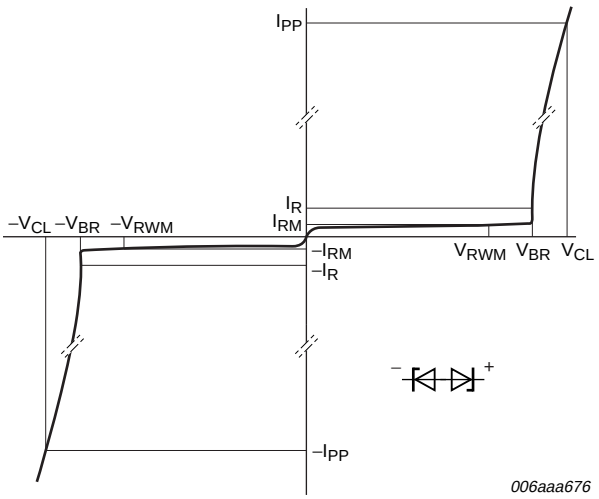


Fig 3. V-I characteristics for a bidirectional ESD protection diode

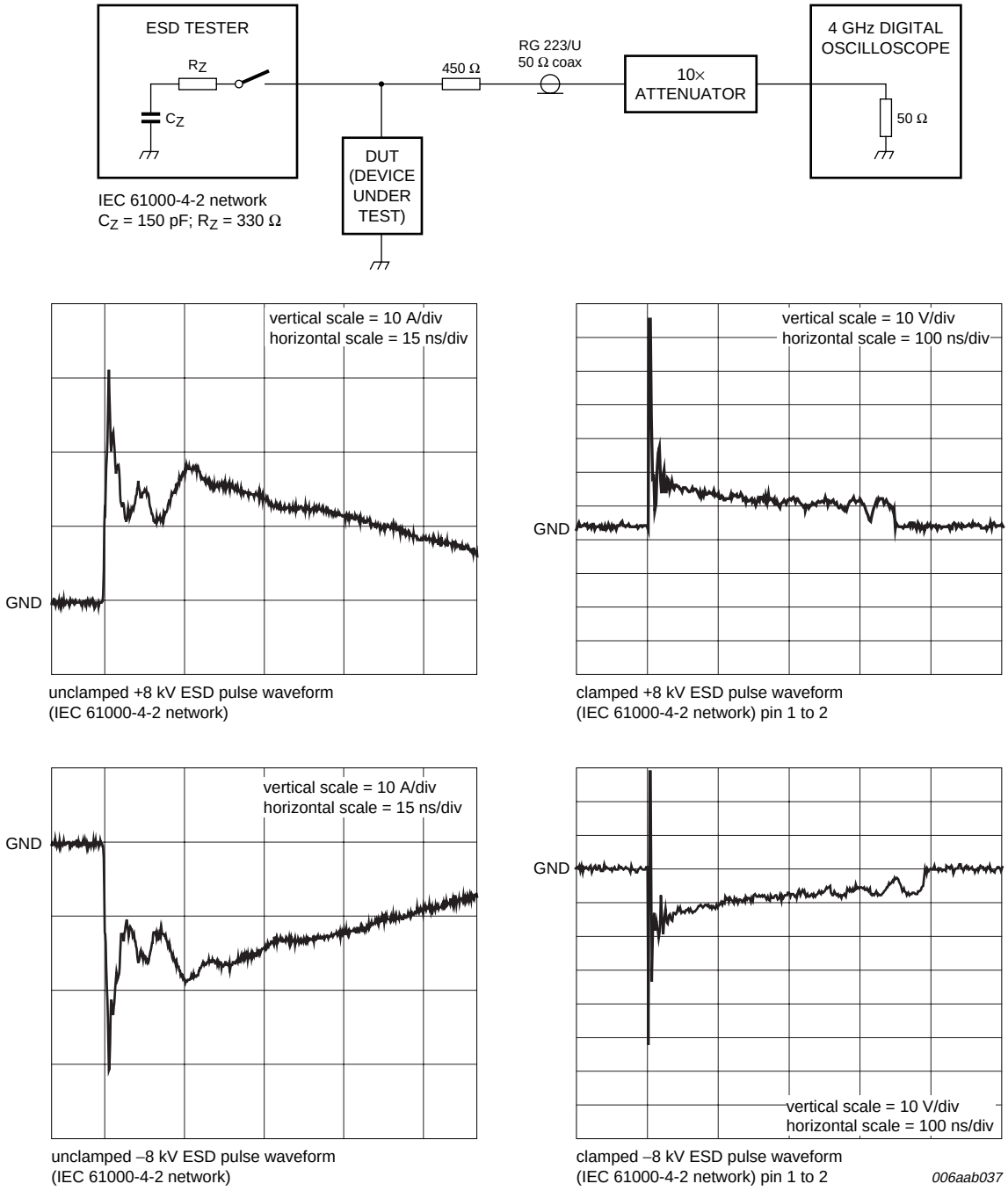


Fig 4. ESD clamping test setup and waveforms

7. Application information

The PESD5V0U2BT is designed for the bidirectional protection of two signal lines from the damage caused by ESD pulses. The PESD5V0U2BT may be used on lines where the signal polarities are either positive or negative with respect to ground.

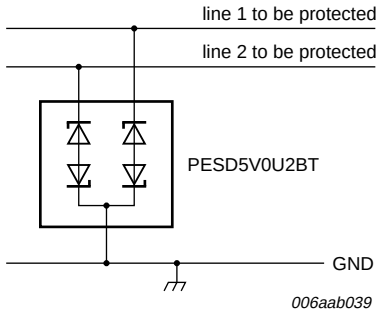


Fig 5. Bidirectional protection of two lines

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the PESD5V0U2BT as close to the input terminal or connector as possible.
2. The path length between the PESD5V0U2BT and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

8. Package outline

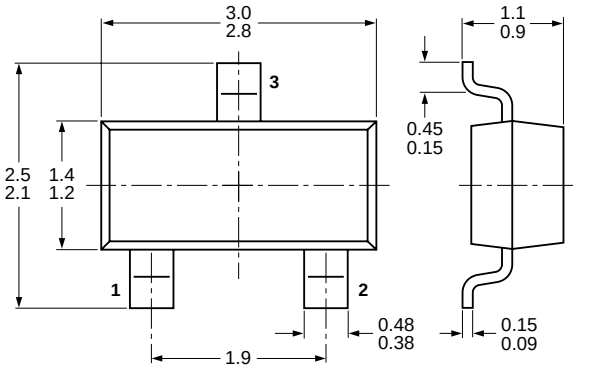


Fig 6. Package outline SOT23 (TO-236AB)

9. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

Type number	Package	Description	Packing quantity	
			3000	10000
PESD5V0U2BT	SOT23	4 mm pitch, 8 mm tape and reel	-215	-235

[1] For further information and the availability of packing methods, see Section 13.

10. Soldering

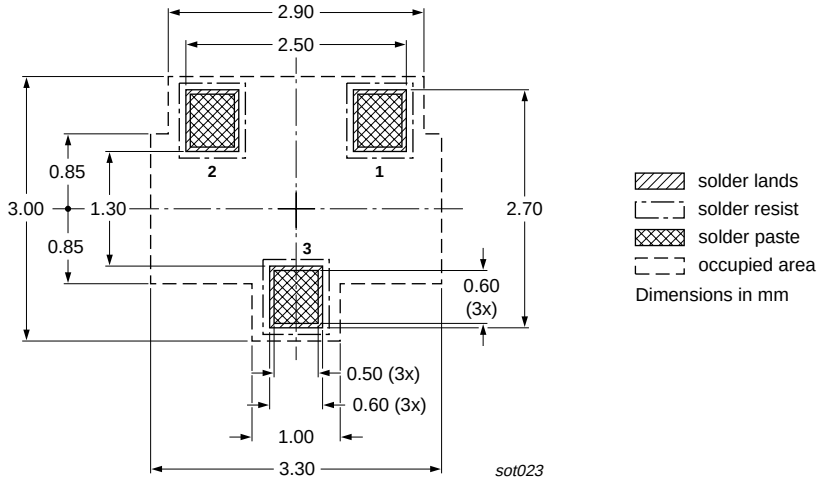


Fig 7. Reflow soldering footprint SOT23 (TO-236AB)

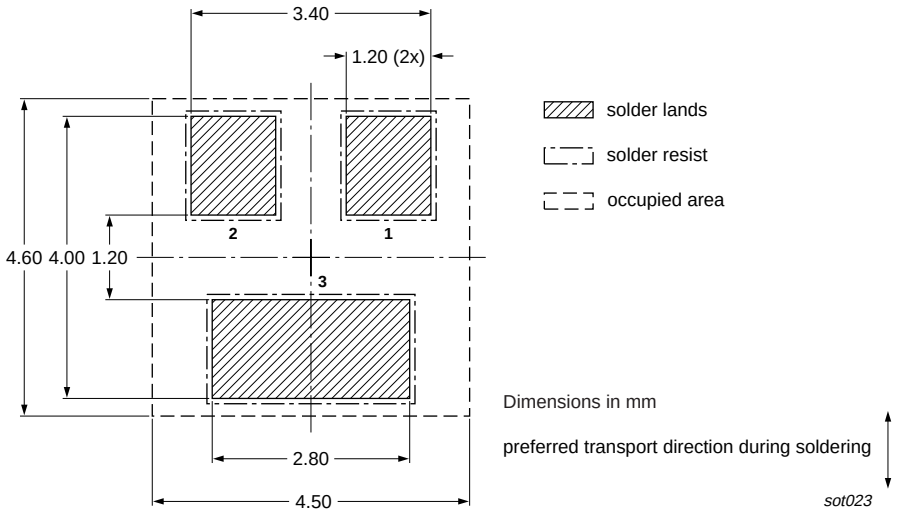


Fig 8. Wave soldering footprint SOT23 (TO-236AB)

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0U2BT_1	20070327	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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14. Contents

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Date of release: 27 March 2007

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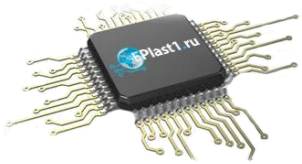

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