DATA SHEET

PCF8573
Clock/calendar with Power Fail Detector

Product specification
Supersedes data of May 1989
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Philips
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CONTENTS

Clock/calendar with Power Fail Detector PCF8573

1 FEATURES

- Serial input/output I²C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- On-chip power fail detector
- Separate ground pin for the clock allows easy implementation of battery back-up during supply interruption
- Crystal oscillator control (32.768 kHz)
- Low power consumption.

2 GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar. Addresses and data are transferred serially via the two-line bidirectional I²C-bus.

The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadmium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DD} - V_{SS1}$	supply voltage, clock (pin 16 to pin 15)	1.1	–	6.0	V
$V_{DD} - V_{SS2}$	supply voltage, I²C-bus (pin 16 to pin 8)	2.5	–	6.0	V
f_{osc}	crystal oscillator frequency	–	32.768	–	kHz

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8573P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
PCF8573T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

5 BLOCK DIAGRAM

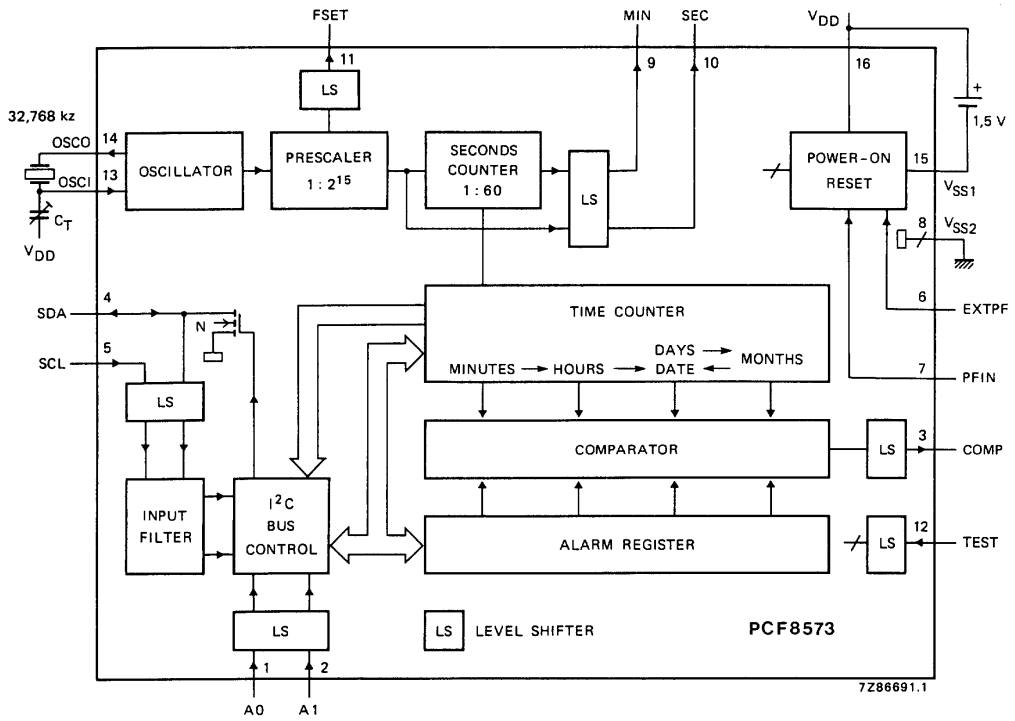


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input
A1	2	address input
COMP	3	comparator output
SDA	4	serial data line; I^2C-bus
SCL	5	serial clock line; I^2C-bus
EXTPF	6	enable power fail flag input
PFIN	7	power fail flag input
V_{SS2}	8	negative supply 2 (I^2C interface)
MIN	9	one pulse per minute output
SEC	10	one pulse per second output
FSET	11	oscillator tuning output
TEST	12	test input; connect to V_{SS2} if not in use
OSCI	13	oscillator input
OSCO	14	oscillator input/output
V_{SS1}	15	negative supply 1 (clock)
V_{DD}	16	common positive supply

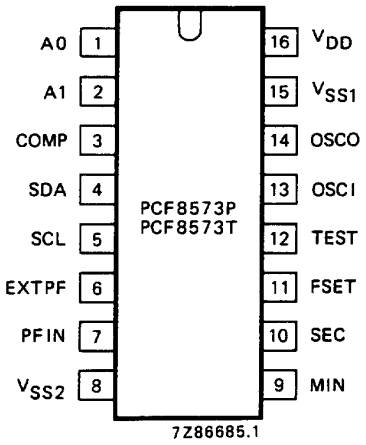


Fig.2 Pinning diagram.

7 FUNCTIONAL DESCRIPTION

7.1 Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32.76 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

7.2 Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I^2C-bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH-to-LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected only once every four years - to allow for leap-year. Cycle lengths are shown in Table 1.

7.3 Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C-bus.

7.4 Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C-bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C-bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C-bus.

Table 1 Cycle length of the time counter

UNIT	NUMBER OF BITS	COUNTING CYCLE	CARRY FOR FOLLOWING UNIT	CONTENT OF MONTH COUNTER
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days[1]	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note

1. During February of a leap-year the ‘Time Counter Days’ may be set to 29 by directly writing into it using the ‘execute address’ function. Leap-years must be tracked by the system software.

7.5 Power on/power fail detection

If the voltage $V_{DD} - V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD} - V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD} - V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF(1)	PFIN(1)	FUNCTION
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

Note

1. 0 = V_{SS1} (LOW); 1 = V_{DD} (HIGH).

The external power fail control operates by absence of the $V_{DD} - V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of V_{DD}–V_{SS1}. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C-bus. A power-on reset for the I^2C-bus control is generated on-chip when the supply voltage $V_{DD} - V_{SS2}$ is less than V_{TH2}.

7.6 Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD} - V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD} - V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD} - V_{SS2}$ supply voltage. If the voltage $V_{DD} - V_{SS2}$ is absent ($V_{DD} = V_{SS2}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD} - V_{SS2}$ and the $V_{DD} - V_{SS1}$ supplies. Because the level shifters invert the input signals, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD} - V_{SS2} = 0$.

8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer (see Fig.3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

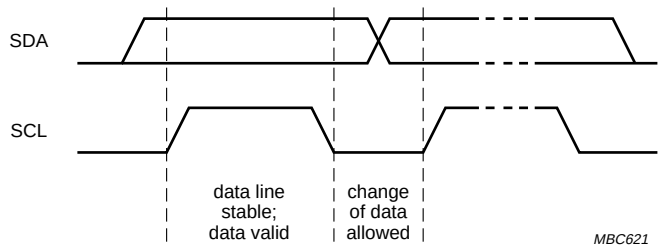


Fig.3 Bit transfer.

8.2 Start and stop conditions (see Fig.4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

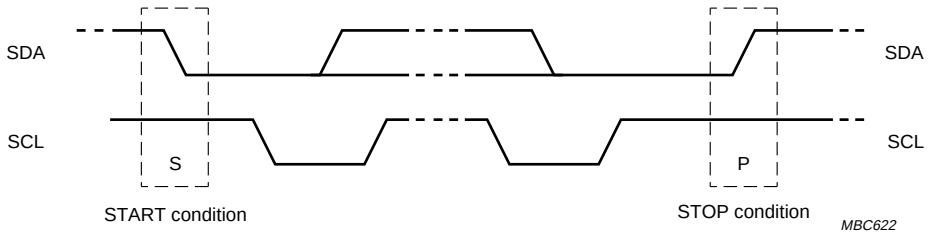


Fig.4 Definition of start and stop conditions.

8.3 System configuration (see Fig.5)

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

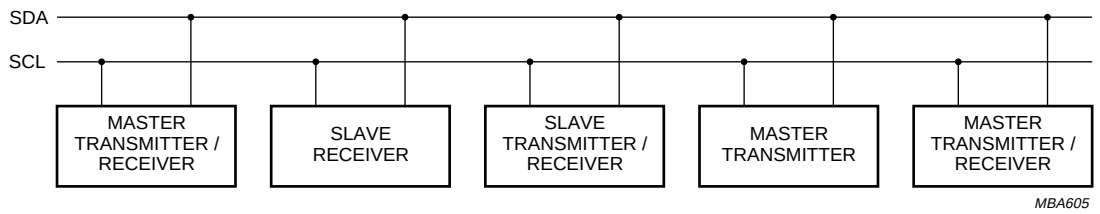


Fig.5 System configuration.

8.4 Acknowledge (see Fig.6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition, see Figs. 9 and 10.

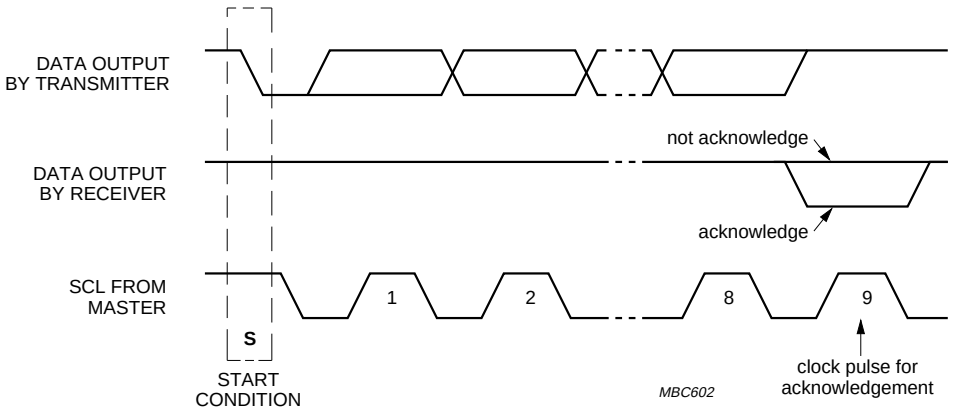


Fig.6 Acknowledgment on the I^2C-bus.

9 I²C-BUS PROTOCOL

9.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The clock/calendar slave address is shown in Fig.7. Bits A0 and A1 correspond to the two hardware address pins A0 and A1. Connecting these to V_{DD} or V_{SS} allows the device to have 1 of 4 different addresses.

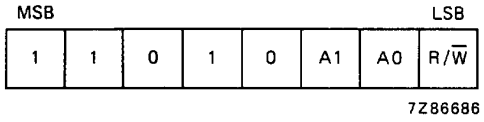


Fig.7 Slave address.

9.2 Clock/calendar READ/WRITE cycles

The I²C-bus configuration for different clock/calendar READ and WRITE cycles is shown in Figs 8, 9 and 10.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-word which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

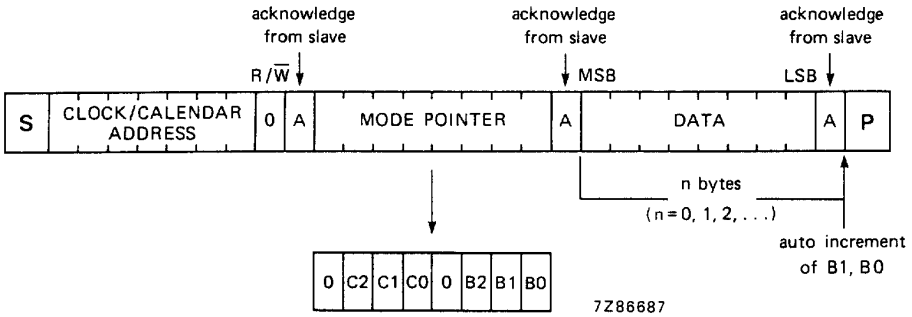
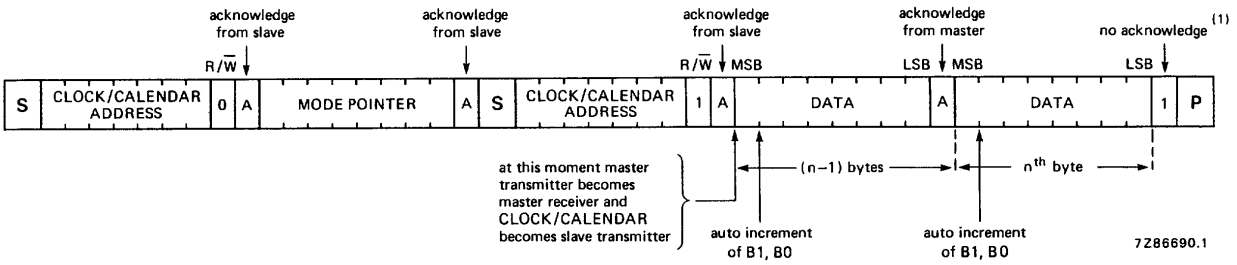
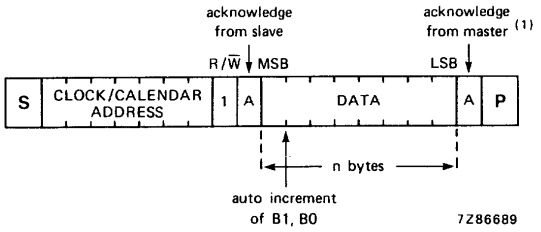


Fig.8 Master transmitter transmits to clock/calendar slave receiver.



(1) The master receiver must signal an end of data to the slave transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave.

Fig.9 Master transmitter reads clock/calendar after setting mode pointer.



(1) The master receiver must signal an end of data to the slave transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave.

Fig.10 Master reads clock/calendar immediately after first byte.

Table 3 MODE-POINTER-word, CONTROL-nibble (bits 8, 7, 6 and 5)

BIT 8	C2	C1	C0	FUNCTION
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (note 1)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

1. If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. –30 s. From the count 30 there is a carry which adjusts the time by max. +30 s.

Table 4 MODE-POINTER-word, ADDRESS-nibble (bits 4, 3, 2 and 1)

BIT 4	B2	B1	B0	ADDRESSED TO:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 6 shows the acknowledgement response of the clock calendar as a slave receiver.

Table 5 Placement of BCD digits in the DATA byte; note 1

MSB			DATA				LSB	
UPPER DIGIT				LOWER DIGIT				
UD	UC	UB	UA	LD	LC	LB	LA	ADDRESSED TO:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Note

1. ‘X’ is the don’t care bit; ‘D’ is the data bit.

Acknowledgement response of the PCF8573 as slave-receiver is shown in Table 6. Note that data is only associated with the ‘execute address’ function where C0, C1, C2 = 0, 0, 0.

Table 6 Slave receiver acknowledgement; note 1

MODE POINTER								ACKNOWLEDGE ON BYTE:		
BIT 8	**C2**	**C1**	**C0**	**BIT 4**	**B2**	**B1**	**B0**	**ADDRESS**	**MODE POINTER**	**DATA**
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Note

1. ‘X’ is ‘don’t care’.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.

The status of the CONTROL-nibble of the MODE-POINTER-WORD (C2, C1, C0) remains unchanged until re-written.

Table 7 Organization of the BCD digits in the DATA byte; note 1

MSB DATA LSB								
UPPER DIGIT				LOWER DIGIT				
UD	**UC**	**UB**	**UA**	**LD**	**LC**	**LB**	**LA**	**ADDRESSED TO:**
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	m	s	NODA	COMP	POWF	control/status flags

Note

1. ‘D’ is the data bit; ‘m’ = minutes; ‘s’ = seconds.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD} - V_{SS1}$	supply voltage (pin 16 to pin 15)	–0.3	+8.0	V
$V_{DD} - V_{SS2}$	supply voltage (pin 16 to pin 8)	–0.3	+8.0	V
V_I	input voltage			
	pins 4 and 5 (with input impedance of minimum 500 Ω)	$V_{SS2} - 0.8$	$V_{DD} + 0.8$	V
	pins 6, 7, 13 and 14	$V_{SS1} - 0.6$	$V_{DD} + 0.6$	V
	any other pin	$V_{SS2} - 0.6$	$V_{DD} + 0.6$	V
I_I	DC input current	–	10	mA
I_O	DC output current	–	10	mA
P_{tot}	total power dissipation per package	–	200	mW
P_O	power dissipation per output	–	100	mW
T_{amb}	operating ambient temperature	–40	+85	°C
T_{stg}	storage temperature	–55	+125	°C

11 HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *“Handling MOS Devices”.*

12 DC CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = –40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DD} - V_{SS2}$	supply voltage (I^2C interface)		2.5	5.0	6.0	V
$V_{DD} - V_{SS1}$	supply voltage (clock)	$t_{HD;\,DAT} \geq 300$ ns	1.1	1.5	$V_{DD} - V_{SS2}$	V
I_{SS1}	supply current at V_{SS1} (pin 15)	see Fig.11				
		$V_{DD} - V_{SS1}$ = 1.5 V	–	–3	–10	µA
		$V_{DD} - V_{SS1}$ = 5 V	–	–12	–50	µA
I_{SS2}	supply current at V_{SS2} (pin 8)	$V_{DD} - V_{SS2}$ = 5 V; I_O = 0 all outputs	–	–	–50	µA
Input SCL, input/output SDA						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS2}$ or V_{DD}	–1	–	+1	µA
C_i	input capacitance		–	–	7	pF
Inputs A0, A1, TEST						
V_{IL}	LOW level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS2}$ or V_{DD}	–250	–	+250	nA
Inputs EXTPF, PFIN						
V_{IL}	LOW level input voltage		0	–	$0.2V_{DD} - V_{SS1}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD} - V_{SS1}$	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS1}$ to V_{DD}	–1.0	–	+1.0	µA
		$V_I = V_{SS1}$ to V_{DD}; T_{amb} = 25 °C	–0.1	–	+0.1	µA
Output SDA (n channel open-drain)						
V_{OL}	LOW level output voltage	output ON; I_O = 3 mA; $V_{DD} - V_{SS2}$ = 2.5 to 6 V	–	–	0.4	V
I_{LI}	input leakage current	$V_{DD} - V_{SS2}$ = 6 V; V_O = 6 V	–1.0	–	+1.0	µA
Output SEC, MIN, COMP, FSET (normal buffer outputs)						
V_{OL}	LOW level output voltage	$V_{DD} - V_{SS2}$ = 2.5 V; I_O = 0.3 mA	–	–	0.4	V
		$V_{DD} - V_{SS2}$ = 4 to 6 V; I_O = 1.6 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$V_{DD} - V_{SS2}$ = 2.5 V; I_O = –0.1 mA	$V_{DD} - 0.4$	–	–	V
		$V_{DD} - V_{SS2}$ = 4 to 6 V; I_O = –0.5 mA	$V_{DD} - 0.4$	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Internal threshold voltages						
V_{TH1}	Power failure detection		1	1.2	1.4	V
V_{TH2}	Power-on reset		1.5	2.0	2.5	V

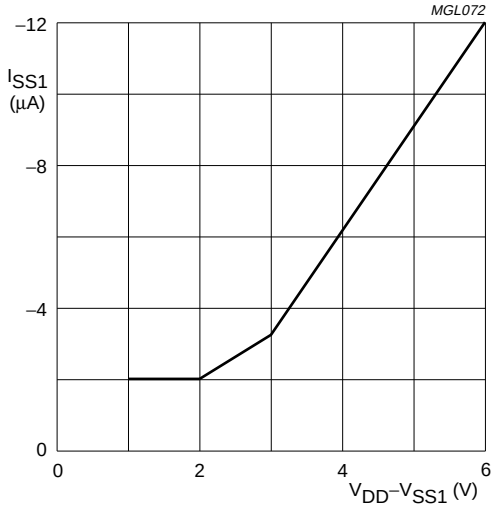


Fig.11 Typical supply current (I_{SS1}) as a function of clock supply voltage ($V_{DD} - V_{SS1}$) at T_{amb} = −40 to +85 °C.

13 AC CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = –40 to +85 °C unless otherwise specified. Typical values at T_{amb} = +25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Rise and fall times of input signals						
t_r	rise time	input EXTPF	–	–	1	µs
		input PFIN	–	–	∞	µs
		all other inputs (levels between V_{IL} and V_{IH})	–	–	1	µs
t_f	fall time	input EXTPF	–	–	1	µs
		input PFIN	–	–	∞	µs
		all other inputs (levels between V_{IL} and V_{IH})	–	–	0.3	µs
Oscillator						
C_{osc}	integrated oscillator capacitance		–	40	–	pF
R_f	oscillator feedback resistance		–	3	–	MΩ
Δf_{osc}	oscillator stability	$\Delta(V_{DD} - V_{SS1})$ = 100 mV; T_{amb} = 25 °C; $(V_{DD} - V_{SS1})$ = 1.55 V	–	2×10^{-7}	–	
Quartz crystal parameters (f = 32.768 kHz)						
R_S	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
I^2C-bus timing (see Fig.12; notes 1 and 2)						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SP}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid		–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs

Notes

1. All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
2. A detailed description of the I^2C-bus specification, with applications, is given in brochure *"The I^2C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

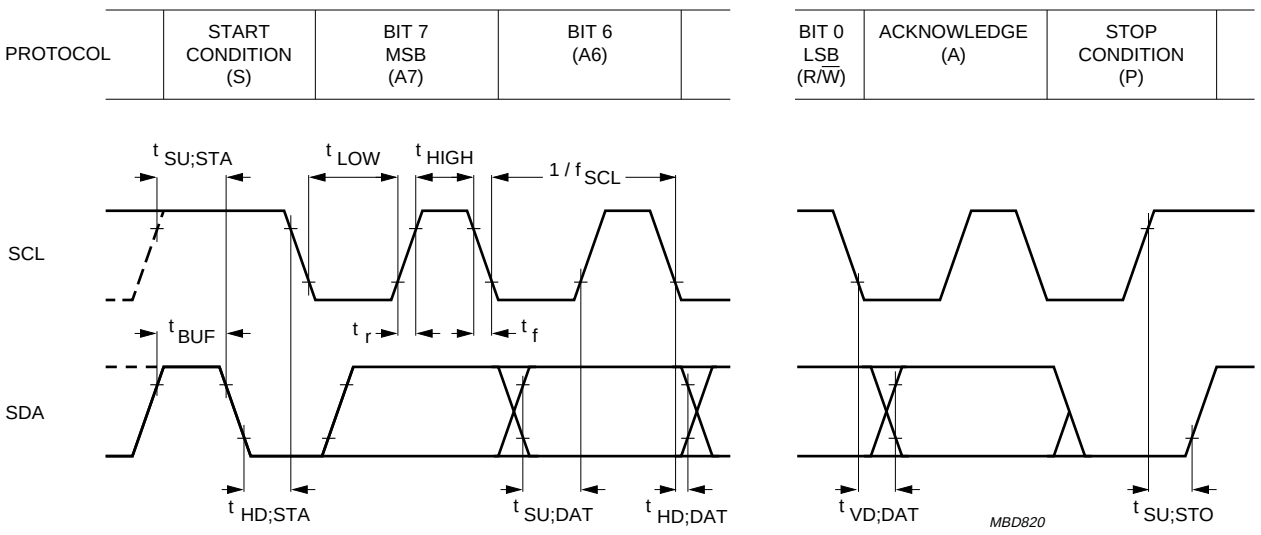


Fig.12 I^2C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

14 APPLICATION INFORMATION

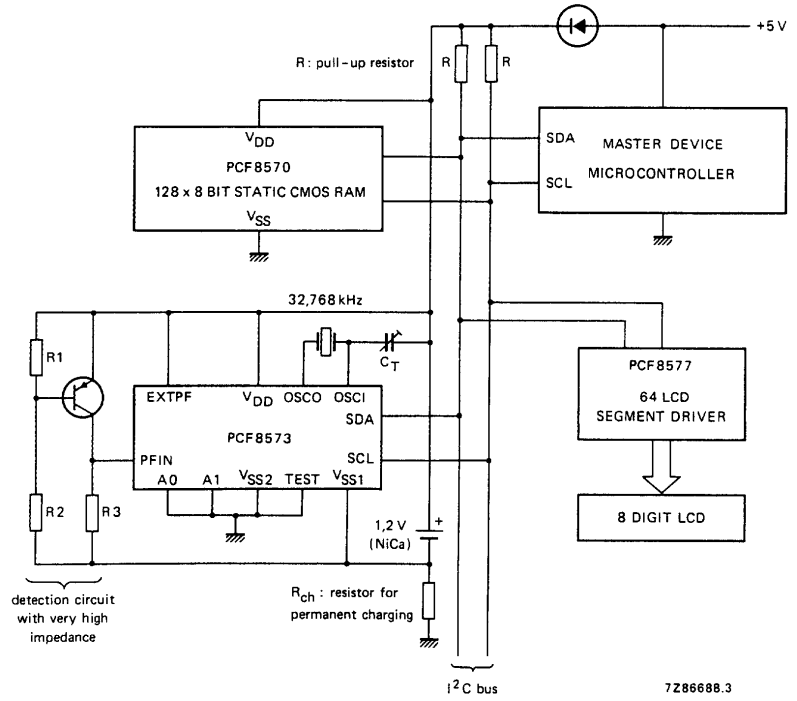


Fig.13 Application example of the PCF8573 clock/calendar with battery backup.

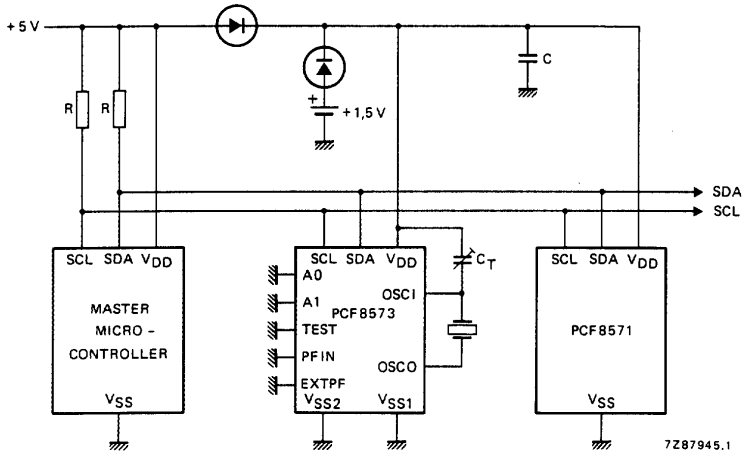
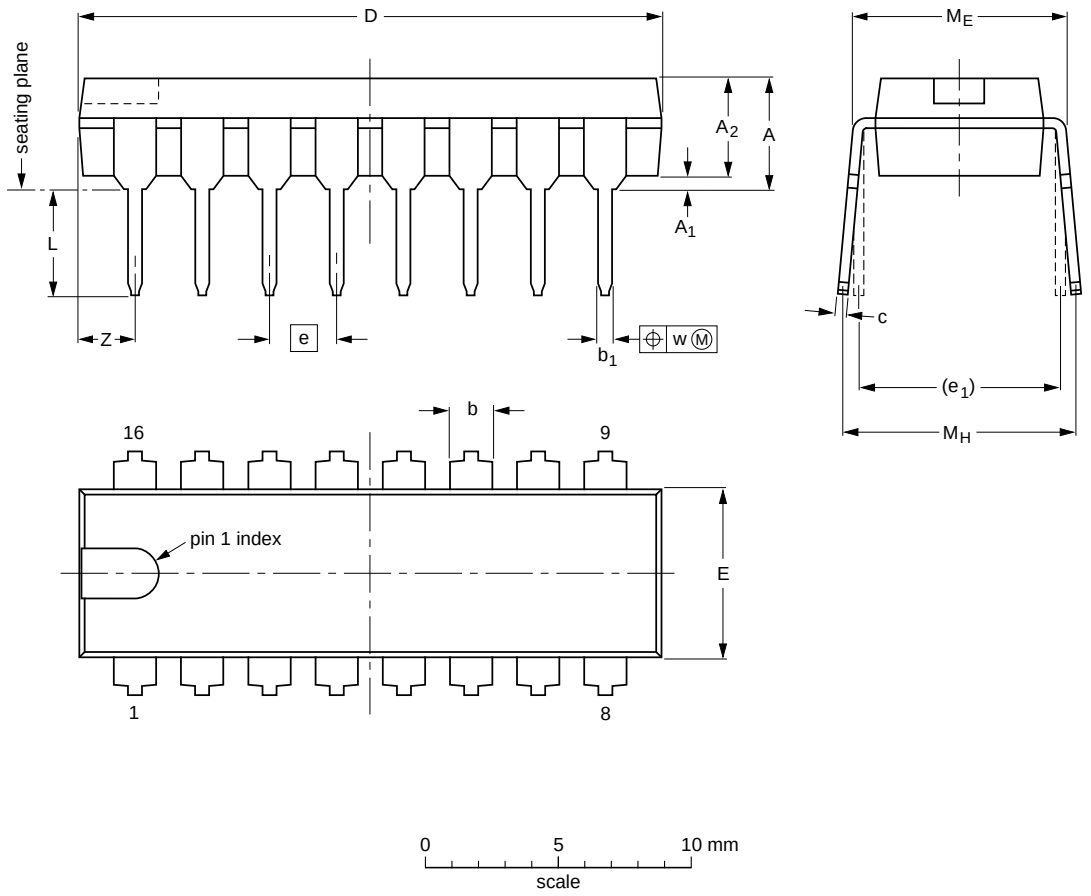


Fig.14 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

15 PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

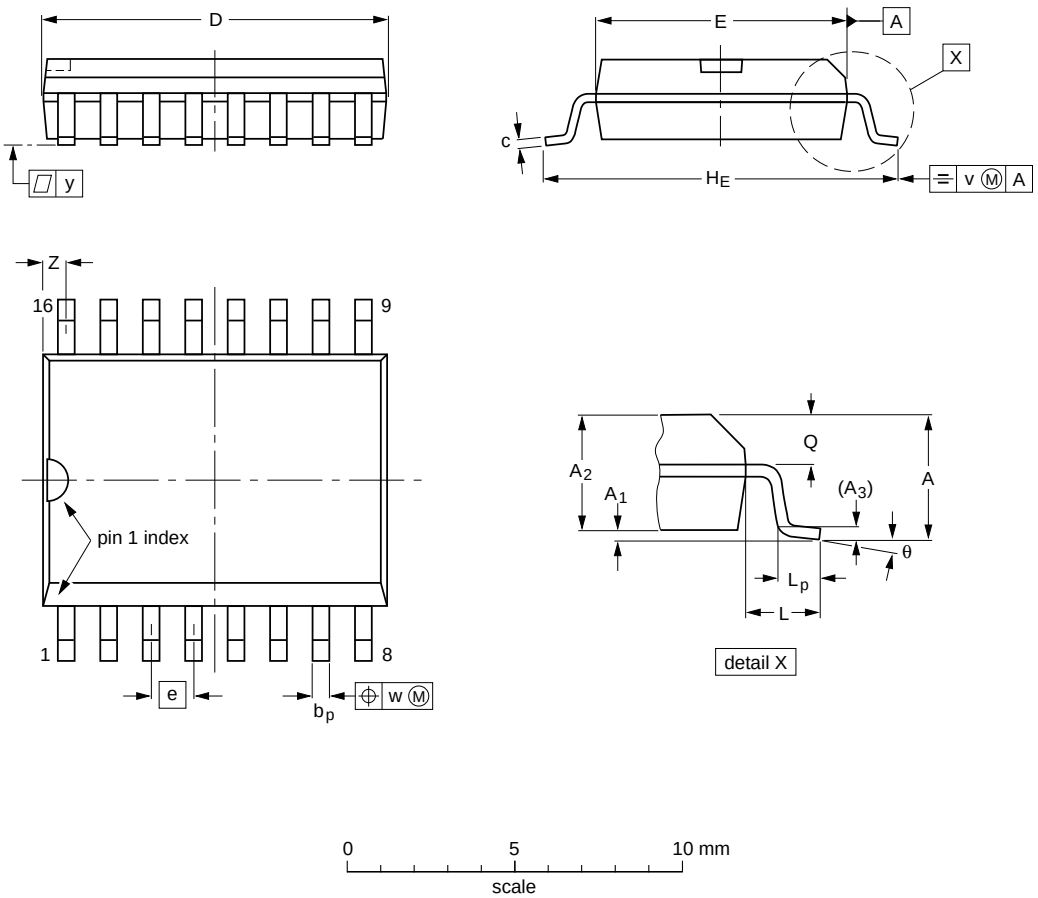
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~92-11-17~~ 95-01-24

16 SOLDERING

16.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

16.2 DIP

16.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

16.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

16.3 SO

16.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

16.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

18 LIFE SUPPORT APPLICATIONS

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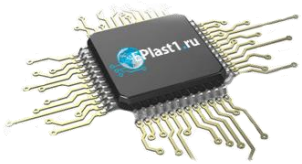

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