Evaluation Board User Guide
UG-382

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Evaluation Board for FSK AD5700/AD5700-1 HART Modem

FEATURES

Convenient connections for power through screw Terminal block
Use of on-chip RC oscillator or an external crystal
Various link options

EQUIPMENT NEEDED

Host controller with UART interface

GENERAL DESCRIPTION

This user guide describes the evaluation board for the AD5700/AD5700-1 Highway Addressable Remote Transducer (HART®) modem. This board can be used to evaluate either the AD5700 or the AD5700-1 part. Both can operate from a single 2 V to 5.5 V supply, with the AD5700-1 having the added feature of an integrated oscillator.

Complete specifications for both products can be found in the AD5700/AD5700-1 data sheet available from Analog Devices, Inc., which should be consulted in conjunction with this user guide when using the evaluation board.

EVALUATION BOARD

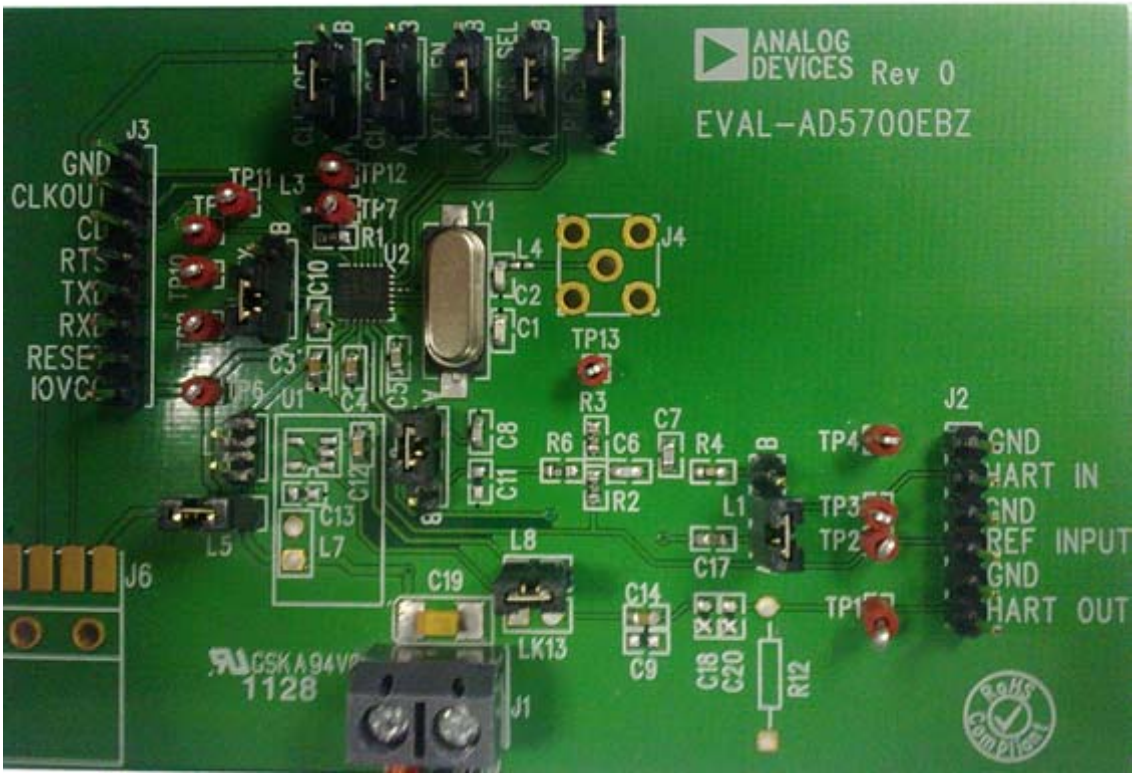

Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

2/12—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

AGND and DGND are connected together on the board to provide a single GND signal. To power the EVAL-AD5700-1EBZ, supply 3.3 V between the V_{CC} and GND inputs for the analog supply of the AD5700/AD5700-1. With L5 inserted (default), this also provides power to IOV_{CC}.

LINK OPTIONS

A number of links on the evaluation board must be set for the required operating setup before using the board. The functions of these link options are described in detail in Table 2. The default setup is using the on-chip reference, the crystal oscillator, and the internal receive filter (see Table 1).

Table 1. Default Link Options

Link No.	Option
CLK_CFG1	A
CLK_CFG0	A
XTAL_EN	A
FILTER_SEL	B
L1	A
L2	A
REF_EN	B
DUPLEX	A
L5	Inserted
L6	Not inserted
L8	Inserted

Table 2. Link Functions

Link No.	Function				
CLK_CFG1, CLK_CFG0, XTAL_EN	The AD5700/AD5700-1 support numerous clocking configurations to allow a simple, low cost solution. The AD5700/AD5700-1 can use an external crystal or ceramic resonator, a CMOS input, or an internal RC oscillator (AD5700-1 only). The CLK_CFG0, CLK_CFG1, and XTAL_EN links configure the clock generation as follows:				
	XTAL_EN	**CLK_CFG1**	**CLK_CFG0**	**CLKOUT**	**Description**
	B	A	A	No output	3.6864 MHz CMOS clock connected at XTAL1 pin
	B	A	B	No output	1.2288 MHz CMOS clock connected at XTAL1 pin
	B	B	A	No output	Internal oscillator enabled
	B	B	B	1.2288 MHz output	Internal oscillator enabled, CLKOUT enabled
	A	A	A	No output	Crystal oscillator enabled
	A	A	B	3.6864 MHz output	Crystal oscillator enabled, CLKOUT enabled
	A	B	A	1.8432 MHz output	Crystal oscillator enabled, CLKOUT enabled
	A	B	B	1.2288 MHz output	Crystal oscillator enabled, CLKOUT enabled
FILTER_SEL, L1, L2	These link options set whether the internal or external receive band-pass filter is used at the HART input. Setting FILTER_SEL to Position B and L1 and L2 to Position A sets the board to use the internal receive band-pass filter. Setting FILTER_SEL to Position A and L1 and L2 to Position B sets the board to use the external receive band-pass filter.				
REF_EN	This sets whether the internal or an external reference is used. Position A—disables the internal reference, and a buffered external 2.5 V reference source must be applied at REF. Position B—enables the internal 1.5 V reference and buffer.				
DUPLEX	Allows the modulator and demodulator of the AD5700/AD5700-1 to be enabled at the same time. Position A—the AD5700/AD5700-1 operate in half-duplex operation (controlled by $\overline{RTS}$). Position B—the AD5700/AD5700-1 operate in full duplex operation, with the modulator and demodulator of the AD5700/AD5700-1 enabled at the same time.				
L5	Allows V_{CC} to be connected directly to IOV_{CC}. Inserted—V_{CC} is connected to IOV_{CC}. Not inserted—V_{CC} is disconnected from IOV_{CC}.				
L6	Do not insert this link.				
L8	This link must be inserted.				

EVALUATION BOARD SCHEMATIC AND ARTWORK

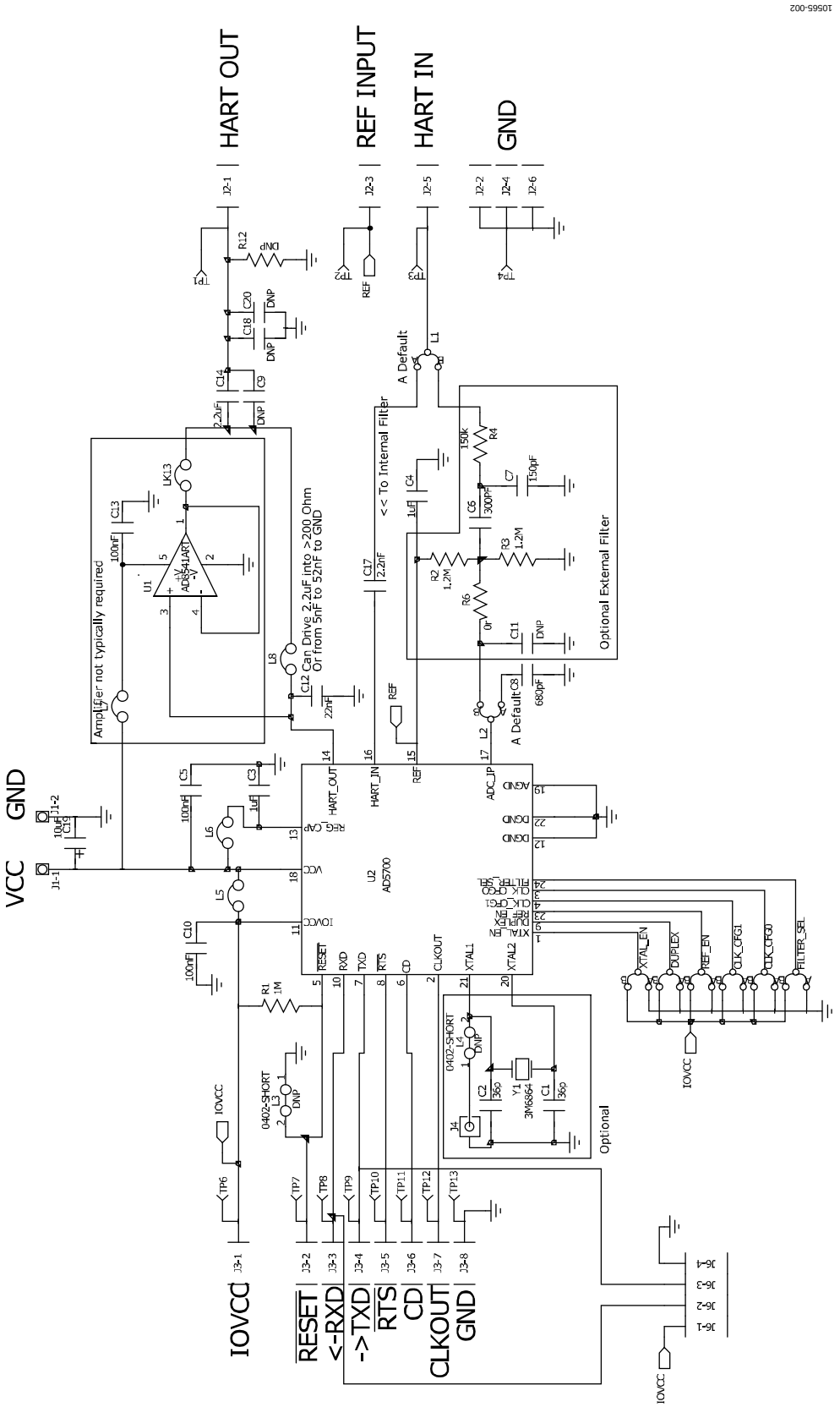

Figure 2. Schematic of Controller Circuitry

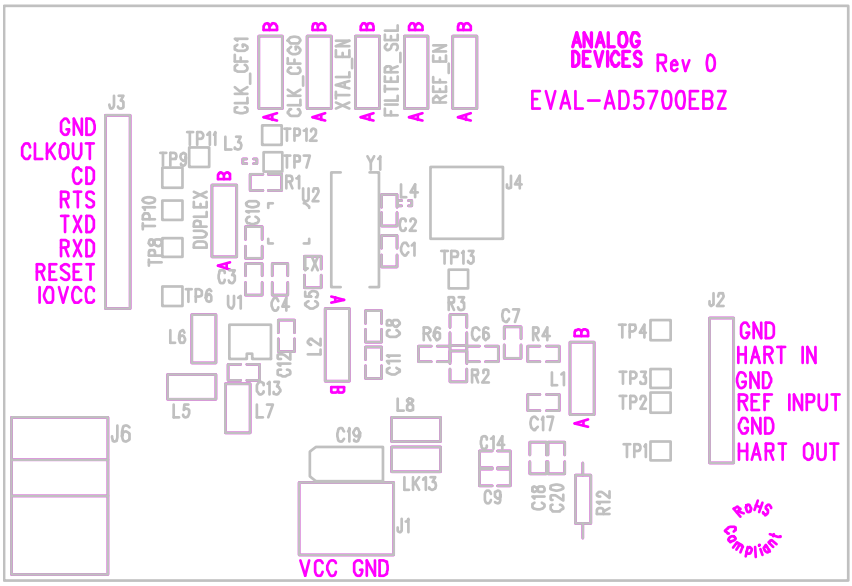

Figure 3. Component Placement Drawing

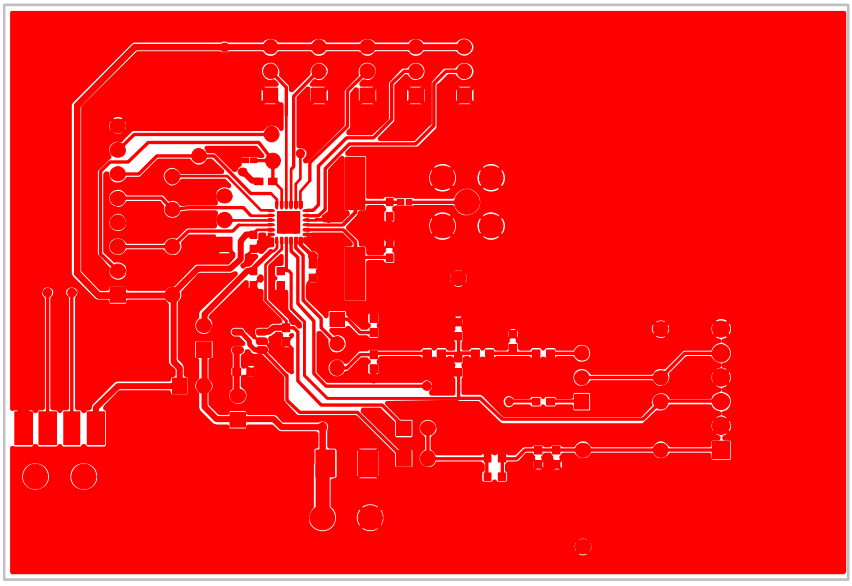

Figure 4. Component Side PCB Drawing

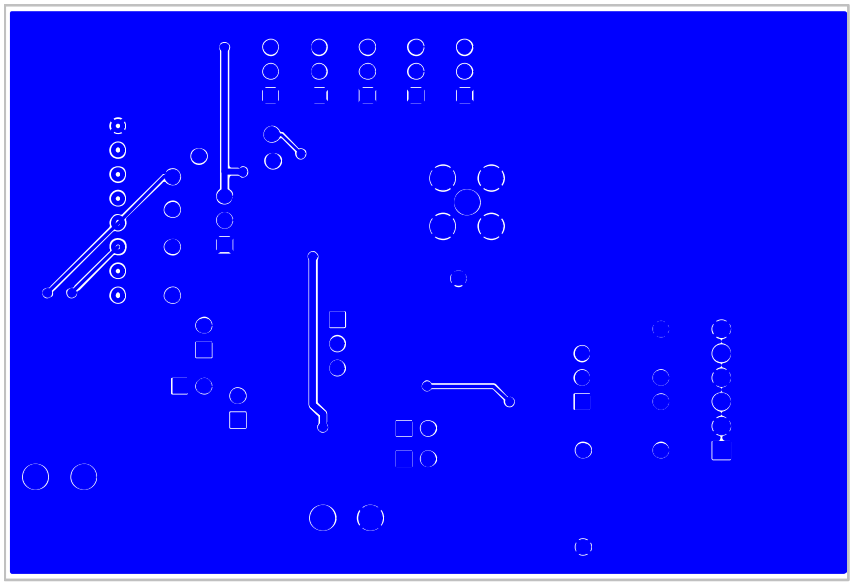

Figure 5. Solder Side PCB Drawing

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Quantity	Reference Designator	Description	Part Number	Supplier/Number
1	U2	HART modem	AD5700-1BCPZ	Analog Devices
2	C1, C2	36 pF, C0G capacitor (0603)	C0603C360J5GACTU	FEC 1865478
2	C3, C4	1 µF, X7R capacitor (0603)	C0603C105K4RACTU	FEC 1828826
2	C5, C10	100 nF, X7R capacitor (0603)	MCCA000159	FEC 1759016
1	C6	300 pF, C0G capacitor (0603)	GRM1885C1H301JA01D	Digi-Key 490-1438-1-ND
1	C7	150 pF, C0G capacitor (0603)	06031A151JAT2A	FEC 1740606
1	C8	680 pF, C0G capacitor (0603)	MCCA000221	FEC 1759084
1	C12	22 nF, X7R capacitor (0603)	06035C223KAT2A	FEC 1658869
1	C14	2.2 µF, X7R capacitor (0603)	GRM188R71A225KE15D	FEC 1797012
1	C17	2.2 nF, C0G capacitor (0603)	C0603C222J5GACTU	FEC 1535565
1	C19	10 µF, tantalum capacitor (Case A)	TCJA106M010R0300	FEC 1135234
10	CLK_CFG0, CLK_CFG1, DUPLEX, FILTER_SEL, REF_EN, XTAL_EN, J2, J3, L1, L2	Headers	M20-9990345	FEC 1022248
1	J1	2-pin terminal block	CTB5000/2	FEC 151789
3	L5, L6, L8	2-pin (0.1" pitch) header and shorting shunt	M20-9990246	FEC 1022247
1	R1	1 MΩ (0603)	MC 0.063W 0603 5% 1M	FEC 9331727
2	R2, R3	1.2 MΩ (0603)	RC0603FR-071M2L	FEC 9238859
1	R4	150 kΩ (0603)	MC 0.063W 0603 1% 150K	FEC 9330623
1	R6	0 Ω (0603)	CRCW06030000Z0EA	FEC 1469739
13	TP1 to TP13	Test point	20-313137	FEC 8731144
1	Y1	Quartz crystal SMD	ABLS-3.6864MHZ-L4Q-T	Digi-Key 535-9893-1-ND

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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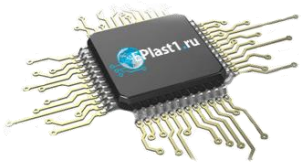

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