

Secondary power supply series for automotive

# 2.69 to 5.5V, Fixed Output, 2.25MHz Synchronous Step-Down Converter



## BD9052xEFJ-C Series

### ●General Description

The BD9052xEFJ-C series is a synchronous rectification type step-down DC/DC converter with a 2.25MHz fixed frequency that operates in with an input voltage range of 2.69V-5.5V. It has an integrated feedback resistor that supplies a fixed output voltage of 1.2V/1.5V/1.8V and a phase compensation constant. Applications can be created with a minimum of three external components. Moreover, the integrated Pch and Nch output MOSFET can supply a maximum output current of 2A.

### ●Features

- Integrated output feedback resistors and phase compensation network, contributes to minimize external components for the applications.
- Excellent load response through current mode control
- Integrated Pch and Nch output MOSFET
- Integrated overcurrent protection with auto-reset
- Integrated output overvoltage detection/short-circuit detection
- Integrated TSD and UVLO
- Light load mode/PWM fixation operation selection pin

### ●Applications

- Automotive equipment
- Car audio and navigation
- TV
- Other electronic equipment

### ●Typical application circuit

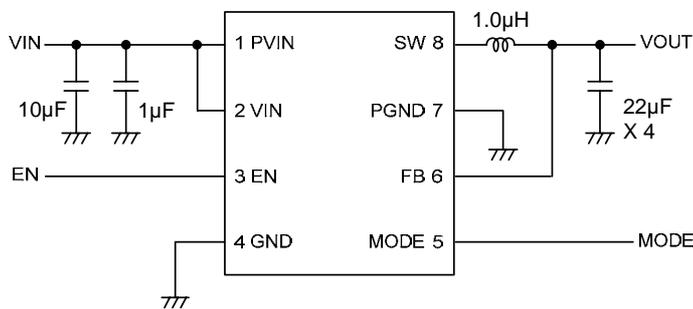


Figure 1. Typical application circuit (BD90525EFJ-C, VIN=5V, IOUT=2A)

### ●Key Specifications

■ Input voltage range	2.69V~5.5[V]
■ Output voltage	
BD90522EFJ-C	1.2 [V](Typ.)
BD90525EFJ-C	1.5 [V](Typ.)
BD90528EFJ-C	1.8 [V](Typ.)
■ Output voltage accuracy	±2.0[%](-40~125°C)
■ Operating frequency	2.25 [MHz] (Typ.)
■ Maximum output current	2.0 [A] (Max.)
■ Circuit current at standby	0[µA](Typ., 25°C)
■ Operational temperature range	-40~+125°C

### ●Package

HTSOP-J8

4.90 mm×6.00 mm×1.00 mm

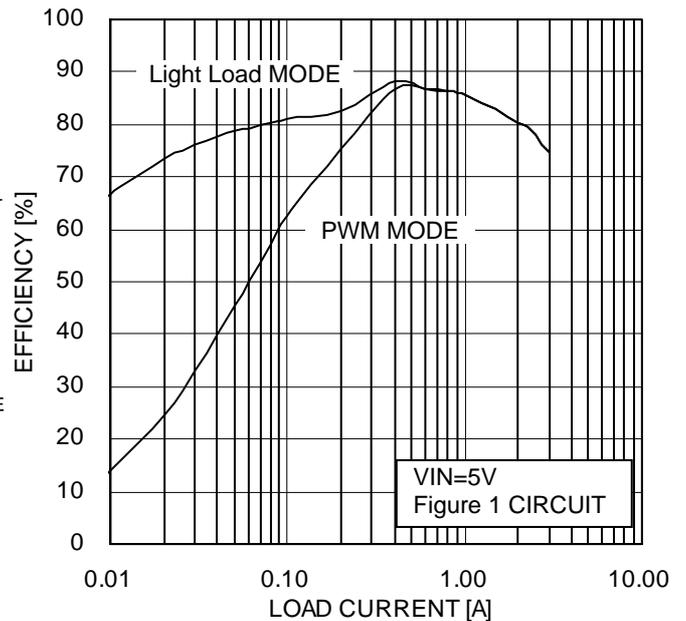
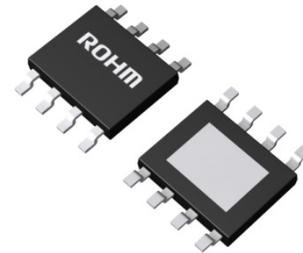


Figure 2. Efficiency (BD90525EFJ-C)

●Pin Configuration [TOP VIEW]

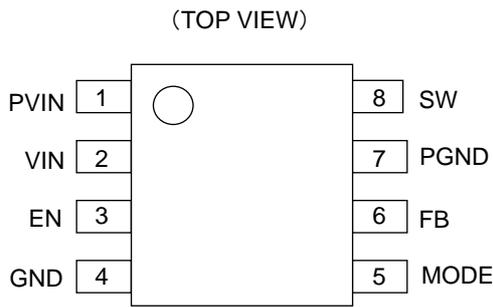


Figure 3. Pin arrangement diagram

●Pin Description

Pin	Symbol	Function
1	PVIN	Power supply pin for output FET
2	VIN	Power supply pin
3	EN	Enable pin
4	GND	GND pin
5	MODE	Light load mode/Fixed PWM mode select pin
6	FB	Output feedback pin
7	PGND	GND pin for output FET
8	SW	SW pin

●Block diagram

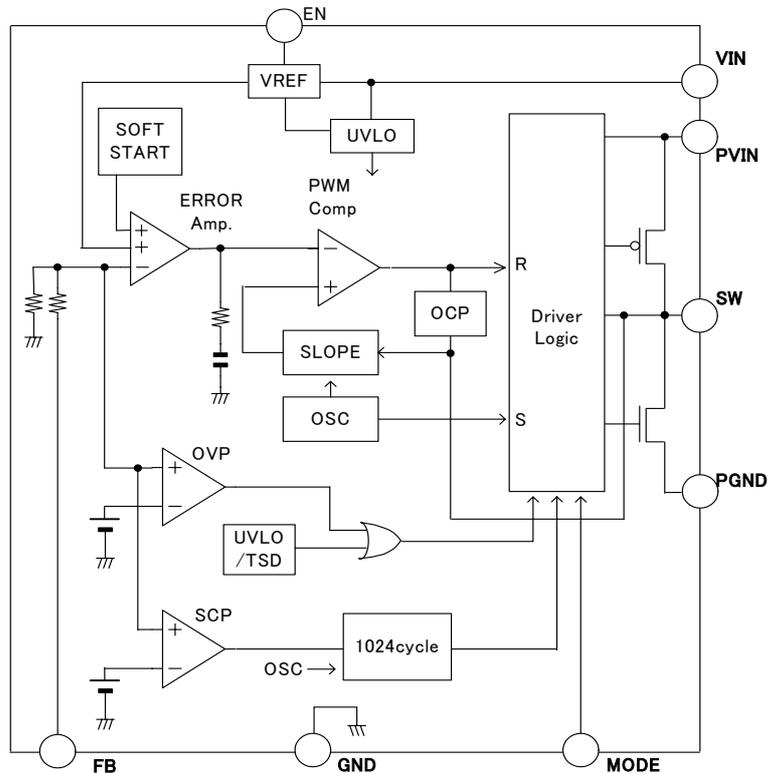


Figure 4. Block diagram

●Block operation descriptions

■ Standby

The circuit enters the state of standby when the EN pin is set to 0.7V or less. All the circuits, such as internal reference voltage VREF, oscillators OSC, and drivers are turned off during standby, and current consumption of the power supply becomes 0 $\mu$ A(25°C, Typ.). Via the FB pin, the output capacitor is discharged at a resistance of 1k $\Omega$ .

■ Start operation

The circuit starts operating when EN pin is set to 2.1V or more. A soft start circuit (SOFT START) is integrated to prevent inrush current to the capacitor when starting. The output voltage reaches a set voltage with 1ms(Typ.) while following the startup of the soft start circuit. There is a delay of about 200 $\mu$ sec until the soft starts begins after the EN pin is turned on and the internal logic operation is started. In order to prevent a defective start, the short-circuit protection is not active during startup.

■ Error amplifier and phase compensation

The voltage of the output feedback pin(FB) is compared with an internal reference voltage. The voltage corresponding to the difference will be generated, and sent to the PWM comparator which determines the duty ratio of the output. The feedback resistor which determines the output voltage, resistance for compensations, and the capacitor are integrated into the BD9052xEFJ-C series.

■ Oscillator

The 2.25MHz(Typ.) internally fixed clock is generated and sent to the slope generation circuit (SLOPE) and to the driver.

■ Light load mode and Forced PWM mode

BD9052xEFJ-C operates in the light load mode when the MODE pin is set to 0.7V or less. When the output load current is small, the switching operation automatically becomes intermittent in the light load mode. The efficiency at light load improves compared to the Forced PWM mode because the switching loss is suppressed by operating intermittently. The intermittently operating load current level changes depending on the input voltage, inductor value, etc.

If the MODE pin is set to 2.1V or more, the chip operates in Forced PWM mode. In the Forced PWM mode, the efficiency at a light load decreases compared with the light load mode. However, because of the fixed frequency switching through the entire load range, noise is more easily countered.

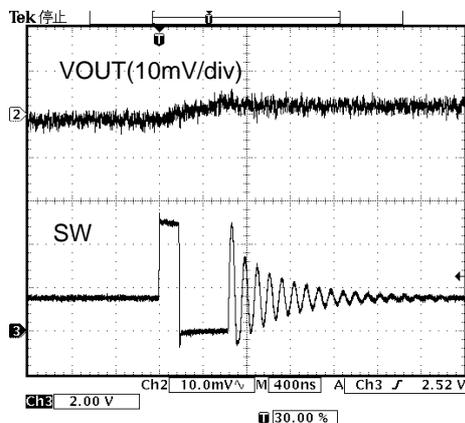


Figure 5. Switching operation at light load mode

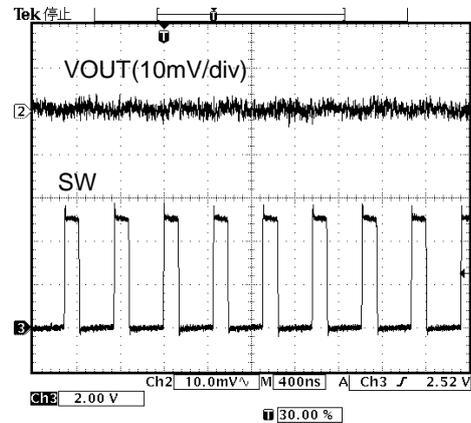


Figure 6. Switching operation at PWM mode

■ Overcurrent detection

When in the output stage the current flowing to the Pch FET is 2.0A(Min.) or more, the Pch FET is turned off and the power supply to the output is intercepted. The overcurrent detection is operated every cycle, limits the switching duty, and returns at the next clock cycle.

- Output short-circuit detection

The output short-circuit detection circuit (SCP) detects a short-circuit of the output when output voltage falls below 70% of a set value during 1024 cycles of the frequency. In this case, the Pch FET and Nch FET of the output are turned off, and the power supply is intercepted. The count is reset when the output voltage returns to 70% or more before 1024 cycles, and the output voltage returns to the set value.

This SCP automatically resets when after 1024 cycles of the frequency after detecting the short-circuit, and switching is restarted. Resetting triggers the soft start operation because the internal soft start circuit is initialized when the short-circuit detection is activated. The short-circuit detection circuit is not active while soft start is starting. In case the short-circuit continues after resetting, the cycle of starting with a soft start, turning off the output after 1024 cycles, and returning after 1024 cycles is repeated.

- Output overvoltage detection

When the output overvoltage detection circuit (OVP) detects that the output voltage is exceeding 120% of a set value, the Pch FET and Nch FET of the output are turned off and the power supply is intercepted. Switching is restarted if after the power supply interception the output decreases and the overvoltage situation is released. The overvoltage detection voltage and the release voltage have a hysteresis of about 100mV.

- UVLO

The UVLO circuit is activated and shuts down the circuit when the input voltage (VIN) decreases to 2.6V or less. When the UVLO is activated, the control circuit of the error amplifier, the oscillator, the driver and the output are turned off. Via the FB pin, the output capacitor is discharged at a resistance of 1kΩ. Afterwards, UVLO is released when the input voltage VIN rises to 2.69V or more, and the output is restored. The output voltage starts with soft start when UVLO is reset.

- Thermal shutdown(TSD)

Thermal shutdown (TSD) is activated when the IC junction part temperature exceeds 175 °C(Typ.). When the TSD is activated the control circuit of the error amplifier, the oscillator, the driver and the output are turned off. There is hysteresis in the detection temperature of TSD, which is reset when the junction temperature decreases to 150°C(Typ.) or less. The output voltage starts with soft start when TSD is reset.

## ● Absolute maximum rating

Parameter	Symbol	Rating	Unit
VIN voltage	VIN	-0.3~7 *1	V
PVIN voltage	PVIN	-0.3~7 *1	V
EN voltage	EN	-0.3~7	V
SW voltage	SW	-1.0~PVIN *1	V
FB voltage	FB	-0.3~7	V
MODE voltage	MODE	-0.3~7	V
Power dissipation	Pd	3.75 *2	W
Operating temperature range	Topr	-40~+125	°C
Storage temperature range	Tstg	-55~+150	°C
Junction temperature	Tj	+150	°C

\*1 Pd should not be exceeded.

\*2 33.3mW/°C reduction when  $T_a \geq 25^\circ\text{C}$  if mounted on 4 layers glass epoxy board of 70mmx70mmx1.6mm

● Recommended operating range( $T_a = -40 \sim +125^\circ\text{C}$ )

Parameter	Symbol	Rating	Unit
VIN voltage	VVIN	2.69~5.5	V
PVIN voltage	VPVIN	2.69~5.5	V
EN voltage	VEN	0~5.5(*1)	V
MODE voltage	VMODE	0~5.5	V
Output current	ISW	0~2	A

\*1 The circuit goes into test mode when the EN pin is set at 6V or higher.

●Electrical characteristics (unless otherwise specified: Ta=-40~+125°C, VIN=PVIN=5V, EN=3.3V)

Parameter	Symbol	Ratings			Unit	Conditions
		Min.	Typ.	Max.		
Standby circuit current	IST	-	0	1	μA	EN=0V, Ta=25°C
Circuit current	ICC	-	650	1300	μA	FB=VFB+0.1V, Ta=25°C
UVLO detection voltage	VUVLO1	2.30	2.45	2.60	V	Sweep down
UVLO release voltage	VUVLO2	2.40	2.55	2.69	V	Sweep up
EN threshold voltage	VEN	0.7	1.4	2.1	V	
EN inflow current	IEN	0.2	0.7	1.2	μA	EN=3.3V
Operating frequency	FOSC	1.8	2.25	2.7	MHz	
Output voltage(BD90522EFJ-C)	VFB	1.176	1.20	1.224	V	Io=0mA
Output voltage(BD90525EFJ-C)	VFB	1.470	1.50	1.530	V	Io=0mA
Output voltage(BD90528EFJ-C)	VFB	1.764	1.80	1.836	V	Io=0mA
FB pull-down resistance	RFB	0.4	1	2	MΩ	FB=VFB
Soft start time	TSS	0.4	1	2	ms	
Pch FET ON resistance	PRON	-	85	-	mΩ	
Nch FET ON resistance	NRON	-	70	-	mΩ	
Overcurrent detection current	IOCP	-	4.5	-	A	
Output overvoltage detection voltage	VOVP	Typ. -0.15	VFB × 1.2	Typ. +0.15	V	
Output short-circuit detection voltage	VSCP	Typ. -0.15	VFB × 0.7	Typ. +0.20	V	
MODE threshold voltage	VMODE	0.9	1.6	2.3	V	
MODE inflow current	IMODE	3.5	7	14	μA	MODE=3.3V

● Typical Performance Curve

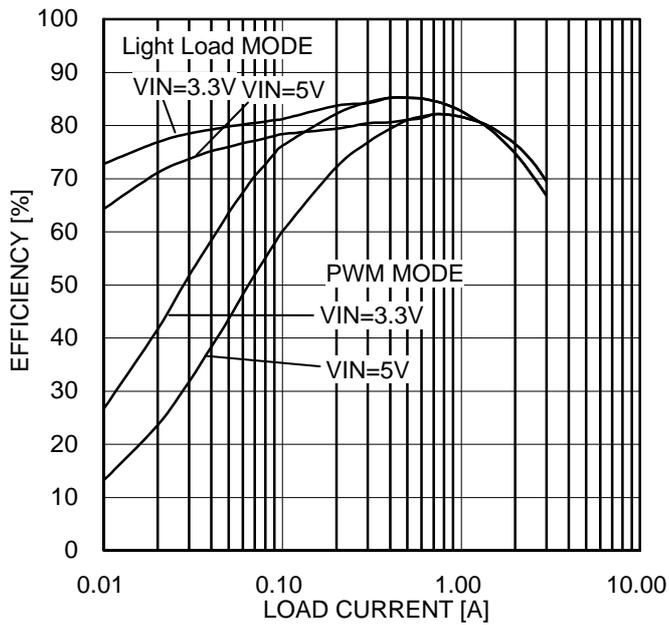


Figure 7. Efficiency(BD90522EFJ-C)

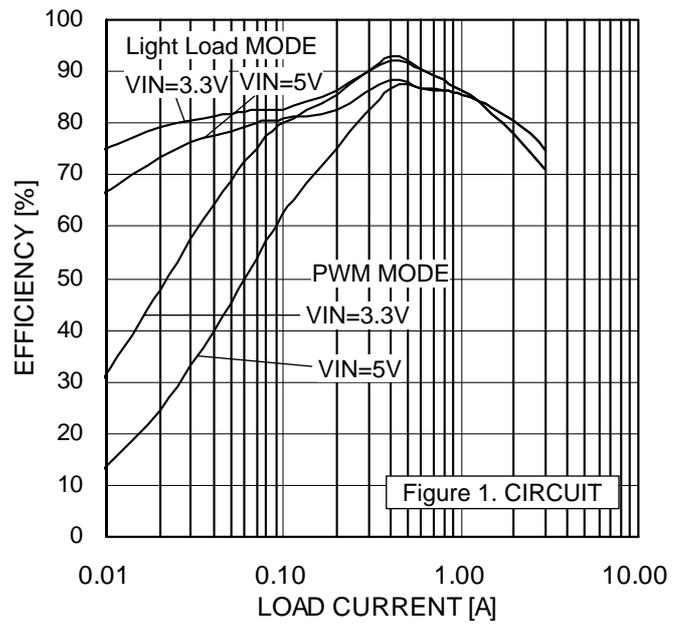


Figure 8. Efficiency(BD90525EFJ-C)

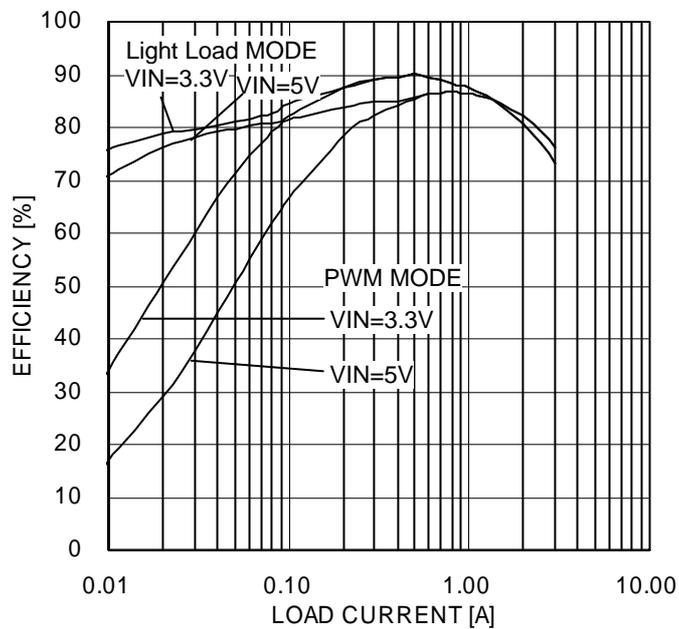


Figure 9. Efficiency(BD90528EFJ-C)

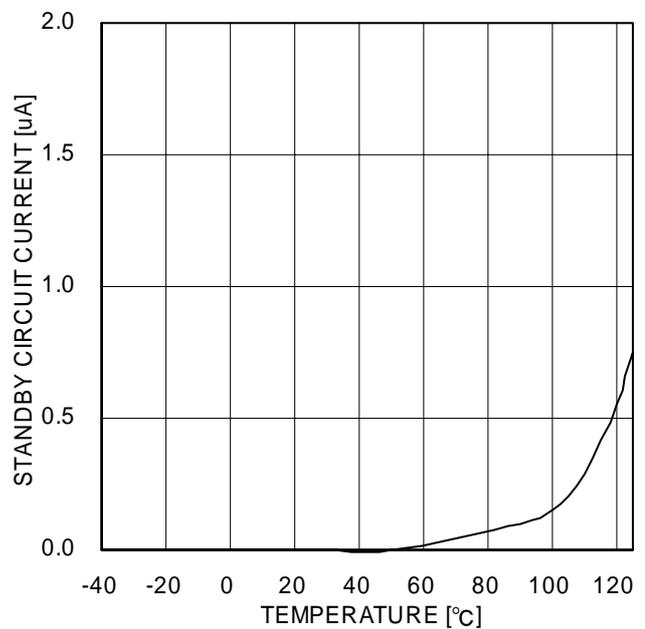


Figure 10. Standby circuit current

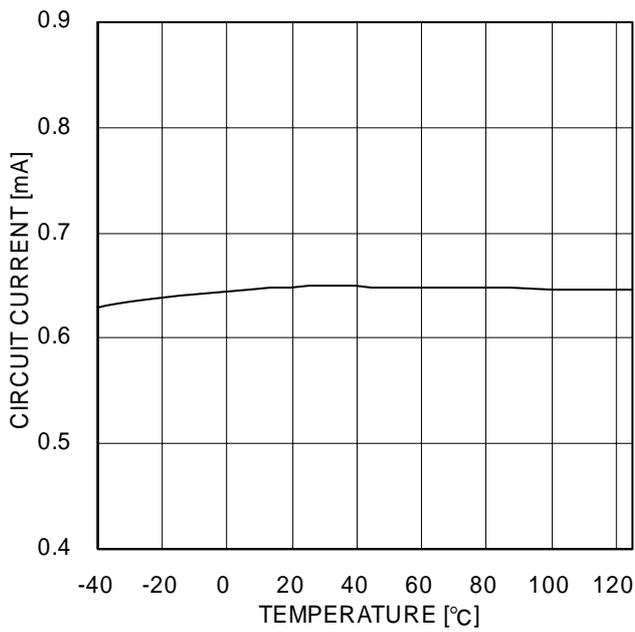


Figure 11. Circuit Current

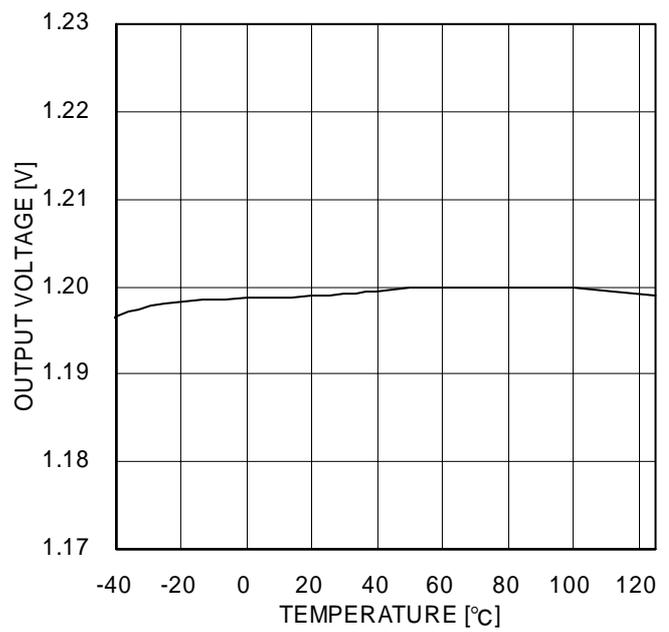


Figure 12. Output voltage vs. temperature (BD90522EFJ-C)

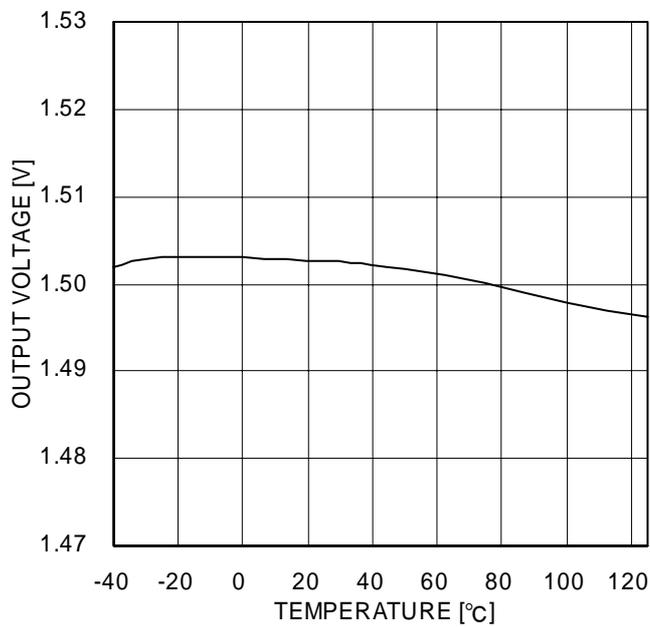


Figure 13. Output voltage vs. temperature (BD90525EFJ-C)

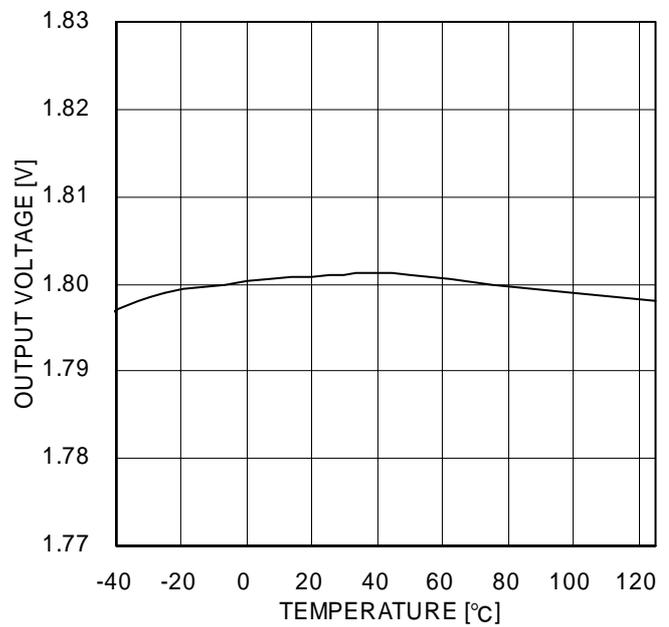


Figure 14. Output voltage vs. temperature (BD90528EFJ-C)

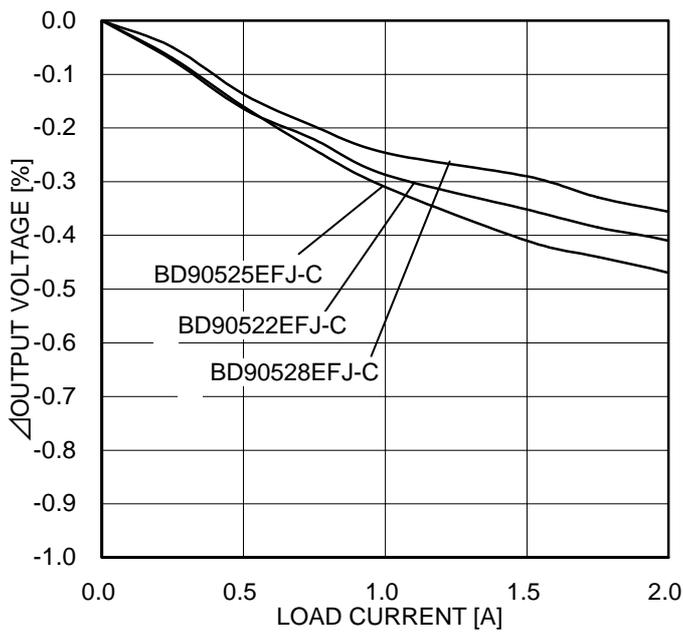


Figure 15. Load regulation

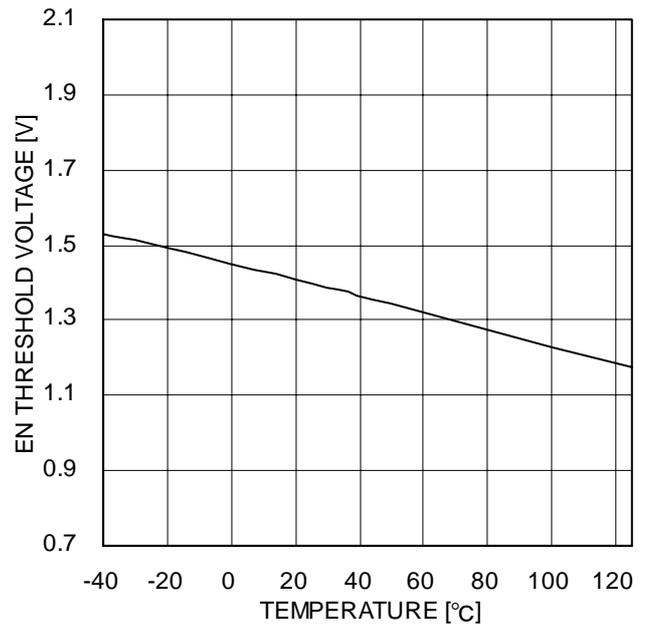


Figure 16. EN threshold voltage

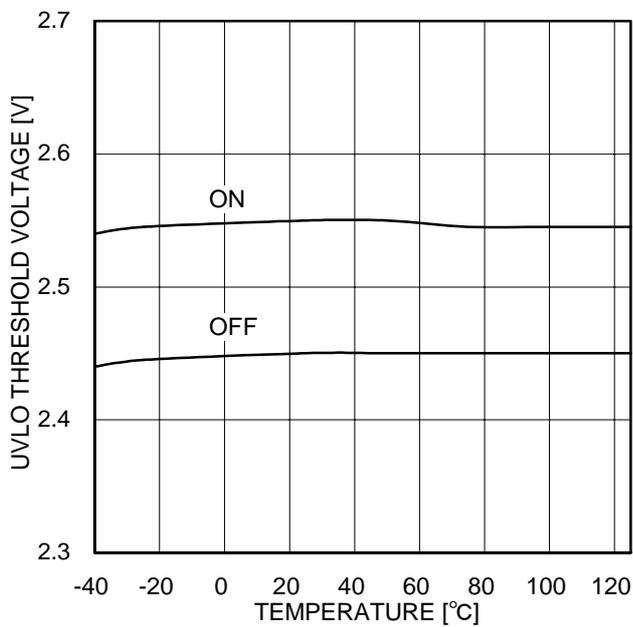


Figure 17. UVLO detect/release voltage

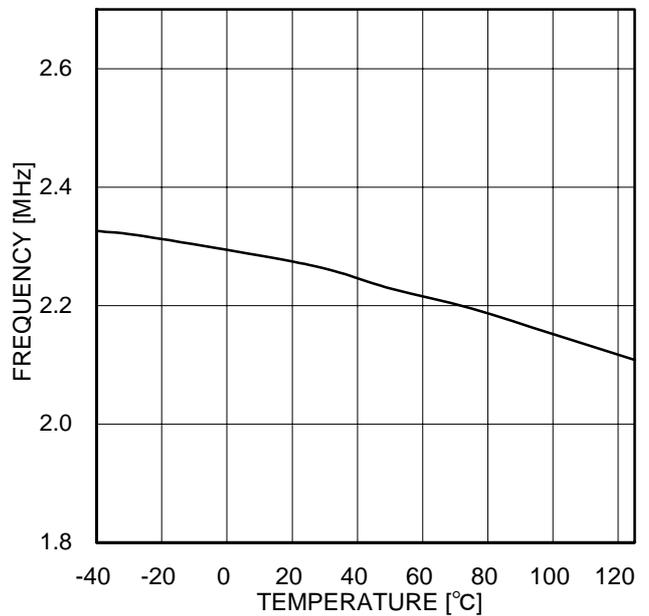


Figure 18. Frequency vs. temperature

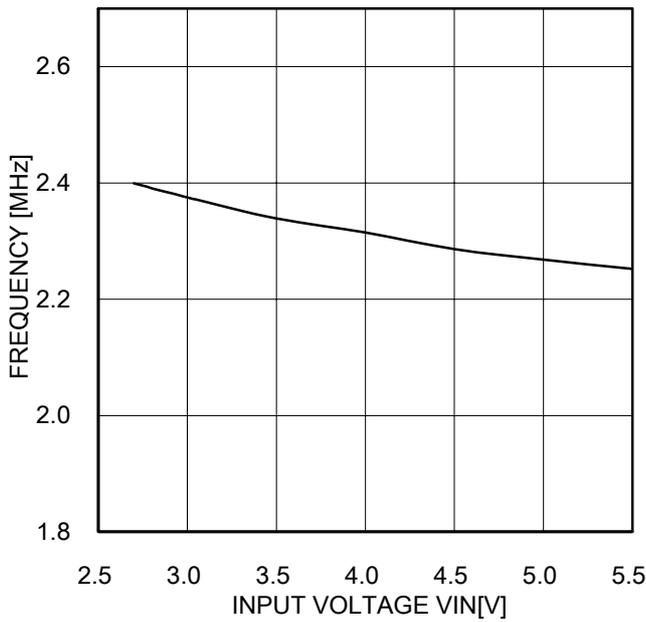


Figure 19. Frequency vs. input voltage

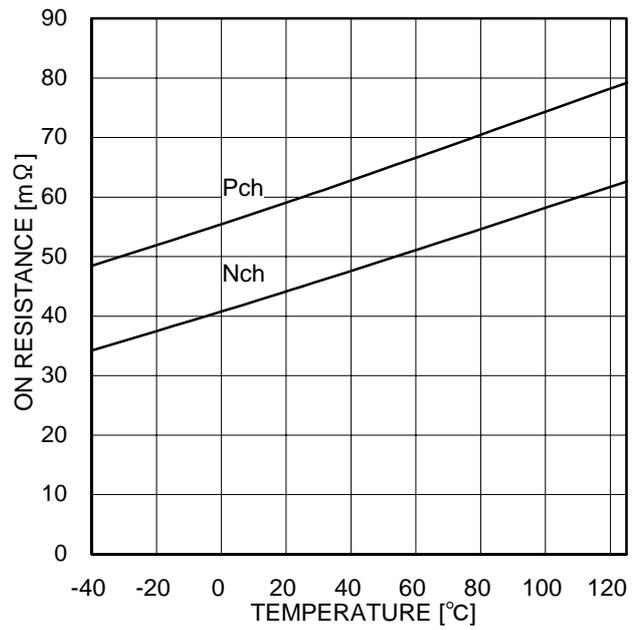


Figure 20. FET ON resistance

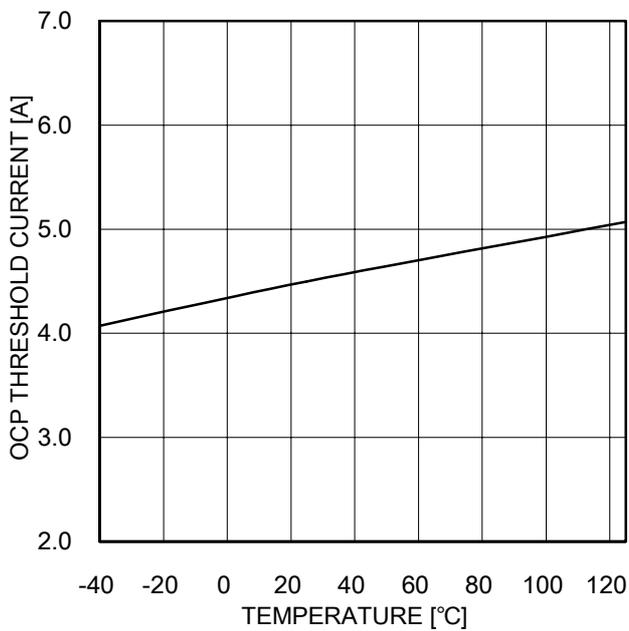


Figure 21. Over current detect vs. temperature

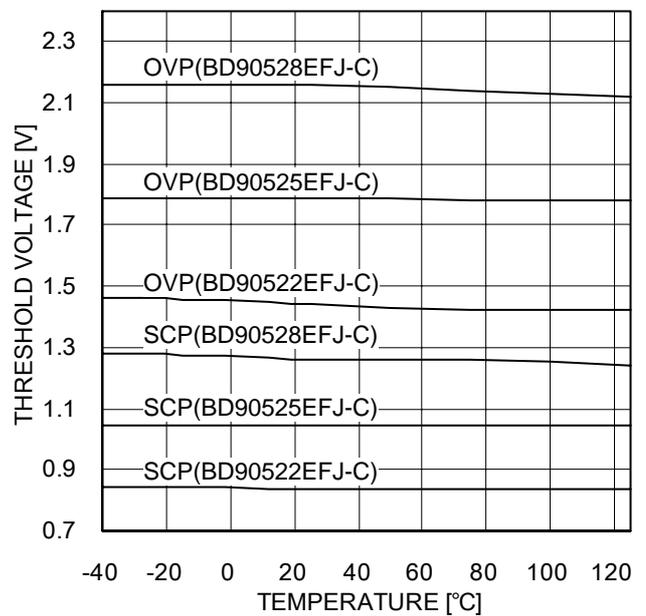


Figure 22. Output over/short detect voltage

The characteristics below are reference data which are measured with the typical application circuit as shown in Figure 1. Also, these characteristics are influenced by the external components and board layout.

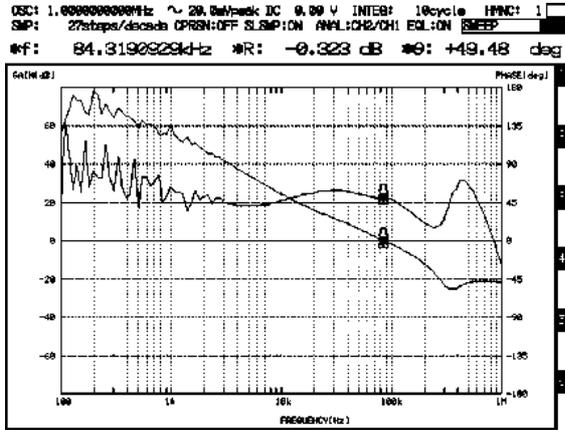


Figure 23. Loop response (BD90522EFJ-C, VIN=5V, IOUT=2A)

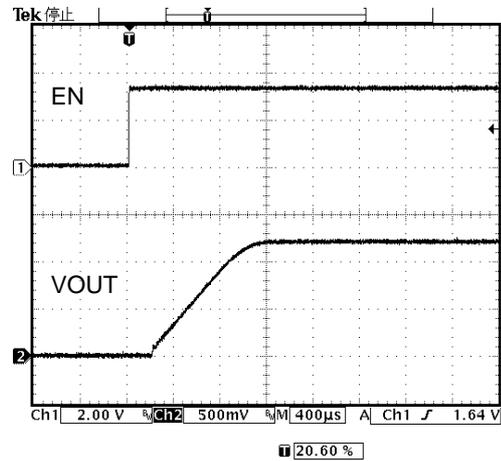


Figure 24. Start-up waveform (BD90522EFJ-C, VIN=5V, MODE=3.3V)

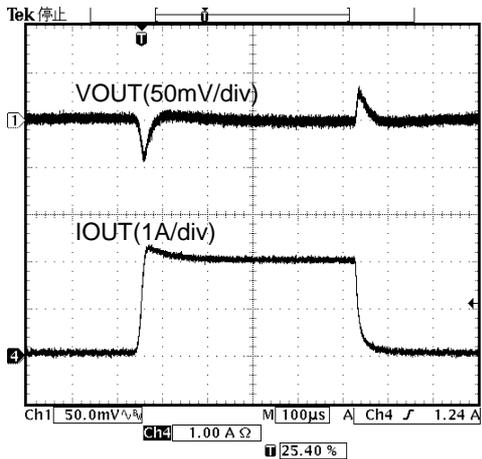


Figure 25. Load response (BD90522EFJ-C, VIN=5V, MODE=3.3V)

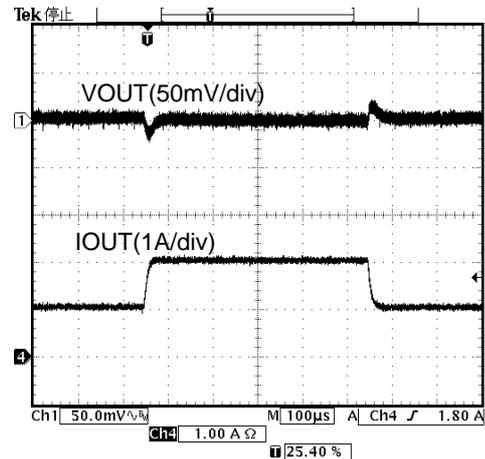


Figure 26. Load response (BD90522EFJ-C, VIN=5V, MODE=3.3V)

● Timing chart

■ Start-up

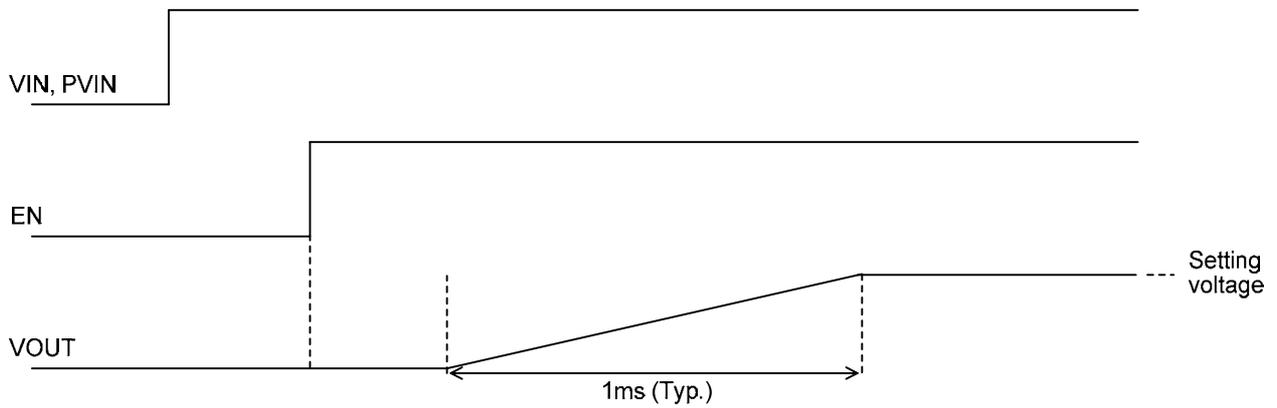


Figure 27. Start-up

■ OCP

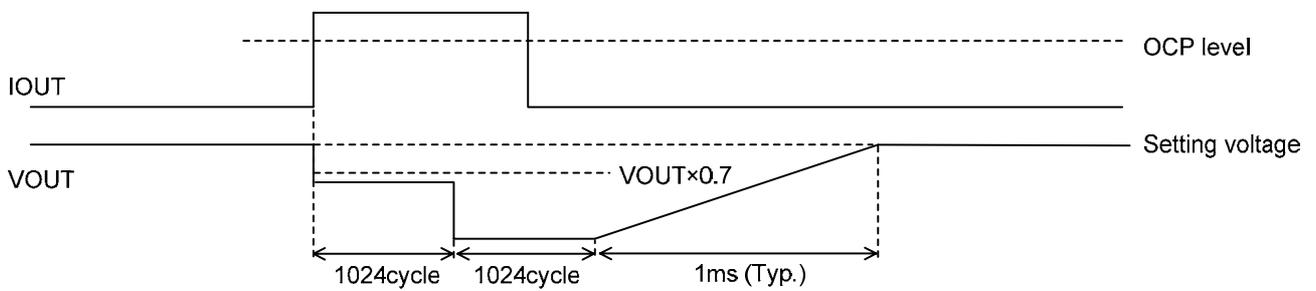


Figure 28. OCP

■ SCP

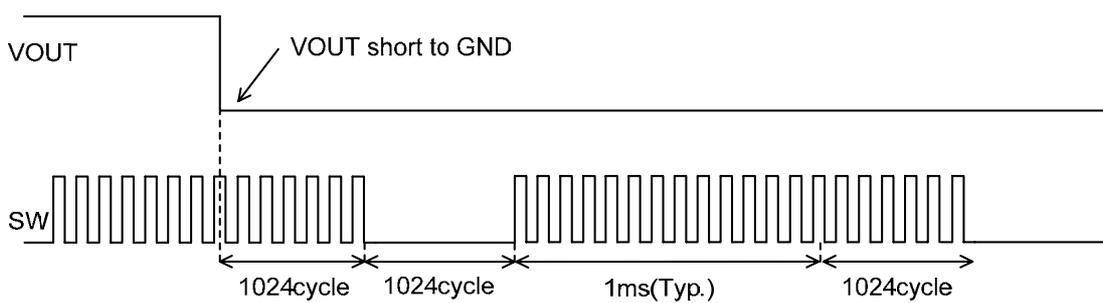


Figure 29. SCP

● Selection of external components

■ Selection of inductor

The inductor value significantly influences the output ripple current. The larger the coil is, the more the ripple current drops will be as shown in the equation below.

$$\Delta I_L = \frac{(P_{VIN} - V_{OUT}) \times V_{OUT}}{L \times P_{VIN} \times f} \quad [A]$$

An inductor with a low value will cause the ripple current to increase and also causes an increase of the ripple element of the output voltage. The optimal output ripple current setting is between 10% ~ 30% of the maximum output current.

$$\Delta I_L = 0.2 \times I_{OUTmax} \quad [A]$$

$$L = \frac{(P_{VIN} - V_{OUT}) \times V_{OUT}}{\Delta I_L \times P_{VIN} \times f} \quad [H]$$

( $\Delta I_L$ : Output ripple current, f: switching frequency)

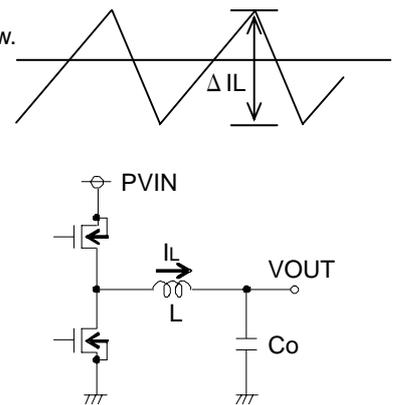


Figure 30. Ripple current

Supplying the coil with a current exceeding the coil's rated current will cause magnetic saturation of the coil and will decrease the efficiency of the coil. Please allow for a sufficient margin in selecting the inductor to ensure that the peak current does not exceed the inductor's rated current. Please select a coil with a small resistance element (DCR, ACR) to reduce the coil loss, and to improve efficiency.

■ Selection of input capacitor

The input capacitor serves to lower the impedance of the power supply connected to the input pin (VIN, PVIN). An increase of the impedance of this power supply can cause input voltage instability and may negatively impact oscillation and ripple rejection characteristics. Therefore, it is necessary to place an input capacitor in close proximity to the VIN, PVIN, GND and PGND pins.

We recommend selecting a ceramic capacitor with a value of 10uF or more that influenced by changes in temperature as little as possible and that has a sufficiently large permissible ripple current. The ripple current RMS can be calculated using the following equation.

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} (V_{IN} - V_{OUT})}{V_{IN}}} \quad [A]$$

Note that depending on the capacitor, the capacitance may be significantly influenced by the applied voltage. Please select a capacitor with good DC bias characteristics and with a high voltage.

■ Selection of output capacitor

We recommend selecting a ceramic capacitor. The ripple element of the output voltage is determined by the ESR of the output capacitor. Please take the permissible voltage of the actual application into consideration when selecting the output capacitor. The ripple element of the output voltage can be calculated by using the equation below. Selecting a low-ESR capacitor can reduce the ripple element of the output voltage. Note that depending on the capacitor, the capacitance may be significantly influenced by the applied voltage. Please select a capacitor with good DC bias characteristics and with a high voltage.

$$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{C_o} \times \frac{V_o}{V_{IN}} \times \frac{1}{f} \quad [V] \quad f: \text{Switching frequency}$$

The startup time needs to be within the soft start time. Therefore, please take the following equation into consideration when selecting the output capacitor

$$C_o \leq \frac{T_{SS} \times (I_{Limit} - I_{OUT})}{V_{OUT}}$$

T<sub>SS</sub>: Soft start time (typ. 1ms)

I<sub>Limit</sub>: Overcurrent detection value (min. 2A)

Non-optimal capacitance values may cause startup problems. Especially in cases of extremely large capacitance values, the possibility exists that the inrush current at startup will activate the overcurrent protection, thus not starting the output. Therefore, verification and confirmation with the actual application is recommended.

■ Selection of Schottky diode

Depending on the application the efficiency may be improved by placing a Schottky diode between the SW pin and PGND pin thereby creating a current path when the synchronous switching (Nch FET) is off. When selecting the Schottky diode ensure that the maximum reverse voltage is higher than the input voltage and that the rated current is higher than the maximum inductor current (the sum of the maximum output current and inductor ripple current).

●Notes on the substrate layout

The substrate layout greatly influences the stable operation of the IC. Depending on the substrate layout the IC might not show its original characteristics or might not function properly. Please note the following points when drawing the substrate layout.

- The input capacitors C1 and C2 should be placed as close as possible to the VIN, PVIN, GND and PGND pins.
- The output voltage feedback line should be separated from lines with a lot of noise such as the SW line.
- The GND signal should be separated from the input capacitor and the GND and PGND of the output capacitor and brought together at one point.
- The output capacitors C3 and C4 should be placed in close proximity to inductor L1.
- The inductor L1 should be placed as close as possible to the SW pin. The pattern area of the SW node should be as small as possible.
- The MODE pin should be pulled down via R3 by GND and pulled up via R2 by VIN. It is also possible to directly supply the MODE pin with voltage.
- The feedback frequency characteristics (phase margin) can be measured by inserting a resistor at the location of R1 and using FRA. However, this should be shorted during normal operation.

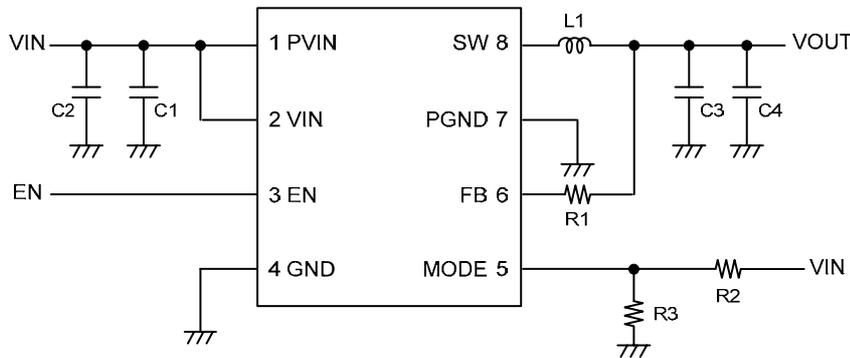


Figure 31. Reference circuit

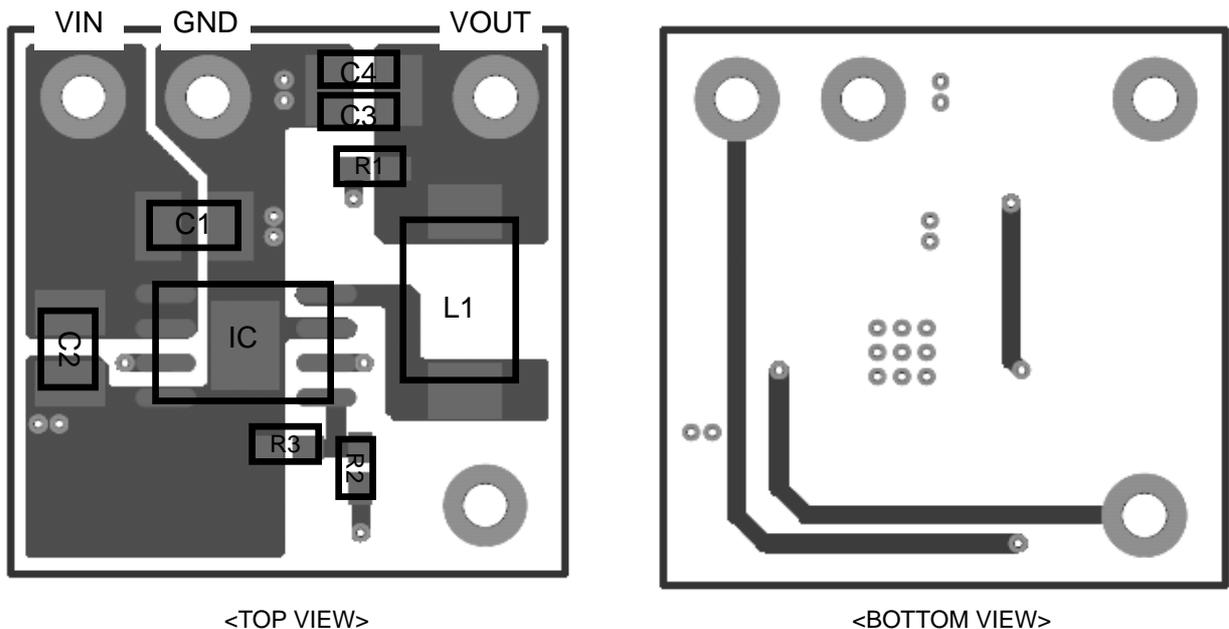


Figure 32. Reference layout pattern

●Heat dissipation

The maximum allowable junction temperature  $T_j$  of BD9052xEFJ-C series is 150°C. In case  $T_j$  exceeds 150°C, the temperature protection circuit is activated and the circuit shuts down. Therefore, it is necessary to design the system requirements and the board layout so that the junction temperature does not exceed 150°C in the power-supply voltage, the output load and the operating temperature range.

The maximum junction temperature can be calculated using the ambient temperature  $T_a$ , the thermal resistance  $\theta_{ja}$  of the package and heat dissipation  $P$  of the IC.

$$T_j = T_a + \theta_{ja} \times P \text{ [}^\circ\text{C]}$$

The thermal resistance  $\theta_{ja}$  of the package changes depending on the number of layers and the copper foil area of the board.

The heat dissipation  $P_{TOTAL}$  of the IC can be calculated by the equation below.

$$P_{TOTAL} = P_{ICC} + P_{RON} + P_{SW} \text{ [W]}$$

$P_{ICC} = V_{IN} \times I_{CC}$  ... Heat dissipation in control circuit  
 $P_{RON} = R_{on} \times I_o^2$  ... Heat dissipation in output FET  
 $P_{SW} = Tr \times I_o \times V_{IN} \times F$  ... Heat dissipation in switching

ICC: circuit current

Ron: ON resistance of the output FET

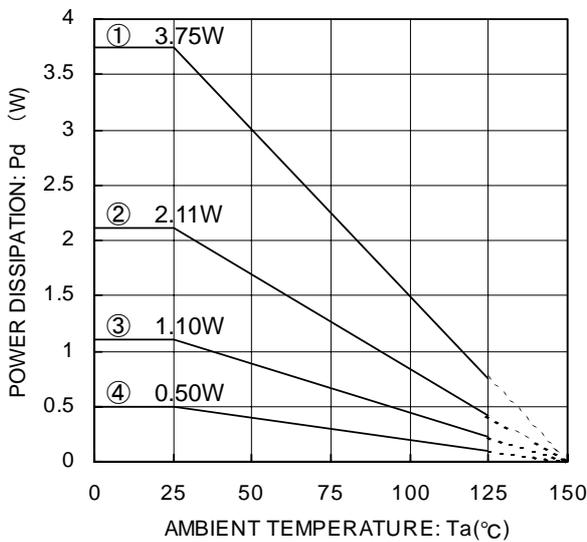
F: frequency

All values are specified in the electrical characteristics.

Tr is the rise time and fall time at switching. In the standard case is 5nsec and in the max case is 10nsec.

Also, these characteristics are influenced by the external components and board layout.

●Thermal derating characteristic

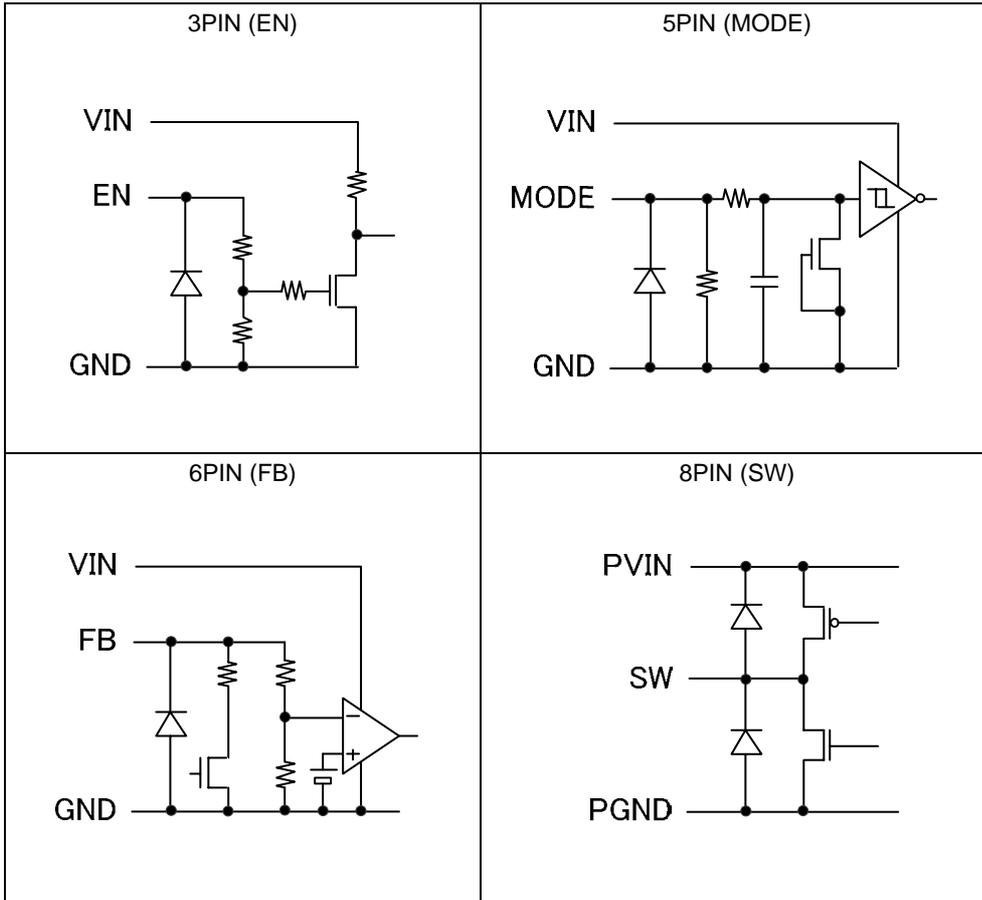


IC mounted on ROHM standard board  
 •Board size: 70mm×70mm×1.6mm  
 •The board and the back exposure heat radiation board part of package are connected with solder.

- ① IC unit,  $\theta_{ja}=249.5^\circ\text{C/W}$
- ② 2 layers board (Copper foil: 15mm×15mm),  $\theta_{ja} =113.6^\circ\text{C/W}$
- ③ 2 layers board (Copper foil: 70mm×70mm),  $\theta_{ja} =59.2^\circ\text{C/W}$
- ④ 4 layers board (Copper foil: 70mm×70mm),  $\theta_{ja} =33.3^\circ\text{C/W}$

Figure 33. Thermal derating characteristic

● I/O equivalence circuit



## ●Operational Notes

1. Absolute maximum ratings  
Exceeding the absolute maximum rating for supply voltage, operating temperature or other parameters may result in damages to or destruction of the chip. In this event it also becomes impossible to determine the cause of the damage (e.g. short circuit, open circuit, etc.). Therefore, if any special mode is being considered with values expected to exceed the absolute maximum ratings, implementing physical safety measures, such as adding fuses, should be considered.
2. Thermal protection circuit (TSD)  
If the junction temperature ( $T_j$ ) exceeds 175°C(Typ.) the thermal protection circuit (TSD) is activated and the output is put in the OFF status. The releasing temperature has hysteresis of about 25°C(typ.). The thermal protection circuit only functions to block thermal overloads from reaching the IC. Its purpose is not to protect the circuit or to guarantee the operations of the IC. Therefore, the IC should not be continuously operated after this circuit has been activated, nor should the IC be used in applications where the activation of this circuit is a prerequisite.
3. Overcurrent protection circuit  
This IC incorporates an integrated overcurrent protection circuit that operates in accordance with the rated output capacity. This circuit serves to protect the IC from damage when the load becomes shorted. The protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous or transitive operation of the protection circuit.
4. High temperature, no load behavior  
In a situation where there is a high temperature and no load, it might be that the leak current of the output transistor causes output voltage to rise (up to maximum  $V_{IN}$ ). In case it is expected that in the application conditions the output load drops below 1mA, please place a 1k $\Omega$  resistor at the output in order to prevent a no-load situation.
5. Power dissipation, ASO  
Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip and lead to a decrease of the reliability. Therefore, allow for sufficient margins to ensure use within the power dissipation rating. Also, please ensure in the design that the absolute maximum rating of the output transistor and the ASO are not exceeded when operating the IC.
6. Operation in strong electromagnetic fields  
Use caution when operating in the presence of strong electromagnetic fields, as this may cause the IC to malfunction.
7. Connection to the power supply connector  
A reverse connection to the power supply connector may cause damages to the IC. In order to prevent against reverse connection damages please externally place a diode between the power supply and the power supply pin of the IC.
8. Inter-pin shorts and mounting errors  
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply or GND pins (caused by poor soldering or foreign objects) may result in damage to the IC.
9. Short to power supply, short to ground, inter-pin shorts  
Please avoid shorts between the output pin and the power supply ( $V_{IN}$ ,  $PV_{IN}$ ), shorts between the output pin and ground (GND, PGND) and shorts between the output pins.
10. Testing on application boards  
When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
11. GND potential  
The potential of the GND pin must be the minimum potential in the system in all operating conditions. Ensure that no pins are at a voltage below the GND at any time, regardless of transient characteristics.
12. Wiring of  $V_{IN}$  and GND  
For the wiring of  $V_{IN}$ ,  $PV_{IN}$ , GND and PGND please create a layout with as wide as possible wires and a minimum distance in between the wires. In case of both small signal lines and high current lines, use single-point grounding to separate the small-signal and high current patterns and to ensure that voltage changes stemming from the wiring resistance and high current do not cause any voltage change in the small-signal. Also place a capacitor at the grounding point for stabilization.

13. Capacitor between PVIN and PGND

The capacitor between PVIN and PGND absorbs the steep changes in voltage and current caused by the PWM drive and thereby suppress fluctuations in the PVIN voltage. However, this effect is diminished due to wiring impedance the further the capacitor is removed from the IC.

14. Input pins

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. Relations between each potential may form as shown in the example below, where a resistor and transistor are connected to a pin:

- With the resistor, when  $GND > Pin A$ , and with the transistor (NPN), when  $GND > Pin B$ :

The P-N junction operates as a parasitic diode.

- With the transistor (NPN), when  $GND > Pin B$ :

The P-N junction operates as a parasitic transistor by interacting with the N layers of elements in proximity to the parasitic diode described above.

Parasitic diodes inevitably occur in the structure of the IC. Their operation can result in mutual interference between circuits and can cause malfunctions and, in turn, physical damage to or destruction of the chip. Therefore do not employ any method in which parasitic diodes can operate such as applying a voltage to an input pin that is lower than the (P substrate) GND.

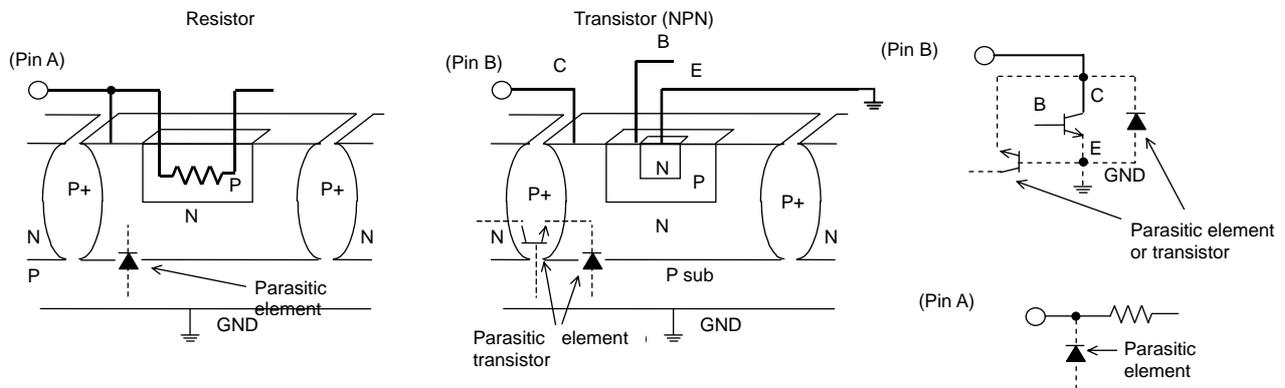


Figure 34. Example of IC structure

15. Application current and constants

The application circuit as shown in Figure 1. and the constants are examples to show the standard operation and application of this IC. In case of creating a design for mass production with different external components please contact ROHM for detailed information.

16. In some applications, the PVIN pin and SW pin potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, while the external capacitor is charged, the PVIN shorts to the GND. To prevent this we recommend reverse polarity diodes in series or placing a bypass diode between the SW pin and PVIN pin.

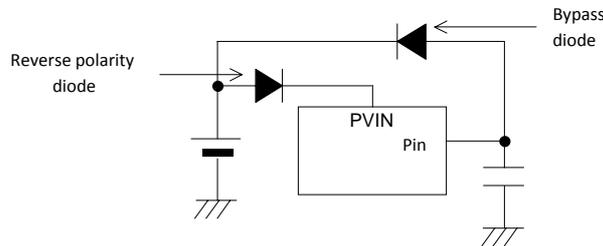


Figure 35. Measure for reverse

Note concerning this document

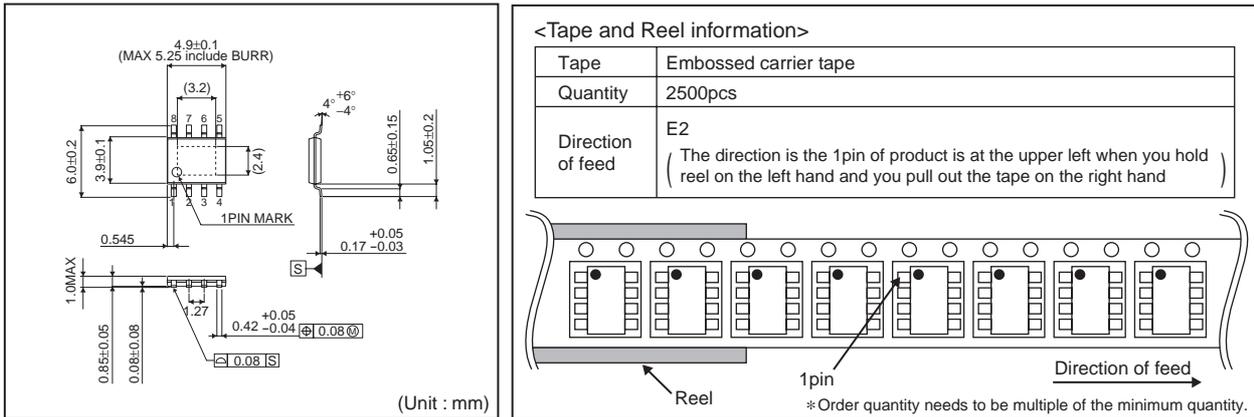
The Japanese version of this document is the official specification. This translation should be seen as a reference to aid reading the official specification. In case of any discrepancies between the two versions, the official version always takes precedence.

●Ordering Information

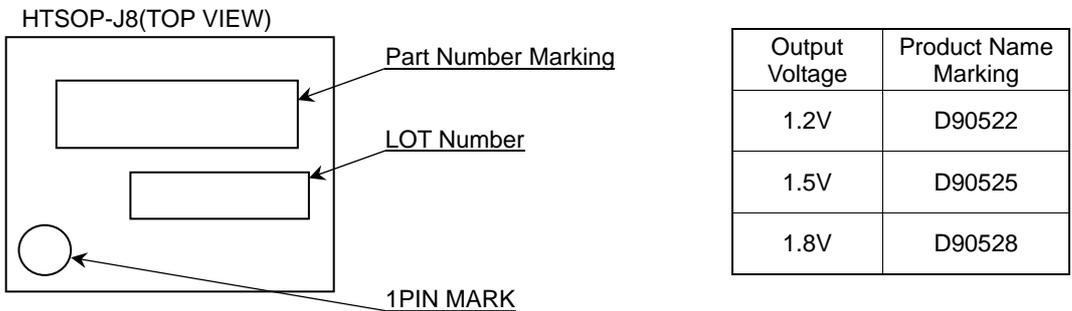


●Physical Dimension Tape and Reel Information

**HTSOP-J8**



●Marking Diagram



## ●Revision History

Rev.	Date	Notes
001	2012/12/17	New release

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