High-Frequency Converter for Telecom Applications

FEATURES

- On-board high-voltage, 1-Ω Switching FET
- Switching Frequencies of Up to 1 MHz
- Synchronization Capability
- Easily Compensated Current-Mode Operation
- Operates with Input Voltages Up to 200 V
- 1.8-MHz Error Amplifier
- Soft-Start
- Latched $\overline{\text{SHUTDOWN}}$

DESCRIPTION

The Si9117 high-efficiency converter for telecom systems running off 48 V is ideal for emerging applications such as interactive video (IV) set-top boxes and microcell base stations, such as those used for Personal Communications Systems (PCS). IV set-top boxes and microcell base stations typically require less than 15 W of power and have access to the analog telephone line power. Both IV set-top boxes and microcell base stations process extremely low-level, modulated analog signals (on the order of μVs), making the frequency and energy content of radiated and conducted noise a major issue. These application circuits are also constrained in terms of available board space and place a premium on minimal footprint.

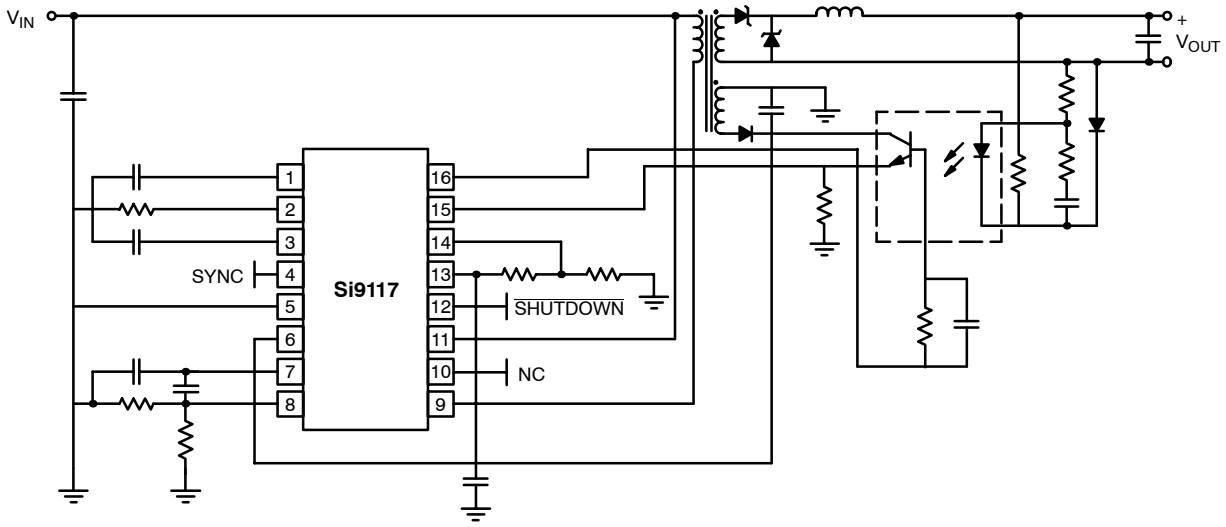
The combination of an on-board, high-voltage, 1-Ω switch and a PWM IC with operational input voltage of 200 V allows operation off of the analog telephone line, even with the worst case battery voltage and ringing voltage. Once the converter has started up, a simple bootstrap circuit can provide power to the IC by raising the source voltage of the n-channel, depletion mode, start-up FET above its gate voltage of 9.2 V. This technique lowers system costs, reduces the area required for circuit implementation, and minimizes circuit power consumption.

Processing high-frequency, modulated analog signals for video or RF requires receivers with sensitivities in the range of 0.5 to 25 μV. At these levels, noise generated by switchmode power conversion can impair the signal recovery process. Controlling radiated noise is a matter of proper layout and shielding. Controlling conducted noise is a matter of limiting its energy and isolating the conducted energy's fundamental and harmonic frequencies to bands which will not affect the frequencies of interest. The high-frequency, synchronized switching of the Si9117 enables this design requirement. First, for a given output current, high-frequency switching attenuates output ripple, minimizing conducted energy. Second, synchronizing the high switching frequency to an external frequency allows the fundamental and its harmonics to be moved out of range of the frequency bands of interest. An additional benefit of high-frequency switching is reduced size and cost of the inductor and the output filter capacitance.

In addition to these mandatory design considerations, the Si9117 is easy to design with and compensate, and takes a minimum of board area to implement: an important benefit in high-volume/small-package applications such as set-top boxes and microcell base stations.

The Si9117 is available in both standard and lead (Pb)-free packages.

APPLICATIONS CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to $-V_{IN}$
V_{CC} . . . . . 18 V
$+V_{IN}$ (Note: $V_{CC} < +V_{IN} + 0.3$ V) . . . . . 200 V
Logic Input ($\overline{SHUTDOWN}$, SYNC) . . . . . -0.3 V to $V_{CC} + 0.3$ V
Linear Inputs (FEEDBACK, SENSE, SOFT-START) . . . . . -0.3 V to $V_{CC} + 0.3$ V
HV Pre-Regulator Input Current (continuous) . . . . . 5 mA
Storage Temperature . . . . . -65 to 150°C
Operating Temperature . . . . . -40 to 85°C
Junction Temperature (T_J) . . . . . 150°C

Drain-Source Voltage (T_A = 25°) (V_{DS})[a] . . . . . 200 V
Continuous Drain Current (T_A = 25°) (I_D)[a] . . . . . 1.0 A
Power Dissipation (Package)[a]
16-Pin SOIC (Y Suffix)[b] . . . . . 900 mW
Thermal Impedance (Θ_{JA})
16-Pin SOIC . . . . . 140°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board, $t \leq 2$ sec.
b. Derate 7.2 mW/°C above 25°C.

RECOMMENDED OPERATING RANGE

Voltages Referenced to $-V_{IN}$
V_{CC} . . . . . 9.5 V to 16.5 V
$+V_{IN}$ . . . . . 15 V to 200 V
f_{OSC} . . . . . 20 kHz to 2 MHz

R_{OSC} . . . . . 56 kΩ to 1 MΩ
C_{OSC} . . . . . 47 pF to 200 pF
Linear Inputs . . . . . 0 to $V_{CC} - 4$ V
Digital Inputs . . . . . 0 to V_{CC}

SPECIFICATIONS

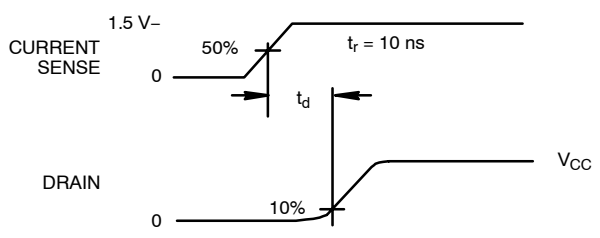
Parameter	Symbol	Test Conditions Unless Specified Oscillator Disabled $-V_{IN}$ = 0 V, V_{CC} = 10 V	Limits Min[a]	Limits Typ[b]	Limits Max[a]	Unit
Reference						
Output Voltage	V_R	OSC Disabled, T_A = 25°C	3.94	4.0	4.06	V
		OSC Disabled Over Voltage and Temperature Ranges[c]	3.88	4.0	4.12	
Short Circuit Current	I_{SREF}	$V_{REF} = -V_{IN}$		–30	–5	mA
Load Regulation	$\Delta V_R/\Delta I_R$	I_{REF} = 0 to –1 mA		10	40	mV
Oscillator						
Initial Accuracy	f_{OSC}[d]	R_{OSC} = 374 kΩ, C_{OSC} = 200 pF	90	100	110	kHz
		R_{OSC} = 70 kΩ, C_{OSC} = 200 pF	450	500	550	
Voltage Stability[c]	Δf/f	R_{OSC} = 70 kΩ, C_{OSC} = 200 pF Δf/f = [f(16.5 V) – f(9.5 V)] / f(9.5 V)		1	2	%
Temperature Coefficient[c]	OSC TC	$-40 \leq T_A \leq 85$°C, f_{OSC} = 100 kHz		200	500	ppm/°C
Sync Output Current (Master Mode)	$I_{SYNC(M)}$	$V_{ROSC} \leq 5$ V	±1.0	±3.0		mA
Sync Output Current (Slave Mode)	$I_{SYNC(S)}$	$V_{ROSC} = V_{CC}$		±1	±500	nA
Error Amplifier (C_{OSC} = $-V_{IN}$ OSC Disabled)						
Input BIAS Current	I_{FB}	V_{FB} = 5 V, NI = V_{REF}		<1.0	±200	nA
Input OFFSET Voltage	V_{OS2}			±5	±25	mV
Open Loop Voltage Gain[c]	A_{VOL}		65	80		dB
Unity Gain Bandwidth[c]	BW		1.8	2.7		MHz
Output Current	I_{OUT}	Source (V_{FB} = 3.5 V, NI = V_{REF})		–2.7	–1.0	mA
		Sink (V_{FB} = 4.5 V, NI = V_{REF})	1.0	2.4		
Power Supply Rejection	PSRR	9.5 V $\leq V_{CC} \leq$ 16.5 V	50	80		dB

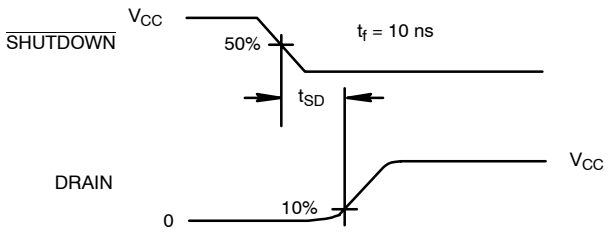
SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified Oscillator Disabled $-V_{IN}$ = 0 V, V_{CC} = 10 V		Limits Min[a]	Typ[b]	Max[a]	Unit
Pre-Regulator/Start-Up							
Input Leakage Current	$+I_{IN}$	$+V_{IN}$ = 200 V, $V_{CC} \geq$ 10 V			<1	10	μA
Pre-Regulator Start-Up Current	I_{START}	$+V_{IN}$ = 48 V, $t_{PW} \leq$ 300 μs, $V_{CC} = V_{UVLO}$		8	20		mA
V_{CC} Pre-Regulator Voltage	V_{PR}	$+V_{IN}$ = 48 V		8.8	9.1	9.4	V
$V_{PR} - V_{UVLO}$ (Turn-On)	V_{DELTA}			0.1	0.25	0.7	
Undervoltage Lockout Hysteresis	V_{HYST}			0.18	0.28	0.4	
Supply							
Supply Current	I_{CC}	$C_{LOAD} \leq$ 50 pF	f_{OSC} = 100 kHz		1.8	2.5	mA
			f_{OSC} = 500 kHz		3.7	4.5	
Protection							
Current Limit Threshold Voltage	V_{SENSE}	V_{FB} = 0 V, NI = V_{REF}		1.035	1.16	1.30	V
Current Limit Delay to Output[c]	t_d	V_{SENSE} = 1.5 V, See Figure 1			105	130	ns
$\overline{\text{SHUTDOWN}}$ Logic Threshold	V_{SD}				2.8	0.5	V
$\overline{\text{SHUTDOWN}}$ Delay to Latched Output[c]	t_{SD}	See Figure 2			0.21	1.0	μs
$\overline{\text{SHUTDOWN}}$ Pull-Up Current	I_{SD}	V_{SD} = 0 V		12	22	30	μA
Soft-Start Current	I_{SS}			12	22	30	
Output Inhibit Voltage	$V_{SS(off)}$	Soft-Start Voltage to Disable Driver Output			1.6	0.5	V
Switch							
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V, T_A = 25°C			0.7	5	μA
Drain-Source On-State Resistance[e]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 1.0 A, T_A = 25°C			0.8	1	Ω

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Guaranteed by design, not subject to production test.
d. $C_{STRAY} \leq$ 5 pF on C_{OSC}.
e. Pulse Test; Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2%.

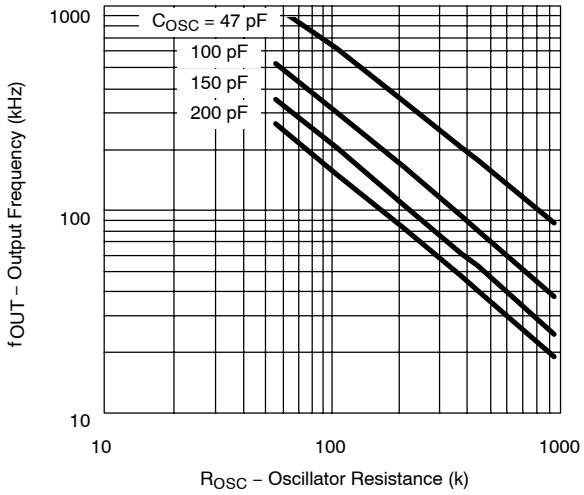
TIMING WAVEFORMS



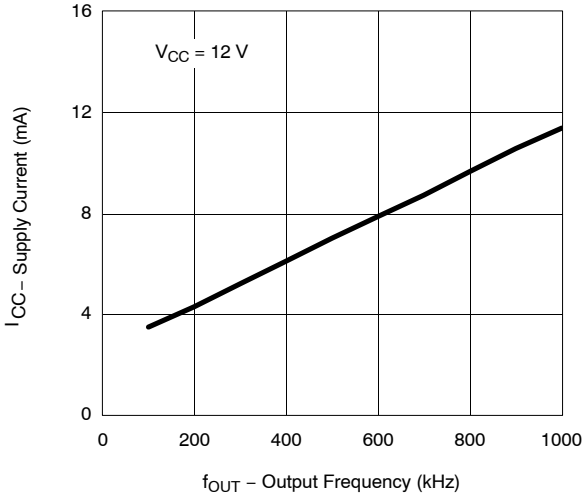


TYPICAL CHARACTERISTICS

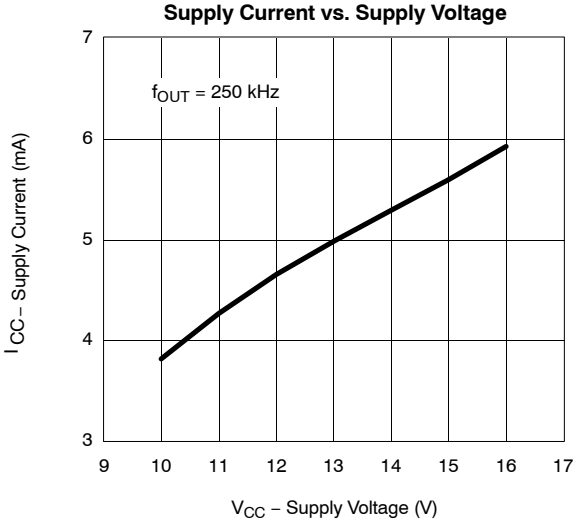
Output Frequency



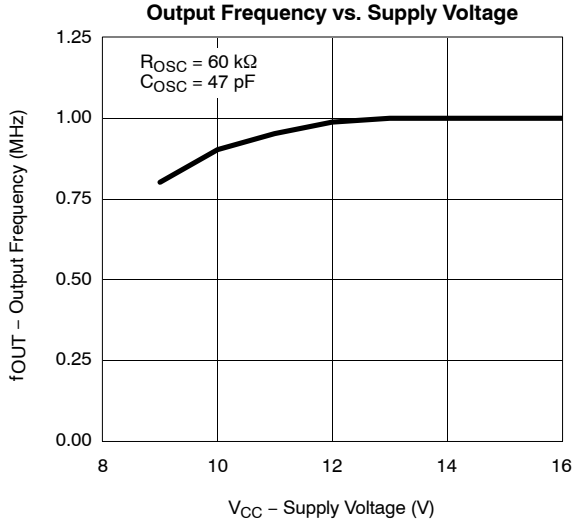
Supply Current vs. Output Frequency



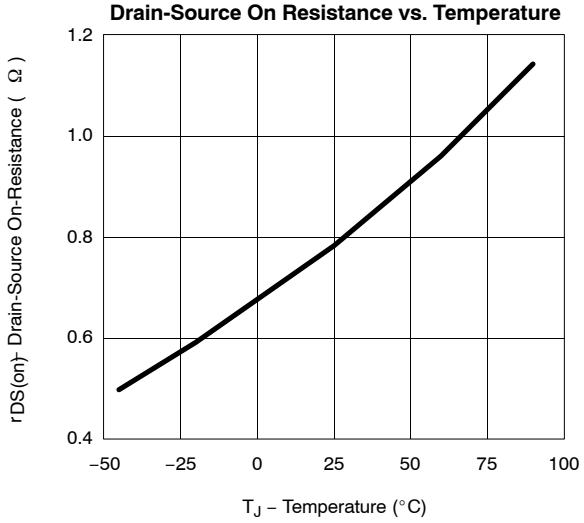
Supply Current vs. Supply Voltage



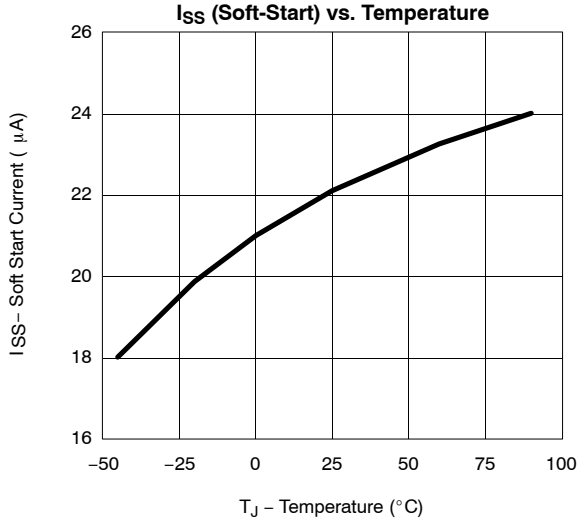
Output Frequency vs. Supply Voltage



Drain-Source On Resistance vs. Temperature



I_{SS} (Soft-Start) vs. Temperature



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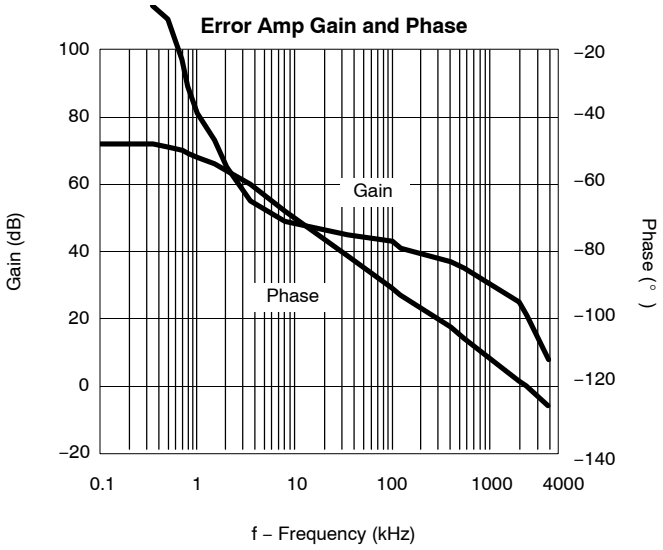
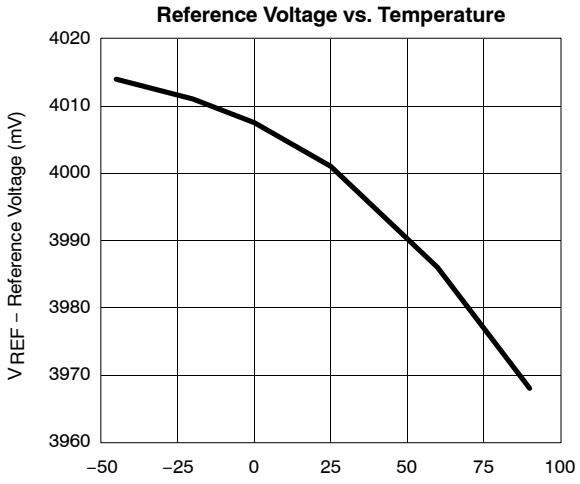
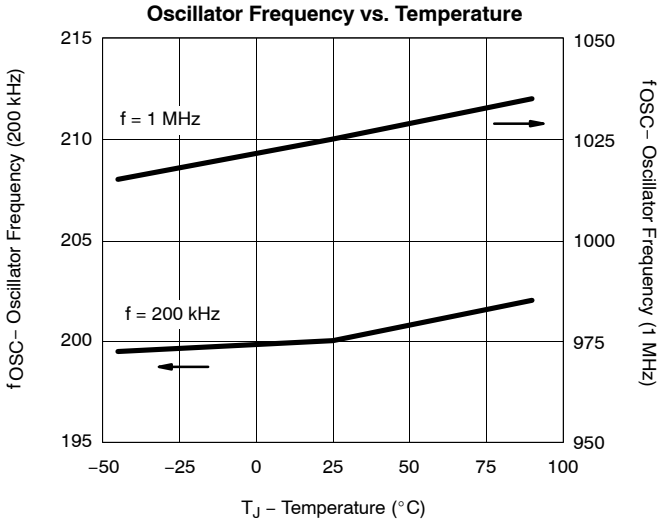
TYPICAL CHARACTERISTICS

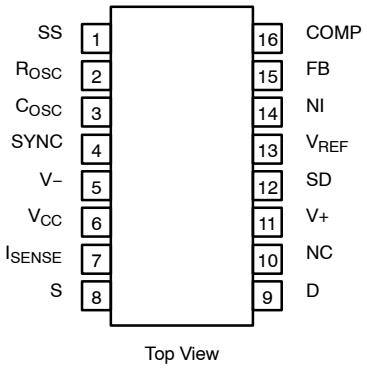






PIN CONFIGURATION AND ORDERING INFORMATION

16-Pin SOIC



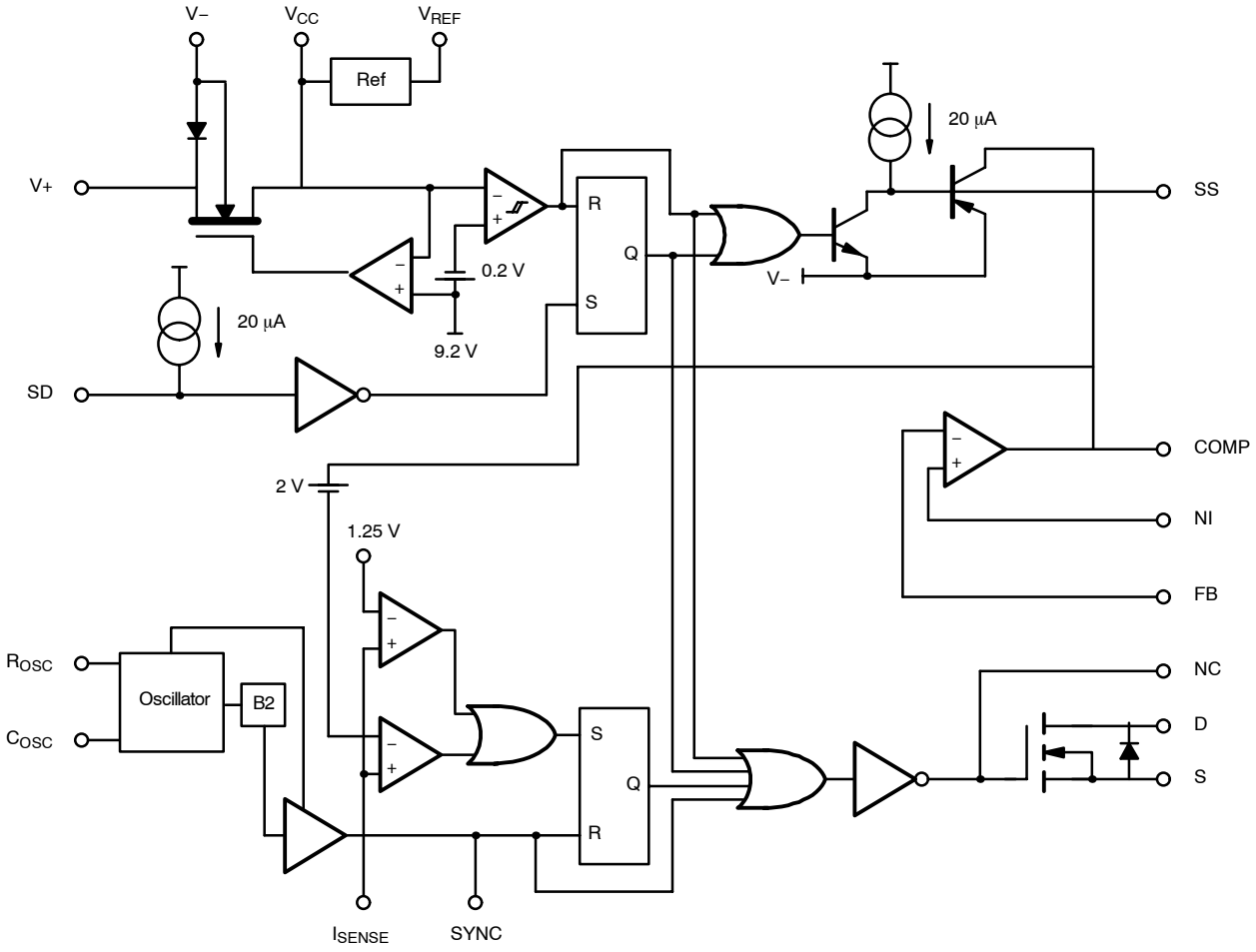
Top View

ORDERING INFORMATION		
Part Number	**Temperature Range**	**Package**
Si9117DY	–40 to 85°C	SOIC-16
Si9117DY-T1		
Si9117DY-T1—E3		

PIN DESCRIPTION

Pin Number	Symbol	Description
1	SS	Generates a 20-μA current source. IC turns or when capacitor is charged to 4.6 V.
2	R_{OSC}	Sets the oscillator charging current. Use the "oscillator frequency vs. R_{OSC}" curve in The Typical Characteristics section.
3	C_{OSC}	Sets oscillator frequency. Use the "Oscillator frequency vs. R_{OSC}" curve in the Typical Characteristics section along with equations 1 and 2 in the Oscillator section of the Description of Operations.
4	SYNC	Synchronization input overrides the oscillator. Slave mode operations is possible, as is operation of the converter at duty cycles >50%. See Oscillator section of the Description of Operations.
5	V–	Ground or negative mode of input power supply.
6	Vcc	Bootstrap power supply pin
7	I_{SENSE}	Current-mode sense input
8	S	Switch FET source.
9	D	Switch FET drain.
10	NC	No connect: for test purposes only. (Normally left open)
11	V+	High voltage (up to 200 V) power supply input.
12	SD	$\overline{\text{Shutdown}}$. Logic low shuts down the controller.
13	V_{REF}	Output of the 4-V reference sources 5 mA.
14	NI	Non-inverting input of the error amplifier. A resistor divider from the reference can be used to set this voltage.
15	FB	Inverting input to the error amplifier; used to maintain output regulation.
16	Comp	Output of the error amplifier. Used to provide compensation for the converter's feedback control loop.

BLOCK DIAGRAM



APPLICATIONS

Description of Operation

The Si9117 is a current mode PWM IC combined with an integrated 1-Ω 200-V MOSFET. Current mode operation offers the following advantages:

- Cycle-by-cycle current limit protection
- Simple loop compensation, eliminating the effect of output inductor
- Excellent fast transient response due to inner control loop
- Automatic input voltage feed-forward compensation

In addition, the Si9117 is duty-cycle limited to avoid core saturation.

High Voltage Pre-Regulator

All switchmode power supplies face a start-up problem caused by the large difference between dc bus voltage and the V_{CC} power rail for supplying the control circuit. The traditional technique has been to keep the control circuit in “sleep mode,” while a small amount of energy is used to “top up” a large enough electrolytic capacitor to get the circuit started. When the circuit starts operating, a winding on the transformer is then used to power the control circuit. Disadvantages with this type of circuit include delayed start-up and large required capacitances for guaranteed operation over the full voltage range. The Si9117 overcomes these problems by using low power consumption, BiC/DMOS circuitry, and a unique high-voltage depletion mode MOSFET (see Figure 1).

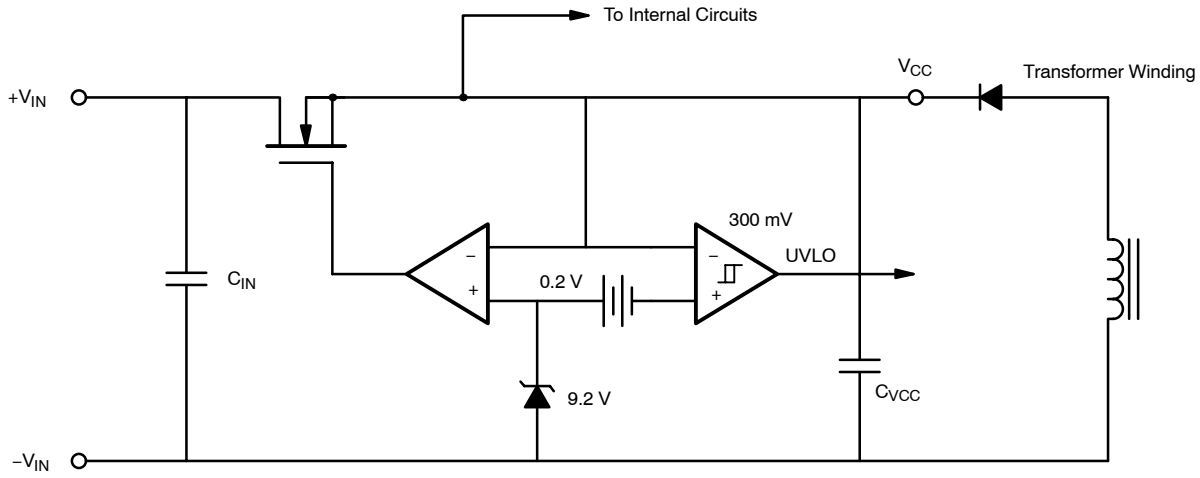


FIGURE 1. Start Circuit

When power is first applied, the depletion transistor is on, and current flows from the input capacitor C_{IN} into the V_{CC} capacitor C_{VCC} until V_{CC} reaches 9.2 V. The converter transformer will then supply the V_{CC} through a bias winding, which will raise V_{CC} to a level higher than 9.2 V. Ideally this will be between 11 and 13 V, thus turning off the high-voltage depletion mode MOSFET. The 9.2-V threshold has a hysteresis of 300 mV to prevent oscillations when the transition voltage is not clearly defined or when high-line supply impedance is encountered.

For applications where the input dc voltage is not high, and the chip power consumption is not excessive, the feedback winding can be eliminated. In such cases, the pre-regulator circuit will behave just like a linear regulator with 9.2-V output and 10-kΩ series resistance. In this case, the parameters to be considered are the dropout voltage at lowest line condition and the power dissipation at highest voltage. The high-voltage depletion mode MOSFET contains an internal body diode, and in situations where the V_{CC} is being powered from a laboratory supply, care must be taken to avoid loading the $+V_{IN}$ rail beyond the current rating of this device. Typically, the reverse characteristics of the device will generate a voltage of 3.4 V on Pin 11 with 10-kΩ load when powering V_{CC} from a lab supply.

In some applications it is necessary to inhibit the start of a converter until a high enough voltage is present on the supply bus. This is the case for the following reasons:

- Circuitry fed from a high line impedance such as a telephone line will have difficulty starting, since the converter will behave like a negative impedance. As the dc voltage decreases, the input current increases because constant power is drawn. This causes severe oscillations, and can in some instances have a destructive effect on the converter.
- During start-up, the Si9117 will begin operation as soon as the UVLO threshold is reached. Since the converter is designed to operate over a much higher range—for example, from 36 to 72 V—then between 10 and 36 V input the output voltage will be out of regulation and undefined. In some cases, digital circuitry will not accept this mode of operation, and system faults will be encountered without a RESET watchdog circuit.

To overcome these problems, a Zener diode of suitable value V_Z can be placed in series with the +Vin pin, preventing start-up until V_Z + 9.2 V is reached.

Shutdown

The shutdown pin is configured to allow fast latched termination of the output pulse. The delay from shutdown to output is typically 300 ns. This delay is short enough to allow this pin to be used for over-voltage applications where fast orderly shutdown is desirable: for example, when control of the feedback loop is lost.

Using an opto-coupler and a TL431, interface is easy (see Figure 2). Once latched, the shutdown can only be reset from the UVLO circuit by re-cycling the power. In the event of an over-voltage, the latch can be reset by momentarily pulling the V_{CC} to a value lower than the UVLO threshold. This approach will generally be acceptable, since the feedback winding will not be supplying power, and the only power maintaining the latch will be supplied by the depletion start transistor. Note, however, that this action will still be subject to the power dissipation limits of the Si9117 package and should ideally be applied as a short fast pulse.

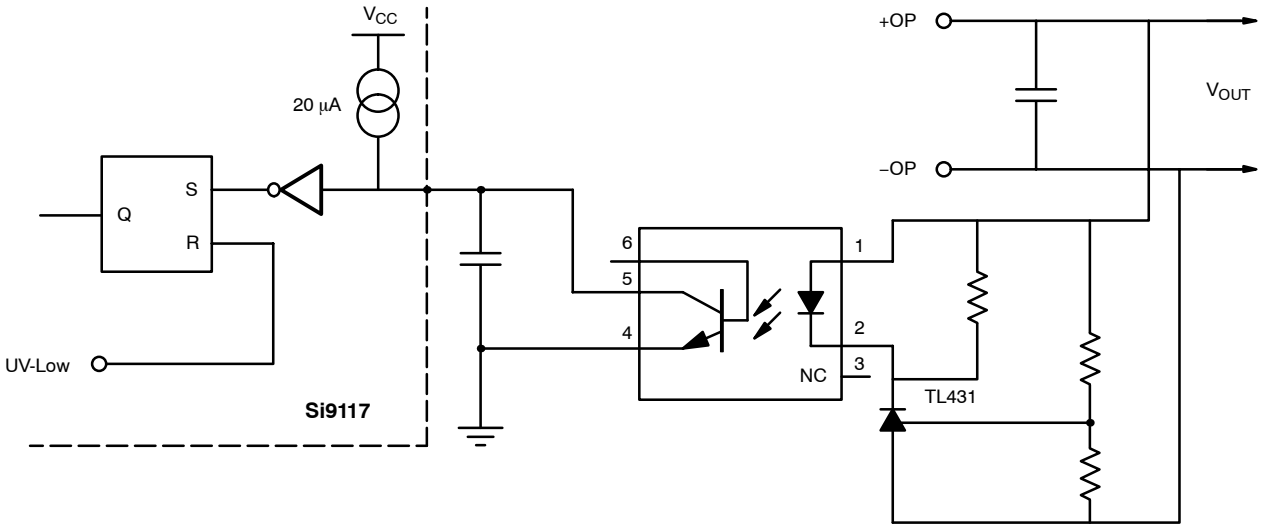


FIGURE 2. Shutdown

Reference

The reference voltage is a fully buffered band gap type which can source 5 mA over the specified voltage tolerance range. The reference should be well de-coupled to prevent instability and jitter. A ceramic 100-nF or small tantalum is recommended, depending on the de-coupling present on the supply pins.

Error Amplifier

The error amplifier consists of a PMOS input folded cascade gain stage followed by a class AB unity gain amplifier. Typical open loop voltage gain is 77 dB, and unity gain bandwidth is typically 2.7 MHz. The soft-start circuit (see Pin 1 description) forces the output to within 0.7 V above ground, and additional clamp diodes limit the positive output excursion to within $2xV_{BE}$ above V_{REF} . Operation at high frequency allows high closed loop bandwidths and permits excellent transient response to both input and output changes. Under normal operation, a small 100-pF bypass capacitor is recommended from N_{INV} to Comp to increase high-frequency noise rejection. This should be calculated, however, in conjunction with the loop dynamics.

Soft-Start

The soft-start circuit is designed to help dc-to-dc converters start in an orderly manner and reduce component stress. The output of the error amplifier is clamped by a PNP transistor.

The external capacitor C_{SS} is supplied by a 20-µA current source and will charge linearly to 4.6 V. In the event of an under-voltage lockout (or during start-up), this capacitor is held low. Soft-start is a very important feature and has many beneficial effects, especially in applications connecting to telecom lines where source impedances are high. In such cases, there is an initial start-up current caused by the input capacitor, followed by a secondary peak caused by the converter running at maximum duty cycle while trying to reach regulation. Where large output capacitances and peak loads are encountered, oscillations may occur. These can be prevented with the use of long soft-start times. The soft-start pin can also be used as a non-latching shutdown pin by connecting it to $-V_{IN}$. This approach allows a shutdown with soft re-start.

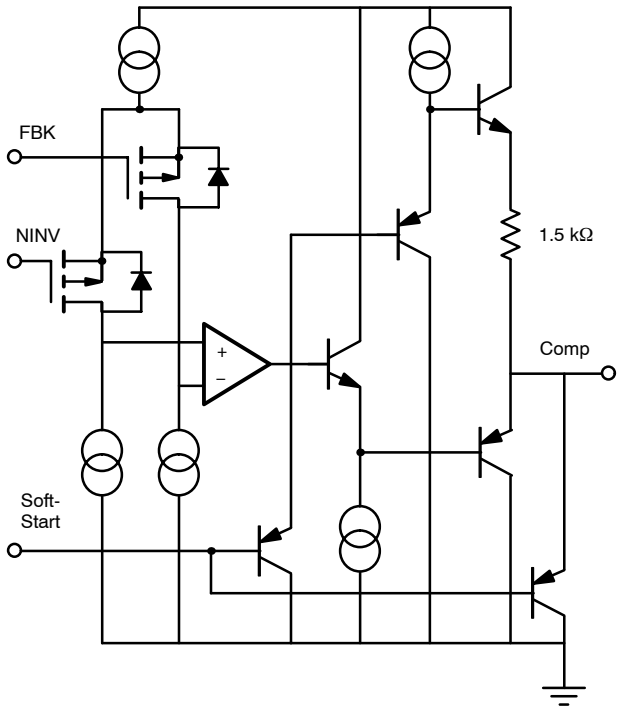


FIGURE 3. Operational Amplifier

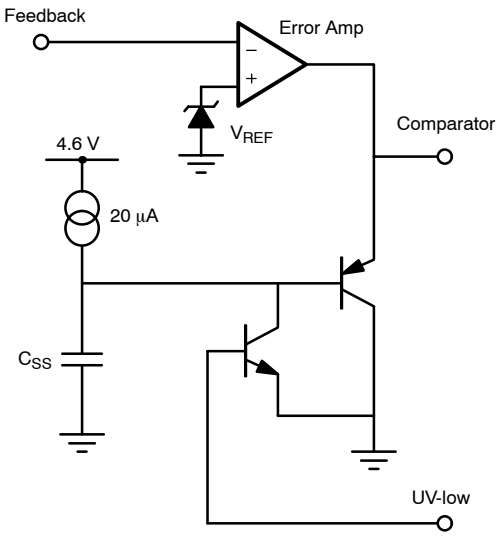


FIGURE 4. Soft-Start

Oscillator

The oscillator circuit uses external timing components R_T and C_T. An internal divide-by-two prevents pulses with greater than 50% duty cycle, so that core saturation can be avoided. When the R_T terminal is connected to V_{CC}, comparator C_2 disconnects the oscillator output from the SYNC terminal using SW_1, and allows an external oscillator circuit to take control of the current mode comparator circuit.

The current programmed by R_T defines the charging current of C_T and the on and off times with the following design equations:

$$T_{ON} = \frac{1.025 \times R_T \times C_T}{8} \quad (1)$$

$$T_{OFF} = 5 \times R_{ql} \times C_T \qquad \text{where } R_{ql} = 25\ \Omega \quad (2)$$

$$F_{OSC} = \frac{1}{2} \times \frac{1}{(T_{ON} + T_{OFF})} \quad (3)$$

Actual values taken from a prototype board have been plotted (Figure 6), and are a close match (except for 47 pF, where stray parasitics have a more significant effect).

In certain circumstances, such as current limiting, it may be desirable to change the frequency of the converter for a period of time to overcome current tails (see Figure 14 for further explanation). With the Si9117, this is easily done by adding or subtracting some current into the R_T terminal:

- The charging current in C_T is set by $8 \times R_T$.
- The voltage at the R_T terminal is 4 V, as supplied by an internal emitter follower from the reference.

The frequency can be changed easily by supplying some of the current into R_T from the V_{CC} rail, thus “starving” the internal current source, and slowing the frequency down. (See Figure 7.)

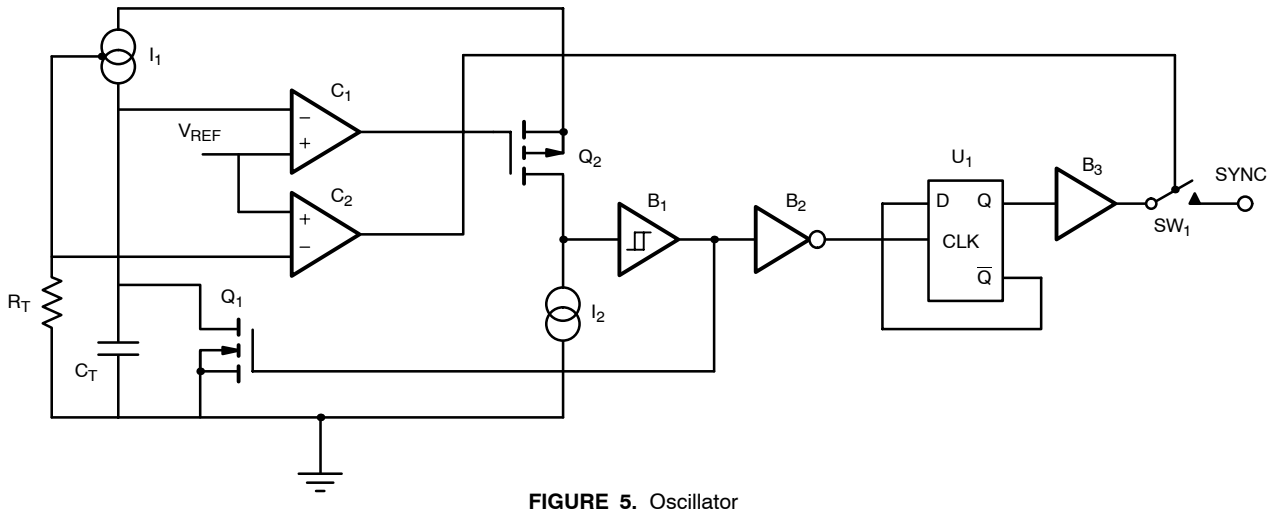


FIGURE 5. Oscillator

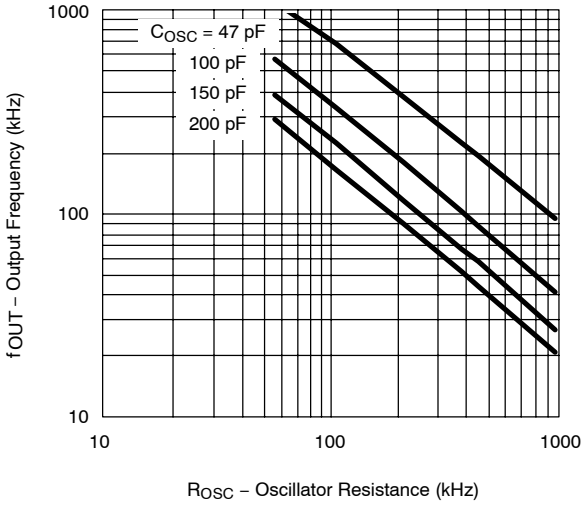


FIGURE 6. Oscillator Frequency Selection

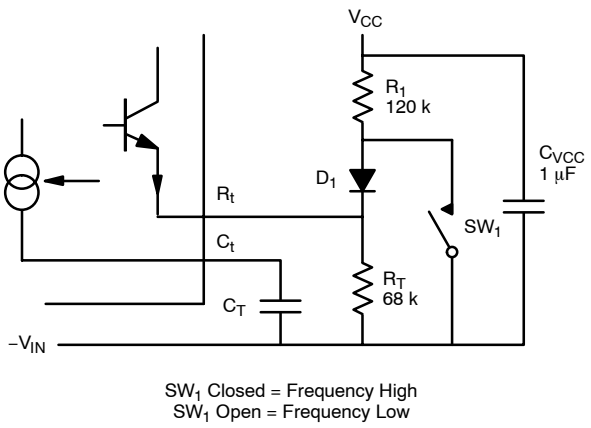


FIGURE 7. Frequency Shifting Using R_t Current Change

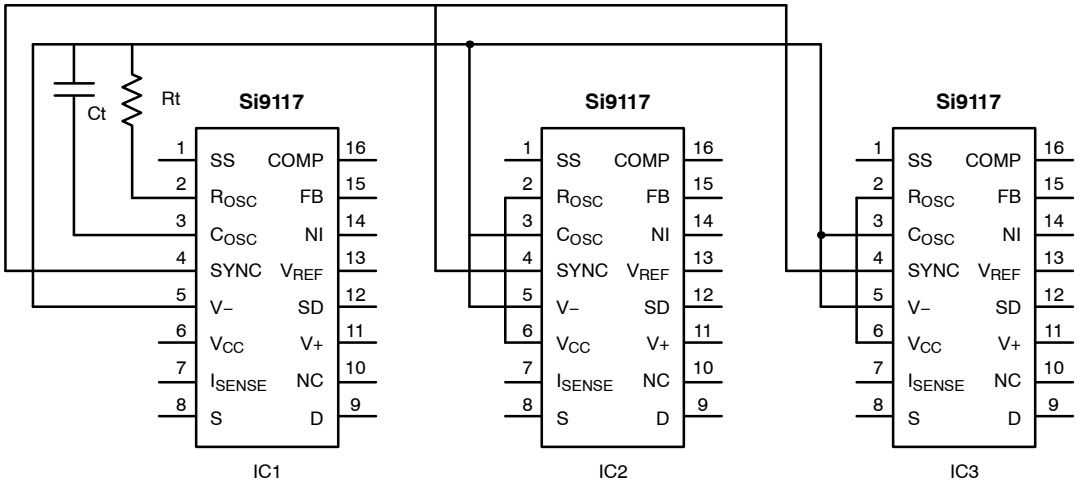


FIGURE 8. Oscillator Synchronization

The current in R_T is set by V = IR where V = 4 V and R = R_T. Using a diode, and some type of switch, the frequency can be easily changed: when SW_1 is closed, D_1 is reverse biased, and has no effect on R_T. When SW_1 is open, current flows through R_1 and D_1 into R_T and removes some of the current supplied by the internal emitter follower.

Synchronization

The *SYNC* input allows operation from a master clock as the connection is made after the divide-by-two. As a result, synchronization in both frequency and phase is possible. This unique feature is important to systems designers who use multiple converters, where noise caused by an unsynchronized “beating” effect is present and causes difficult EMI/EMC problems. If an external clock is used, duty cycles of > 50% are possible due to the position of the *SYNC* pin , after the divide-by-two. Where > 50% conduction is used, core reset must be allowed, in order to prevent core saturation. Synchronization is in master/slave mode, with one device (the “master”) setting the switching frequency and others (the “slaves”) with disabled oscillators locked to it. Alternatively, all devices can be clocked using a master oscillator. (See Figure 8.)

During slave mode, the unused C_T pin should be connected to ground, and the R_T to V_{CC}.

V_{IN} and V_{DD}

These pins are used for powering the Si9117 and should consequently be well de-coupled. In selecting the right de-coupling, the MOSFET gate drive requirements should be considered, as the de-coupling capacitor will also have to supply the required peak current. Generally speaking, the best combination would be a 1- to 10-µF electrolytic for bulk energy and a 100-nF ceramic for high-frequency bypass. The V_{CC} rail should be carefully observed at the switch on and off occurrences using ac de-coupling, and the peak voltage spikes should be measured. These should be less than 200 mV. Excessive noise on the V_{CC} will appear on other pins and may cause instability or jitter on the control waveforms.

Switch

The switch FET is designed specifically for converters in the 5- to 10-W power range. It has a 200-V V_{DS} rating with 1-Ω $r_{DS(on)}$. Using the Gate charge curve, for a gate drive of 12 V from the Si9117, the total gate charge for 100-V V_{DS} will be 10 nC. From Q = i x t, it is easy to deduce that with a 400 mA internal gate drive, a time of 50 ns will be obtained (see Figure 9).

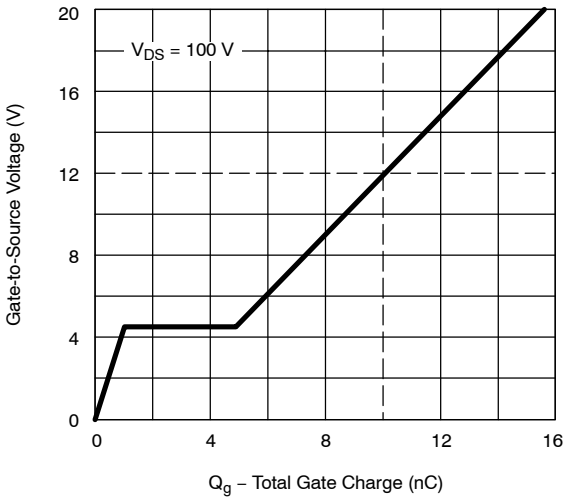


FIGURE 9. Si9117 Internal MOSFET Gate Charge

Current Sense

The current sense comparator performs the current mode control function by comparing the output of the error amplifier (V_C) with the current in the output inductor. It is impractical to measure the output inductor current, but the rising slope of the current can supply all the necessary information if sampled in the MOSFET as a scaled equivalent. Certain precautions are necessary, however, due to data distortion, noise, and the rarity of ideal operating conditions.

Sensed current waveforms often have leading-edge spikes or noise caused by reverse recovery of rectifiers, equivalent capacitive loading on the secondary, and inductive circuit effects. Inductive sense resistors must not be used, as they cause large damaging spikes and distort the sensed waveforms. These spikes can confuse the PWM comparator into believing that an overload condition is present. In addition, the Si9117 uses a single pin (–Vin) for all the return current requirements, including the output driver. As a result, the current pulse from the gate charge transfer into the MOSFET will appear on the sense pin and be filtered out.

Waveform A (Figure 11) has an ideal textbook appearance, but is in fact rarely encountered. Waveforms B and C are typical yet close to the threshold limit, and thus could lead to instability. The addition of a simple RC network on the sensed waveform suppresses this leading-edge spike. The low pass filter should be selected so that only the leading-edge spike is suppressed and the overall waveform is not distorted. The waveform must contain a clean rising slope for the error amplifier to intersect. If the RC time constant is too long, then the waveform will be distorted and lead to falling-edge jitter on the turn-off edge.

Slope compensation can also be used to eliminate noise or jitter. A sample of the oscillator voltage is superimposed on the error amplifier to produce a clean crossing of the thresholds and to avoid any hunting.

The Si9117 has built-in leading-edge blanking/ suppression to eliminate some of the effects of these spikes.

The two comparators used to operate the circuit have different delay times as follows:

- The current mode comparator needs more noise immunity, and therefore has a deliberately slower delay time to block out noise and spikes which are present on the leading edge. Typical delay times should be around 100 ns.
- The peak current limiting comparator has the fastest response time, since it is used only to protect the circuit in the event of an overload. The delay times for this comparator should be around 70 ns.

High-Frequency Design Requirements

When designing converters for high switching frequency, a certain discipline is required to determine the right choice of components. This process should be an iterative choice and the board layout should be properly planned before CAD layout is undertaken.

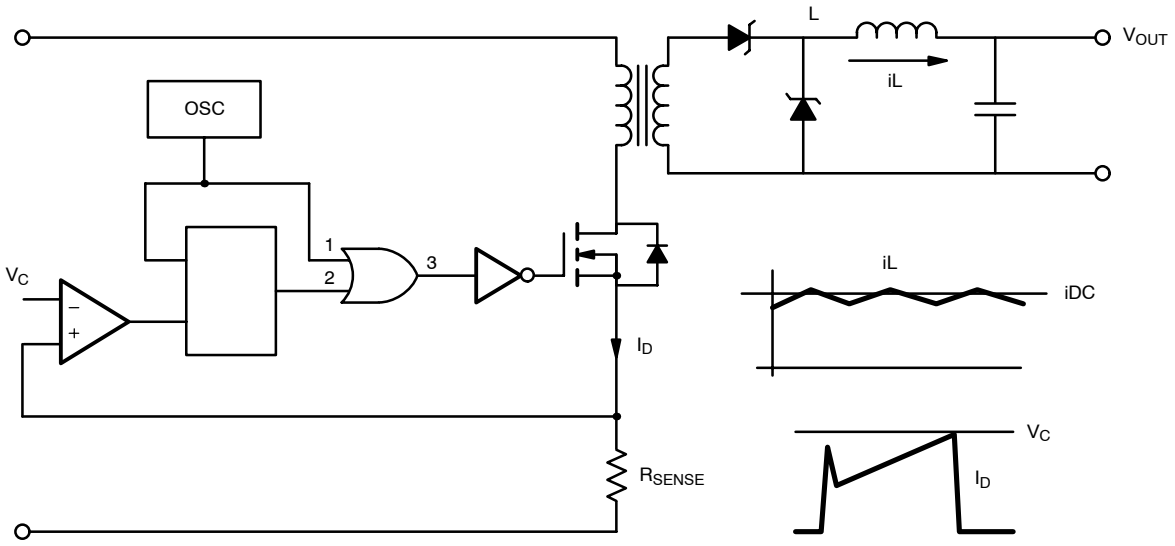


FIGURE 10. Constant Frequency Current Mode Control

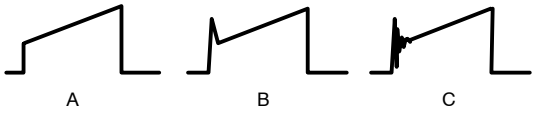


FIGURE 11. Current Waveforms

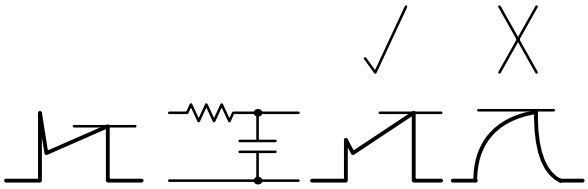


FIGURE 12. Current Sense Filtering Network

Layout Considerations

The main current loop flows from the input capacitor—through the transformer, MOSFET, and sense resistor—and returns to the capacitor. This current will have high rates of change and associated fast voltage and current edges. It is essential to avoid the injection of noise into the other circuitry.

To prevent this result, a “fishbone” type arrangement is recommended (Figure 13). Designers are encouraged to separate different grounds with “imaginary” dummy resistors. These can be removed at a later stage. Main current loops must be designed to be as short as possible: from C_{IN} to the transformer, through the MOSFET and Sense resistor, and back into C_{IN}. It is obvious that signals switching 50 V or 1 A in 25 ns should not be mixed with signals that are controlling a closed-loop, high-gain feedback system which is capable of regulating the output voltage to less than 1 mV.

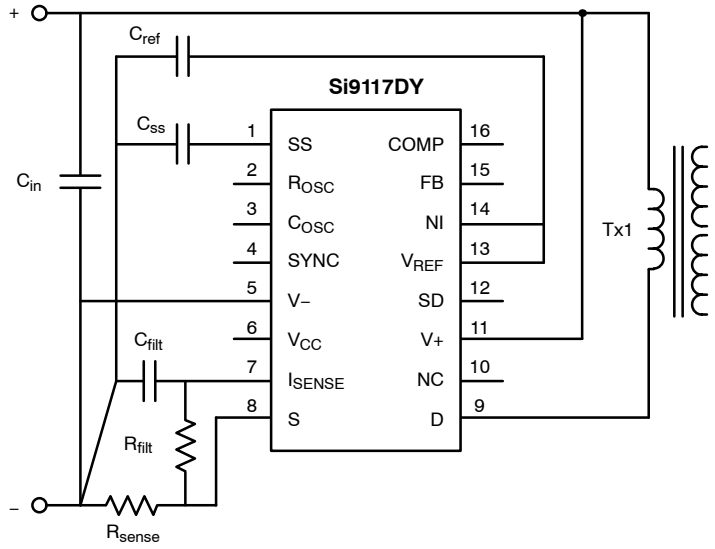


FIGURE 13.

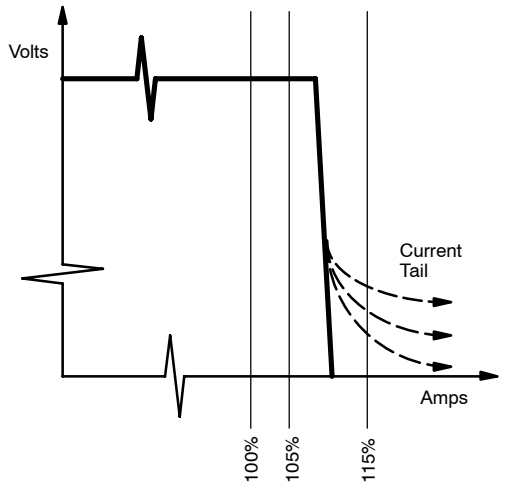


FIGURE 14.

Choosing the Switching Frequency

When selecting the switching frequency, it is usually best to choose the lowest possible frequency that the design solution will accept. In PWM control topologies, the maximum switching frequency will be strongly governed by short circuit behavior. When a short circuit is applied to the output, the control circuit is required to reduce the duty cycle to the smallest possible value to maintain constant current operation (Figure 14).

Ideally, the converter should deliver 105% of the output current within regulation and no more than 115% under short circuit. At 500 kHz, the period of conversion is 2 μs and the maximum on time is 1 μs. High minimum duty ratios will result in current tails and require rectifier oversizing to avoid destructive currents under overload conditions.

The Si9117 has a sync-to-output delay of less than 70 ns, so the minimum duty cycle for operation at 500 kHz would be 70 ns/1 μs = 7%. This minimum should be considered when the short circuit current is determined. Designers should note that a shunt placed across the output of the converter is probably not a realistic load in the event of a failure, and the real circuit impedance will probably be substantially lower. In such circumstances, it may be necessary to shift the frequency of the converter to a lower value during overload. Frequency shifting can be accomplished by altering the steady state values of the oscillator programming components (see oscillator section, Figure 7).

Short Circuit Behavior

Short circuit behavior is different for both common topologies, and must be paid special attention.

- In flyback converters, all windings appear in “parallel” with each other. When one winding is shorted, all other flyback windings are also shorted through it. In multiple output converters, therefore, any single winding without a separate secondary current-limiting protection will “drag down” all the other windings. As a result, if a bias winding is used to power the control circuit, it will stop delivering power. When this occurs, the Si9117 depletion device will turn on and regulate the supply rail to 9.2 V, as in its normal starting mode. In this event, designers should calculate the worst-case power dissipation caused by the voltage drop across the depletion transistor at the highest applied voltage across it and with the current flowing through it.

- In forward converters, traditionally the bias winding is also taken in forward conduction mode, but without any series inductance. In the event of a short circuit, the pulse width is reduced to minimum, but it is sufficient to supply enough power to the control circuit. This is an advantage, and avoids the problems encountered with flyback converters. Power may also be taken in flyback mode, however, when the duty cycle is low. There will be very little flyback voltage present, since the applied volt/microseconds is low and the core need not, therefore, fly back very far to reset.

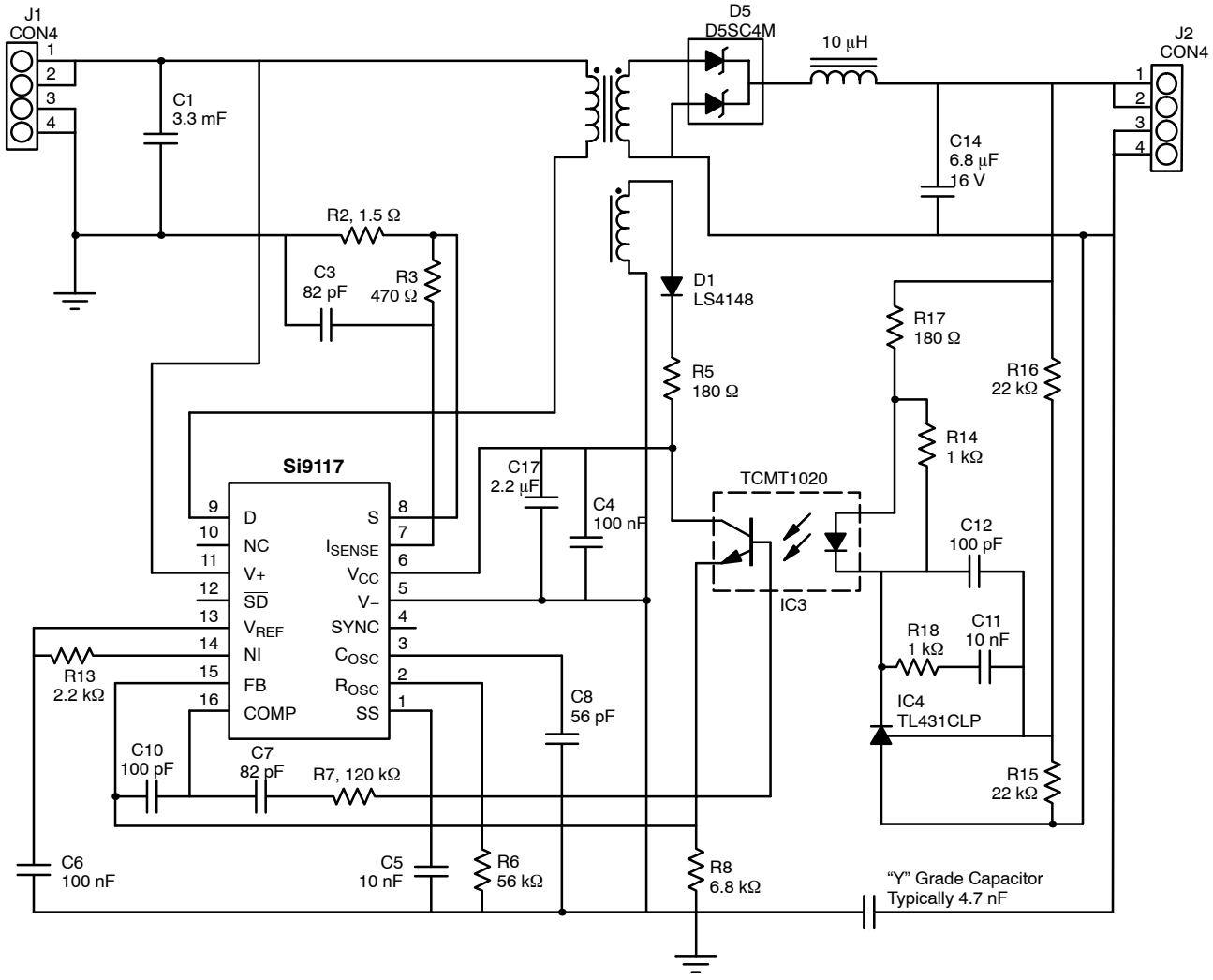


FIGURE 15. Complete Schematic Diagram

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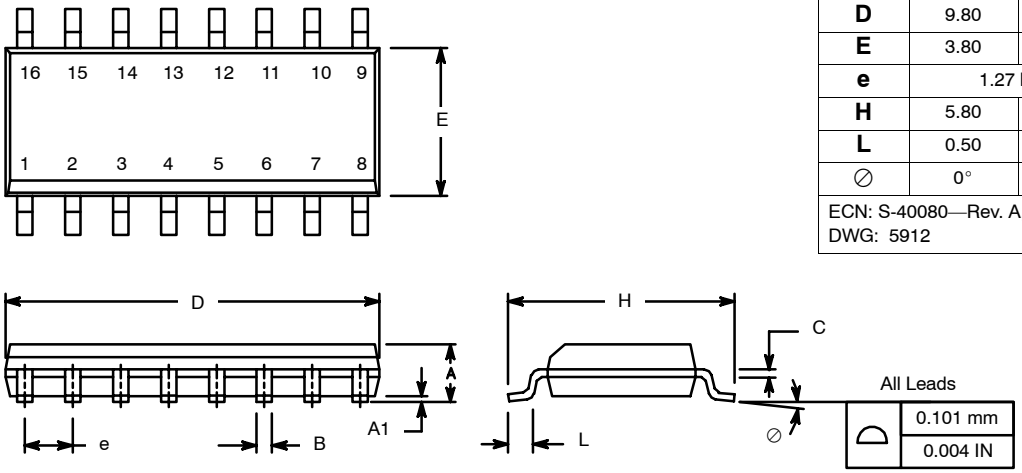

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

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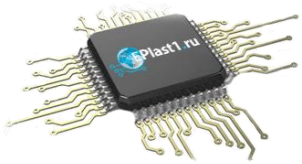

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