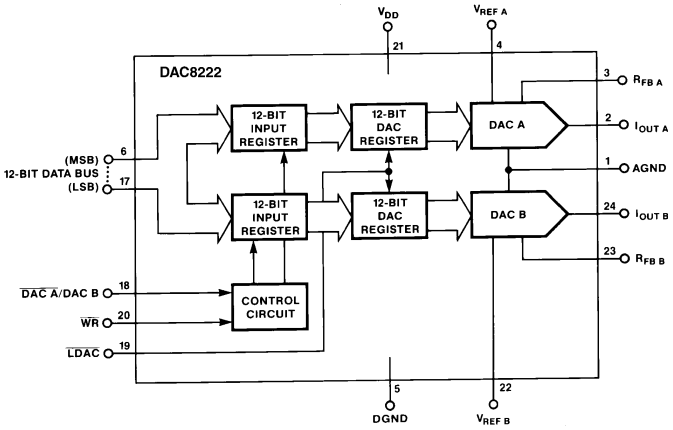
Dual 12-Bit Double-Buffered Multiplying CMOS D/A Converter

DAC8222

FEATURES
- Two Matched 12-Bit DACs on One Chip
- Direct Parallel Load of All 12 Bits for High Data Throughput
- Double-Buffered Digital Inputs
- 12-Bit Endpoint Linearity (±1/2 LSB) Over Temperature
- +5 V to +15 V Single Supply Operation
- DACs Matched to 1% Max
- Four-Quadrant Multiplication
- Improved ESD Resistance
- Packaged in a Narrow 0.3" 24-Lead DIP and 0.3" 24- Lead SOL Package
- Available in Die Form

APPLICATIONS
- Automatic Test Equipment
- Robotics/Process Control/Automation
- Digital Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

FUNCTIONAL DIAGRAM



GENERAL DESCRIPTION

The DAC8222 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has a 12-bit wide data port that allows a 12-bit word to be loaded directly. This achieves faster throughput time in stand-alone systems or when interfacing to a 16-bit processor. A common 12-bit input TTL/CMOS compatible data port is used to load the 12-bit word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit and 16-bit bus systems. (See DAC8248 for a complete 8-bit data bus interface product.) A common bus allows the DAC8222 to be packaged in a narrow 24-lead 0.3" DIP and save PCB space.

The DAC is controlled with two signals, $\overline{WR}$ and $\overline{LDAC}$. With logic low at these inputs, the DAC registers become transparent. This allows direct unbuffered data to flow directly to either DAC output selected by $\overline{DAC\ A}$/DAC B. Also, the DAC's double-buffered digital inputs will allow both DACs to be simultaneously updated.

DAC8222's monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The chip consists of two thin-film R-2R resistor ladder networks, four 12-bit registers, and DAC control logic circuitry. The device has separate reference-input and feedback resistors for each DAC and operates on a single supply from +5 V to +15 V. Maximum power dissipation at +5 V using zero or V_{DD} logic levels is less than 0.5 mW.

The DAC8222 is manufactured with highly stable thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS technology. Improved latch-up resistant design eliminates the need for external protective Schottky diodes.

REV. C

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DAC8222–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5 V or +15 V, $V_{REF\,A} = V_{REF\,B}$ = +10 V, $V_{OUT\,A} = V_{OUT\,B}$ = 0 V; AGND = DGND = 0 V; T_A = Full Temperature Range Specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
STATIC ACCURACY							
Resolution	N			12			Bits
Relative Accuracy	INL	Endpoint Linearity Error	DAC8222A/E/G			±1/2	LSB
			DAC8222F/H			±1	LSB
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic				±1	LSB
Full-Scale Gain Error[1]	G_{FSE}	DAC8222A/E				±1	LSB
		DAC8222G				±2	LSB
		DAC8222F/H				±4	LSB
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG_{FS}	(Notes 2, 7)			±2	±5	ppm/°C
Output Leakage Current $I_{OUT\,A}$ (Pin 2), $I_{OUT\,B}$ (Pin 24)	I_{LKG}	All Digital Inputs = 0000 0000 0000	T_A = +25°C		±5	±10	nA
			T_A = Full Temp. Range			±50	nA
Input Resistance ($V_{REF\,A}$, $V_{REF\,B}$)	R_{REF}	(Note 9)		8	11	15	kΩ
Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$				±0.2	±1	%
DIGITAL INPUTS							
Digital Input High	V_{INH}	V_{DD} = +5 V		2.4			V
		V_{DD} = +15 V		13.5			V
Digital Input Low	V_{INL}	V_{DD} = +5 V				0.8	V
		V_{DD} = +15 V				1.5	V
Input Current	I_{IN}	V_{IN} = 0 V or V_{DD}	T_A = +25°C		±0.001	±1	μA
		and V_{INL} or V_{INH}	T_A = Full Temp. Range			±10	μA
Input Capacitance[2]	C_{IN}	DB0–DB11				10	pF
		$\overline{WR}$, $\overline{LDAC}$, $\overline{DAC\ A}$/DAC B				15	pF
POWER SUPPLY							
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH}				2	mA
		All Digital Inputs 0 V or V_{DD}			10	100	μA
DC Power Supply Rejection Ratio (ΔGain/ΔV_{DD})	PSRR	ΔV_{DD} = ±5%				0.002	%/%
AC PERFORMANCE CHARACTERISTICS[2]							
Propagation Delay[4, 5]	t_{PD}	T_A = +25°C				350	ns
Current Settling Time[5, 6]	t_S	T_A = +25°C				1	μs
Output Capacitance	C_O	Digital Inputs = All 0s				90	pF
		$C_{OUT\,A}$, $C_{OUT\,B}$				90	pF
		Digital Inputs = All 1s				120	pF
		$C_{OUT\,A}$, $C_{OUT\,B}$				120	pF
AC Feedthrough at $I_{OUT\,A}$ or $I_{OUT\,B}$	FT_A	$V_{REF\,A}$ to $I_{OUT\,A}$; $V_{REF\,A}$ = 20 V p-p;				–70	dB
		f = 100 kHz; T_A = +25°C				–70	dB
		$V_{REF\,B}$ to $I_{OUT\,B}$; $V_{REF\,B}$ = 20 V p-p;				–70	dB
	FT_B	f = 100 kHz; T_A = +25°C				–70	dB

SWITCHING CHARACTERISTICS[2, 3]		V_{DD} = +5 V			V_{DD} = +15 V	
		+25°C	–40°C to +85°C[8]	–55°C to +125°C	All Temps[10]	
DAC Select to Write Set-Up Time	t_{AS}	150	180	210	60	ns min
DAC Select to Write Hold Time	t_{AH}	0	0	0	0	ns min
$\overline{LDAC}$ to Write Set-Up Time	t_{LS}	80	100	120	60	ns min
$\overline{LDAC}$ to Write Hold Time	t_{LH}	20	20	20	20	ns min
Data Valid to Write Set-Up Time	t_{DS}	220	240	260	100	ns min
Data Valid to Write Hold Time	t_{DH}	0	0	0	10	ns min
Write Pulse Width	t_{WR}	130	160	170	90	ns min
$\overline{LDAC}$ Pulse Width	t_{LWD}	100	120	130	60	ns min

NOTES

[1]Measured using internal $R_{FB\,A}$ and $R_{FB\,B}$. Both DAC digital inputs = 1111 1111 1111.

[2]Guaranteed and not tested.

[3]See timing diagram.

[4]From 50% of digital input to 90% of final analog output current. $V_{REF\,A} = V_{REF\,B}$ = +10 V; OUT A, OUT B load = 100 Ω, C_{EXT} = 13 pF.

[5]$\overline{WR}$, $\overline{LDAC}$ = 0 V; DB0–DB11 = 0 V to V_{DD} or V_{DD} to 0 V.

[6]Settling time is measured from 50% of the digital input change to where the output voltage settles within 1/2 LSB of full scale.

[7]Gain TC is measured from +25°C to T_{MIN} or from +25°C to T_{MAX}.

[8]These limits apply for the commercial and industrial grade products.

[9]Absolute temperature coefficient is approximately +50 ppm/°C.

[10]These limits also apply as typical values for V_{DD} = +12 V with +5 V CMOS logic levels and T_A = +25°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to AGND . . . . . 0 V, +17 V
V_{DD} to DGND . . . . . 0 V, +17 V
AGND to DGND . . . . . –0.3 V, V_{DD} +0.3 V
Digital Input Voltage to DGND . . . . . –0.3 V, V_{DD} +0.3 V
I_{OUTA}, I_{OUTB} to AGND . . . . . –0.3 V, V_{DD} +0.3 V
V_{REFA}, V_{REFB} to AGND . . . . . ±25 V
V_{RFBA}, V_{RFBB} to AGND . . . . . ±25 V
Operating Temperature Range
AW Version . . . . . –55°C to +125°C
EW, FW, FP Versions . . . . . –40°C to +85°C
GP, HP, HS Versions . . . . . 0°C to +70°C
Junction Temperature . . . . . +150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[1]	θ_{JC}	Units
24-Lead Hermetic DIP (W)	69	10	°C/W
24-Lead Plastic DIP (P)	62	32	°C/W
24-Lead SOL (S)	72	24	°C/W

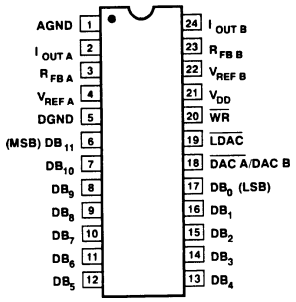
NOTE
[1]θ_{JA} is specified for worst-case mounting conditions, i.e., q_{JA} is specified for device in socket for Cerdip, and P-DIP packages; $_{JA}$ is specified for device soldered to printed circuit board for SO package.

CAUTION

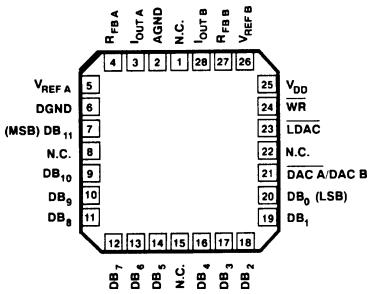
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are Zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper antistatic handling procedures.
5. Devices can suffer permanent damage and/or reliability degradation if stressed above the limits listed under Absolute Maximum Ratings for extended periods.

PIN CONNECTIONS

24-Lead 0.3" Cerdip
24-Lead Plastic DIP
24-Lead SOL



28-Terminal LCC



NC = NO CONNECT

ORDERING GUIDE

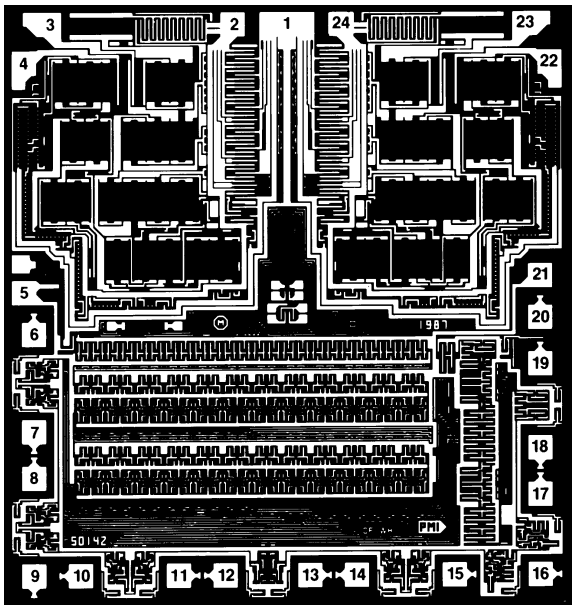
Model	INL (LSB)	GFSE (LSB)	Temperature Range	Package Description	Package Option
DAC8222EW	±1/2	±1	–40°C to +85°C	Cerdip-24	Q-24
DAC8222GP	±1/2	±2	0°C to +70°C	P-DIP-24	N-24
DAC8222BTC/883*	±1	±4	–55°C to +125°C	LCC-28	E-28A
DAC8222FW	±1	±4	–40°C to +85°C	Cerdip-24	Q-24
DAC8222FP	±1	±4	–40°C to +85°C	P-DIP-24	N-24
DAC8222FS	±1	±4	–40°C to +85°C	SOL-24	R-24

*Consult factory for DAC8222/883 MIL-STD data sheet.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the DAC8222 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DICE CHARACTERISTICS



DIE SIZE 0.124 × 0.132 inch, 16,368 sq. mils
(3.15 × 3.55 mm, 10.56 sq. mm)

1. AGND
2. $I_{OUT\ A}$
3. $R_{FB\ A}$
4. $V_{REF\ A}$
5. DGND
6. DB11(MSB)
7. DB10
8. DB9
9. DB8
10. DB7
11. DB6
12. DB5
13. DB4
14. DB3
15. DB2
16. DB1
17. DB0 (LSB)
18. $\overline{\text{DAC A}}$/DAC B
19. $\overline{\text{LDAC}}$
20. $\overline{\text{WR}}$
21. V_{DD}
22. $V_{REF\ B}$
23. $R_{FB\ B}$
24. $I_{OUT\ B}$

Substrate (die backside) is internally connected to V_{DD}.

WAFER TEST LIMITS (@ V_{DD} = +5 V or +15 V, $V_{REF\ A} = V_{REF\ B}$ = +10 V, $V_{OUT\ A} = V_{OUT\ B}$ = 0 V; AGND = DGND = 0 V; T_A = +25°C)

Parameter	Symbol	Conditions	DAC8222G Limit	Units
Relative Accuracy	INL	Endpoint Linearity Error	±1	LSB max
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic	±1	LSB max
Full Scale Gain Error[1]	G_{FSE}	Digital Inputs = 1111 1111 1111	±4	LSB max
Output Leakage		Digital Inputs = 0000 0000 0000	±50	nA max
($I_{OUT\ A}$, $I_{OUT\ B}$)	I_{LKG}	Pads 2 and 24		
Input Resistance				
($V_{REF\ A}$, $V_{REF\ B}$)	R_{REF}	Pads 4 and 22	8/15	kΩ max
Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$		±1	% max
Digital Input High	V_{INH}	V_{DD} = +5 V	2.4	V min
		V_{DD} = +15 V	13.5	V min
Digital Input Low	V_{INL}	V_{DD} = +5 V	0.8	V max
		V_{DD} = +15 V	1.5	V min
Digital Input Current	I_{IN}	V_{IN} = 0 V or V_{DD}; V_{INL} or V_{INH}	±1	μA max
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	2	
		All Digital Inputs 0 V or V_{DD}	0.1	mA max
DC Supply Rejection	PSR	ΔV_{DD} = ±5%	0.002	%/% max
(ΔGain/ΔV_{DD})				

NOTES
[1]Measured using internal $R_{FB\ A}$ and $R_{FB\ B}$.
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

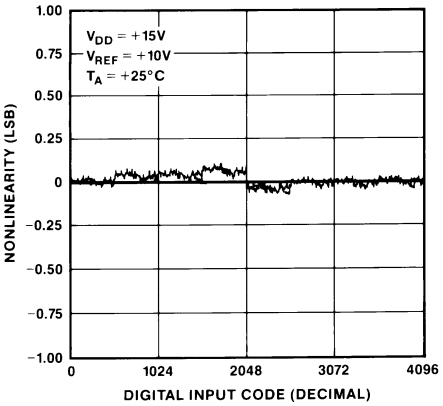


Figure 1. Channel-to-Channel Matching (DAC A and B are Superimposed)

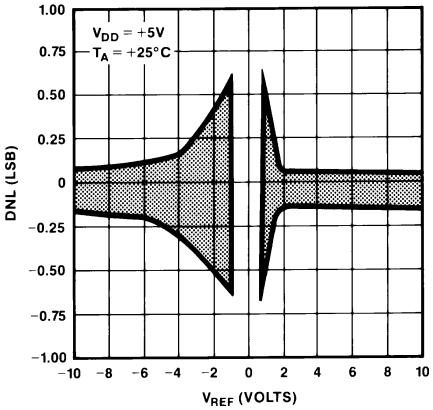


Figure 2. Differential Nonlinearity vs. V_{REF}

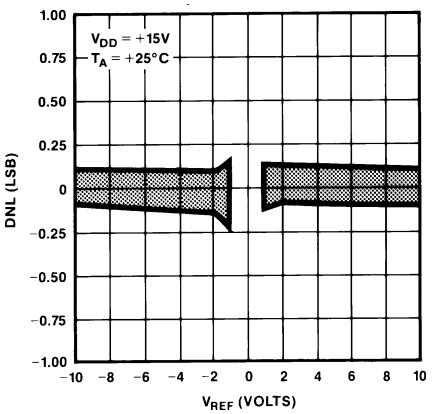


Figure 3. Differential Nonlinearity vs. V_{REF}

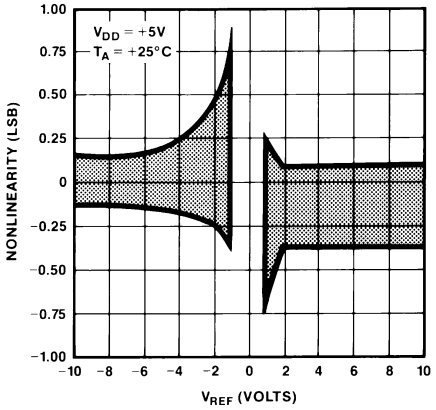


Figure 4. Nonlinearity vs. V_{REF}

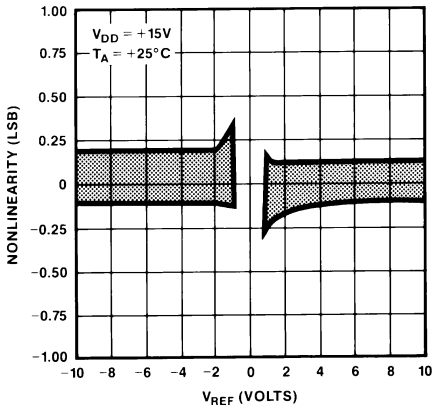


Figure 5. Nonlinearity vs. V_{REF}

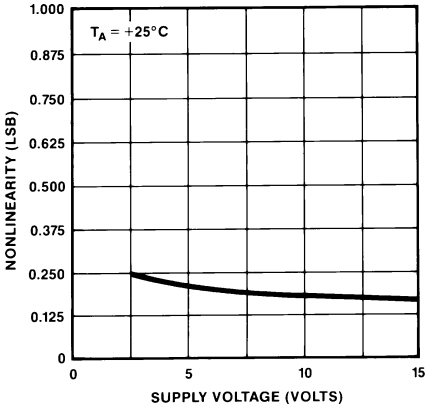


Figure 6. Nonlinearity vs. V_{DD}

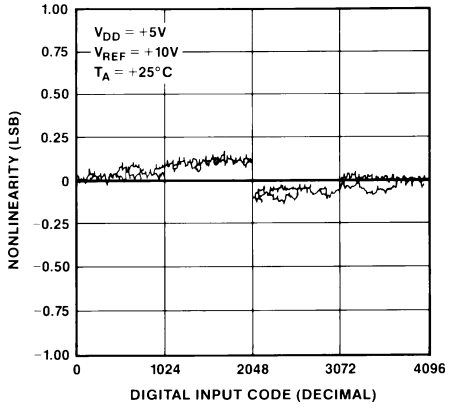


Figure 7. Nonlinearity vs. Code (DAC A and B are Superimposed)

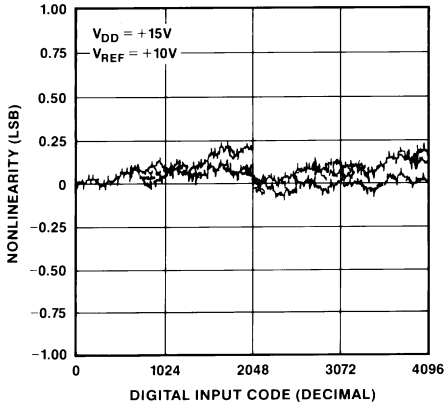


Figure 8. Nonlinearity vs. Code at T_A = –55°C, +25°C, +125°C for DAC A and B (All Superimposed)

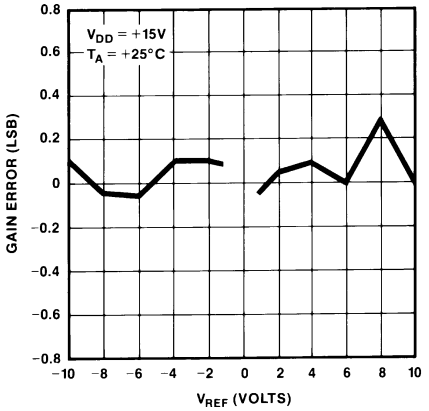


Figure 9. Absolute Gain Error Changes vs. V_{REF}

TYPICAL PERFORMANCE CHARACTERISTICS

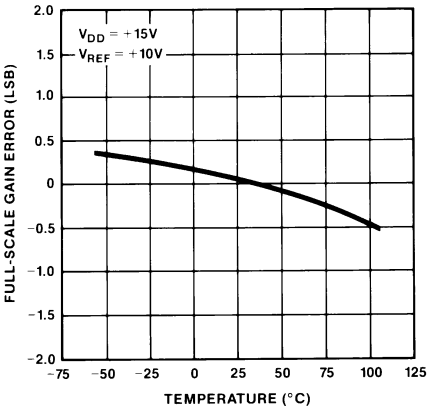


Figure 10. Full-Scale Gain Error vs. Temperature

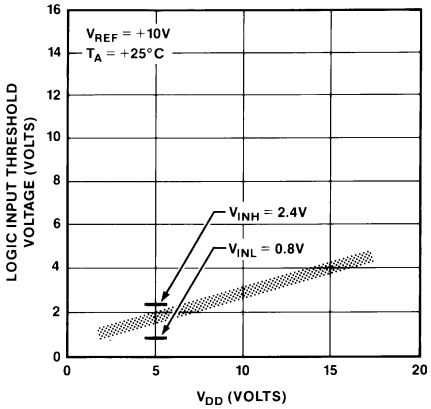


Figure 11. Logic Input Threshold Voltage vs. Supply Voltage (V_{DD})

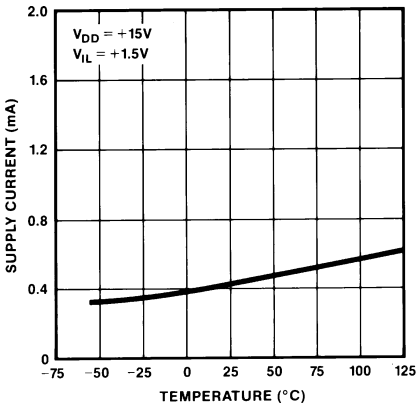


Figure 12. Supply Current vs. Temperature

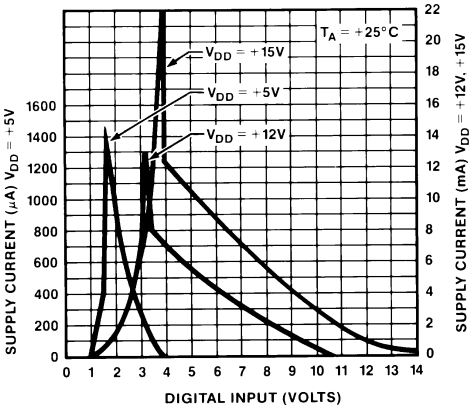


Figure 13. Supply Current vs. Logic Input Voltage

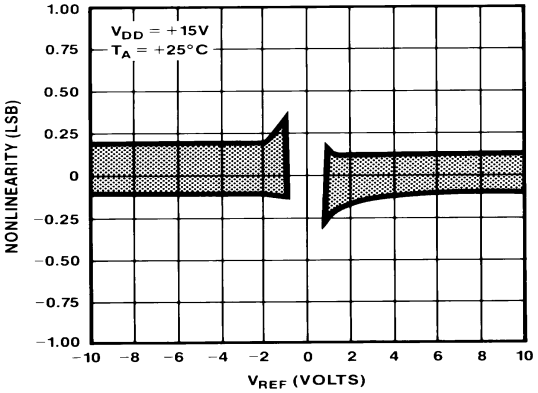


Figure 14. Multiplying Mode Frequency Response vs. Digital Code

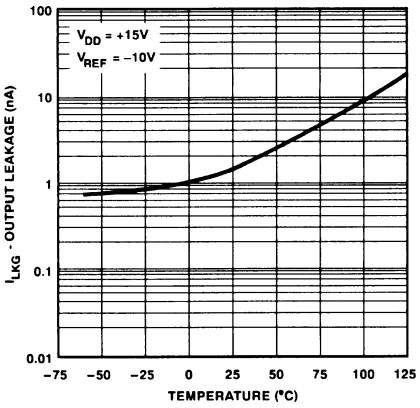


Figure 15. Output Leakage Current vs. Temperature

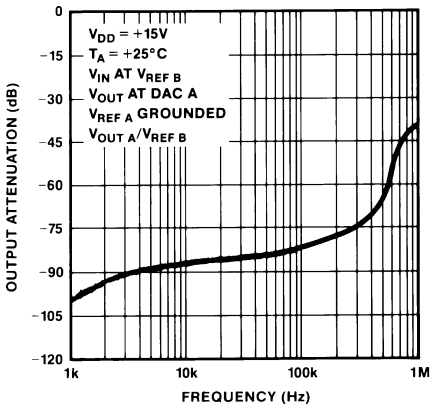


Figure 16. Analog Crosstalk vs. Frequency

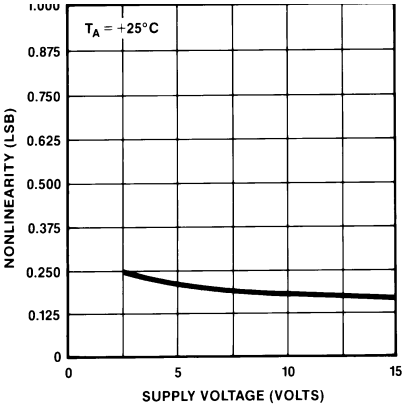


Figure 17. Interface Timing vs. V_{DD}

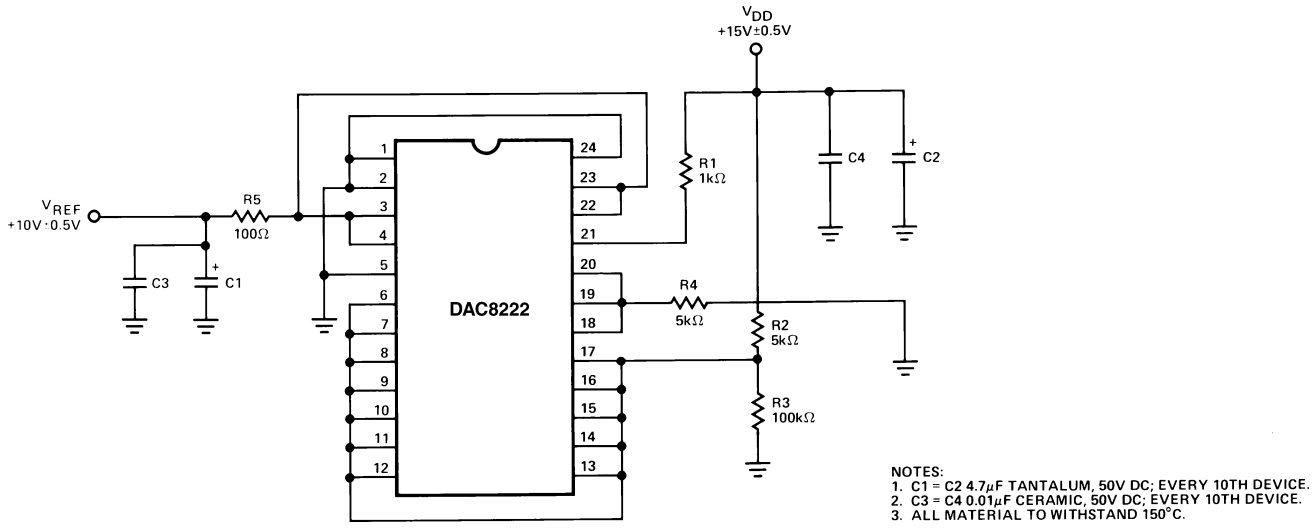


Figure 18. Burn-In Circuit

PARAMETER DEFINITIONS

RESOLUTION (n)

The resolution of a DAC is the number of states (2^n) into which the full-scale range (FSR) is divided (or resolved); where *n* is equal to the number of bits.

RELATIVE ACCURACY (INL)

Relative accuracy, or integral nonlinearity, is the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed in terms of least significant bit (LSB), or as a percent of full scale.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog output from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called the differential nonlinearity error or DNL. DACs with DNL greater than ±1 LSB may be nonmonotonic ±1/2 LSB INL guarantees monotonicity and ±1 LSB maximum DNL.

GAIN ERROR (G_{FSE})

Gain error is the difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal.

See Orientation in Digital-to-Analog Converters Section of the current data book, for additional parameter definitions.

GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The DAC8222 contains four 12-bit registers (two input registers and two DAC registers), two highly stable thin-film R-2R resistor ladder networks, and interface control logic circuitry. Also included are 24 single-pole, double-throw, NMOS transistor current switches.

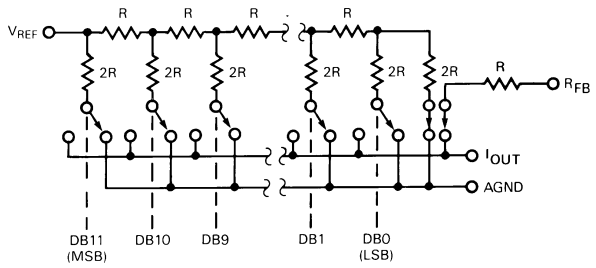


Figure 19. Simplified Single DAC Circuit Configuration. (Switches Are Shown for All Digital Inputs at Zero)

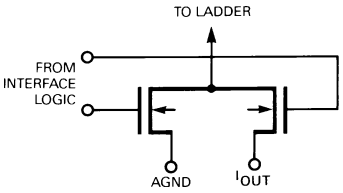


Figure 20. N-Channel Current Steering Switch

Figure 19 shows a simplified circuit for the R-2R ladder network and transistor switches for one DAC. R is typically 11 kΩ. The transistor switches are binarily scaled in size to maintain a constant voltage drop across each switch. Figure 20 shows a single NMOS transistor switch.

The binary-weighted currents are switched between I_{OUT} and AGND by the N-channel MOS transistor switches. The selection between I_{OUT} and AGND is determined by the digital input code. It is important to note here that the voltage difference

between I_{OUT} and AGND terminals be as close to zero as practical in order to keep DAC errors to a minimum. This is normally done by connecting AGND to the noninverting input of an op amp and I_{OUT} to the inverting input. The DAC's internal resistor (R_{FB}) can be used for the feedback resistor by connecting the op amp's output directly to the DAC's R_{FB} terminal. The op amp also provides the current-to-voltage conversion for the DAC's output current. The output voltage is dependent on the DAC's digital input code and V_{REF}, and is given by:

$$V_{OUT} = -V_{REF} \times D/4096$$

where *D* is the digital input code integer number that is between 0 and 4095.

The DAC's input resistance, V_{REF} (Figure 19), is always equal to a constant value, R. This means that V_{REF} can be driven by a reference voltage or current, ac or dc (positive or negative). It is recommended that a low-temperature-coefficient external R_{FB} resistor be used if a current source is employed.

The DAC's output capacitance (C_{OUT}) is code dependent and varies from 90 pF (all digital inputs low) to 120 pF (all digital inputs high).

Figure 19 shows a transistor switch in series with the R-2R ladder terminating resistor and R_{FB} resistor. They were designed into the DAC to binarily match the ladder leg switches and improve power supply rejection and gain error temperature coefficient. The gates of these transistor switches are connected to V_{DD}, so that an "open-circuit" exists when V_{DD} is not applied. This means that an op amp's output voltage will go to either "rail" if powered up before the DAC. Also, R_{FB} resistance cannot be measured without V_{DD} being applied.

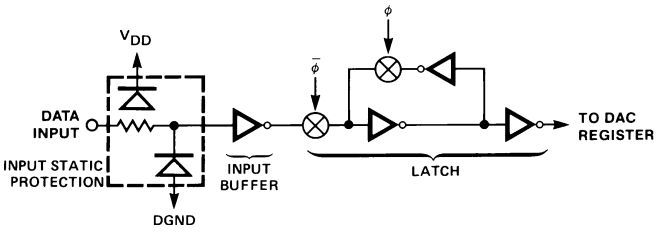


Figure 21. Digital Input Structure For One Bit

DIGITAL SECTION

The DAC8222's digital inputs are CMOS inserters. They were designed to convert TTL and CMOS input logic levels into voltage levels to drive the internal circuitry. The digital inputs are TTL compatible at V_{DD} = +5 V and CMOS compatible at V_{DD} = +15 V. The DAC8222 can use +5 V CMOS logic levels with V_{DD} = +12 V; however, supply current will rise to approximately 5 mA–6 mA.

Figure 21 shows the DAC's digital input register structure for one bit. This circuit drives the DAC register. Digital controls ϕ and $\bar{\phi}$ shown are generated from $\overline{\text{DAC A}}$/DAC B and $\overline{\text{WR}}$ control signals.

As shown in Figure 21, these inputs are electrostatic-discharge protected with two internal distributed diodes; they are connected between V_{DD} and DGND. Each digital input has a typical input current of less than 1 nA.

When the digital inputs are in the region of +1.2 V to +2.8 V (peaking at +1.8 V) using a +5 V power supply or in the region of +1.7 V to +12 V (peaking at +3.9 V) with a +15 V power supply, the input register transistors are operating in their linear region and draw current from the power supply. It is therefore, recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible to keep supply currents at a minimum. The DAC8222 may be operated with any supply voltage between the range of +5 V to +15 V.

INTERFACE CONTROL LOGIC

The DAC8222's input control logic circuitry is shown in Figure 22. Note how the $\overline{\text{WR}}$ signal is used in conjunction with $\overline{\text{DAC A}}$/ DAC B to load data into either input register. $\overline{\text{LDAC}}$ loads data from the input registers to the DAC register; the DAC's analog output voltage is determined by the data contained in each DAC register.

The truth table for the DAC registers is shown in the Mode Selection Table. Note how the input register is transparent when $\overline{\text{WR}}$ is low and $\overline{\text{LDAC}}$ is high, and that the DAC register is transparent when $\overline{\text{WR}}$ is high and $\overline{\text{LDAC}}$ is low ($\overline{\text{LDAC}}$ updates the DAC's analog output voltage). The DAC is transparent from input to output when $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ are both low, and the DAC is latched (input and output is not being updated) when $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ are both high.

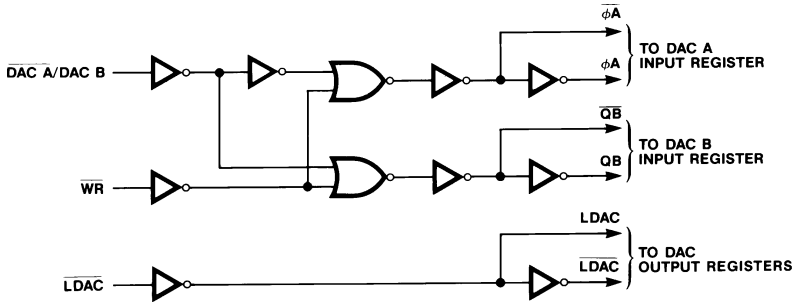


Figure 22. Input Control Logic

Table I. Mode Selection

Digital Inputs			Register Status			
			DAC A		DAC B	
DAC $\overline{A}$/B	$\overline{WR}$	$\overline{LDAC}$	Input Register	DAC Register	Input Register	DAC Register
L	L	L	WRITE	WRITE	LATCHED	WRITE
H	L	L	LATCHED	WRITE	WRITE	WRITE
L	L	H	WRITE	LATCHED	LATCHED	LATCHED
H	L	H	LATCHED	LATCHED	WRITE	LATCHED
X	H	L	LATCHED	WRITE	LATCHED	WRITE
X	H	H	LATCHED	LATCHED	LATCHED	LATCHED

L = Low, H = High, X = Don't Care

INTERFACE CONTROL LOGIC

$\overline{DAC\ A}$/DAC B (Pin 18)–DAC Selection. Active low for $\overline{DAC\ A}$ and active high for DAC B.

$\overline{WR}$ (Pin 20)–$\overline{WRITE}$. Active Low. Used to write data into either DAC A or DAC B input registers, or active high latches data into the input registers.

$\overline{LDAC}$ (Pin 19)–$\overline{LOAD\ DAC}$. Active Low. Used to simultaneously transfer data from $\overline{DAC\ A}$ and DAC B input registers to both DAC outputs. The DAC becomes transparent (activity on the digital inputs appear at the analog output) when both $\overline{WR}$ and $\overline{LDAC}$ are low. Data is latched into the output registers on the rising edge of $\overline{LDAC}$.

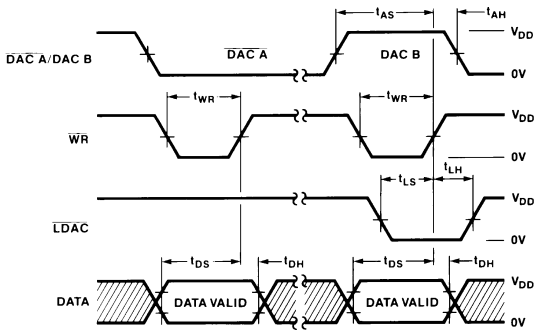
WRITE TIMING CYCLES

Two timing diagrams are shown and are at the user's discretion which to use.

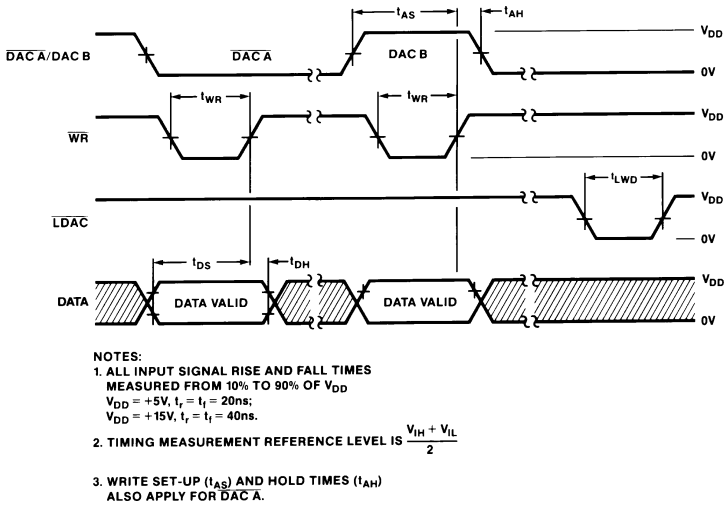
The TWO-CYCLE UPDATE, as the name implies, allows both DAC registers to be loaded and the outputs updated in two cycles. Data is first loaded into one DAC's input register on the first write cycle, and then new data loaded into the other DAC's input register while simultaneously updating both DAC outputs on the second cycle.

The THREE-CYCLE UPDATE allows $\overline{DAC\ A}$ and DAC B registers to be loaded and analog output to be updated at a later time. The first two cycles load both DACs as above, and the third cycle updates the outputs.

The $\overline{LDAC}$ and $\overline{DAC\ A}$/DAC B control pins can be tied together and controlled with a single strobe. When using the DAC in this configuration, DAC B must be loaded first.



Two-Cycle Update



Three-Cycle Update

Figure 23. Write Cycle Timing Diagram

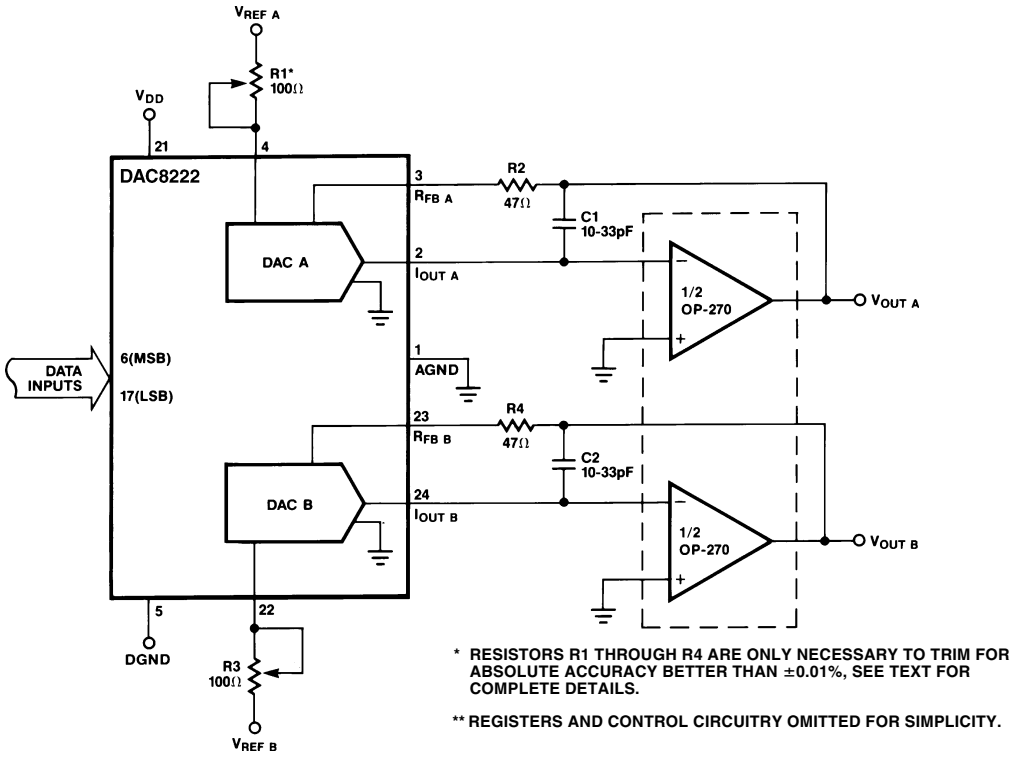


Figure 24. Unipolar Configuration (Two-Quadrant Multiplication)

APPLICATIONS INFORMATION

UNIPOLAR OPERATION

Figure 24 shows a simple unipolar (2-quadrant multiplication) circuit using the DAC8222 and OP270 dual op amp (use two OP42s for higher speeds), and Table II the corresponding code table. Resistors R1, R2, and R3, R4 are used only if full-scale gain adjustments are required. Low temperature coefficient (approximately 50 ppm/°C) resistors or trimmers should be used. Maximum full-scale error without these resistors for the top grade device and V_{REF} = ±10 V is 0.024% and 0.097% for the low grade. C1 and C2 provide phase compensation to help reduce overshoot and ringing when high speed op amps are used.

Full-scale adjustment is accomplished by loading the digital inputs with all 1s and adjusting R1 (or R3) so that

$$V_{OUT} = V_{REF} \times \left(\frac{4095}{4096}\right)$$

Full-scale can also be adjusted by varying V_{REF} voltage, thus eliminating R1, R2, R3 and R4. Zero adjustment is performed by setting the DAC's digital inputs to all 0s and adjusting the op amp's offset adjust so that V_{OUT} = 0 V. To maintain monotonicity and minimize gain and linearity errors, it is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB (244 μV) over the operating temperature range of interest.

Table II. Unipolar Binary Code Table (Refer to Figure 24)

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUT} (DAC A or DAC B)
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0 V

NOTE

1 LSB = (2^{-12}) (V_{REF}) = $\frac{1}{4096}$ (V_{REF})

BIPOLAR OPERATION

The bipolar (offset binary) four-quadrant operation configuration using the DAC8222 is shown in Figure 25 and the corresponding code in Table III. The circuit makes use of the OP470 a quad op amp (use four OP42s for higher speeds).

Resistors R1, R2, R3, and R4 may be omitted and full-scale output voltage may be adjusted by varying V_{REF} or the value of R5 and R8. If resistors R1, R2, R3, and R4 are omitted,

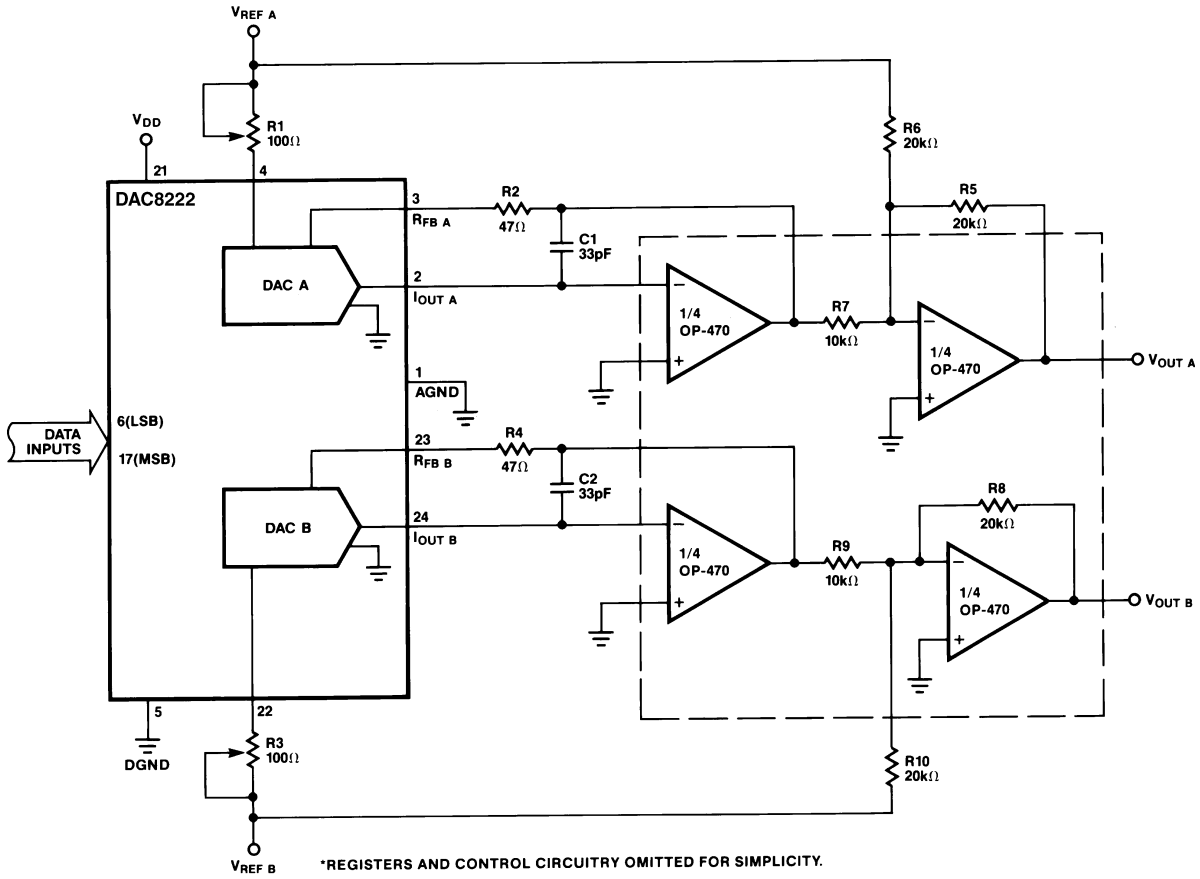


Figure 25. Bipolar Configuration (Four-Quadrant Multiplication)

Table III. Bipolar (Offset Binary) Code Table (Refer to Figure 25)

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUT} ($\overline{\text{DAC A}}$ or DAC B)
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0 V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTE

$1\ LSB = (2^{-11})\ (V_{REF}) = \frac{1}{2048}\ (V_{REF})$

resistors R5, R6, R7, should be ratio-matched to 0.01% so that gain error meets data sheet specifications. (Corresponding resistors, R8, R9, and R10 for DAC B should also be matched to 0.01%). The resistors should have identical temperature coefficients if operating over the full temperature range.

Zero and full-scale are adjusted one of two ways and are at the user's discretion. Zero-output can be adjusted by first setting the digital inputs to 1000 0000 0000 and adjusting R1 (R3 for DAC B) so that V_{OUTA} (or $V_{OUT\,B}$) equals 0 V. If R1, R2 (R3, R4 for DAC B) are omitted, then V_{OUT} = 0 V can be adjusted by varying R6, R7 (R9, R10 for DAC B) ratios. Full-scale is adjusted by setting the digital inputs to 1111 1111 1111 and varying R5 (R8 for DAC B). Full-scale can also be adjusted by varying V_{REF}. Full-scale output is equal to V_{REF} minus one LSB.

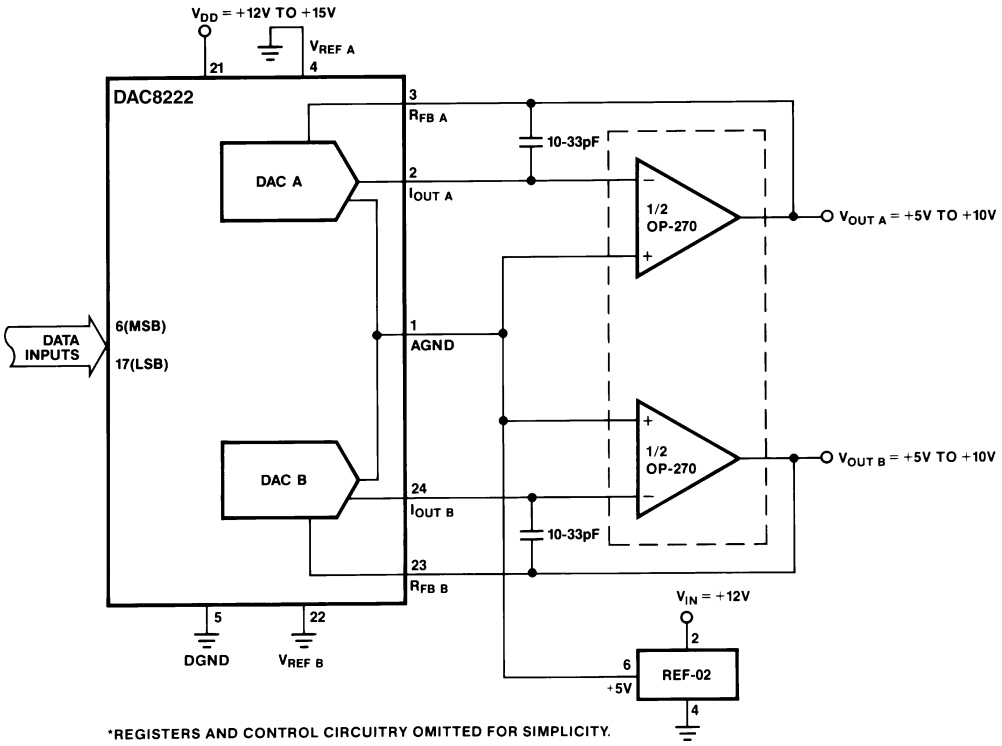


Figure 26. Single Supply Operation (Current Switching Mode)

SINGLE SUPPLY OPERATION

CURRENT STEERING MODE

Because the DAC8222's R-2R resistor ladder terminating resistor is internally connected to AGND, it lends itself well to single supply operation in the current steering mode. This means that AGND can be raised above system ground as shown in Figure 26. The output voltage range will be from +5 V to +10 V depending on the digital input code and is given by:

$$V_{OUT} = V_{OS} + (n/4096)\ (V_{OS})$$

where V_{OS} = Offset Reference Voltage (+5 V in Figure 26)
n = Decimal Equivalent of the Digital Input Word

VOLTAGE SWITCHING MODE

Figure 27 shows the DAC8222 in a single supply voltage switching mode of operation. In this configuration, the DAC's R-2R ladder acts as a voltage divider. The output voltage at the V_{REF} pin exhibits a constant impedance R (typically 11 kΩ) and must be buffered by an op amp. R_{FB} pins are not used in this circuit configuration. The reference input voltage must be maintained within +1.25 V of AGND and V_{DD} from +12 V to +15 V to preserve device accuracy.

The output voltage expression is given by:

$$V_{OUT} = V_{REF}\ (n/4096)$$

where n = Decimal Equivalent of the Digital Input Word

APPLICATIONS TIPS

GENERAL GROUND MANAGEMENT

Grounding techniques should be tailored to each individual system. Ground loops should be avoided, and ground current paths should be as short as possible and have a low impedance.

The DAC8222's AGND and DGND pins should be tied together at the device socket to prevent digital transients from appearing at the analog output. This common point then becomes the single ground point connection. AGND and DGND should then be brought out separately and tied to their respective power supply grounds. Ground loops can be created if both grounds are tied together at more than one location, i.e., tied together at the device and at the digital and analog power supplies.

A PC board ground plane can be used for the single point ground connection should the connections not be practical at the device socket. If neither of these connections is practical or allowed, the device should be placed as close as possible to the system's single point ground connection. Back-to-back Schottky diodes should then be connected between AGND and DGND.

POWER SUPPLY DECOUPLING

Power supplies used with the DAC8222 should be well filtered and regulated. Local supply decoupling consisting of a 1 μF to 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic is highly recommended. The capacitors should be connected between the V_{DD} and DGND pins and at the device socket.

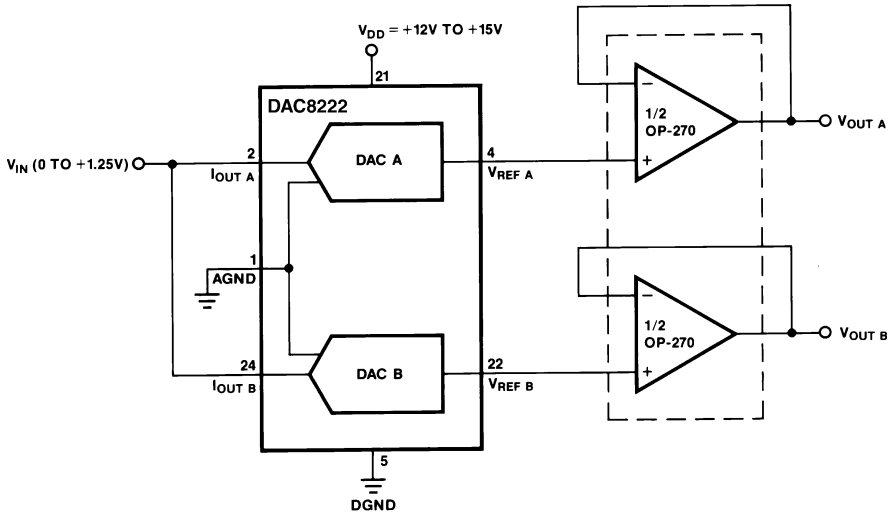


Figure 27. Single Supply Operation (Voltage Switching Mode)

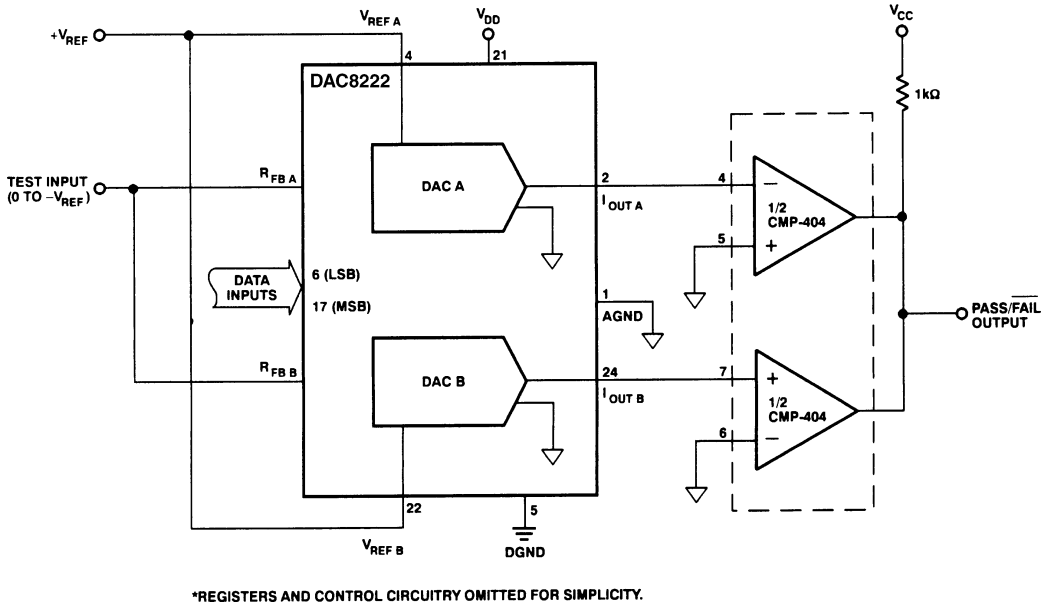


Figure 28. Digitally-Programmable Window Detector (Upper/Lower Limit Detector)

BASIC APPLICATIONS

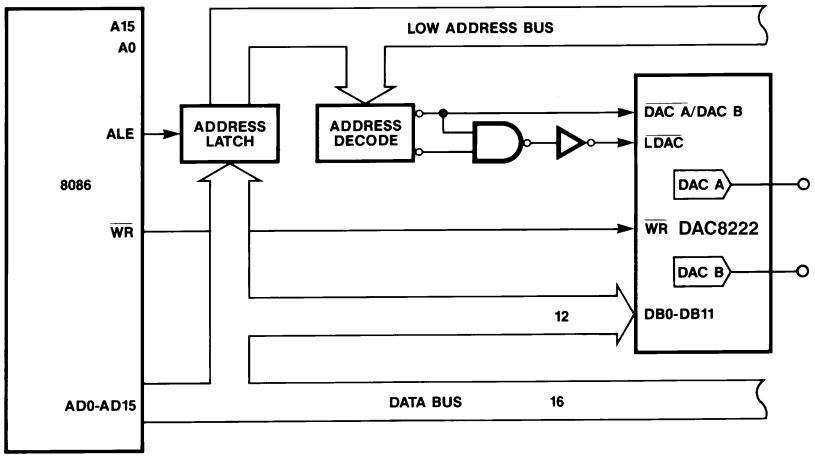
PROGRAMMING WINDOW DETECTOR

Figure 28 shows the DAC8222 used in a programmable window detector configuration. The required upper and lower limits for the test are loaded into $\overline{\text{DAC A}}$ and DAC B. If a signal at the test input is not within the programmed limits, the output will indicate a logic zero.

MICROPROCESSOR INTERFACE CIRCUITS

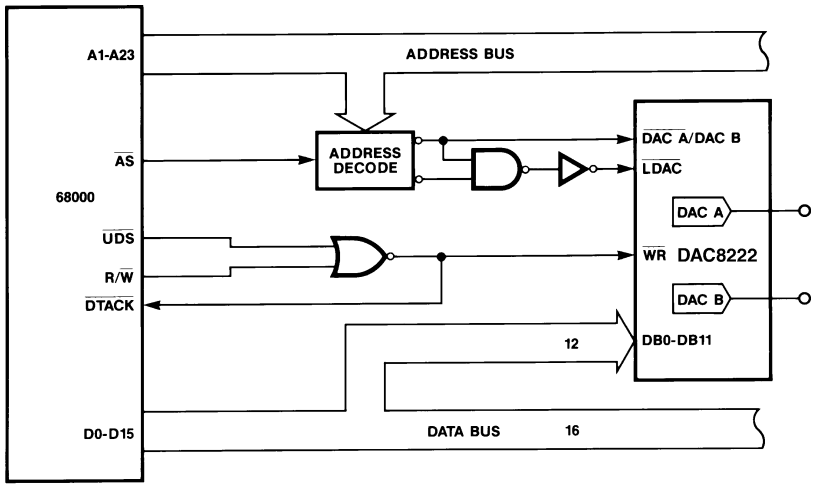
The DAC8222's versatile loading structure greatly simplifies interfacing to 16-bit bus systems; it also reduces the number of "glue" logic components. Data loading into its 12-bit wide data input is achieved by use of only two control signals, $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$. DAC selection is controlled with a single $\overline{\text{DAC A}}$/DAC B line.

Figures 29 and 30 show how easily the DAC8222 interfaces with the 8086 and 68000 16-bit microprocessors.



*REGISTERS AND CONTROL CIRCUITRY OMITTED FOR SIMPLICITY.

Figure 29. DAC8222 to 8086 Interface



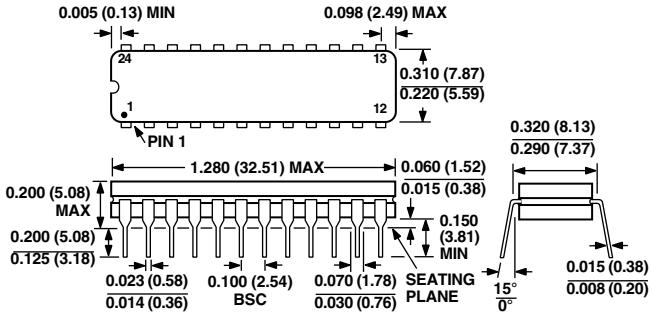
*REGISTERS AND CONTROL CIRCUITRY OMITTED FOR SIMPLICITY.

Figure 30. DAC8222 to 68000 Interface

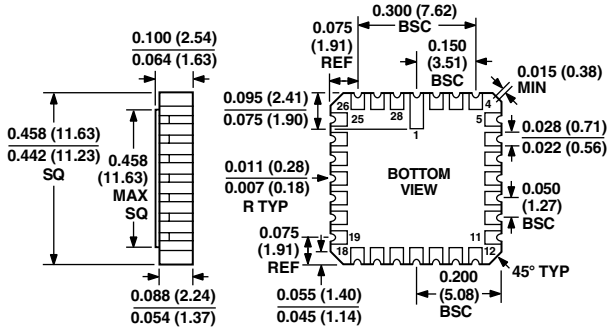
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

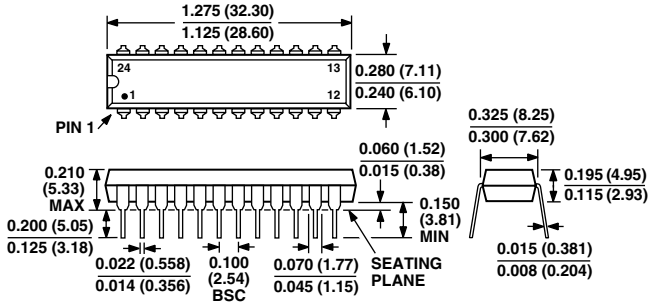
24-Lead Cerdip
(Q-24)



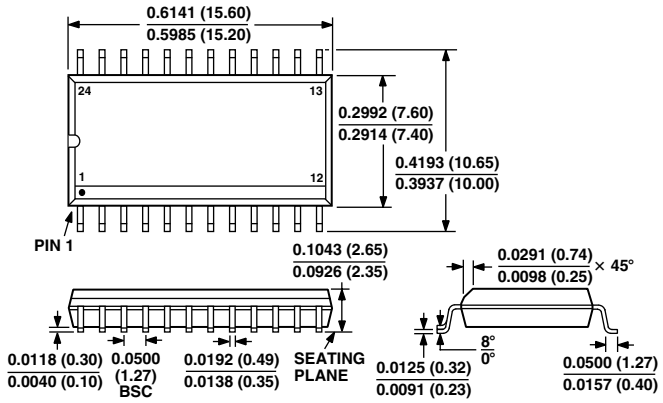
28-Terminal Leadless Ceramic Chip Carrier
(E-28A)



24-Lead Plastic DIP
(N-24)



24-Lead Wide-Body SOL
(R-24)



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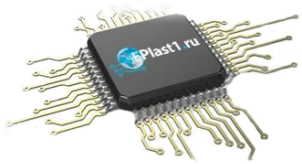

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