BATTERY PROTECTION IC FOR 2-SERIAL-CELL PACK

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The S-8232 series is a lithium-ion / lithium-polymer rechargeable battery protection IC incorporating high-accuracy voltage detection circuit and delay circuit.
The S-8232 series is suitable for 2-cell serial lithium-ion / lithium-polymer battery packs.

■ Features

(1) Internal high-accuracy voltage detection circuit
- Overcharge detection voltage 3.85 V ± 25 mV to 4.60 V ± 25 mV Applicable in 5 mV step
- Overcharge release voltage 3.60 V ± 50 mV to 4.60 V ± 50 mV Applicable in 5 mV step
  (The overcharge release voltage can be selected within the range where a difference from overcharge detection voltage is 0 V to 0.3 V.)
- Overdischarge detection voltage 1.70 V ± 80 mV to 2.60 V ± 80 mV Applicable in 50 mV step
- Overdischarge release voltage 1.70 V ± 100 mV to 3.80 V ± 100 mV Applicable in 50 mV step
  (The overdischarge release voltage can be selected within the range where a difference from overdischarge detection voltage is 0 V to 1.2 V.)
- Overcurrent detection voltage 1 0.07 V ± 20 mV to 0.30 V ± 20 mV Applicable in 5 mV step

(2) High input-voltage device : Absolute maximum ratings 18 V.
(3) Wide operating voltage range : 2.0 V to 16 V
(4) The delay time for every detection can be set via an external capacitor.
(Each delay time for Overcharge detection, Overdischarge detection, Overcurrent detection are "Proportion of hundred to ten to one".)
(5) Two overcurrent detection levels (Protection for short-circuiting)
(6) Internal auxiliary over voltage detection circuit (Fail-safe for overcharge detection voltage)
(7) Internal charge circuit for 0 V battery (Unavailable is option)
(8) Low current consumption
- Operation mode 7.5 μA typ. 14.2 μA max. (– 40°C to + 85°C)
- Power-down mode 0.2 nA typ. 0.1 μA max. (– 40°C to + 85°C)

(9) Lead-free, Sn100%, halogen-free*1

***1.** Refer to "■ **Product Name Structure**" for details.

■ Applications

- Lithium-ion rechargeable battery packs
- Lithium- polymer rechargeable battery packs

■ Package

- 8-Pin TSSOP

■ Block Diagram

Remark Resistor (RCOL) is connected to the Nch transistor although CO pin serves as a CMOS output. For this, impedance becomes high when outputting "L" from CO pin. Refer to the "■ **Electrical Characteristics**" for the impedance value.

Figure 1

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■ Product Name Structure

1. Product Name

S-8232 xx FT - T2 - x

- x: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
  - S: Lead-free, halogen-free
  - G: Lead-free (for details, please contact our sales office)
- T2: IC direction in tape specifications *1
- FT: Package code
  - FT : 8-Pin TSSOP
- xx: Serial code
  - Sequentially set from AA to ZZ

***1.** Refer to the tape specifications.

2. Package

Package Name	Drawing Code		
	Package	Tape	Reel
8-Pin TSSOP	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-SD

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3. Product Name List

Table 1 (1 / 2)

Product name	Overcharge detection voltage 1, 2 [V_{CU}]	Overcharge release voltage 1, 2 [V_{CD}]	Overdischarge detection voltage 1, 2 [V_{DD}]	Overdischarge release voltage1, 2 [V_{DU}]	Overcurrent detection voltage 1 [V_{IOV1}]	Overcharge detection delay time [t_{CU}] (C3 = 0.22 µF)	0 V battery charging function
S-8232AAFT-T2-x	4.25 V ± 25 mV	4.05 V ± 50 mV	2.40 V ± 80 mV	3.00 V ± 100 mV	0.150 V ± 20 mV	1.0 s	Available
S-8232ABFT-T2-x	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Available
S-8232ACFT-T2-x	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Unavailable
S-8232AEFT-T2-x	4.35 V ± 25 mV	4.28 V ± 50 mV	2.15 V ± 80 mV	2.80 V ± 100 mV	0.100 V ± 20 mV	1.0 s	Available
S-8232AFFT-T2-x	4.25 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	2.70 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Available
S-8232AGFT-T2-x	4.25 V ± 25 mV	4.05 V ± 50 mV	2.20 V ± 80 mV	2.40 V ± 100 mV	0.200 V ± 20 mV	1.0 s	Available
S-8232AHFT-T2-x	4.25 V ± 25 mV	4.05 V ± 50 mV	2.20 V ± 80 mV	2.40 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Available
S-8232AIFT-T2-x	4.325 V ± 25 mV	4.325 V ± 25 mV*1 *2	2.40 V ± 80 mV	3.00 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Unavailable
S-8232AJFT-T2-x	4.25 V ± 25 mV	4.05 V ± 50 mV	2.40 V ± 80 mV	3.00 V ± 100 mV	0.150 V ± 20 mV	1.0 s	Unavailable
S-8232AKFT-T2-x	4.20 V ± 25 mV	4.00 V ± 50 mV	2.30 V ± 80 mV	2.90 V ± 100 mV	0.200 V ± 20 mV	1.0 s	Available
S-8232ALFT-T2-x	4.30 V ± 25 mV	4.05 V ± 50 mV	2.00 V ± 80 mV	3.00 V ± 100 mV	0.200 V ± 20 mV	1.0 s	Available
S-8232AMFT-T2-x	4.19 V ± 25 mV	4.19 V ± 25 mV*1	2.00 V ± 80 mV	3.00 V ± 100 mV	0.190 V ± 20 mV	1.0 s	Available
S-8232ANFT-T2-x	4.325 V ± 25 mV	4.325 V ± 25 mV*1 *3	2.40 V ± 80 mV	3.00 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Unavailable
S-8232AOFT-T2-x	4.30 V ± 25 mV	4.05 V ± 50 mV	2.00 V ± 80 mV	3.00 V ± 100 mV	0.230 V ± 20 mV	1.0 s	Available
S-8232APFT-T2-x	4.28 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	2.90 V ± 100 mV	0.100 V ± 20 mV	1.0 s	Unavailable
S-8232ARFT-T2-x	4.325 V ± 25 mV	4.325 V ± 25 mV*1 *3	2.00 V ± 80 mV	2.50 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Unavailable
S-8232ASFT-T2-x*4	4.295 V ± 25 mV	4.20 V ± 50 mV*3	2.30 V ± 80 mV	3.00 V ± 100 mV	0.300 V ± 20 mV	1.0 s	Unavailable
S-8232ATFT-T2-x	4.125 V ± 25 mV	4.125 V ± 25 mV*1	2.00 V ± 80 mV	3.00 V ± 100 mV	0.190 V ± 20 mV	1.0 s	Available
S-8232AUFT-T2-x	4.30 V ± 25 mV	4.10 V ± 50 mV	2.40 V ± 80 mV	3.00 V ± 100 mV	0.200 V ± 20 mV	1.0 s	Unavailable
S-8232AVFT-T2-x	4.30 V ± 25 mV	4.05 V ± 50 mV	2.00 V ± 80 mV	3.00 V ± 100 mV	0.300 V ± 20mV	1.0 s	Available
S-8232AWFT-T2-x	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.150 V ± 20 mV	1.0 s	Unavailable
S-8232AXFT-T2-x	4.325 V ± 25 mV	4.200 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.20 V ± 20 mV	1.0 s	Unavailable
S-8232AYFT-T2-x	4.30 V ± 25 mV	4.05 V ± 50 mV	2.00 V ± 80 mV	2.00 V ± 80 mV	0.20 V ± 20 mV	1.0 s	Available
S-8232AZFT-T2-x	4.30 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	2.30 V ± 80 mV	0.20 V ± 20 mV	1.0 s	Available
S-8232NAFT-T2-x	4.325 V ± 25 mV	4.325 V ± 25 mV*1 *3	2.40 V ± 80 mV	3.00 V ± 100 mV	0.15 V ± 20 mV	1.0 s	Unavailable
S-8232NBFT-T2-x	4.35 V ± 25 mV	4.25 V ± 50 mV	3.00 V ± 80 mV	3.70 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Unavailable
S-8232NCFT-T2-x	4.275 V ± 25 mV	4.05 V ± 50 mV	2.20 V ± 80 mV	3.00 V ± 100 mV	0.20 V ± 20 mV	1.0 s	Unavailable
S-8232NDFT-T2-x	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	2.30 V ± 80 mV	0.15 V ± 20 mV	1.0 s	Available
S-8232NEFT-T2-x	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.23 V ± 20 mV	1.0 s	Available
S-8232NFFT-T2-x	4.325 V ± 25 mV	4.1 V ± 50 mV*3	2.30 V ± 80 mV	2.90 V ± 100 mV	0.21 V ± 20 mV	1.0 s	Unavailable
S-8232NGFT-T2-x	4.35 V ± 25 mV	4.15 V ± 50 mV	2.60 V ± 80 mV	3.00 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Available
S-8232NHFT-T2-x	4.28 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	2.90 V ± 100 mV	0.11 V ± 20 mV	1.0 s	Unavailable
S-8232NIFT-T2-x	4.25 V ± 25 mV	4.05 V ± 50 mV*3	2.50 V ± 80 mV	3.00 V ± 100 mV	0.15 V ± 20 mV	1.0 s	Unavailable
S-8232NJFT-T2-x	4.28 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	2.90 V ± 100 mV	0.11 V ± 20 mV	1.0 s	Available
S-8232NKFT-T2-x	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	2.30 V ± 80 mV	0.12 V ± 20 mV	1.0 s	Available
S-8232NLFT-T2-x	4.30 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.23 V ± 20 mV	1.0 s	Available
S-8232NMFT-T2-x	4.28 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	2.90 V ± 100 mV	0.08 V ± 20 mV	1.0 s	Available

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Table 1 (2 / 2)

Product name	Overcharge detection voltage 1, 2 [V_{CU}]	Overcharge release voltage 1, 2 [V_{CD}]	Overdischarge detection voltage 1, 2 [V_{DD}]	Overdischarge release voltage1, 2 [V_{DU}]	Overcurrent detection voltage 1 [V_{IOV1}]	Overcharge detection delay time [t_{CU}] (C3 = 0.22 μF)	0 V battery charging function
S-8232NNFT-T2-x	4.28 V ± 25 mV	4.08 V ± 50 mV*3	2.20 V ± 80 mV	2.40 V ± 100 mV	0.13 V ± 20 mV	1.0 s	Unavailable
S-8232NOFT-T2-x	4.295 V ± 25 mV	4.045 V ± 50 mV*3	2.20 V ± 80 mV	2.40 V ± 100 mV	0.13 V ± 20 mV	1.0 s	Unavailable
S-8232NPFT-T2-x	4.25 V ± 25 mV	4.05 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Unavailable
S-8232NQFT-T2-x	4.25 V ± 25 mV	4.05 V ± 50 mV	2.60 V ± 80 mV	3.00 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Unavailable
S-8232NRFT-T2-x	4.15 V ± 25 mV	3.95 V ± 50 mV	2.60 V ± 80 mV	3.00 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Unavailable
S-8232NSFT-T2-x	4.15 V ± 25 mV	3.95 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Unavailable
S-8232NTFT-T2-x	4.225 V ± 25 mV	4.15 V ± 50 mV	2.00 V ± 80 mV	2.00 V ± 80 mV	0.09 V ± 20 mV	1.0 s	Unavailable
S-8232NUFT-T2-x	3.85 V ± 25 mV	3.75 V ± 50 mV	2.23 V ± 80 mV	2.23 V ± 80 mV	0.15 V ± 20 mV	1.0 s	Available
S-8232NWFT-T2-x	4.21 V ± 25 mV	4.125 V ± 50 mV	2.00 V ± 80 mV	2.00 V ± 80 mV	0.09 V ± 20 mV	1.0 s	Unavailable
S-8232NXFT-T2-x	4.25 V ± 25 mV	4.05 V ± 50 mV	2.80 V ± 80 mV	3.10 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Unavailable
S-8232NYFT-T2-x	4.25 V ± 25 mV	4.15 V ± 50 mV	2.90 V ± 80 mV	3.10 V ± 100 mV	0.30 V ± 20 mV	1.0 s	Unavailable
S-8232NZFT-T2-x	4.21 V ± 25 mV	3.98 V ± 50 mV	2.30 V ± 80 mV	2.90 V ± 100 mV	0.11 V ± 20 mV	1.0 s	Unavailable
S-8232PAFT-T2-x	4.305 V ± 25 mV	4.125 V ± 50 mV	2.00 V ± 80 mV	2.00 V ± 80 mV	0.09 V ± 20 mV	1.0 s	Unavailable
S-8232PBFT-T2-y	4.35 V ± 25 mV	4.15 V ± 50 mV	2.30 V ± 80 mV	3.00 V ± 100 mV	0.20 V ± 20 mV	1.0 s	Unavailable
S-8232PCFT-T2-x	4.21 V ± 25 mV	4.00 V ± 50 mV	2.40 V ± 80 mV	3.00 V ± 100 mV	0.20 V ± 20 mV	1.0 s	Unavailable
S-8232PFFT-T2-U	4.225 V ± 25 mV	4.025 V ± 50 mV*2	2.70 V ± 80 mV	3.40 V ± 100 mV	0.15 V ± 20 mV	1.0 s	Unavailable

***1.** No overcharge detection / release hysteresis
***2.** The magnification of final overcharge is 1.11; the others are 1.25.
***3.** No final overcharging function
***4.** Refer to the ***2** in the "■ **Operation**".
(Overcharge detection/release hysteresis", "no final overcharge function", and "0 V battery charge inhibiting function)

Remark 1. Please contact our sales office for the products with detection voltage value other than those specified above.
2. x: G or U
y: S or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.
4. The overdischarge detection voltage can be selected within the range from 1.7 to 3.0 V. When the overdischarge detection voltage is higher than 2.6 V, the overcharge detection voltage and the overcharge release voltage are limited as "**Table 2**".

Table 2

Overdischarge detection voltage 1, 2 [V_{DD}]	Overcharge detection voltage 1, 2 [V_{CU}]	Voltage difference between overcharge detection voltage and overcharge release voltage [$V_{CU} - V_{CD}$]
1.70 V to 2.60 V	3.85 V to 4.60 V	0 V to 0.30 V
1.70 V to 2.80 V	3.85 V to 4.60 V	0 V to 0.20 V
1.70 V to 3.00 V	3.85 V to 4.50 V	0 V to 0.10 V

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■ Pin Configuration

8-Pin TSSOP
Top view

Figure 2

Table 3

Pin No.	Symbol	Description
1	SENS	Detection pin for voltage between VC and SENS (Detection pin for overcharge and overdischarge)
2	DO	FET gate connection pin for discharge control (CMOS output)
3	CO	FET gate connection pin for charge control (CMOS output)
4	VM	Detection pin for voltage between VSS and VM (Overcurrent detection pin)
5	VSS	Input pin for negative power supply
6	ICT	Capacitor connection pin for detection delay
7	VC	Input pin for middle voltage
8	VCC	Input pin for positive power supply

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■ Absolute Maximum Ratings

Table 4

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VCC and VSS	V_{DS}	VCC	V_{SS} − 0.3 to V_{SS} + 18	V
SENS input pin voltage	V_{SENS}	SENS	V_{SS} − 0.3 to V_{CC} + 0.3	V
ICT input pin voltage	V_{ICT}	ICT	V_{SS} − 0.3 to V_{CC} + 0.3	V
VM input pin voltage	V_{VM}	VM	V_{CC} − 18 to V_{CC} + 0.3	V
DO output pin voltage	V_{DO}	DO	V_{SS} − 0.3 to V_{CC} + 0.3	V
CO output pin voltage	V_{CO}	CO	V_{VM} − 0.3 to V_{CC} + 0.3	V
Power dissipation	P_D	—	300 (When not mounted on board)	mW
			700*1	mW
Operating ambient temperature	T_{opr}	—	− 40 to + 85	°C
Storage temperature	T_{stg}	—	− 40 to + 125	°C

***1.** When mounted on board

[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

Figure 3 Power Dissipation of Package (When Mounted on Board)

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■ Electrical Characteristics

Table 5

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DETECTION VOLTAGE								
Overcharge detection voltage 1, 2	$V_{CU1,2}$	3.85 V to 4.60 V, Adjustable	$V_{CU1,2}$ − 0.025	$V_{CU1,2}$	$V_{CU1,2}$ + 0.025	V	1, 2	1
Auxiliary overcharge detection voltage 1, 2 *1 V_{CUaux1}, V_{CUaux2} = V_{CU1}, V_{CU2} × 1.25 or V_{CUaux1}, V_{CUaux2} = V_{CU1}, V_{CU2} × 1.11	$V_{CUaux1,2}$	$V_{CU1,2}$ × 1.25	$V_{CU1,2}$ × 1.21	$V_{CU1,2}$ × 1.25	$V_{CU1,2}$ × 1.29	V	1, 2	1
	$V_{CUaux1,2}$	$V_{CU1,2}$ × 1.11	$V_{CU1,2}$ × 1.07	$V_{CU1,2}$ × 1.11	$V_{CU1,2}$ × 1.15	V	1, 2	1
Overcharge release voltage 1, 2	$V_{CD1,2}$	3.60 V to 4.60 V, Adjustable	$V_{CD1,2}$ − 0.050	$V_{CD1,2}$	$V_{CD1,2}$ + 0.050	V	1, 2	1
Overdischarge detection voltage 1, 2	$V_{DD1,2}$	1.70 V to 2.60 V, Adjustable	$V_{DD1,2}$ − 0.080	$V_{DD1,2}$	$V_{DD1,2}$ + 0.080	V	1, 2	1
Overdischarge release voltage 1, 2	$V_{DU1,2}$	1.70 V to 3.80 V, Adjustable	$V_{DU1,2}$ − 0.100	$V_{DU1,2}$	$V_{DU1,2}$ + 0.100	V	1, 2	1
Overcurrent detection voltage 1	V_{IOV1}	0.07 V to 0.30 V, Adjustable	V_{IOV1} − 0.020	V_{IOV1}	V_{IOV1} + 0.020	V	3	1
Overcurrent detection voltage 2	V_{IOV2}	Load short circuit, V_{CC} reference	− 1.57	− 1.20	− 0.83	V	3	1
Temperature coefficient 1 for detection voltage *2	T_{COE1}	Ta = − 40°C to + 85°C *4	− 0.6	0	0.6	mV/°C	—	—
Temperature coefficient 2 for detection voltage *3	T_{COE2}	Ta = − 40°C to + 85°C *4	− 0.24	− 0.05	0	mV/°C	—	—
DELAY TIME (C3 = 0.22 µF)								
Overcharge detection delay time 1, 2	$t_{CU1,2}$	1.0 s	0.73	1.00	1.35	s	8, 9	5
Overdischarge detection delay time 1, 2	$t_{DD1,2}$	0.1 s	68	100	138	ms	8, 9	5
Overcurrent detection delay time 1	t_{IOV1}	0.01 s	6.7	10	13.9	ms	10	5
INPUT VOLTAGE								
Input voltage between VCC and VSS	V_{DS}	Absolute maximum rating	− 0.3	—	18	V	—	—
OPERATING VOLTAGE								
Operating voltage between VCC and VSS *5	V_{DSOP}	Output logic fixed	2.0	—	16	V	—	—
CURRENT CONSUMPTION								
Current consumption during normal operation	I_{OPE}	V1 = V2 = 3.6 V	2.1	7.5	12.7	µA	4	2
Current consumption at power down	I_{PDN}	V1 = V2 = 1.5 V	0	0.0002	0.04	µA	4	2
OUTPUT VOLTAGE								
DO voltage "H"	$V_{DO(H)}$	I_{OUT} = 10 µA	V_{CC} − 0.05	V_{CC} − 0.003	V_{CC}	V	6	3
DO voltage "L"	$V_{DO(L)}$	I_{OUT} = 10 µA	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.05	V	6	3
CO voltage "H"	$V_{CO(H)}$	I_{OUT} = 10 µA	V_{CC} − 0.15	V_{CC} − 0.019	V_{CC}	V	7	4
CO PIN INTERNAL RESISTANCE								
Resistance between VM and CO	R_{COL}	V_{CO} − V_{VM} = 9.4 V	0.29	0.6	1.44	MΩ	7	4
INTERNAL RESISTANCE								
Resistance between VCC and VM	R_{VCM}	V_{CC} − V_{VM} = 0.5 V	105	240	575	kΩ	5	2
Resistance between VSS and VM	R_{VSM}	V_{VM} − V_{SS} = 1.1 V	511	597	977	kΩ	5	2
0 V BATTERY CHARGE FUNCTION								
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charging function "available"	0.38	0.75	1.12	V	11	6
0 V battery charge inhibition battery voltage 1, 2	$V_{0INH1,2}$	0 V battery charging function "unavailable"	0.32	0.88	1.44	V	12, 13	6

***1.** Auxiliary overcharge detection voltage is equal to the overcharge detection voltage times 1.11 for the products without overcharge hysteresis, and times 1.25 for other products.

***2.** Temperature coefficient 1 for detection voltage should be applied to overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.

***3.** Temperature coefficient 2 for detection voltage should be applied to overcurrent detection voltage.

***4.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

***5.** The DO and CO pin logic are established at the operating voltage.

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Table 6

(Ta = − 20°C to + 70°C unless otherwise specified *1)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DETECTION VOLTAGE								
Overcharge detection voltage 1, 2	$V_{CU1, 2}$	3.85 V to 4.60 V, Adjustable	$V_{CU1, 2}$ − 0.045	$V_{CU1, 2}$	$V_{CU1, 2}$ + 0.040	V	1, 2	1
Auxiliary overcharge detection voltage 1, 2 *2 V_{CUaux1}, V_{CUaux2} = V_{CU1}, V_{CU2} × 1.25 or V_{CUaux1}, V_{CUaux2} = V_{CU1}, V_{CU2} × 1.11	$V_{CUaux1, 2}$	$V_{CU1, 2}$ × 1.25	$V_{CU1, 2}$ × 1.19	$V_{CU1, 2}$ × 1.25	$V_{CU1, 2}$ × 1.31	V	1, 2	1
	$V_{CUaux1, 2}$	$V_{CU1, 2}$ × 1.11	$V_{CU1, 2}$ × 1.05	$V_{CU1, 2}$ × 1.11	$V_{CU1, 2}$ × 1.17	V	1, 2	1
Overcharge release voltage 1, 2	$V_{CD1, 2}$	3.60 V to 4.60 V, Adjustable	$V_{CD1, 2}$ − 0.070	$V_{CD1, 2}$	$V_{CD1, 2}$ + 0.065	V	1, 2	1
Overdischarge detection voltage 1, 2	$V_{DD1, 2}$	1.70 V to 2.60 V, Adjustable	$V_{DD1, 2}$ − 0.100	$V_{DD1, 2}$	$V_{DD1, 2}$ + 0.095	V	1, 2	1
Overdischarge release voltage 1, 2	$V_{DU1, 2}$	1.70 V to 3.80 V, Adjustable	$V_{DU1, 2}$ − 0.120	$V_{DU1, 2}$	$V_{DU1, 2}$ + 0.115	V	1, 2	1
Overcurrent detection voltage 1	V_{IOV1}	0.07 V to 0.30 V, Adjustable	V_{IOV1} − 0.029	V_{IOV1}	V_{IOV1} + 0.029	V	3	1
Overcurrent detection voltage 2	V_{IOV2}	Load short circuit, V_{CC} reference	− 1.66	− 1.20	− 0.74	V	3	1
Temperature coefficient 1 for detection voltage *3	T_{COE1}	Ta = − 40°C to + 85°C *1	− 0.6	0	0.6	mV/°C	—	—
Temperature coefficient 2 for detection voltage *4	T_{COE2}	Ta = − 40°C to + 85°C *1	− 0.24	− 0.05	0	mV/°C	—	—
DELAY TIME (C3 = 0.22 μF)								
Overcharge detection delay time 1, 2	$t_{CU1, 2}$	1.0 s	0.60	1.00	1.84	s	8, 9	5
Overdischarge detection delay time 1, 2	$t_{DD1, 2}$	0.1 s	67	100	140	ms	8, 9	5
Overcurrent detection delay time 1	t_{IOV1}	0.01 s	6.5	10	14.5	ms	10	5
INPUT VOLTAGE								
Input voltage between VCC and VSS	V_{DS}	Absolute maximum rating	− 0.3	—	18	V	—	—
OPERATING VOLTAGE								
Operating voltage between VCC and VSS *5	V_{DSOP}	Output logic fixed	2.0	—	16	V	—	—
CURRENT CONSUMPTION								
Current consumption during normal operation	I_{OPE}	V1 = V2 = 3.6 V	1.9	7.5	13.8	μA	4	2
Current consumption at power down	I_{PDN}	V1 = V2 = 1.5 V	0	0.0002	0.06	μA	4	2
OUTPUT VOLTAGE								
DO voltage "H"	$V_{DO(H)}$	I_{OUT} = 10 μA	V_{CC} − 0.14	V_{CC} − 0.003	V_{CC}	V	6	3
DO voltage "L"	$V_{DO(L)}$	I_{OUT} = 10 μA	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.14	V	6	3
CO voltage "H"	$V_{CO(H)}$	I_{OUT} = 10 μA	V_{CC} − 0.24	V_{CC} − 0.019	V_{CC}	V	7	4
CO PIN INTERNAL RESISTANCE								
Resistance between VM and CO	R_{COL}	V_{CO} − V_{VM} = 9.4 V	0.24	0.6	1.96	MΩ	7	4
INTERNAL RESISTANCE								
Resistance between VCC and VM	R_{VCM}	V_{CC} − V_{VM} = 0.5 V	86	240	785	kΩ	5	2
Resistance between VSS and VM	R_{VSM}	V_{VM} − V_{SS} = 1.1 V	418	597	1332	kΩ	5	2
0 V BATTERY CHARGE FUNCTION								
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charging function "available"	0.29	0.75	1.21	V	11	6
0 V battery charge inhibition battery voltage 1, 2	$V_{0INH1, 2}$	0 V battery charging function "unavailable"	0.23	0.88	1.53	V	12, 13	6

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

***2.** Auxiliary overcharge detection voltage is equal to the overcharge detection voltage times 1.11 for the products without overcharge hysteresis, and times 1.25 for other products.

***3.** Temperature coefficient 1 for detection voltage should be applied to overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.

***4.** Temperature coefficient 2 for detection voltage should be applied to overcurrent detection voltage.

***5.** The DO pin and CO pin logic are established at the operating voltage.

NOT RECOMMENDED FOR NEW DESIGN

Table 7

(Ta = – 40°C to +85°C unless otherwise specified *1)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
DETECTION VOLTAGE								
Overcharge detection voltage 1, 2	$V_{CU1,2}$	3.85 V to 4.60 V, Adjustable	$V_{CU1,2}$ – 0.055	$V_{CU1,2}$	$V_{CU1,2}$ + 0.045	V	1, 2	1
Auxiliary overcharge detection voltage 1, 2 *2 V_{CUaux1}, V_{CUaux2} = V_{CU1}, V_{CU2} × 1.25 or V_{CUaux1}, V_{CUaux2} = V_{CU1}, V_{CU2} × 1.11	$V_{CUaux1,2}$	$V_{CU1,2}$ × 1.25	$V_{CU1,2}$ × 1.19	$V_{CU1,2}$ × 1.25	$V_{CU1,2}$ × 1.31	V	1, 2	1
	$V_{CUaux1,2}$	$V_{CU1,2}$ × 1.11	$V_{CU1,2}$ × 1.05	$V_{CU1,2}$ × 1.11	$V_{CU1,2}$ × 1.17	V	1, 2	1
Overcharge release voltage 1, 2	$V_{CD1,2}$	3.60 V to 4.60 V, Adjustable	$V_{CD1,2}$ – 0.080	$V_{CD1,2}$	$V_{CD1,2}$ + 0.070	V	1, 2	1
Overdischarge detection voltage 1, 2	$V_{DD1,2}$	1.70 V to 2.60 V, Adjustable	$V_{DD1,2}$ – 0.110	$V_{DD1,2}$	$V_{DD1,2}$ + 0.100	V	1, 2	1
Overdischarge release voltage 1, 2	$V_{DU1,2}$	1.70 V to 3.80 V, Adjustable	$V_{DU1,2}$ – 0.130	$V_{DU1,2}$	$V_{DU1,2}$ + 0.120	V	1, 2	1
Overcurrent detection voltage 1	V_{IOV1}	0.07 V to 0.30 V, Adjustable	V_{IOV1} – 0.033	V_{IOV1}	V_{IOV1} + 0.033	V	3	1
Overcurrent detection voltage 2	V_{IOV2}	Load short circuit, V_{CC} reference	– 1.70	– 1.20	– 0.71	V	3	1
Temperature coefficient 1 for detection voltage *3	T_{COE1}	Ta = – 40°C to + 85°C *1	– 0.6	0	0.6	mV/°C	—	—
Temperature coefficient 2 for detection voltage *4	T_{COE2}	Ta = – 40°C to + 85°C *1	– 0.24	– 0.05	0	mV/°C	—	—
DELAY TIME (C3 = 0.22 µF)								
Overcharge detection delay time 1, 2	$t_{CU1,2}$	1.0 s	0.55	1.00	2.06	s	8, 9	5
Overdischarge detection delay time 1, 2	$t_{DD1,2}$	0.1 s	67	100	141	ms	8, 9	5
Overcurrent detection delay time 1	t_{IOV1}	0.01 s	6.3	10	14.7	ms	10	5
INPUT VOLTAGE								
Input voltage between VCC and VSS	V_{DS}	Absolute maximum rating	– 0.3	—	18	V	—	—
OPERATING VOLTAGE								
Operating voltage between VCC and VSS *5	V_{DSOP}	Output logic fixed	2.0	—	16	V	—	—
CURRENT CONSUMPTION								
Current consumption during normal operation	I_{OPE}	V1 = V2 = 3.6 V	1.8	7.5	14.2	µA	4	2
Current consumption at power down	I_{PDN}	V1 = V2 = 1.5 V	0	0.0002	0.10	µA	4	2
OUTPUT VOLTAGE								
DO voltage "H"	$V_{DO(H)}$	I_{OUT} = 10 µA	V_{CC} – 0.17	V_{CC} – 0.003	V_{CC}	V	6	3
DO voltage "L"	$V_{DO(L)}$	I_{OUT} = 10 µA	V_{SS}	V_{SS} + 0.003	V_{SS} + 0.17	V	6	3
CO voltage "H"	$V_{CO(H)}$	I_{OUT} = 10 µA	V_{CC} – 0.27	V_{CC} – 0.019	V_{CC}	V	7	4
CO PIN INTERNAL RESISTANCE								
Resistance between VM and CO	R_{COL}	V_{CO} – V_{VM} = 9.4 V	0.22	0.6	2.20	MΩ	7	4
INTERNAL RESISTANCE								
Resistance between VCC and VM	R_{VCM}	V_{CC} – V_{VM} = 0.5 V	79	240	878	kΩ	5	2
Resistance between VSS and VM	R_{VSM}	V_{VM} – V_{SS} = 1.1 V	387	597	1491	kΩ	5	2
0 V BATTERY CHARGE FUNCTION								
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charging function "available"	0.26	0.75	1.25	V	11	6
0 V battery charge inhibition battery voltage 1, 2	$V_{0INH1,2}$	0 V battery charging function "unavailable"	0.20	0.88	1.57	V	12, 13	6

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.
***2.** Auxiliary overcharge detection voltage is equal to the overcharge detection voltage times 1.11 for the products without overcharge hysteresis, and times 1.25 for other products.
***3.** Temperature coefficient 1 for detection voltage should be applied to overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.
***4.** Temperature coefficient 2 for detection voltage should be applied to overcurrent detection voltage.
***5.** The DO pin and CO pin logic are established at the operating voltage.

NOT RECOMMENDED FOR NEW DESIGN

■ Test Circuits

(1) Test Condition 1, Test Circuit 1

Set S1 = OFF, V1 = V2 = 3.6 V, and V3 = 0 V under normal status. Increase V1 from 3.6 V gradually. The V1 voltage when CO = "L" is overcharge detection voltage 1 (V_{CU1}). Decrease V1 gradually. The V1 voltage when CO = "H" is overcharge release voltage 1 (V_{CD1}). Further decrease V1. The V1 voltage when DO = "L" is overdischarge voltage 1 (V_{DD1}). Increase V1 gradually. The V1 voltage when DO = "H" is overdischarge release voltage 1 (V_{DU1}). Set S1 = ON, and V1 = V2 = 3.6 V and V3 = 0 V under normal status. Increase V1 from 3.6 V gradually. The V1 voltage when CO = "L" is auxiliary overcharge detection voltage 1 (V_{CUaux1}).

(2) Test Condition 2, Test Circuit 1

Set S1 = OFF, V1 = V2 = 3.6 V, and V3 = 0 V under normal status. Increase V2 from 3.6 V gradually. The V2 voltage when CO = "L" is overcharge detection voltage 2 (V_{CU2}). Decrease V2 gradually. The V2 voltage when CO = "H" is overcharge release voltage 2 (V_{CD2}). Further decrease V2. The V2 voltage when DO = "L" is overdischarge voltage 2 (V_{DD2}). Increase V2 gradually. The V2 voltage when DO = "H" is overdischarge release voltage 2 (V_{DU2}). Set S1 = ON, and V1 = V2 = 3.6 V and V3 = 0 V under normal status. Increase V2 from 3.6 V gradually. The V2 voltage when CO = "L" is auxiliary overcharge detection voltage 2 (V_{CUaux2}).

(3) Test Condition 3, Test Circuit 1

Set S1 = OFF, V1 = V2 = 3.6 V, and V3 = 0 V under normal status. Increase V3 from 0 V gradually. The V3 voltage when DO = "L" is overcurrent detection voltage 1 (V_{IOV1}). Set S1 = ON, V1 = V2 = 3.6 V, V3 = 0 under normal status. Increase V3 from 0 V gradually. (The voltage change rate < 1.0 V / ms) V3 – (V1 + V2) voltage when DO = "L" is overcurrent detection voltage 2 (V_{IOV2}).

(4) Test Condition 4, Test Circuit 2

Set S1 = ON, V1 = V2 = 3.6 V, and V3 = 0 V under normal status and measure current consumption. Current consumption I1 is the normal status current consumption (I_{OPE}). Set S1 = OFF, V1 = V2 = 1.5 V under overdischarge status and measure current consumption. Current consumption I1 is the power-down current consumption (I_{PDN}).

(5) Test Condition 5, Test Circuit 2

Set S1 = ON, V1 = V2 = V3 = 1.5 V, and V3 = 2.5 V under overdischarge status. (V1 + V2 – V3) / I2 is the internal resistance between VCC and VM (RVCM).
Set S1 = ON, V1 = V2 = 3.6 V, and V3 = 1.1 V under overcurrent status. V3 / I2 is the internal resistance between VSS and VM (RVSM).

(6) Test Condition 6, Test Circuit 3

Set S1 = ON, S2 = OFF, V1 = V2 = 3.6 V, and V3 = 0 V under normal status. Increase V4 from 0 V gradually. The V4 voltage when I1 = 10 μA is DO voltage "H" ($V_{DO(H)}$).
Set S1 = OFF, S2 = ON, V1 = V2 = 3.6 V, and V3 = 0.5 V under overcurrent status. Increase V5 from 0 V gradually. The V5 voltage when I2 = 10 μA is the DO voltage "L" ($V_{DO(L)}$).

NOT RECOMMENDED FOR NEW DESIGN

(7) Test Condition 7, Test Circuit 4

Set S1 = ON, S2 = OFF, V1 = V2 = 3.6 V and V3 = 0 V under normal status. Increase V4 from 0 V gradually. The V4 voltage when I1 = 10 μA is the CO "H" voltage ($V_{CO(H)}$).
Set S1 = OFF, S2 = ON, V1 = V2 = 4.7, V3 = 0 V, and V5 = 9.4 V under overcharge status. (V5) / I2 is the internal resistance between VM and CO (RCOL).

(8) Test Condition 8, Test Circuit 5

Set V1 = V2 = 3.6 V, and V3 = 0 V under normal status. Increase V1 from (V_{CU1} − 0.2 V) to (V_{CU1} + 0.2 V) immediately (within 10 μs). The time after V1 becomes (V_{CU1} + 0.2 V) until CO goes "L" is the overcharge detection delay time 1 (t_{CU1}).
Set V1 = V2 = 3.6 V, and V3 = 0 V under normal status. Decrease V1 from (V_{DD1} + 0.2 V) to (V_{DD1} − 0.2 V) immediately (within 10 μs). The time after V1 becomes (V_{DD1} − 0.2 V) until DO goes "L" is the overdischarge detection delay time 1 (t_{DD1}).

(9) Test Condition 9, Test Circuit 5

Set V1 = V2 = 3.6 V, and V3 = 0 V under normal status. Increase V2 from (V_{CU2} − 0.2 V) to (V_{CU2} + 0.2 V) immediately (within 10 μs). The time after V2 becomes (V_{CU2} + 0.2 V) until CO goes "L" is the overcharge detection delay time 2 (t_{CU2}).
Set V1 = V2 = 3.6 V, and V3 = 0 V under normal status. Decrease V2 from (V_{DD2} + 0.2 V) to (V_{DD2} − 0.2 V) immediately (within 10 μs). The time after V2 becomes (V_{DD2} − 0.2 V) until DO goes "L" is the overdischarge detection delay time 2 (t_{DD2}).

(10) Test Condition 10, Test Circuit 5

Set V1 = V2 = 3.6 V, and V3 = 0 V under normal status. Increase V3 from 0 V to 0.5 V immediately (within 10 μs). The time after V3 becomes 0.5 V until DO goes "L" is the overcurrent detection delay time 1 (t_{IOV1}).

(11) Test Condition 11, Test Circuit 6

Set V1 = V2 = 0 V, and V3 = 0 V, and increase V3 gradually. The V3 voltage when CO = "L" (V_{VM} + 0.3 V or higher) is the 0 V charge starting voltage (V_{0CHA}).

(12) Test Condition 12, Test Circuit 6

Set V1 = 0 V, V2 = 3.6 V, and V3 = 12 V, and increase V1 gradually. The V1 voltage when CO = "H" (V_{VM} + 0.3 V or higher) is the 0 V charge inhibiting voltage 1 (V_{0INH1}).

(13) Test Condition 13, Test Circuit 6

Set V1 = 3.6 V, V2 = 0 V, and V3 = 12 V, and increase V2 gradually. The V2 voltage when CO = "H" (V_{VM} + 0.3 V or higher) is the 0 V charge inhibiting voltage 2 (V_{0INH2}).

NOT RECOMMENDED FOR NEW DESIGN

Test Circuit 1

Test Circuit 2

Test Circuit 3

Test Circuit 4

Test Circuit 5

Test Circuit 6

Figure 4

NOT RECOMMENDED FOR NEW DESIGN

■ Operation

Remark Refer to "■ **Battery Protection IC Connection Example**".

Normal Status *1, *2

This IC monitors the voltages of the two serially connected batteries and the discharge current to control charging and discharging. When the voltages of two batteries are more than the overdischarge detection voltage ($V_{DD1, 2}$), less than the overcharge detection voltage ($V_{CU1, 2}$), and the current flowing through the batteries becomes equal or lower than a specified value (the VM pin voltage is equal or lower than overcurrent detection voltage 1), the charging and discharging FETs are turned on. In this status, charging and discharging can be carried out freely. This is normal status. In this status, the VM and VSS pins are shorted by the RVSM resistor.

Overcurrent Status

When the discharging current becomes equal to or higher than a specified value (the VM pin voltage is equal to or higher than the overcurrent detection voltage1) during discharging under the normal status and it continues for the overcurrent detection delay time (t_{IOV1}) or longer, the discharging FET is turned off to stop discharging. This is overcurrent status. The VM and VSS pins are shorted by the RVSM resistor in this status. The charging FET is also turned off. While the discharging FET is off and a load is connected, the VM pin voltage is equal to the V_{CC} potential.
The overcurrent status returns to the normal status when impedance between the EB– and EB+ pins (refer to **Figure 8**) is 200 MΩ or higher, by action such as releasing the load. When the load is released, the VM pin, which is shorted to the VSS pin by the RVSM resistor, goes back to the V_{SS} potential. The IC detects that the VM pin potential returns to overcurrent detection voltage 1 (V_{IOV1}) or lower and returns to the normal status.

Overcharge Status

Following two cases are detected as overcharge status :

(1) If any of the battery voltages becomes higher than the overcharge detection voltage ($V_{CU1, 2}$) during charging under the normal status and it continues for the overcharge detection delay time ($t_{CU1, 2}$) or longer, the charging FET turns off to stop charging. This is overcharge status. In this status, the VM and VSS pins are shorted by the RVSM resistor.

(2) Although the status is shorter than the overcharge detection delay time ($t_{CU1, 2}$), if any of the battery voltages becomes higher than the auxiliary overcharge detection voltage ($V_{CUaux1, 2}$), the charging FET turns off to stop charging. This is also overcharge status. In this status, the VM and VSS pins are shorted by the RVSM resistor.

The auxiliary overcharge detection voltages ($V_{CUaux1, 2}$) are correlated with the overcharge detection voltages ($V_{CU1, 2}$) and are defined by following equations :

$V_{CUaux1, 2}$ [V] = 1.25 × $V_{CU1, 2}$ [V]
or $V_{CUaux1, 2}$ [V] = 1.11 × $V_{CU1, 2}$ [V]

The overcharge status is released in two cases :

(1) The battery voltage which exceeded the overcharge detection voltage ($V_{CU1, 2}$) falls below the overcharge release voltage ($V_{CD1, 2}$), the charging FET turns on and the IC returns to the normal status.

(2) If the battery voltage which exceeded the overcharge detection voltage ($V_{CU1, 2}$) is equal or higher than the overcharge release voltage ($V_{CD1, 2}$), however, discharging starts with removing the charger and connecting the load, the charging FET turns on and the IC returns to the normal status.

The mechanism to release is as follows: the discharge current flows via an internal parasitic diode of the charging FET, immediately after connecting the load and discharging starts. Therefore the VM pin's voltage momentarily increases about 0.6 V (voltage as much as V_F voltage of the diode has) plus the VSS pin's voltage. The IC detects this voltage by using overcurrent detection voltage 1 (V_{IOV1}) so that the IC releases the overcharge status and returns to the normal status.

Overdischarge Status

If any of the battery voltages falls below the overdischarge detection voltage ($V_{DD1, 2}$) during discharging under the normal status and it continues for the overdischarge detection delay time ($t_{DD1, 2}$) or longer, the discharging FET turns off and discharging stops. This is overdischarge status. When the discharging FET turns off, the VM pin voltage becomes equal to the V_{CC} voltage and the IC's current consumption falls below the power-down current consumption (I_{PDN}). This is power-down status. The VM and VCC pins are shorted by the RVCM resistor in the overdischarge and power-down statuses.
The power-down status is released when the charger is connected and the voltage between VM and VCC is overcurrent detection voltage 2 or higher. In this status, When all the battery voltages becomes equal to or higher than the overdischarge release voltage ($V_{DU1, 2}$) in this status, The IC returns to the normal status from the overdischarge status.

NOT RECOMMENDED FOR NEW DESIGN

Delay Circuit

The overcharge detection delay time ($t_{CU1, 2}$), the overdischarge detection delay time ($t_{DD1, 2}$), and the overcurrent detection delay time 1 (t_{IOV1}) change with an external capacitor (C3). Since one capacitor determine each delay time, delay times are correlated as seen in the following ratio :

Overcharge delay time : Overdischarge delay time : Overcurrent delay time = 100 : 10 : 1

The delay times are calculated by the following equations : (Ta = – 40°C to + 85°C)

	Min.,	Typ.,	Max.	
Overcharge detection delay time t_{CU} [s] = Delay factor	(2.500,	4.545,	9.364)	× C3 [μF]
Overdischarge detection delay time t_{DD} [s] = Delay factor	(0.3045,	0.4545,	0.6409)	× C3 [μF]
Overcurrent detection delay time t_{IOV1} [s] = Delay factor	(0.02864,	0.04545,	0.06682)	× C3 [μF]

Remark The overcurrent detection delay time 2 is not set Overcurrent detection voltage 2 (V_{IOV2}).

0 V Battery Charging Function *3

This function is used to recharge both of two serially-connected batteries after they self-discharge to 0 V. When the 0 V charging start voltage (V_{0CHA}) or higher is applied to between VM and VCC by connecting the charger, the charging FET gate is fixed to V_{CC} potential.

When the voltage between the gate and the source of the charging FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging FET turns on to start charging. At this time, the discharging FET turns off and the charging current flows through the internal parasitic diode in the discharging FET. If all the battery voltages become equal to or higher than the overdischarge release voltage ($V_{DU1, 2}$), the IC returns to the normal status.

0 V Battery Charge Inhibiting Function *3

This function is used for inhibiting charging after either of the connected batteries goes 0 V due to its self-discharge. When the voltage of either of the connected batteries goes below the 0 V charge inhibit voltage 1 and 2 ($V_{0INH1, 2}$), the charging FET gate is fixed to "EB–" to inhibit charging. Charging is possible only when the voltage of both connected batteries goes 0 V charge inhibit voltage 1 and 2 ($V_{0INH1, 2}$) or more.

Note that charging may be possible when the total voltage of both connected batteries is less than the minimum value ($V_{DSOPmin}$) of the operating voltage between VCC and VSS even if the voltage of either of the connected batteries is the 0 V charge inhibit voltage 1 and 2 ($V_{0INH1, 2}$) or less. Charging is inhibited when the total voltage of both connected batteries reaches the minimum value ($V_{DSOPmin}$) of the operating voltage between VCC and VSS.

When using this optional function, a resistor of 4.7 MΩ is needed between the gate and the source of the charging control FET (refer to **Figure 8**).

***1.** When connecting batteries for the first time, the IC may fail to enter the normal status (is not in the status to charge). If so, once set the VM pin to VSS voltage (short between VM and VSS or connect a charger) to return to the normal status.

***2.** In this product with "overcharge detection/release hysteresis", "no final overcharge function", and "0 V battery charge inhibiting function" (indicated in ***4**, in "**2. Product Name List**" in "■ **Product Name Structure**"), the following action, other products do not have, is seen. But it does not affect on actual use.

In the normal status, the battery voltage is the overcharge release voltage ($V_{CD1, 2}$) or higher, and the overcharge detection voltage ($V_{CU1, 2}$) or lower but after that, the IC goes in the overcurrent status by connecting an overload. Usually the IC returns to the normal status by detaching the overload, but the charging FET may turn off and the IC may go in the overcharge status. After that, connect the load again to start charging. The FET turns on and the IC returns to the normal status (Refer to "**Overcharge status**").

***3.** Some lithium ion batteries are not recommended to be recharged after having been completely discharged. Please contact battery manufacturer when you select a 0 V battery charging function.

NOT RECOMMENDED FOR NEW DESIGN

■ Timing Charts

1. Overcharge Detection

***1.** <1> Normal status
<2> Over charge status
<3> Over discharge status
<4> Over current status

Remark The charger is assumed to charge with a constant current.

Figure 5

NOT RECOMMENDED FOR NEW DESIGN

2. Overdischarge Detection

***1.** <1> Normal status
<2> Over charge status
<3> Over discharge status
<4> Over current status

Remark The charger is assumed to charge with a constant current.

Figure 6

NOT RECOMMENDED FOR NEW DESIGN

3. Overcurrent Detection

***1.** <1> Normal status
<2> Over charge status
<3> Over discharge status
<4> Over current status

Remark The charger is assumed to charge with a constant current.

Figure 7

NOT RECOMMENDED FOR NEW DESIGN

■ Battery Protection IC Connection Example

Figure 8

Table 8 Constants for External Components

Symbol	Parts	Purpose	Typ.	Min.	Max.	Remark
FET1	Nch MOS FET	Discharge control	—	—	—	—
FET2	Nch MOS FET	Charge control	—	—	—	—
R1	Chip resistor	ESD protection	1 kΩ	300 Ω	1 kΩ	—
C1	Chip capacitor	For power fluctuation	0.22 μF	0 μF	1 μF	—
R2	Chip resistor	ESD protection	1 kΩ	300 Ω	1 kΩ	—
C2	Chip capacitor	For power fluctuation	0.22 μF	0 μF	1 μF	—
R4	Chip resistor	ESD protection	1 kΩ	= R1 min.	= R1 max.	Same value as R1 and R2. *1
C3	Chip capacitor	Delay time setting	0.22 μF	0 μF	1 μF	Attention should be paid to leak current of C3. *2
R3	Chip resistor	Protection for charger reverse connection	1 kΩ	300 Ω	5 kΩ	Discharge can't be stopped at less than 300 Ω when a charger is reverse-connected. *3
R5	Chip resistor	0 V battery charging inhibition	(4.7 MΩ)	(1 MΩ)	(10 MΩ)	R5 should be added when the product has 0 V battery charge inhibition. Lower resistance increases current consumption. *4

***1.** R4 = R1 is required. Overcharge detection voltage increases by R4. For example 10 kΩ (R4) increases overcharge detection voltage by 20 mV.

***2.** The overcharge detection delay time (t_{CU}), the overdischarge detection delay time (t_{CD}), and the over current detection delay time (t_{IOV}) change with the external capacitor C3.

***3.** When the resistor R3 is set less than 300 Ω and a charger is reverse-connected, current which exceeds the power dissipation of the package will flow and the IC may break. But excessive R3 causes increase of overcurrent detection voltage 1 (V_{IOV1}). V_{IOV1} changes to $V_{IOV1} = (R3 + R_{VSM}) / R_{VSM} \times V_{IOV1}$. For example, 50 kΩ resistor (R3) increases overcurrent detection voltage 1 (V_{IOV1}) from 0.100 V to 0.113 V.

***4.** A 4.7 MΩ resistor is needed for R5 to inhibit 0 V battery charging. Current consumption increases when the R5 resistance is below 4.7 MΩ. R5 should be connected when the product has 0 V battery charging inhibition.

Caution 1. The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

NOT RECOMMENDED FOR NEW DESIGN

■ Precautions

- After the overcurrent detection delay, if either one of battery voltages equals the overdischarge detection voltage ($V_{DD1,2}$) or lower, the overdischarge detection delay time becomes shorter than 10ms (min.). It occurs because capacitor C3 sets all of delay times (refer to the **Figure 9**) .

Figure 9

[Cause]
When overcurrent detection is released until t_{IOV1}, the capacitor C3 is charged by S-8232 Series. If all battery voltage is lower than $V_{DD1,\ 2}$ at that time, charging goes on. So delay time is shorter than typical.

[Conclusion]
This phenomenon occurs when all battery voltage is nearly equal to the overdischarge voltage ($V_{DD1,\ 2}$) after overcurrent detected. It means that the battery capacity is small and those must be charged in the future. Even if the state changes to overdischarge status, the battery package capacity is same as typical.

- When one of the battery voltages is overdischarge detection voltage ($V_{DD1,\ 2}$) or lower and the other one becomes higher than the overcharge detection voltage ($V_{CU1,\ 2}$), the IC detects the overcharge without the overcharge detection delay time (t_{CU}) (refer to the **Figure 10**) .

Figure 10

[Cause]
It is same as the overdischarge detection under the overcurrent status. It occurs because capacitor C3 sets all of delay times.

[Conclusion]
This phenomenon occurs when one battery voltage is lower than overdischarge voltage ($V_{DD1,\ 2}$) and batteries are charged by charger. Since voltage difference between two batteries is large in this situation, the S-8232 Series immediately stops the charging of the other battery to reduce voltage difference. This action improves the safety of a battery pack and dose not do any harm to the pack.

NOT RECOMMENDED FOR NEW DESIGN

- After the overcurrent detection, the load was connected for a long time, even if one of the battery voltage became lower than overdischarge detection voltage ($V_{DD1, 2}$), the IC can't detects the overdischarge as long as the load is connected. Therefore the IC's current consumption at the one of the battery voltage is lower than the overdischarge detection voltage is same as normal status current consumption (I_{OPE}) (refer to the **Figure 11**).

Figure 11

[Cause]

The reason is as follows. If the overcurrent detection and overdischarge detection occur at same time, the overcurrent detection takes precedence the overdischarge detection. As long as the IC detects overcurrent, the IC can't detect overdischarge.

[Conclusion]

If the load is taken off at least one time, the overcurrent is released and the overdischarge detection works.

Unless keeping the IC with load for a long time, the reduction of battery voltage will be neglected, because of the IC's current consumption (typ. 7.5 μA) is small.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

NOT RECOMMENDED FOR NEW DESIGN

■ Characteristics (Typical Data)

1. Detection Voltage Temperature Characteristics

Overcharge detection voltage1 vs. temperature

Overcharge detection voltage2 vs. temperature

Overcharge release voltage1 vs. temperature

Overcharge release voltage2 vs. temperature

Auxiliary overcharge detection voltage1 vs. temperature

Auxiliary overcharge detection voltage2 vs. temperature

NOT RECOMMENDED FOR NEW DESIGN

Overdischarge detection voltage1 vs. temperature

Overdischarge detection voltage2 vs. temperature

Overdischarge release voltage1 vs. temperature

Overdischarge release voltage1 vs. temperature

Overcurrent1 detection voltage vs. temperature

Overcurrent1 detection voltage vs. temperature

NOT RECOMMENDED FOR NEW DESIGN

2. Current Consumption Temperature Characteristics

Current consumption vs. temperature in normal mode

Current consumption vs. temperature in power-down mode

3. Delay Time Temperature Characteristics

Overcharge detection1 time vs. temperature

Overcharge detection1 time vs. temperature

Overcurrent1 detection time vs. temperature

Caution Please design all applications of the S-8232 Series with safety in mind.

NOT RECOMMENDED FOR NEW DESIGN

NOT RECOMMENDED FOR NEW DESIGN

No. FT008-A-P-SD-1.1

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

NOT RECOMMENDED FOR NEW DESIGN

No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

Enlarged drawing in the central part

No. FT008-E-R-SD-1.0

NOT RECOMMENDED FOR NEW DESIGN

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

NOT RECOMMENDED FOR NEW DESIGN

SII
Seiko Instruments Inc.
www.sii-ic.com

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ABLIC:
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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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