ANALOG DEVICES

LC^{2}MOS
µP-Compatible 14-Bit DAC
AD7534

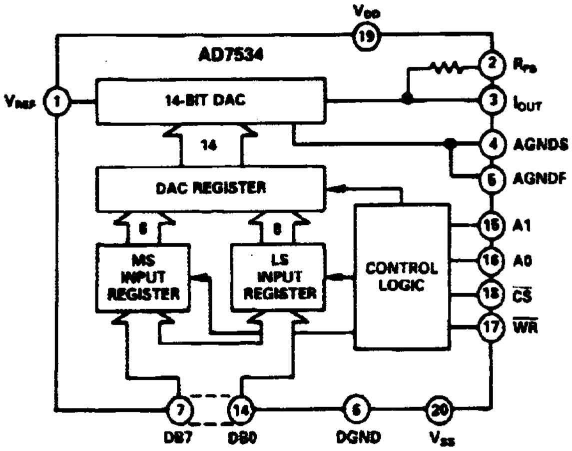
FEATURES

All Grades 14-Bit Monotonic Over the Full Temperature Range
Full 4-Quadrant Multiplication
Microprocessor-Compatible with Double Buffered Inputs
Exceptionally Low Gain Temperature Coefficient, 0.5ppm/°C typ
Small 20-Pin DIP and Surface Mount Package
Low Output Leakage (<20nA) Over the Full Temperature Range

APPLICATIONS

Microprocessor Based Control Systems
Digital Audio Reconstruction
High Precision Servo Control
Control and Measurement in High Temperature Environments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7534 is a 14-bit monolithic CMOS D/A converter which uses thin-film resistors and laser trimming to achieve excellent linearity.

The device is configured to accept right-justified data in two bytes from an 8-bit data bus. Standard Chip Select and Memory Write logic is used to access the DAC. Address lines A0 and A1 control internal register loading and transfer.

A novel low leakage configuration (patent pending) enables the AD7534 to exhibit excellent output leakage current characteristics over the specified temperature range.

The device is fully protected against CMOS "latch up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op amp. The AD7534 is manufactured using the Linear Compatible CMOS (LC^{2}MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Guaranteed Montonicity
   The AD7534 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Output Leakage
   By tying V_{SS} (Pin 20) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
3. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allows direct interfacing to most of the popular 8-bit and 16-bit microprocessors.
4. Monolithic Construction
   For increased reliability and reduced package size – 0.3" 20-pin DIP and 20-terminal surface mount package.

REV. A

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AD7534—SPECIFICATIONS[1] (V_{DD} = +11.4V to +15.75V[2], V_{REF} = +10V; V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV. All specifications T_{min} to T_{max} unless otherwise stated)

Parameter	J, A Versions	K, B Versions	S Version	T Version	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	over temperature.
Full Scale Error	±8	±4	±8	±4	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Gain Temperature Coefficient[3]						
ΔGain/ΔTemperature	±5	±2.5	±5	±2.5	ppm/°C max	Typical value is 0.5ppm/°C
Output Leakage Current I_{OUT} (Pin 3)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs 0V
T_{min} to T_{max}	±10	±10	±20	±20	nA max	V_{SS} = −300mV
T_{min} to T_{max}	±25	±25	±150	±150	nA max	V_{SS} = 0V
REFERENCE INPUT						
Input Resistance, Pin 1	3.5	3.5	3.5	3.5	kΩ min	Typical Input Resistance = 6kΩ
	10	10	10	10	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V min/V max	Specifications guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range.
I_{DD}	3	3	3	3	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test. (V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV, Output Amplifier is AD544 except where stated).

Parameter	V_{DD} = +11.4V to +15.75V		Units	Test Conditions/Comments
	T_A = 25°C	T_A = T_{min}, T_{max}		
Output Current Settling Time	1.5	–	μs max	To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time is 0.8μs.
Digital to Analog Glitch Impulse	100	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.
Multiplying Feedthrough Error[4]	3	5	mV p-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0's.
Power Supply Rejection				
ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 3)	260	260	pF max	DAC register loaded with all 1's
C_{OUT} (Pin 3)	130	130	pF max	DAC register loaded with all 0's
Output Noise Voltage Density (10Hz–100kHz)	15	–	nV/√Hz typ	Measured between R_{FB} and I_{OUT}

NOTES

[1] Temperature range as follows: J, K Versions: 0 to +70°C
A, B Versions: −25°C to +85°C
S, T Versions: −55°C to +125°C

[2] Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3] Guaranteed by Product Assurance testing.

[4] Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	Address Valid to Write Setup Time
t_2	0	0	0	ns min	Address Valid to Write Hold Time
t_3	140	160	180	ns min	Data Setup Time
t_4	20	20	30	ns min	Data Hold Time
t_5	0	0	0	ns min	Chip Select to Write Setup Time
t_6	0	0	0	ns min	Chip Select to Write Hold Time
t_7	170	200	240	ns min	Write Pulse Width

NOTES

[1] Temperature range as follows:

	J, K Versions:	0 to +70°C
	A, B Versions:	−25°C to +85°C
	S, T Versions:	−55°C to +125°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise stated)

V_{DD} (Pin 19) to DGND	−0.3V, +17V
V_{SS} (Pin 20) to AGND	−15V, +0.3V
V_{REF} (Pin 1) to AGND	±25V
V_{RFB} (Pin 2) to AGND	±25V
Digital Input Voltage (Pins 7–18) to DGND	−0.3V, V_{DD}
V_{PIN3} to DGND	−0.3V, V_{DD}
AGND to DGND	−0.3V, V_{DD}
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	
Commercial (J, K Versions)	0 to +70°C
Industrial (A, B Versions)	−25°C to +85°C
Extended (S, T Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

Model	Temperature Range	Relative Accuracy	Full Scale Error	Package Option*
AD7534JN	0°C to +70°C	±2LSB	±8LSB	N-20
AD7534KN	0°C to +70°C	±1LSB	±4LSB	N-20
AD7534JP	0°C to +70°C	±2LSB	±8LSB	P-20A
AD7534KP	0°C to +70°C	±LSB	±4LSB	P-20A
AD7534AQ	−25°C to +85°C	±2LSB	±8LSB	Q-20
AD7534BQ	−25°C to +85°C	±1LSB	±4LSB	Q-20
AD7534SQ	−55°C to +125°C	±2LSB	±8LSB	Q-20
AD7534TQ	−55°C to +125°C	±1LSB	±4LSB	Q-20

*N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full scale error and is normally expressed in Least Significant Bits or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1LSB max over the operating temperature range ensures monotonicity.

FULL-SCALE ERROR

Full scale error or gain error is a measure of the output error between an ideal DAC and the actual device output. Full scale error is adjustable to zero with an external potentiometer.

DIGITAL TO ANALOG GLITCH IMPULSE

The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. The measurement takes place with V_{REF} = AGND.

OUTPUT CAPACITANCE

Capacitance from I_{OUT} to AGND.

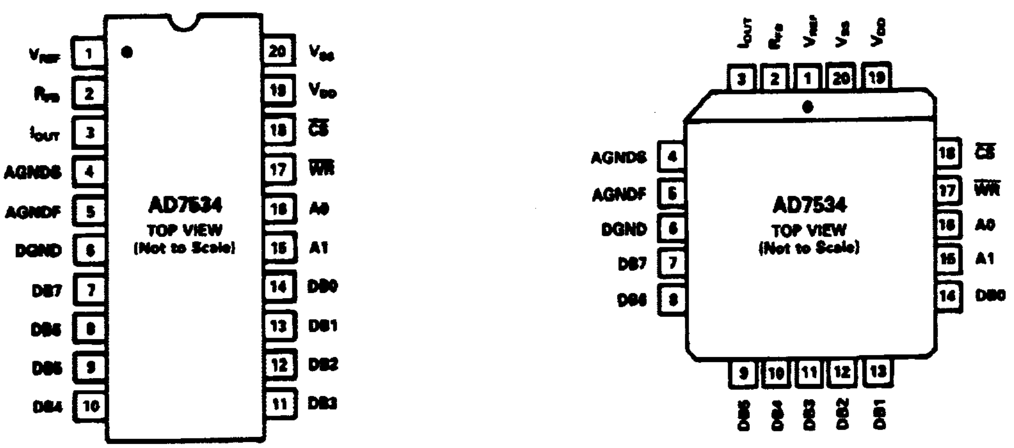
OUTPUT LEAKAGE CURRENT

Current which appears at I_{OUT} with the DAC register loaded to all 0's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to I_{OUT} with DAC register loaded to all zeros.

PIN CONFIGURATIONS



Pin Function Description — AD7534

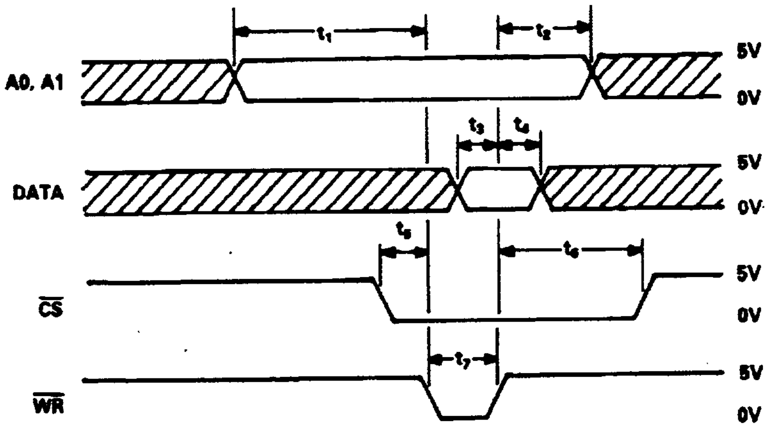
Pin	Function	Description
1	V_{REF}	Reference Input Voltage
2	R_{FB}	Feedback resistor. Used to close the loop around an external op-amp.
3	I_{OUT}	Current Output Terminal
4	AGNDS	Analog ground sense line. Reference point for external circuitry. This pin should carry minimal current.
5	AGNDF	Analog ground force line; carries current from internal analog ground connections. A_{GNDF} and A_{GNDS} are tied together internally.
6	DGND	Digital Ground
7	DB7	Data Bit 7
8	DB6	Data Bit 6
9	DB5	Data Bit 5 or Data Bit 13 (DAC MSB)
10	DB4	Data Bit 4 or Data Bit 12
11	DB3	Data Bit 3 or Data Bit 11
12	DB2	Data Bit 2 or Data Bit 10
13	DB1	Data Bit 1 or Data Bit 9
14	DB0	Data Bit 0 or Data Bit 8
15	A1	Address line 1
16	A0	Address line 0
17	$\overline{\text{WR}}$	Write input. Active low.
18	$\overline{\text{CS}}$	Chip Select Input. Active low.

$\overline{\text{WR}}$	$\overline{\text{CS}}$	A1	A0	Function
X[1]	1	X	X	Device not selected
1	X	X	X	No data transfer
0	0	0	0	DAC loaded directly from Data Bus[2]
0	0	0	1	MS Input Register loaded from Data Bus
0	0	1	0	LS Input Register loaded from Data Bus
0	0	1	1	DAC Register loaded from Input Registers.

NOTES

1. X = Don't Care
2. When $A_1 = 0$, $A_0 = 0$ all DAC registers are transparent, so by placing all 0's or all 1's on the data inputs the user can load the DAC to zero or full scale output in one write operation. This facility simplifies system calibration.

Pin	Function	Description
19	V_{DD}	+12V to +15V supply input.
20	V_{SS}	Bias pin for High Temperature Low Leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figures 4, 5 or 6 for recommended circuitry.



NOTES

1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. AD7534 Timing Diagram

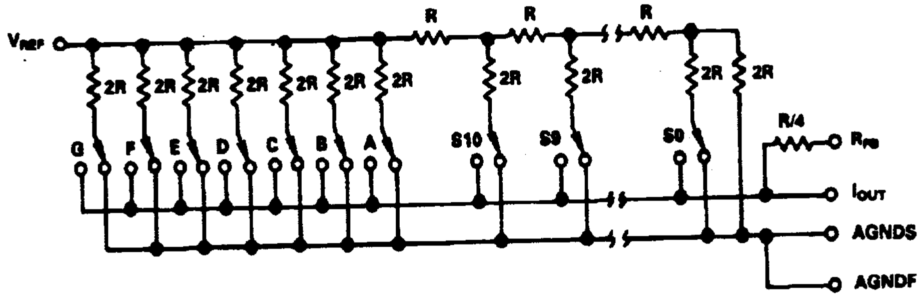


Figure 2. Simplified Circuit Diagram for the AD7534 D/A Section

CIRCUIT INFORMATION – D/A SECTION

Figure 2 shows a simplified circuit diagram for the AD7534 D/A section. The three MSB's of the 14-bit Data Word are decoded to drive the seven switches A-G. The 11 LSB's of the Data Word drive an inverted R-2R ladder which steers the binarily weighted current available to it between I_{OUT} and AGNDF.

If I is taken as the input current at V_{REF} the input current to the R-2R ladder is I/8. 7/8 I flows in the parallel ladder structure. Switches A-G steer binarily weighted current between I_{OUT} and AGNDF.

The input resistance at V_{REF} is constant and may be driven by a voltage source or a current source of positive or negative polarity.

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent circuit for the analog section of the AD7534 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R_O denotes the equivalent output resistance of the DAC which varies with input code. C_{OUT} is the capacitance due to the current steering switches and varies from about 90pF to 180pF (typical values) depending upon the digital input. $g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the transfer function of the R-2R ladder, N.

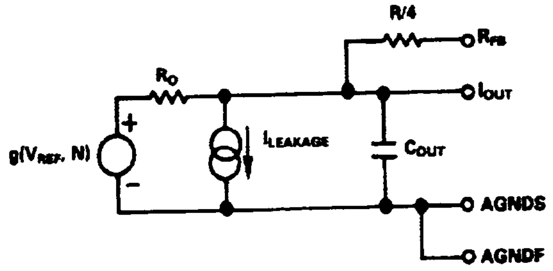


Figure 3. AD7534 Equivalent Analog Output Circuit

CIRCUIT INFORMATION – DIGITAL SECTION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from DGND to each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close as possible to 0 and 5V logic levels.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 4 is given in Table I.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high speed op-amps are used.

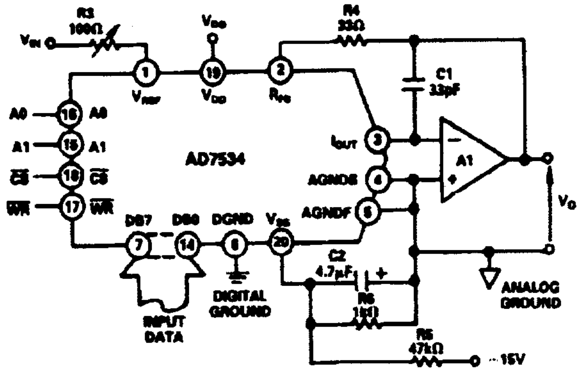


Figure 4. Unipolar Binary Operation

Binary Number In DAC Register	Analog Output, V_{OUT}
MSB LSB 11 1111 1111 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10 0000 0000 0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -1/2\,V_{IN}$
00 0000 0000 0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00 0000 0000 0000	0V

Table I. Unipolar Binary Code Table for AD7534

ZERO OFFSET AND GAIN ADJUSTMENT FOR FIGURE 4.

Calibration codes for zero and full scale adjust (all 0's, all 1's) can be loaded in one write operation (see Pin Function Description).

Zero Offset Adjustment

1. Load DAC register with all 0's.
2. Adjust offset of amplifier A1 so that V_O is at a minimum (i.e., ≤30µV).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R3 so that $V_O = -V_{IN}\left(\frac{16383}{16384}\right)$

In fixed reference applications full scale can also be adjusted by omitting R3 and R4 and trimming the reference voltage magnitude.

For high temperature applications, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7534, Gain Error trimming is not necessary.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used.

With the DAC loaded to 10 0000 0000 0000, adjust R3 for $V_O = 0V$. Alternatively, one can omit R3 and R4 and adjust the ratio of R7 and R8 for $V_O = 0V$. Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R9.

Resistors R7, R8 and R9 should be matched to 0.003%. Mismatch of R7 and R8 causes both offset and full scale error. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficient match.

The code table for Figure 5 is given in Table II.

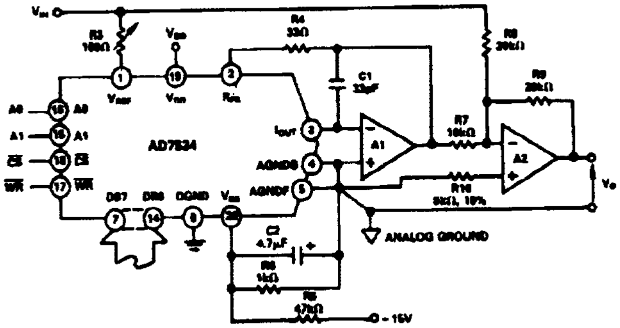


Figure 5. Bipolar Operation

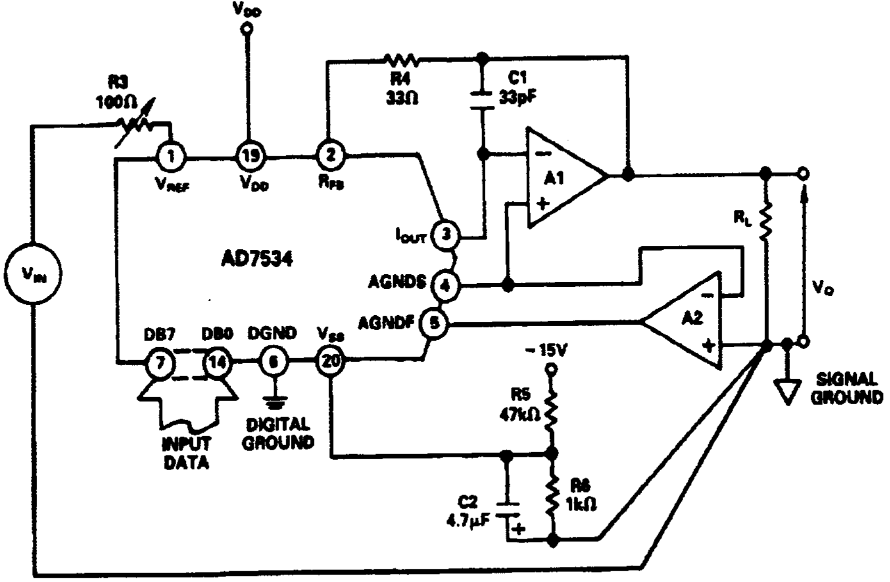
Binary Number in DAC Register MSB LSB	Analog Output
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0
01 1111 1111 1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right)$

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 5.

GROUNDING TECHNIQUES

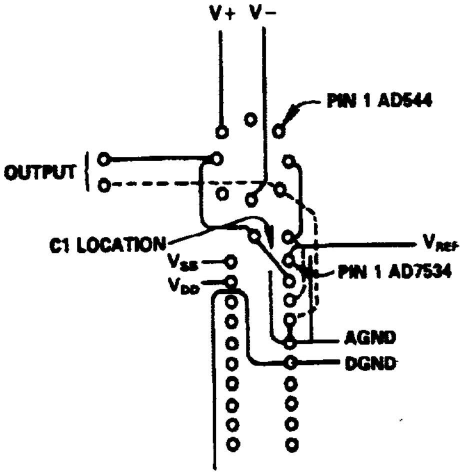
Since the AD7534 is specified for high accuracy, it is important to use a proper grounding technique. The two AGND pins (AGNDF and AGNDS) provide flexibility in this respect. In Figure 4, AGNDS and AGNDF are externally shorted and A2 is not used. Voltage drops due to bond wire resistances are not compensated for in this circuit. This means that an extra linearity error of less than 0.1LSB is added to the DAC linearity error. If the user wishes to eliminate this extra error, then the circuit of Figure 6 should be used. Here, A2 is used to maintain AGNDS at Signal Ground potential. By using the Force, Sense technique all switch contacts on the DAC are at exactly the same potential and any error due to bond wire resistance is eliminated.

Figure 7 shows a Printed Circuit Board layout for the AD7534 with a single output amplifier. The input to V_{REF} (pin 1) is shielded to reduce ac feedthrough while the digital inputs are shielded to minimize digital feedthrough. The tracks connecting I_{OUT} and AGNDS to the inverting and noninverting op amp inputs are kept as short as possible. Gain trim components, R3 and R4, have been omitted.



NOTE
CONTROL INPUTS OMITTED FOR CLARITY

Figure 6. Unipolar Binary Operation with Forced Ground



LAYOUT IS FOR DOUBLE SIDED PCB.
DOTTED LINE INDICATES TRACK ON COMPONENT SIDE.

Figure 7. Suggested Layout for AD7534 Incorporating Output Amplifier

ZERO OFFSET AND GAIN ADJUSTMENT FOR FIGURE 6

Zero Offset Adjustment

1. Load DAC register with all 0's.
2. Adjust offset of amplifier A2 for minimum potential at AGNDS. This potential should be ≤30μV with respect to Signal Ground.
3. Adjust offset of amplifier A1 so that V_O is at a minimum (i.e. ≤30μV).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R3 so that $V_O = -V_{IN}\left(\frac{16383}{16384}\right)$

LOW LEAKAGE CONFIGURATION

For CMOS Multiplying D/A converters, as the device is operated at higher temperatures the output leakage current increases. For a 14-bit resolution system, this can be a significant source of error. The AD7534 features a leakage reduction configuration to keep the leakage current low over an extended temperature range. One may operate the device with or without this configuration. If V_{SS} (pin 20) is tied to AGND then the DAC will exhibit normal output leakage current at high temperatures. To use the low leakage facility, V_{SS} should be tied to a voltage of approximately −0.3V as in Figures 4, 5 and 6. A simple resistor divider (R5, R6) produces −312mV from −15V. The capacitor C2 in parallel with R6 is an integral part of the low leakage configuration and must be 4.7μF or greater. Figure 8 is a plot of leakage current versus temperature for both conditions. It clearly shows the improvement gained by using the low leakage configuration.

OP AMP SELECTION

In choosing an amplifier to be used with the AD7534, three parameters are of prime importance. These are Input Offset Voltage (V_{OS}), Input Bias Current, (I_{BIAS}) and Offset Voltage Drift. To maintain specified accuracy with V_{REF} at 10V, V_{OS} must be less than 30μV while I_{BIAS} should be less than 2nA. Also the open loop gain of the amplifier must be sufficiently high to keep $V_{OS} \leq 30\mu V$ for the full output voltage range. Thus for a max output of 10V, A_{VOL} must be greater than 340,000.

An amplifier with low offset voltage drift is required to give the desired system accuracy over an operating temperature range.

At low frequencies the AD OP-07 satisfies the above requirements and in most cases will not need an offset adjust potentiometer.

For high frequency operation, one may use a wide bandwidth amplifier such as the AD544 or the LF356 with either an offset adjust potentiometer or automatic nulling circuitry.

The choice of amplifier depends entirely on the required system accuracy, the required temperature range, and the operating frequency.

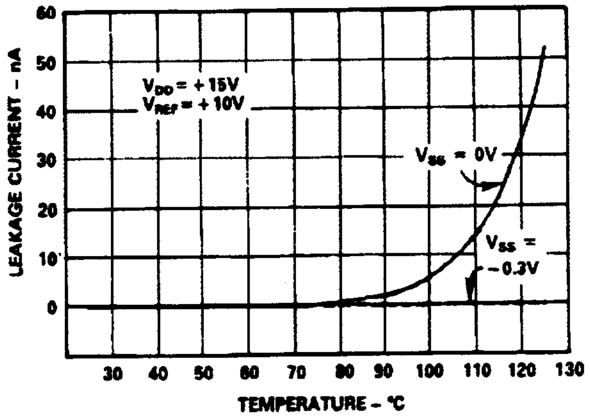


Figure 8. Graph of Typical Leakage Current vs. Temperature for AD7534

MICROPROCESSOR INTERFACING

AD7534 – 8085A INTERFACE

A typical interface circuit for the AD7534 and the 8085A microprocessor is given in Figure 9. The microprocessor sees the DAC as four memory locations, identified by address lines A0, A1. In standard operation, three of these memory locations are used. A sample program for loading the DAC with a 14-bit word is given in Table III. The AD7534 has address locations 3000–3003.

The six MSBs are written into location 3001, and the eight LSBs are written to 3002. Then with a write instruction to 3003 the full 14-bit word is loaded to the DAC register and the analog equivalent appears at the output.

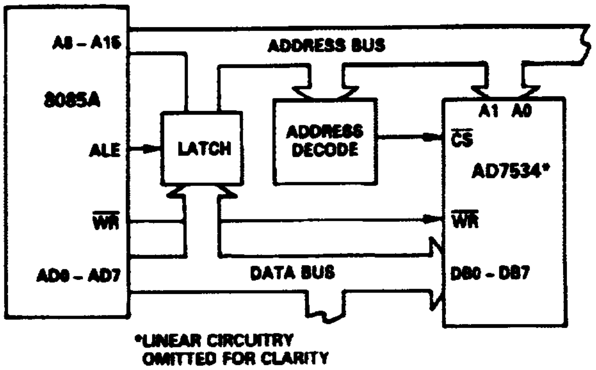


Figure 9. AD7534 – 8085A Interface

AD7534 – 8086 INTERFACE

The AD7534 may be interfaced to the 16-bit 8086 microprocessor using the circuit of Figure 10. The bottom 8 bits (AD0–AD7) of the 16-bit data bus are connected to the DAC data bus. The 14-bit word is loaded in two bytes using the MOV instruction. A further MOV loads the DAC register and causes the analog data to appear at the converter output. For the example given here, the appropriate DAC register addresses are D002, D004, D006. The program for loading the DAC is given below in Table IV.

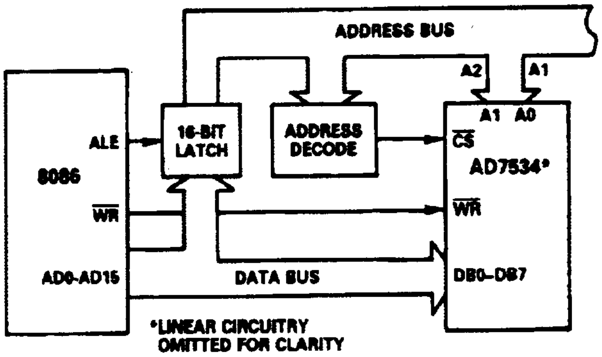


Figure 10. AD7534 – 8086 Interface Circuit

Address	Op-Code	Mnemonic
2000	26	MVI H,# 30
01	30	
02	2E	MVI L,# 01
03	01	
04	3E	MVI A,# "MS"
05	"MS"	
06	77	MOV M,A
07	2C	INR L
08	3E	MVI A,# "LS"
09	"LS"	
0A	77	MOV M, A
0B	2C	INR L
0C	77	MOV M,A
200D	CF	RST I

Table III. Program Listing for Figure 9

ASSUME DS: DACLOAD, CS : DACLOAD
DACLOAD SEGMENT AT 000

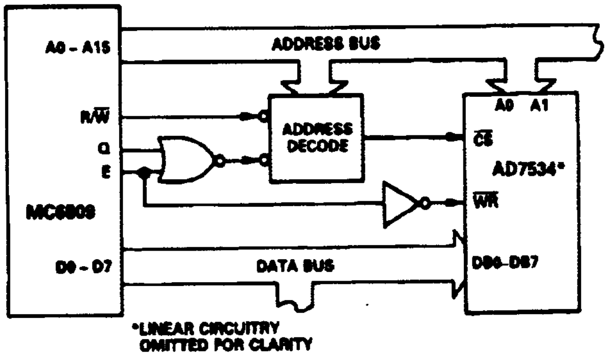
00	8CC9	MOV CX, CS	: DEFINE DATA SEGMENT REGISTER EQUAL
02	8ED9	MOV DS, CX	: TO CODE SEGMENT REGISTER
04	BF02D0	MOV DI, # D002	: LOAD DI WITH D002
07	C605"MS"	MOV MEM, # "MS"	: MS INPUT REGISTER LOADED WITH "MS"
0A	47	INC DI	
0B	47	INC DI	
0C	C605"LS"	MOV MEM, # "LS"	: LS INPUT REGISTER LOADED WITH "LS"
0F	47	INC DI	
10	47	INC DI	
11	C60500	MOV MEM, # 00	: CONTENTS OF INPUT REGISTERS ARE LOADED TO THE DAC REGISTER.
14	EA0000	JMP MEM	: CONTROL IS RETURNED TO THE MONITOR PROGRAM
17	00FF		

Table IV. Sample Program for Loading AD7534 from 8086

AD7534 – MC6809 INTERFACE

Figure 11 shows an interface circuit which enables the AD7534 to be programmed using the MC6809 8-bit microprocessor. By making use of the 16-bit D Accumulator, the transfer of data is simplified. The two key processor instructions are:

LDD Load D Accumulator from memory.
STD Store D Accumulator to memory.

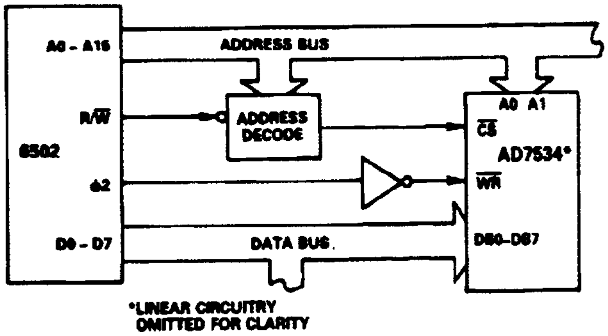


*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 11. AD7534 – MC6809 Interface Circuit

AD7534 – 6502 INTERFACE

The interface circuit for the 6502 microprocessor is shown in Figure 12.

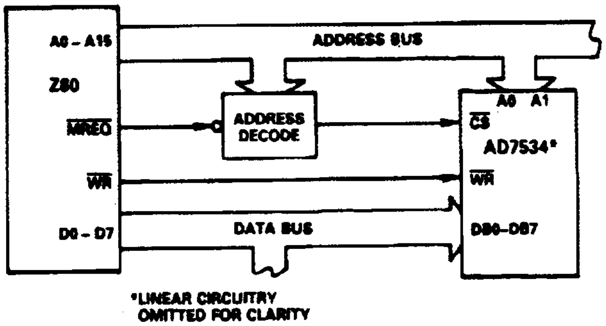


*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 12. AD7534 – 6502 Interface

AD7534 – Z80 INTERFACE

Interfacing to the Z80 microprocessor requires a minimal amount of extra components. The circuit consists of the Z80 processor, the AD7534 and an address decoder for the DAC. Figure 13, below, illustrates the circuit.



*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 13. AD7534 – Z80 Interface

AD7534 – MC68000 INTERFACE

Interfacing between the MC68000 and the AD7534 is accomplished using the circuit of Figure 14. The following routine writes data to the DAC input registers and then outputs the data via the DAC register.

```
        ·A2 B003                              Address Register 2 is loaded with E003.
01000   MOVE.W      # W, D0                   The desired DAC data, W, is loaded
                                              into Data Register 0. W may be any value
                                              between 0 and 16383 (decimal) or 0
                                              and 3FFF (hexadecimal).
        MOVEP.W     D0,$0000(A2)              The data W is transferred between D0
                                              and the Input Registers of the DAC.
                                              The high order byte of data is trans-
                                              ferred first. The memory address is
                                              specified using the address register in-
                                              direct plus displacement addressing
                                              mode. The address used in this instance
                                              (B003) is odd and so data is transferred
                                              on the low order half of the data bus
                                              (D0-D7).
        MOVE.W      D0,$E006                  This instruction provides appropriate
                                              signals to transfer the data W from the
                                              DAC Input Registers to the DAC Regis-
                                              ter, which controls the switches in the
                                              14-bit D/A structure.
        MOVE.B      # 228,D7                  Control is returned to the System Monitor
                                              Program using these two instructions.
        TRAP        # 14
```

Since only the lower half of the Data Bus is used in this interfacing system, it is also suitable for use with the MC68008. This provides the user with an eight bit data bus instead of the MC68000's sixteen bit data bus.

DIGITAL FEEDTHROUGH

In the preceeding interface configurations, most digital inputs to the AD7534 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this digital feedthrough isolate the DAC from the noise source. Figure 15 shows an interface circuit which physically isolates the DAC from the bus. One may also use other means, such as peripheral interface devices, to reduce the digital feedthrough.

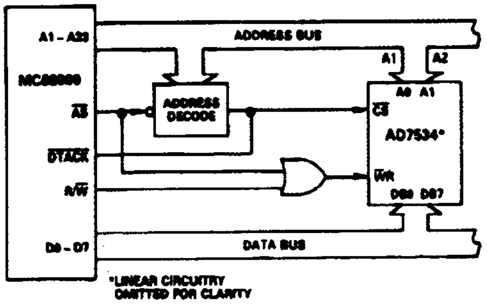


Figure 14. AD7534 – MC68000 Interface

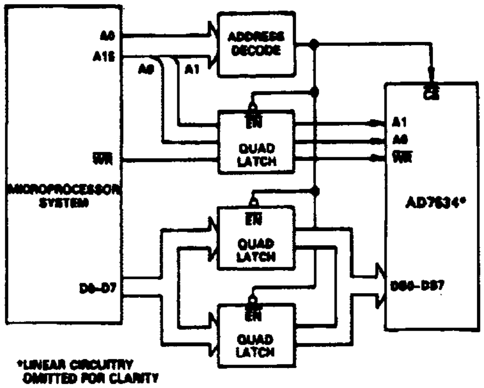


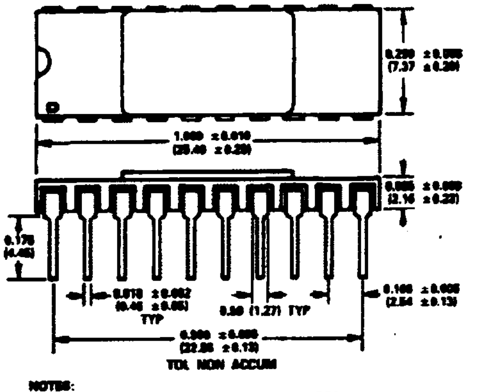
Figure 15. AD7534 Interface Circuit Using Latches to Minimize Digital Feedthrough

MECHANICAL INFORMATION

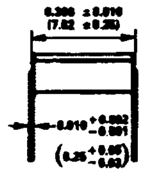
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

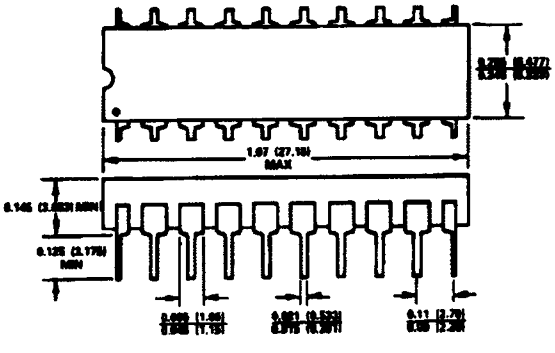
20-PIN CERAMIC DIP (SUFFIX D)



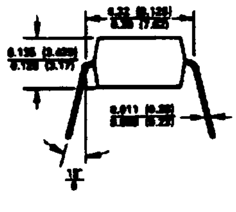
NOTES:
1. LEAD NUMBER 1 IDENTIFIED BY DOT OR NOTCH.
2. LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.



20-PIN PLASTIC DIP (SUFFIX N)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42



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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
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