

1. OUTLINE

1.1 Features

Ultra-low power consumption technology

- VDD = single power supply voltage of 2.7 to 5.5 V
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high-speed (0.04167 μ s: @ 24 MHz operation with high-speed on-chip oscillator) to low-speed (1.0 μ s: @ 1 MHz operation with high-speed on-chip oscillator)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register \times 8) \times 4 banks
- On-chip RAM: 1.5 KB

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Code flash memory

- Code flash memory: 8 to 16 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (flash shield window function)

High-speed on-chip oscillator

- Select from 48 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 4 MHz, and 1 MHz
- High accuracy: \pm 2.0%

Operating ambient temperature

- TA = -40 to +85°C

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 6 levels)

Event link controller (ELC)

- Event signals of 18 to 19 types can be linked to the specified peripheral function.

Serial interfaces

- CSI: 1 channel
- UART: 2 channels
- Simplified I²C: 1 channel

Timer

- 16-bit timer: 7 channels
(Timer Array Unit (TAU): 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels)
- 12-bit interval timer: 1 channel
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

A/D converter

- 8/10-bit resolution A/D converter (VDD = 2.7 to 5.5 V)
- Analog input: 8 to 12 channels
- Internal reference voltage (1.45 V) and temperature sensor^{Note}

Note: Selectable only in HS (high-speed main) mode.

Comparator

- 2 channels
- The voltage from a dedicated 8-bit DAC (resolution of 256 with VDD/AVREFP or VSS/AVREFM as the internally generated reference voltage) can be selected as the reference voltage.

Programmable gain amplifier

I/O port

- I/O port: 26 to 40
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 2.5/3 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit

Remark: The function mounted depend on the product.
See 1.6 Outline of Functions.

○ ROM, RAM capacities

Flash ROM	RAM	30 pins	32 pins	44 pins
16 KB	1.5 KB <i>Note</i>	R5F11EAAASP	R5F11EBAAFP	R5F11EFAAFP
8 KB		R5F11EA8ASP	R5F11EB8AFP	R5F11EF8AFP

Note This is 630 bytes when the self-programming function is used.

1.2 List of Part Numbers

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1G

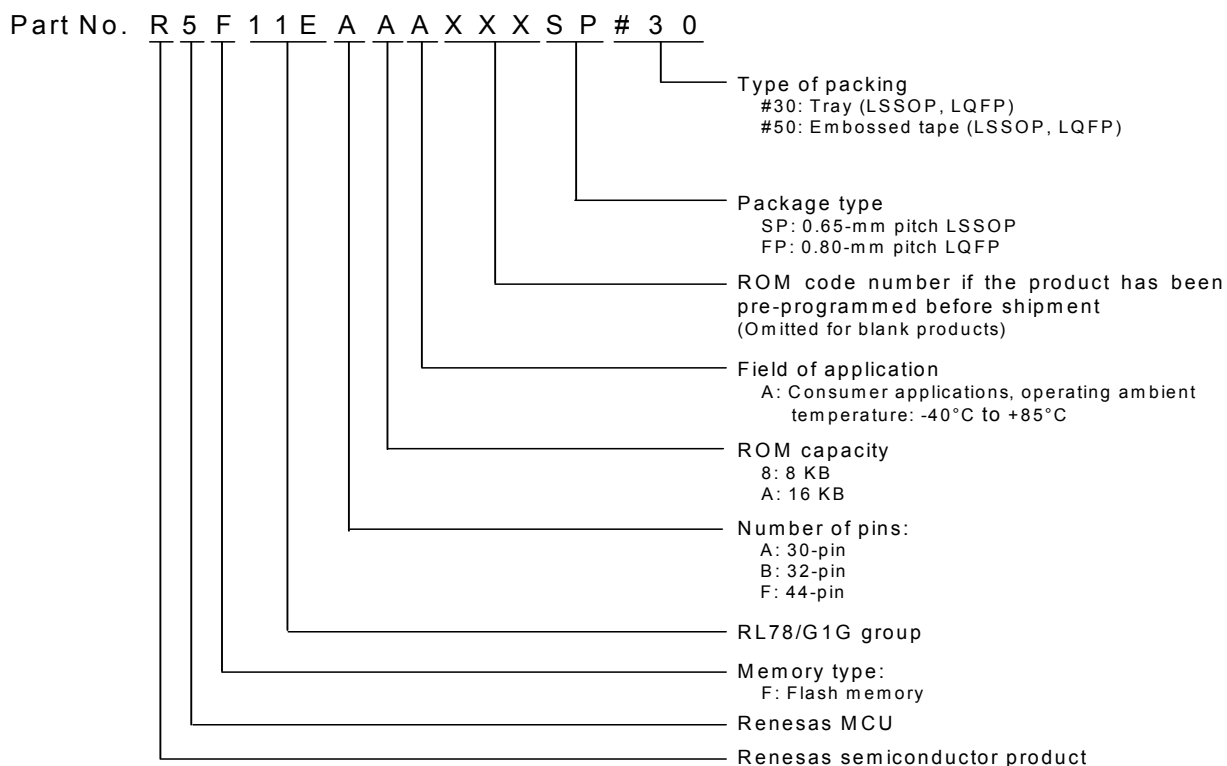


Table 1 - 1 Orderable Part Numbers

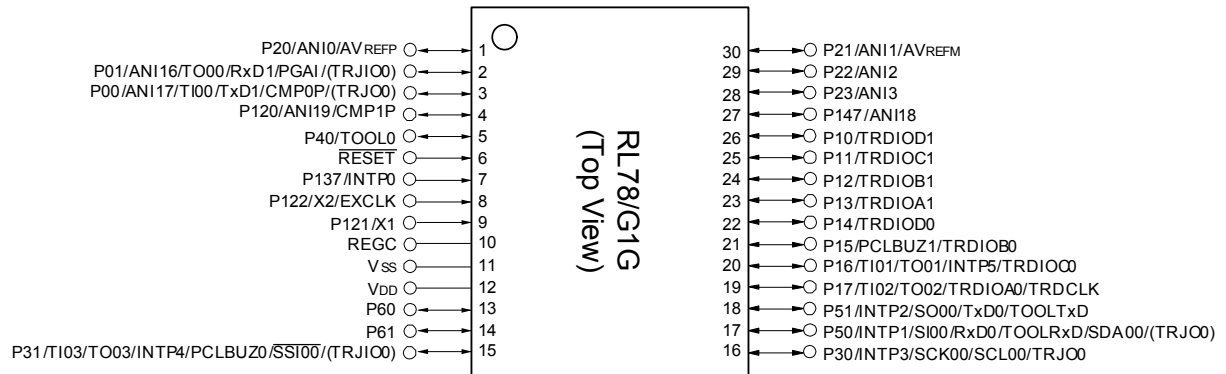
Pin Count	Package	Part Number
44 pins	44-pin plastic LQFP (10 × 10 mm)	R5F11EFAAFP#30, R5F11EFAAFP#50
		R5F11EF8AFP#30, R5F11EF8AFP#50
32 pins	32-pin plastic LQFP (7 × 7 mm)	R5F11EBAAFP#30, R5F11EBAAFP#50
		R5F11EB8AFP#30, R5F11EB8AFP#50
30 pins	30-pin plastic LSSOP (7.62 mm (300))	R5F11EAAASP#30, R5F11EAAASP#50
		R5F11EA8ASP#30, R5F11EA8ASP#50

1.3 Pin Configuration (Top View)

1.3.1 30-pin products

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- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



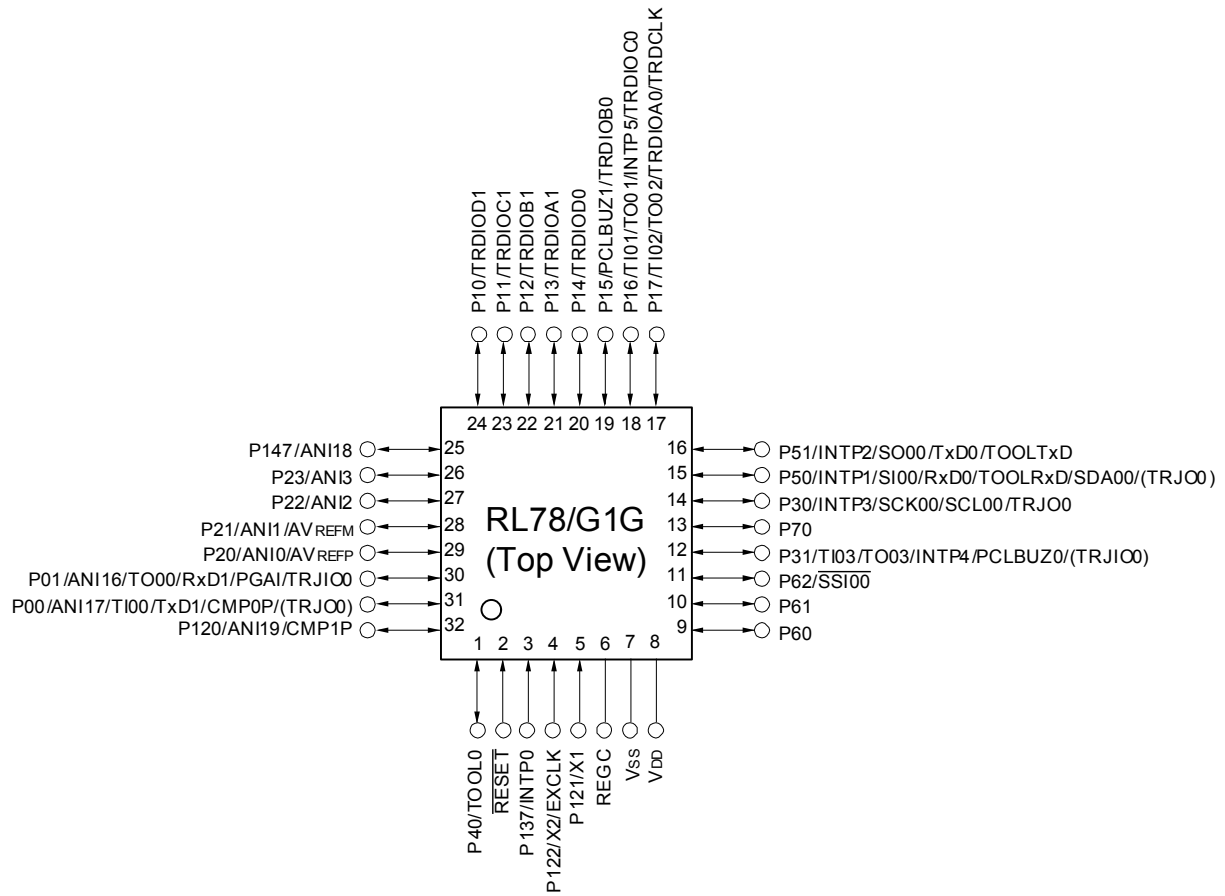
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. The functions in parentheses shown in the above figure can be assigned by setting peripheral I/O redirection register 1 (PIOR1).

1.3.2 32-pin products

- <R> • 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)



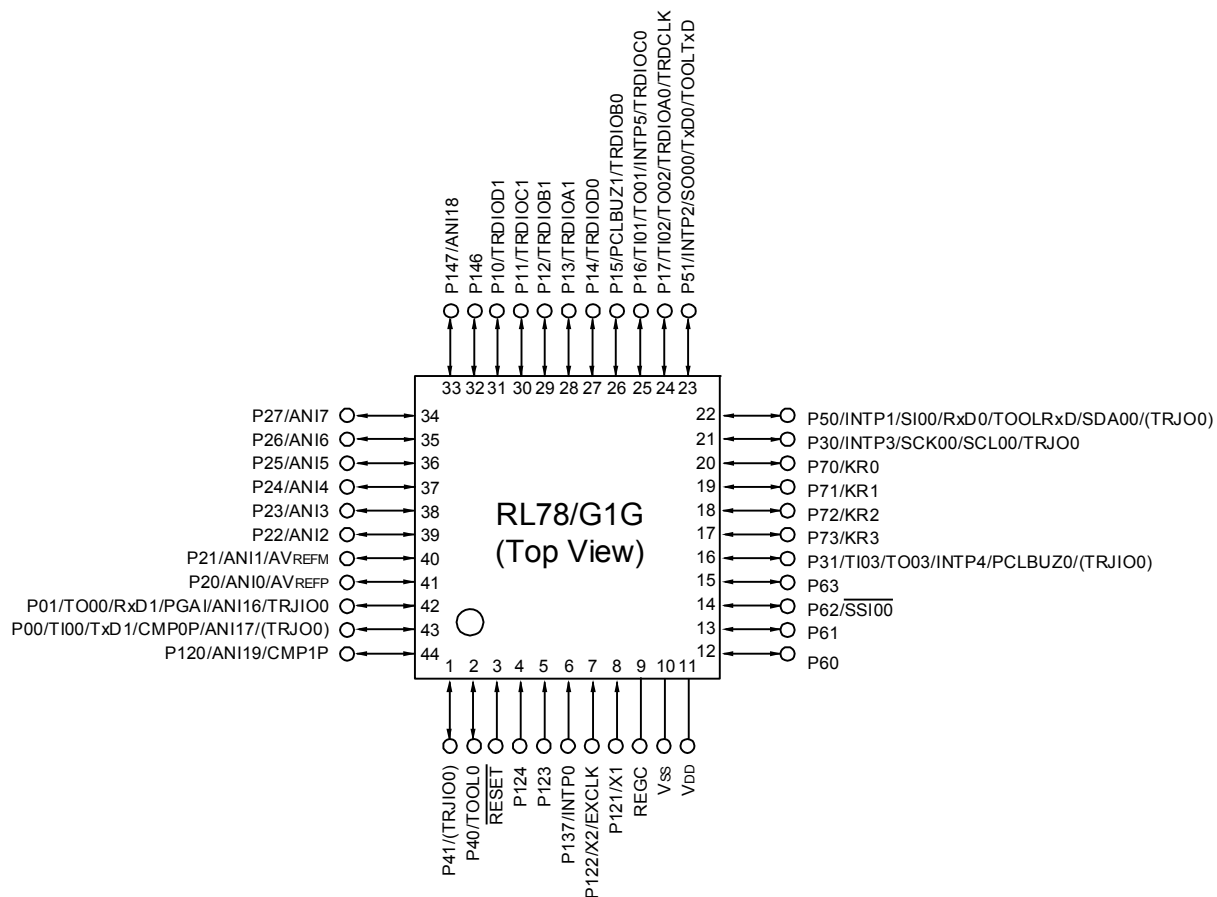
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. The functions in parentheses shown in the above figure can be assigned by setting peripheral I/O redirection register 1 (PIOR1).

1.3.3 44-pin products

- <R> • 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)



Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

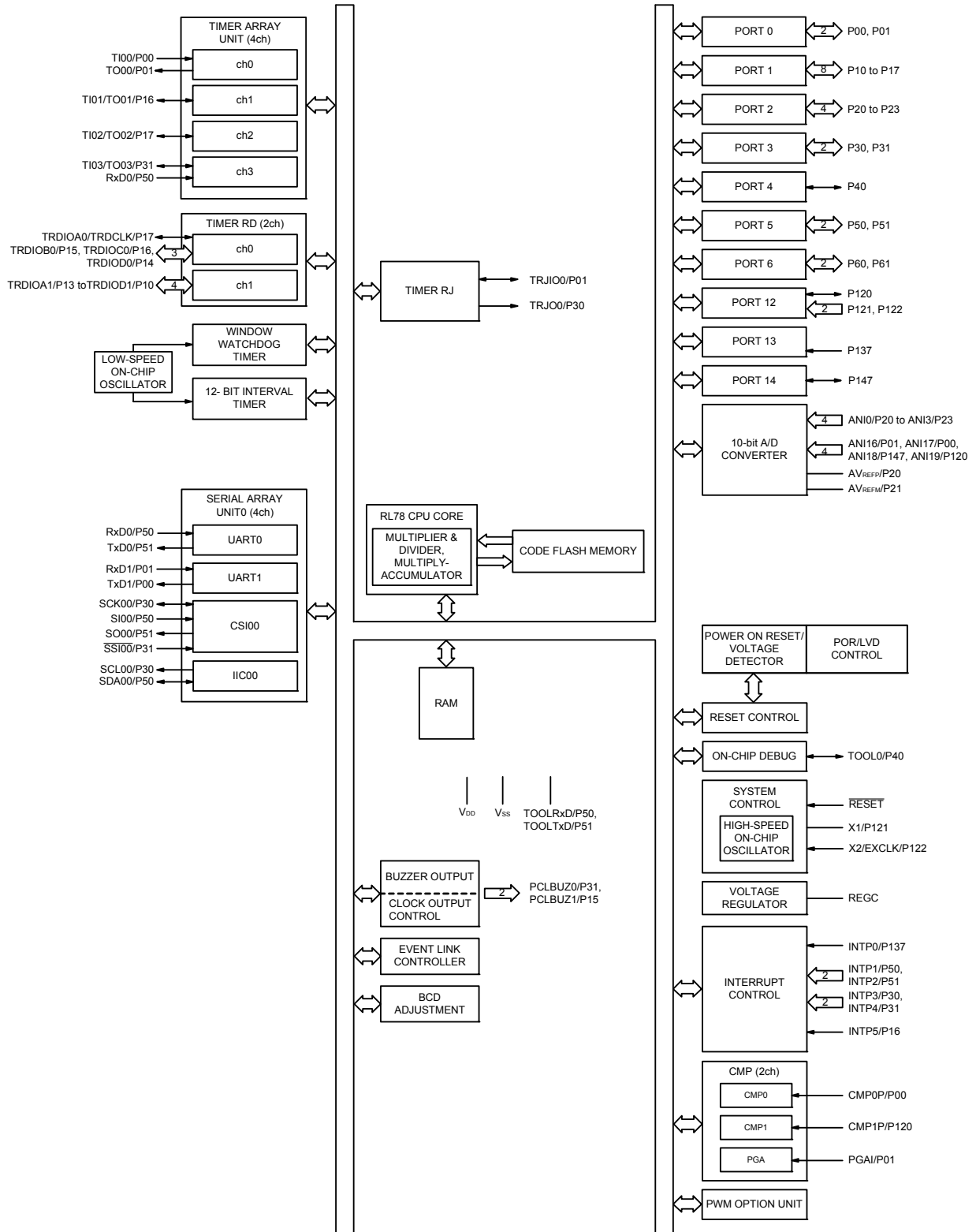
Remark 2. The functions in parentheses shown in the above figure can be assigned by setting peripheral I/O redirection register 1 (PIOR1).

1.4 Pin Identification

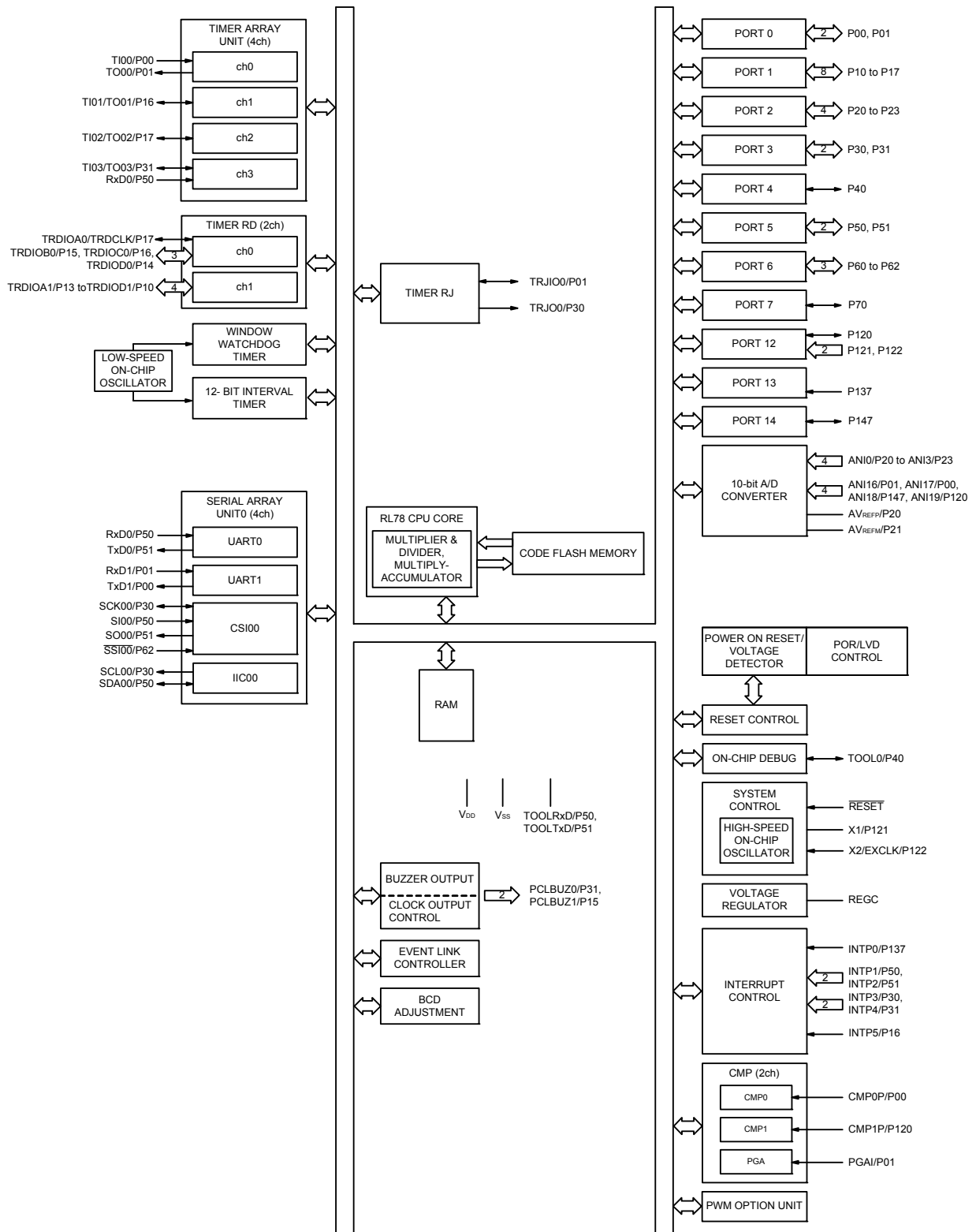
ANI0 to ANI7, ANI16 to ANI19:	Analog input
AVREFM:	A/D converter reference potential (- side) input
AVREFP:	A/D converter reference potential (+ side) input
EXCLK:	External clock input (main system clock)
INTP0 to INTP5:	External interrupt input
KR0 to KR3:	Key Return
P00, P01:	Port 0
P10 to P17:	Port 1
P20 to P27:	Port 2
P30, P31:	Port 3
P40, P41:	Port 4
P50, P51:	Port 5
P60 to P63:	Port 6
P70 to P73:	Port 7
P120 to P124:	Port 12
P137:	Port 13
P146, P147:	Port 14
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output
REGC:	Regulator capacitance
<u>RESET</u> :	Reset
RxD0, RxD1:	Receive data
SCK00:	Serial clock input/output
SCL00:	Serial clock output
SDA00:	Serial data input/output
SI00:	Serial data input
SO00:	Serial data output
<u>SSI00</u> :	Serial interface chip select input
TI00 to TI03:	Timer input
TO00 to TO03, TRJ00:	Timer output
TOOL0:	Data input/output for tool
TOOLRxD, TOOLTxD:	Data input/output for external device
TRDCLK:	Timer external input clock
TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, TRJIO0	Timer input/output
TxD0, TxD1:	Transmit data
CMP0P, CMP1P:	Comparator input
PGAI:	PGA input
V _{DD} :	Power supply
V _{SS} :	Ground
X1, X2:	Crystal oscillator (main system clock)

1.5 Block Diagram

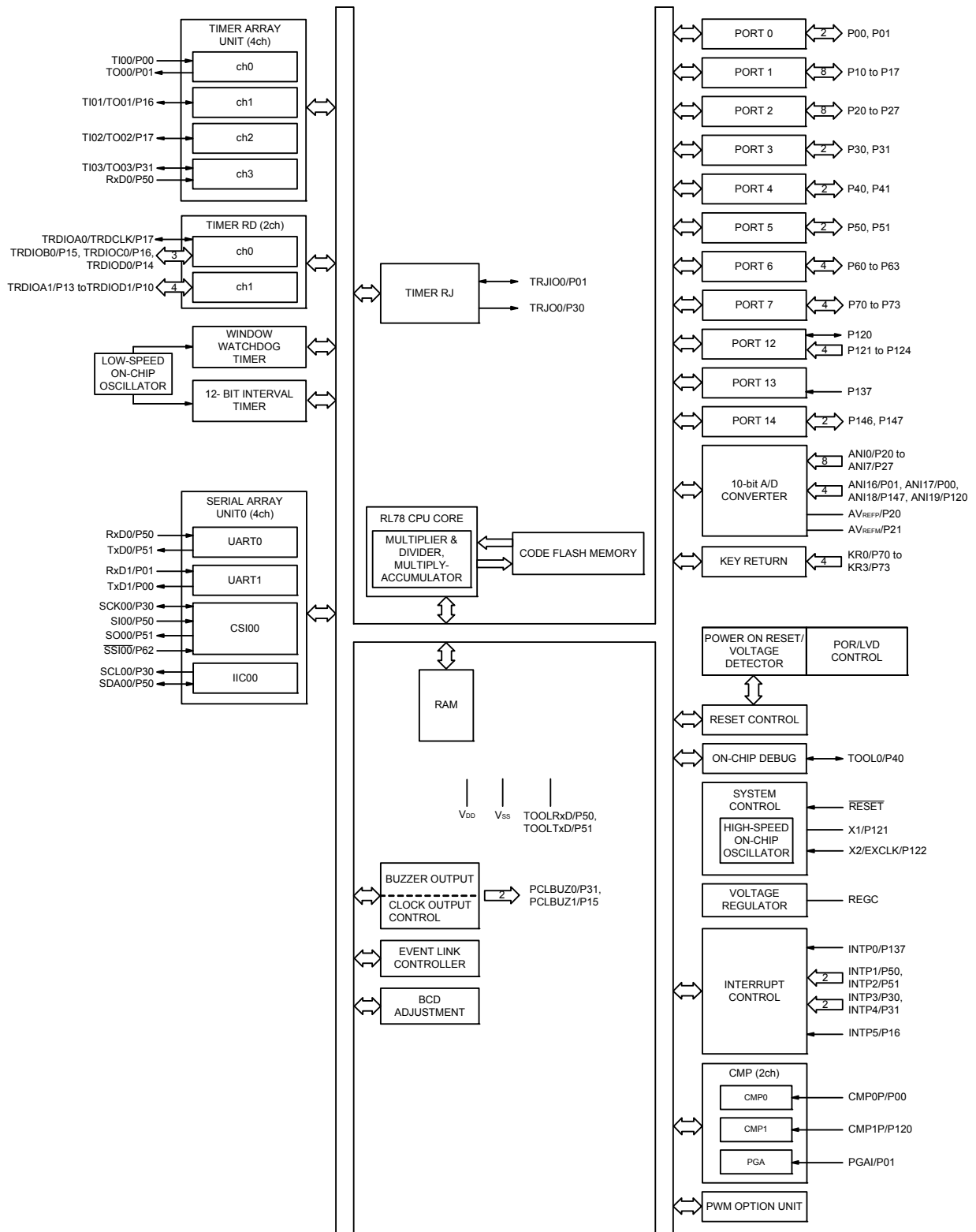
1.5.1 30-pin products



1.5.2 32-pin products



1.5.3 44-pin products



1.6 Outline of Functions

[30-pin, 32-pin, 44-pin products (code flash memory 8 KB to 16 KB)]

Caution The above outline of the functions applies when peripheral I/O redirection register 1 (PIOR1) is set to 00H.

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Item		30-pin	32-pin	44-pin
		R5F11EA8ASP, R5F11EAAASP	R5F11EB8AFP, R5F11EBAAFP	R5F11EF8AFP, R5F11EFAAFP
Code flash memory (KB)		8 to 16		
RAM (KB)		1.5		
Address space		1 MB		
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V)		
	High-speed on-chip oscillator clock (f _{IH})	LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 2.7 to 5.5 V) HS (high-speed main) mode: 1 to 24 MHz (V _{DD} = 2.7 to 5.5 V)		
Low-speed on-chip oscillator clock		15 kHz (TYP.); V _{DD} = 2.7 to 5.5 V		
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)		
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f _{IH} = 24 MHz operation)		
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)		
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 		
I/O port	Total	26	28	40
	CMOS I/O	23	25	35
	CMOS input	3	3	5
	CMOS output	—		
	N-ch open-drain I/O (6 V tolerance)	—		
Timer	16-bit timer	7 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels)		
	Watchdog timer	1 channel		
	12-bit interval timer	1 channel		
	Timer output	Timer outputs: 14 channels PWM outputs: 9 channels		

Caution Since a library is used when rewriting the flash memory using the user program, flash ROM and RAM areas are used. Refer to the RL78 Family Flash Self-Programming Library Type01 User's Manual before using these products.

(2/2)

Item	30-pin	32-pin	44-pin
	R5F11EA8ASP, R5F11EAAASP	R5F11EB8AFP, R5F11EBAAFP	R5F11EF8AFP, R5F11EFAAFP
Clock output/buzzer output	2 • 2.44 kHz, 4.88 kHz, 9.77 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f _{MAIN} = 20 MHz operation)		
8/10-bit resolution A/D converter	8 channels		12 channels
Comparator	2 channels		
PGA	1 channel		
Serial interface	• CSI: 1 channel/UART0: 1 channel/simplified I ² C: 1 channel • UART1: 1 channel		
Event link controller (ELC)	Event input: 18 Event trigger output: 6		Event input: 19 Event trigger output: 6
Vectored interrupt sources	Internal	20	
	External	6	7
Key interrupt	—		4
Reset	<ul style="list-style-type: none"> • Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 		
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V 		
Voltage detector	2.75 V to 4.06 V (6 stages)		
On-chip debug function	Provided		
Power supply voltage	V _{DD} = 2.7 to 5.5 V		
Operating ambient temperature	T _A = -40 to +85°C		

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS

Caution 1. The RL78 microcontroller has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted are as follows according to product.

2.1 Pins Mounted According to Product

2.1.1 Port functions

Refer to 2.1.1 30-pin products, 2.1.2 32-pin products, and 2.1.3 44-pin products in the RL78/G1G User's Manual.

2.1.2 Non-port functions

Refer to 2.2.1 With functions for each product in the RL78/G1G User's Manual.

2.2 Absolute Maximum Ratings

Absolute Maximum Ratings

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Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} +0.3 Note 1	V
Input voltage	V _{I1}	P00, P01, P10 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P121 to P124, P137, P146, P147, EXCLK, $\overline{\text{RESET}}$	-0.3 to V _{DD} +0.3 Note 2	V
Output voltage	V _{O1}	P00, P01, P10 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147	-0.3 to V _{DD} +0.3 Note 2	V
Analog input voltage	V _{AI1}	ANI0 to ANI7, ANI16 to ANI19	-0.3 to V _{DD} +0.3 Notes 2, 3 and -0.3 to AV _{REF} (+) +0.3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

Absolute Maximum Ratings

(2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147	-40	mA
		Total of all pins -170 mA	P00, P01, P40, P41, P120	-70	mA
			P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P73, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27	-0.5	mA
		Total of all pins		-2	mA
	Output current, low	IOL1	Per pin	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147	40
Total of all pins 170 mA			P00, P01, P40, P41, P120	70	mA
			P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P73, P146, P147	100	mA
IOL2		Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature		TA	In normal operation mode		-40 to +85
	In flash memory programming mode				
Storage temperature	Tstg			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3 Oscillator Characteristics

2.3.1 X1 oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_x) ^{Note}	Ceramic resonator/ crystal resonator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to 5.4 System Clock Oscillator in the RL78/G1G User's Manual.

2.3.2 On-chip oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f_{IH}		1		24	MHz
	f_{HOCO}		1		48	
High-speed on-chip oscillator clock frequency accuracy			-2		+2	%
Low-speed on-chip oscillator clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2.4 DC Characteristics

2.4.1 Pin characteristics

(TA = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147	2.7 V ≤ V _{DD} ≤ 5.5 V			-10.0 Note 2	mA
		Total of P00, P01, P40, P41, P120 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V			-55.0	mA
			2.7 V ≤ V _{DD} < 4.0 V			-10.0	mA
		Total of P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P73, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ V _{DD} ≤ 5.5 V			-80.0	mA
			2.7 V ≤ V _{DD} < 4.0 V			-19.0	mA
	Total of all pins (When duty ≤ 70% ^{Note 3})	2.7 V ≤ V _{DD} ≤ 5.5 V			-135.0	mA	
	I _{OH2}	Per pin for P20 to P27	2.7 V ≤ V _{DD} ≤ 5.5 V			-0.1 Note 2	mA
Total of all pins (When duty ≤ 70% ^{Note 3})		2.7 V ≤ V _{DD} ≤ 5.5 V			-1.5	mA	

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
 <Example> Where n = 80% and I_{OH} = -10.0 mA
 Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
 A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P10, P15, P17, P30, P50, P51 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	IOL1	Per pin for P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147			20.0 Note 2	mA
		Total of P00, P01, P40, P41, P120 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ VDD ≤ 5.5 V		70.0	mA
			2.7 V ≤ VDD < 4.0 V		15.0	mA
		Total of P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P73, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ VDD ≤ 5.5 V		80.0	mA
			2.7 V ≤ VDD < 4.0 V		35.0	mA
	Total of all pins (When duty ≤ 70% ^{Note 3})			150.0	mA	
	IOL2	Per pin for P20 to P27			0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.7 V ≤ VDD ≤ 5.5 V		5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pin.

Note 2. However, do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	VIH1	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120 to P124, P146, P147	Normal input buffer	0.8 VDD		VDD	V
	VIH2	P01, P10, P15 to P17, P30, P31, P50	TTL input buffer 4.0 V ≤ VDD ≤ 5.5 V	2.2		VDD	V
			TTL input buffer 3.3 V ≤ VDD < 4.0 V	2.0		VDD	V
			TTL input buffer 2.7 V ≤ VDD < 3.3 V	1.50		VDD	V
	VIH3	P20 to P27		0.7 VDD		VDD	V
	VIH4	EXCLK, $\overline{\text{RESET}}$		0.8 VDD		VDD	V
Input voltage, low	VIL1	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120 to P124, P146, P147	Normal input buffer	0		0.2 VDD	V
	VIL2	P01, P10, P15 to P17, P30, P31, P50	TTL input buffer 4.0 V ≤ VDD ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ VDD < 4.0 V	0		0.5	V
			TTL input buffer 2.7 V ≤ VDD < 3.3 V	0		0.32	V
	VIL3	P20 to P27		0		0.3 VDD	V
	VIL4	EXCLK, $\overline{\text{RESET}}$		0		0.2 VDD	V

Caution The maximum value of VIH of pins P00, P10, P15, P17, P30, P50, and P51 is VDD, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	VOH1	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147	4.0 V ≤ VDD ≤ 5.5 V, IOH1 = -10.0 mA	VDD - 1.5		V
			4.0 V ≤ VDD ≤ 5.5 V, IOH1 = -3.0 mA	VDD - 0.7		V
			2.7 V ≤ VDD ≤ 5.5 V, IOH1 = -2.0 mA	VDD - 0.6		V
			2.7 V ≤ VDD ≤ 5.5 V, IOH1 = -1.0 mA	VDD - 0.5		V
	VOH2	P20 to P27	2.7 V ≤ VDD ≤ 5.5 V, IOH2 = -100 μA	VDD - 0.5		V
Output voltage, low	VOL1	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147	4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 20.0 mA		1.3	V
			4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 8.5 mA		0.7	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 3.0 mA		0.6	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 1.5 mA		0.4	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 0.3 mA		0.4	V
	VOL2	P20 to P27	2.7 V ≤ VDD ≤ 5.5 V, IOL2 = 400 μA		0.4	V

Caution P00, P10, P15, P17, P30, P50, and P51 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	ILIH1	P00, P01, P10 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P123, P124, P137, P146, P147, RESET	Vi = VDD		1	μA		
	ILIH2	P121, P122 (X1, X2, EXCLK)	Vi = VDD		1	μA		
			In resonator connection		10	μA		
Input leakage current, low	ILIL1	P00, P01, P10 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P123, P124, P137, P146, P147, RESET	Vi = VSS		-1	μA		
	ILIL2	P121, P122 (X1, X2, EXCLK)	Vi = VSS		-1	μA		
			In resonator connection		-10	μA		
On-chip pull-up resistance	Ru	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147	Vi = VSS, in input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4.2 Supply current characteristics

(1) Flash ROM: 16 KB of 30-pin to 44-pin products

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Notes 3, 4	fHOCO = 48 MHz, fIH = 24 MHz	Basic operation	VDD = 5.0 V		1.8		mA
				VDD = 3.0 V			1.8			
		HS (high-speed main) mode Notes 3, 4	fHOCO = 48 MHz, fIH = 24 MHz	Normal operation	VDD = 5.0 V		3.9	6.9	mA	
					VDD = 3.0 V		3.9	6.9		
					fHOCO = 24 MHz, fIH = 24 MHz	VDD = 5.0 V		3.7		6.3
						VDD = 3.0 V		3.7		6.3
		fHOCO = 16 MHz, fIH = 16 MHz	VDD = 5.0 V		2.8	4.6				
			VDD = 3.0 V		2.8	4.6				
		LS (low-speed main) mode Notes 3, 4	fIH = 8 MHz	Normal operation	VDD = 3.0 V		1.2	2.0	mA	
		HS (high-speed main) mode Notes 2, 4	fMX = 20 MHz, VDD = 5.0 V	Normal operation	Square wave input		3.1	5.3	mA	
					Resonator connection		3.3	5.5		
				Normal operation	Square wave input		3.1	5.3		
					Resonator connection		3.3	5.5		
				fMX = 10 MHz, VDD = 5.0 V	Normal operation	Square wave input		2.0		3.1
Resonator connection						2.0	3.2			
fMX = 10 MHz, VDD = 3.0 V	Normal operation			Square wave input		2.0	3.1			
				Resonator connection		2.0	3.2			
LS (low-speed main) mode Notes 2, 4	fMX = 8 MHz, VDD = 3.0 V	Normal operation	Square wave input		1.2	1.9	mA			
			Resonator connection		1.2	2.0				

Note 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, watchdog timer, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

Note 2. When high-speed on-chip oscillator is stopped.

Note 3. When high-speed system clock is stopped.

Note 4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high speed main) mode: VDD = 2.7 V to 5.5 V@1 MHz to 24 MHz

LS (low speed main) mode: VDD = 2.7 V to 5.5 V@1 MHz to 8 MHz

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (48 MHz max.)

Remark 3. fIH: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 4. Temperature condition of the TYP. value is TA = 25°C

(1) Flash ROM: 16 KB of 30-pin to 44-pin products

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit		
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Notes 4, 6	fHOCO = 48 MHz, fIH = 24 MHz	VDD = 5.0 V		0.60	2.40	mA	
					VDD = 3.0 V		0.60	2.40		
				fHOCO = 24 MHz, fIH = 24 MHz	VDD = 5.0 V		0.40	1.83		
					VDD = 3.0 V		0.40	1.83		
				fHOCO = 16 MHz, fIH = 16 MHz	VDD = 5.0 V		0.38	1.38		
				VDD = 3.0 V		0.38	1.38			
				LS (low-speed main) mode Notes 4, 6	fIH = 8 MHz	VDD = 3.0 V		260	710	μA
			HS (high-speed main) mode Notes 3, 6	fMX = 20 MHz, VDD = 5.0 V	Square wave input		0.28	1.55	mA	
					Resonator connection		0.42	1.74		
				fMX = 20 MHz, VDD = 3.0 V	Square wave input		0.28	1.55		
	Resonator connection				0.42	1.74				
	fMX = 10 MHz, VDD = 5.0 V	Square wave input			0.19	0.86				
		Resonator connection			0.27	0.93				
	LS (low-speed main) mode Notes 3, 6	fMX = 8 MHz, VDD = 3.0 V	Square wave input		95	550	μA			
			Resonator connection		145	590				
IDD3	STOP mode Note 5	TA = -40°C				0.18	0.51	μA		
		TA = +25°C				0.24	0.51			
		TA = +50°C				0.29	1.10			
		TA = +70°C				0.41	1.90			
		TA = +85°C				0.90	3.30			

Note 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, watchdog timer, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator is stopped.

Note 4. When high-speed system clock is stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.

Note 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high speed main) mode: VDD = 2.7 V to 5.5 V@1 MHz to 24 MHz

LS (low speed main) mode: VDD = 2.7 V to 5.5 V@1 MHz to 8 MHz

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (48 MHz max.)

Remark 3. fIH: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 4. Temperature condition of the TYP. value is TA = 25°C

(2) Peripheral Functions (Common to all products)**(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
12-bit interval timer operating current	I _{IT} Notes 1, 8				0.02		μA	
Watchdog timer operating current	I _{WDT} Notes 1, 2	f _{IL} = 15 kHz			0.22		μA	
A/D converter operating current	I _{ADC} Note 3	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.3	1.7	mA	
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.5	0.7		
A/D converter reference voltage current	I _{ADREF}				75		μA	
Temperature sensor operating current	I _{TMPS}				75		μA	
Comparator operating current	I _{COMP} Note 4	Per channel of comparator 1	When the comparator is operating		45.0	65.0	μA	
			When the comparator is stopped		0.0	0.1		
Programmable gain amplifier operating current	I _{PGA} Note 5	When the programmable gain amplifier is operating			240.0	340.0	μA	
		When the programmable gain amplifier is stopped			0.0	0.1		
LVD operating current	I _{LVI} Note 6				0.08		μA	
SNOOZE operating current	I _{SNOZ}	ADC operation	The mode is performed Note 7			0.50	0.60	mA
			The A/D conversion operations are performed	Low voltage mode AV _{REFP} = V _{DD} = 3.0 V		1.20	1.44	
		CSI/UART operation			0.70	0.84	mA	

Note 1. When high speed on-chip oscillator and high-speed system clock are stopped.

Note 2. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontroller is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

Note 3. Current flowing only to the A/D converter. The current value of the RL78 microcontroller is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

Note 4. Current flowing only to the comparator. The current value of the RL78 microcontroller is the sum of I_{DD1} or I_{DD2} and I_{COMP} when the comparator operates in operating mode or HALT mode.

Note 5. Current flowing only to the programmable gain amplifier. The current value of the RL78 microcontroller is the sum of I_{DD1} or I_{DD2} and I_{PGA} when the programmable gain amplifier operates in operating mode or HALT mode.

Note 6. Current flowing only to the LVD circuit. The current value of the RL78 microcontroller is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.

Note 7. For details on the transition time to SNOOZE mode, refer to **18.3.3 SNOOZE mode in the RL78/G1G User's Manual**.

Note 8. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontroller is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 3. Temperature condition of the TYP. value is TA = 25°C

2.5 AC Characteristics

2.5.1 Basic operation

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

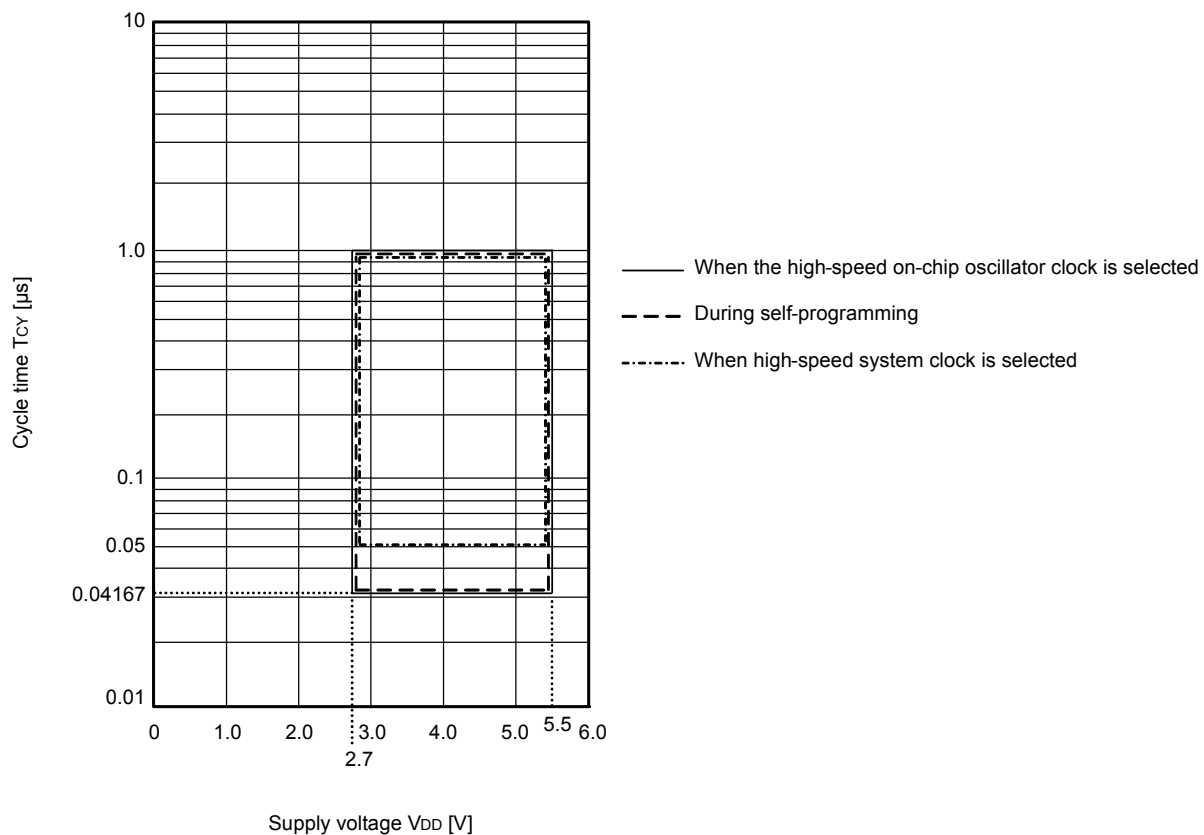
Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.04167		1	μs
			LS (low-speed main) mode	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.125		1	μs
		In the self programming mode	HS (high-speed main) mode	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.04167		1	μs
			LS (low-speed main) mode	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.125		1	μs
External main system clock frequency	f_{EX}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			1.0		20.0	MHz
External main system clock input high-level width, low-level width	t_{EXH} , t_{EXL}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			24			ns
Ti00 to Ti03 input high-level width, low-level width	t_{TIH} , t_{TIL}				$1/f_{MCK} + 10$			ns
Timer RJ input cycle	f_C	TRJIO	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		100			ns
Timer RJ input high-level width, low-level width	f_{WH} , f_{WL}	TRJIO	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		40			ns
TO00 to TO03, TRJIO0, TRJO, TRDIOA0/1, TRDIOB0/1, TRDIOC0/1, TRDIOD0/1 output frequency	f_{TO}	HS (high-speed main) mode	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			12	MHz	
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$			8	MHz	
		LS (low-speed main) mode	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			16	MHz	
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$			8	MHz	
		LS (low-speed main) mode	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$				4	MHz
Interrupt input high-level width, low-level width	t_{INTH} , t_{INTL}	INTP0 to INTP5	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1			μs
Key interrupt input low-level width	t_{KR}	KR0-KR3	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		250			ns
RESET low-level width	t_{RSL}				10			μs

Remark f_{MCK} : Timer array unit operation clock frequency

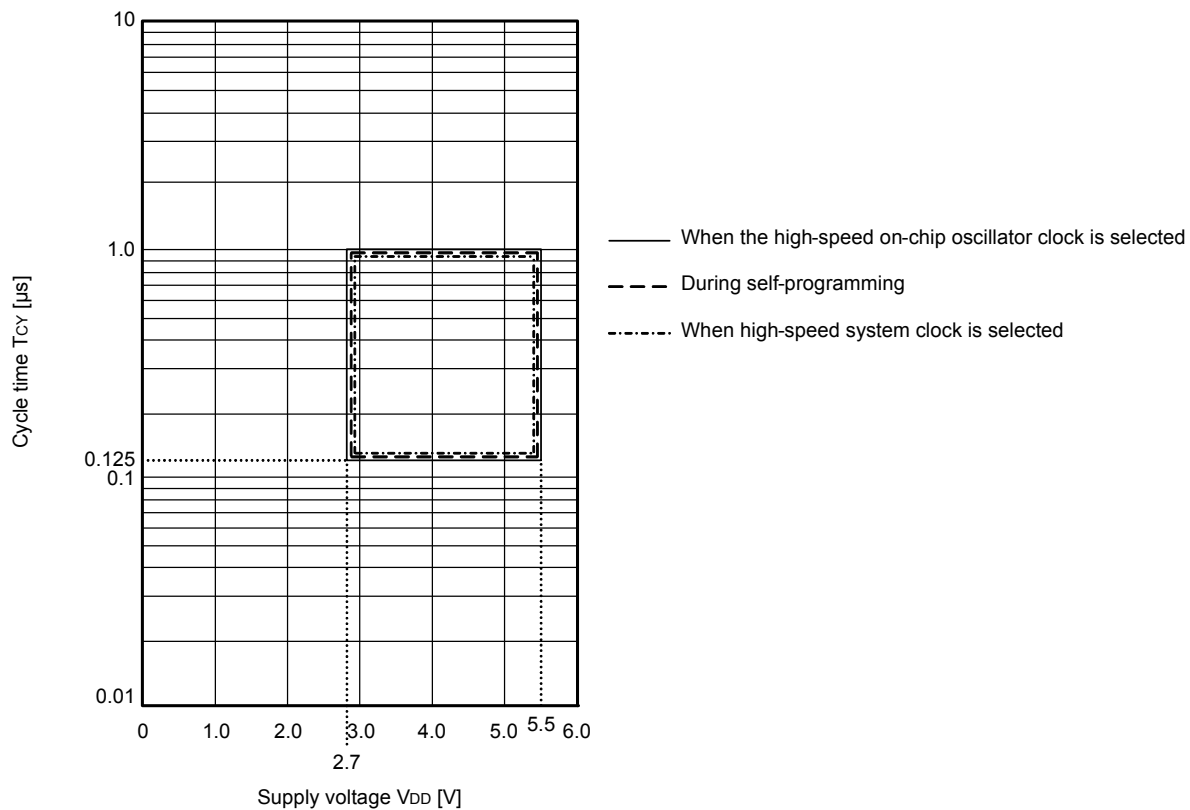
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0), n: Channel number (n = 0 to 3))

Minimum Instruction Execution Time during Main System Clock Operation

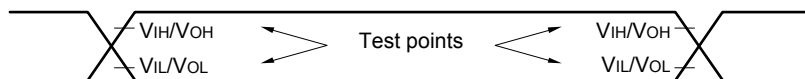
TCY vs VDD (HS (high-speed main) mode)



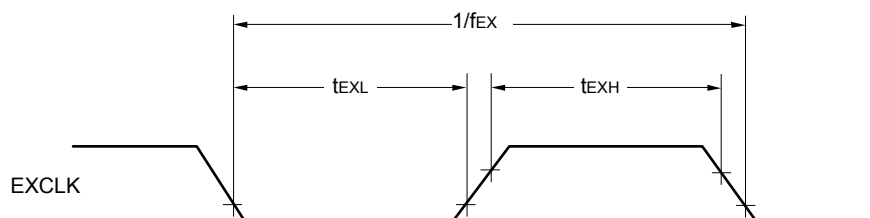
TCY vs VDD (LS (low-speed main) mode)



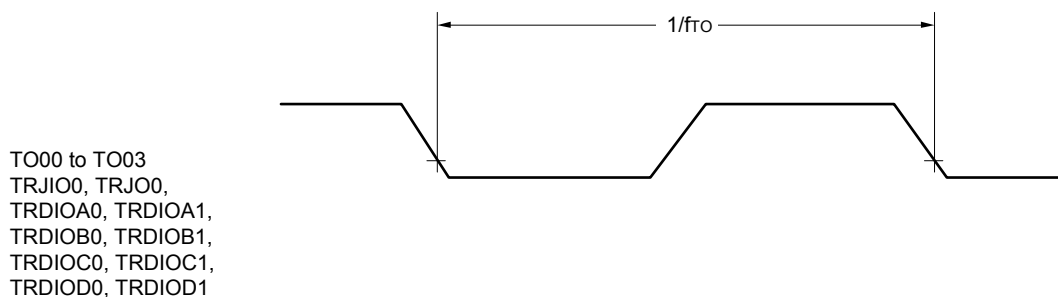
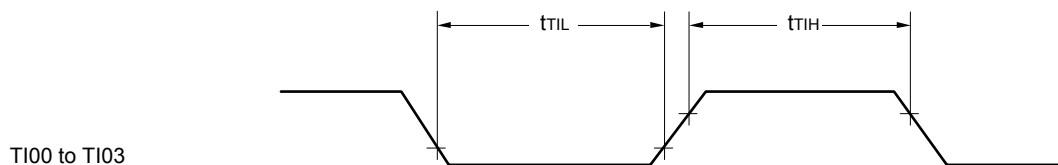
AC Timing Test Points



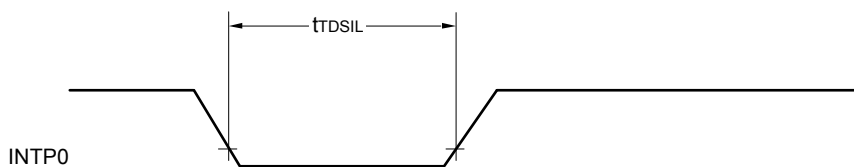
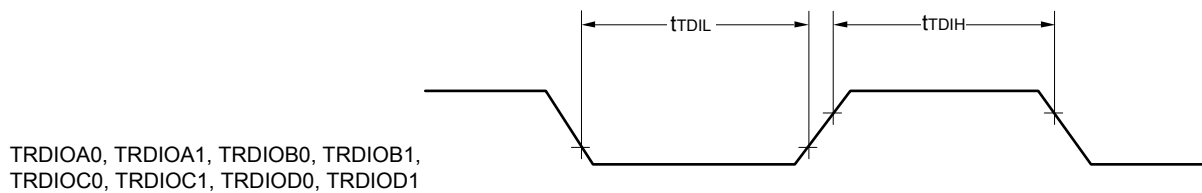
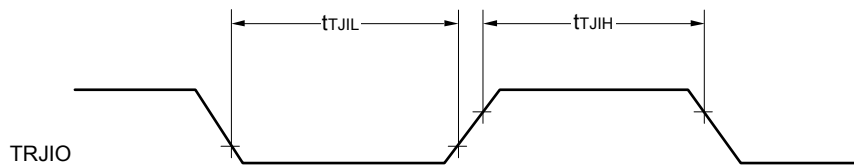
External System Clock Timing



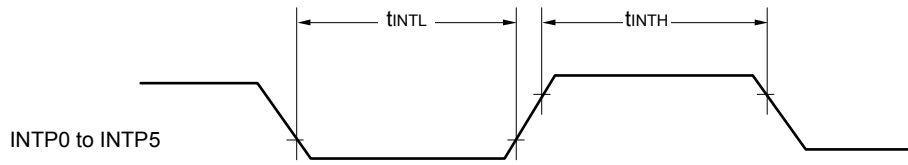
TI/TO Timing



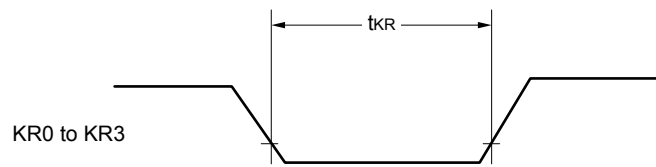
TO00 to TO03
 TRJIO0, TRJO0,
 TRDIOA0, TRDIOA1,
 TRDIOB0, TRDIOB1,
 TRDIOC0, TRDIOC1,
 TRDIOD0, TRDIOD1



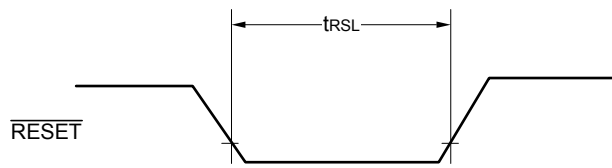
Interrupt Request Input Timing



Key Interrupt Input Timing

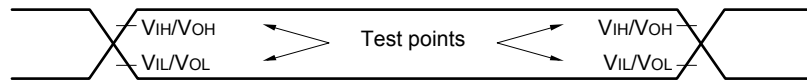


$\overline{\text{RESET}}$ Input Timing



2.6 Peripheral Functions Characteristics

AC Timing Test Points



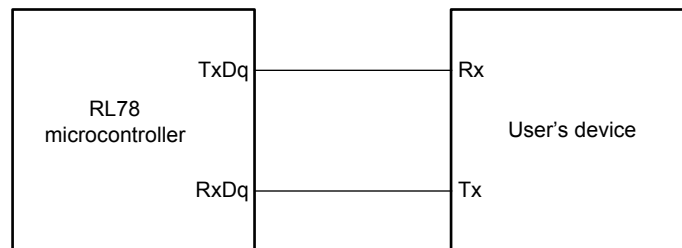
2.6.1 Serial array unit

(1) During communication at same potential (UART mode)

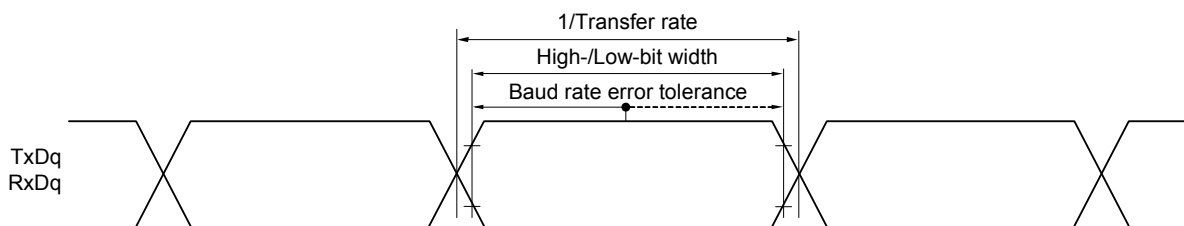
(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1		2.7 V ≤ VDD ≤ 5.5 V		fMCK/6		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 2		4.0		1.3	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ VDD ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (2.7 V ≤ VDD ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 5)

Remark 2. fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 2/f _{CLK}	2.7 V ≤ V _{DD} ≤ 5.5 V	83.3		250		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V		t _{KCY1} /2 - 7		t _{KCY1} /2 - 50		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V		t _{KCY1} /2 - 10		t _{KCY1} /2 - 50		ns
Slp setup time (to SCKp↑) Note 1	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V		23		110		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V		33		110		ns
Slp hold time (from SCKp↑) Note 2	t _{KSI1}	2.7 V ≤ V _{DD} ≤ 5.5 V		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t _{KSO1}	C = 20 pF Note 4			10		10	ns

Note 1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

Note 2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

Note 3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. This value is valid only when CSI00's peripheral I/O redirect function is not used.

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number,
n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$ $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	167		500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 12$		$t_{KCY1}/2 - 50$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 18$		$t_{KCY1}/2 - 50$		ns
Slp setup time (to SCKp \uparrow) Note 1	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	44		110		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	44		110		ns
Slp hold time (from SCKp \uparrow) Note 2	t_{KSI1}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	19		19		ns
Delay time from SCKp \downarrow to SOp output Note 3	t_{KSO1}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ $C = 30\text{ pF}$ Note 4		25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp \uparrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

Remark 2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number, n: Channel number (mn = 00))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 5}	tkCY2	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$20\text{ MHz} < f_{MCK}$	$8/f_{MCK}$		—		ns
			$f_{MCK} \leq 20\text{ MHz}$	$6/f_{MCK}$		$6/f_{MCK}$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$16\text{ MHz} < f_{MCK}$	$8/f_{MCK}$		—		ns
			$f_{MCK} \leq 16\text{ MHz}$	$6/f_{MCK}$		$6/f_{MCK}$		ns
SCKp high-/low-level width	tkH2, tkL2	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$tkCY2/2 - 7$		$tkCY2/2 - 7$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$tkCY2/2 - 8$		$tkCY2/2 - 8$		ns
Slp setup time (to SCKp \uparrow) ^{Note 1}	tsIK2	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 20$		$1/f_{MCK} + 30$		ns
Slp hold time (from SCKp \uparrow) ^{Note 2}	tkSI2	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 31$		$1/f_{MCK} + 31$		ns
Delay time from SCKp \downarrow to SOp output ^{Note 3}	tkSO2	$C = 30\text{ pF}$ ^{Note 4}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$2/f_{MCK} + 44$		$2/f_{MCK} + 110$	ns
$\overline{\text{SSI00}}$ setup time	tSSI K	DAPmn = 0	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	120		120		ns
		DAPmn = 1	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$1/f_{MCK} + 120$		$1/f_{MCK} + 120$		ns
$\overline{\text{SSI00}}$ hold time	tkSSI	DAPmn = 0	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$1/f_{MCK} + 120$		$1/f_{MCK} + 120$		ns
		DAPmn = 1	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	120		120		ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp \uparrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

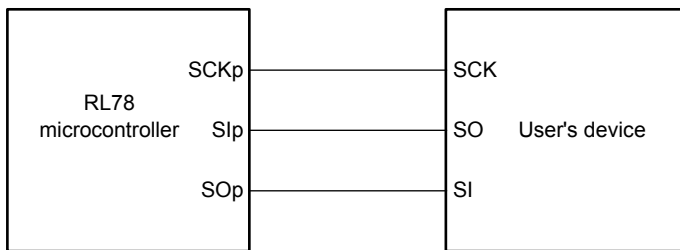
Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

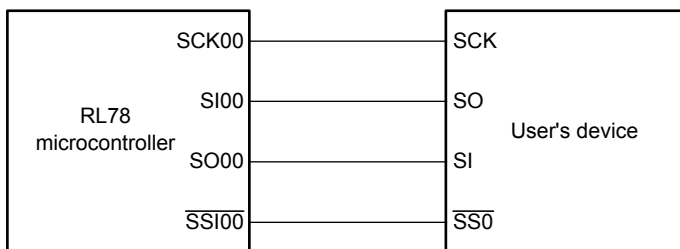
Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

CSI mode connection diagram (during communication at same potential)



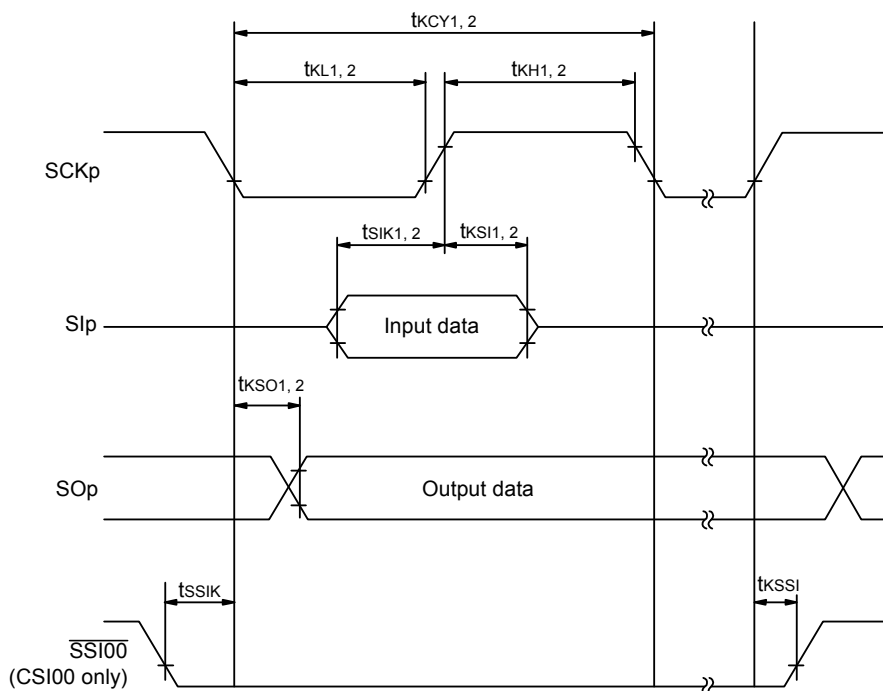
**CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))**



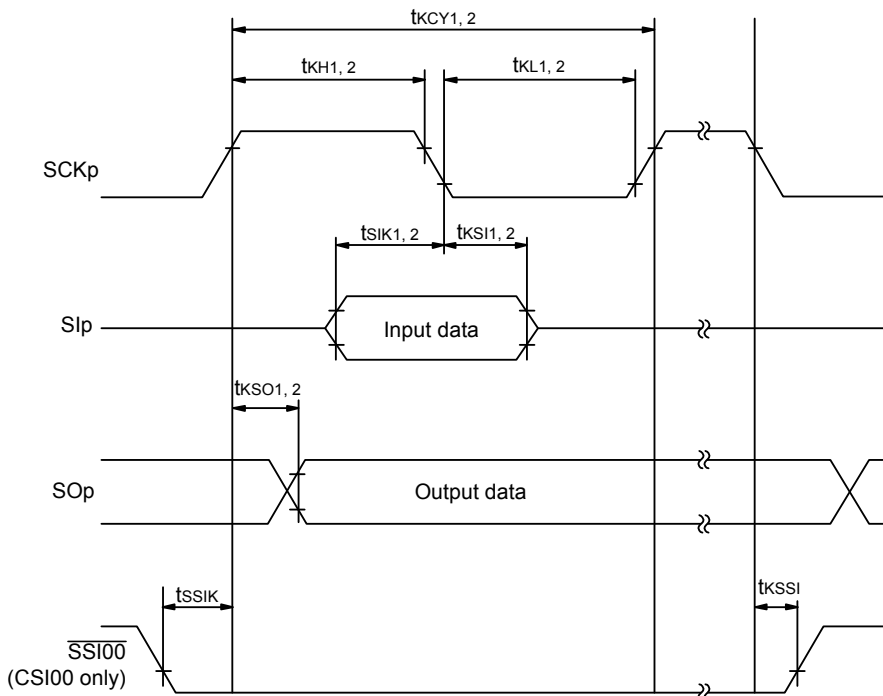
Remark 1. p: CSI number (p = 00)

Remark 2. m: Unit number, n: Channel number (mn = 00)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00)

Remark 2. m: Unit number, n: Channel number (mn = 00)

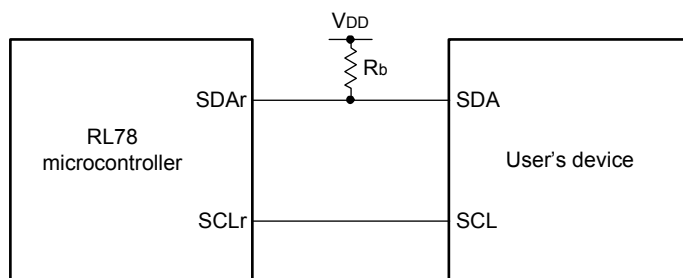
(5) During communication at same potential (simplified I²C mode)**(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		400 Note 1	kHz
		2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ		400 Note 1		400 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1150		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		1150		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1150		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		1150		ns
Data setup time (reception)	t _{SU: DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 85 Note 2		1/f _{MCK} + 145 Note 2		ns
		2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 Note 2		1/f _{MCK} + 145 Note 2		ns
Data hold time (transmission)	t _{HD: DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	ns
		2.7 V ≤ V _{DD} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	355	0	355	ns

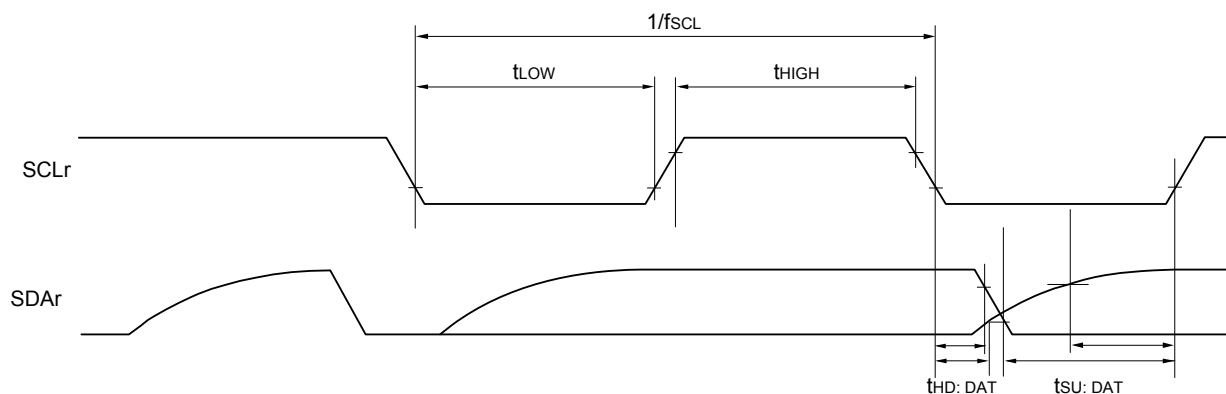
Note 1. The value must also be equal to or less than f_{MCK}/4.**Note 2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Caution Select the normal input buffer and the N-ch open drain output (VDD tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Remark 1. Rb[Ω]: Communication line (SDAr) pull-up resistance, Cb[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00), g: PIM number (g = 3, 5), h: POM number (h = 3, 5)

Remark 3. fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0),

n: Channel number (n = 0), mn = 00)

(6) Communication at different potential (2.5 V, 3 V) (UART mode)**($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit	
			MIN.	MAX.	MIN.	MAX.		
Transfer rate		Reception	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		4.0		1.3	Mbps
			$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$		$f_{MCK}/6$ Note 1		$f_{MCK}/6$ Note 1	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		4.0		1.3	Mbps
			$2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$		$f_{MCK}/6$ Notes 1, 2		$f_{MCK}/6$ Notes 1, 2	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3		4.0		1.3	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when $FRQSEL4 = 1$.

Note 2. Use it with $V_{DD} \geq V_b$.

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)
LS (low-speed main) mode: 8 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remark 1. $V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 5)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03))

Remark 4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.

$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$: $V_{IH} = 2.2\text{ V}$, $V_{IL} = 0.8\text{ V}$

$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$: $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.5\text{ V}$

$2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$: $V_{IH} = 1.50\text{ V}$, $V_{IL} = 0.32\text{ V}$

(6) Communication at different potential (2.5 V, 3 V) (UART mode)**(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit	
			MIN.	MAX.	MIN.	MAX.		
Transfer rate		transmission	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V		1.2 Note 4		1.2 Note 4	Mbps
			2.7 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V		Note 5, 6		Note 5, 6	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V		0.43 Note 7		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ and $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ and $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with $V_{DD} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using $f_{mck}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

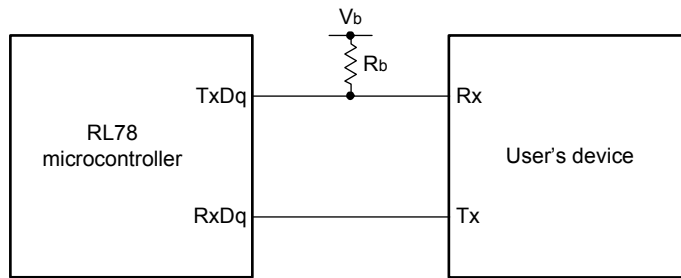
Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 5)

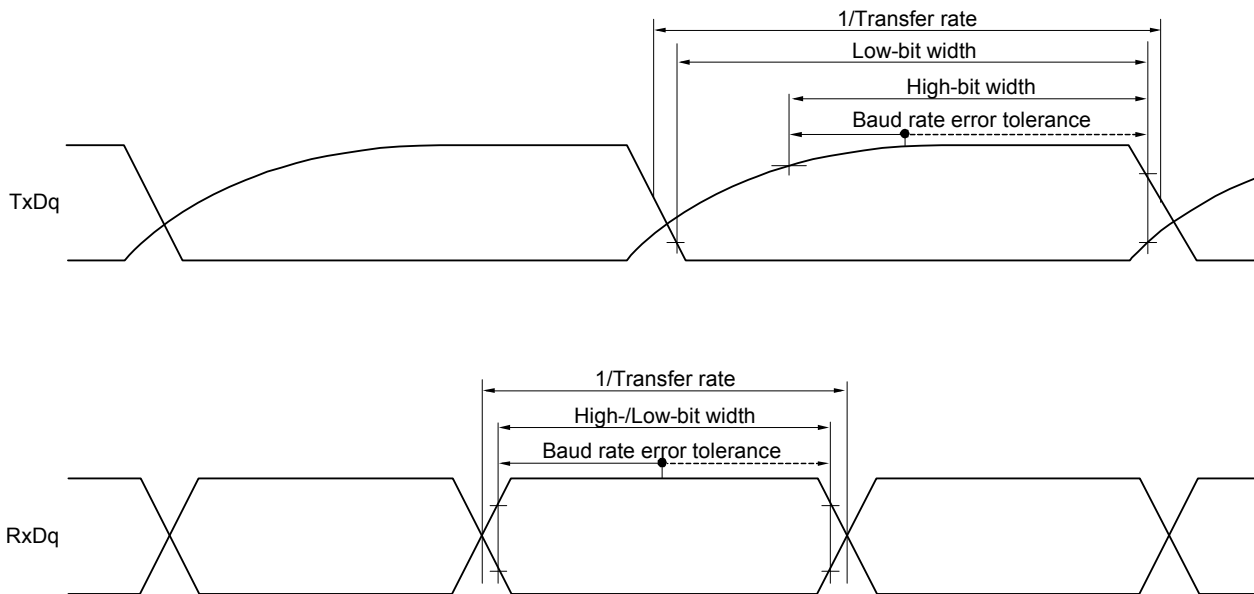
Remark 3. f_{mck} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03))

Remark 4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.
 $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$: $V_{IH} = 2.2\text{ V}$, $V_{IL} = 0.8\text{ V}$
 $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$: $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.5\text{ V}$
 $2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$: $V_{IH} = 1.50\text{ V}$, $V_{IL} = 0.32\text{ V}$

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 5)

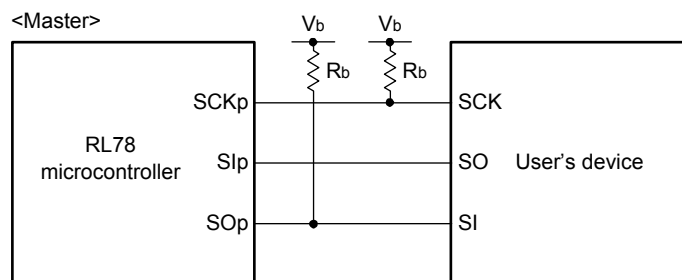
(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 2/f _{CLK} 4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	200		1150		ns
			300		1150		ns
SCKp high-level width	t _{KH1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 50		t _{KCY1} /2 - 50		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 120		t _{KCY1} /2 - 120		ns
SCKp low-level width	t _{KL1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 7		t _{KCY1} /2 - 50		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 10		t _{KCY1} /2 - 50		ns
Slp setup time (to SCKp↑) Note 1	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	58		479		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	121		479		ns
Slp hold time (from SCKp↑) Note 1	t _{KSI1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	10		10		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	10		10		ns
Delay time from SCKp↓ to SOP output Note 1	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		60		60	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		130		130	ns
Slp setup time (to SCKp↓) Note 2	t _{SIK1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	23		110		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	33		110		ns
Slp hold time (from SCKp↓) Note 2	t _{KSI1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	10		10		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	10		10		ns
Delay time from SCKp↑ to SOP output Note 2	t _{KSO1}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ		10		10	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ		10		10	ns

(Notes, Caution and Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

Remark 3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Remark 4. This value is valid only when CSI00's peripheral I/O redirect function is not used.

(8) Communication at different potential (2.5 V, 3 V) (fmck/4) (CSI mode) (master mode, SCKp... internal clock output)
($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)(1/2)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 \geq 4/fCLK 4.0 V \leq V _{DD} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V, C _b = 30 pF, R _b = 1.4 k Ω	300		1150		ns
			500		1150		ns
			1150		1150		ns
SCKp high-level width	tkH1	4.0 V \leq V _{DD} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V, C _b = 30 pF, R _b = 1.4 k Ω 2.7 V \leq V _{DD} < 4.0 V, 2.3 V \leq V _b \leq 2.7 V, C _b = 30 pF, R _b = 2.7 k Ω 2.7 V \leq V _{DD} < 3.3 V, 1.6 V \leq V _b \leq 2.0 V, C _b = 30 pF, R _b = 5.5 k Ω	tkCY1/2 - 75		tkCY1/2 - 75		ns
			tkCY1/2 - 170		tkCY1/2 - 170		ns
			tkCY1/2 - 458		tkCY1/2 - 458		ns
SCKp low-level width	tkL1	4.0 V \leq V _{DD} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V, C _b = 30 pF, R _b = 1.4 k Ω 2.7 V \leq V _{DD} < 4.0 V, 2.3 V \leq V _b \leq 2.7 V, C _b = 30 pF, R _b = 2.7 k Ω 2.7 V \leq V _{DD} < 3.3 V, 1.6 V \leq V _b \leq 2.0 V, C _b = 30 pF, R _b = 5.5 k Ω	tkCY1/2 - 12		tkCY1/2 - 50		ns
			tkCY1/2 - 18		tkCY1/2 - 50		ns
			tkCY1/2 - 50		tkCY1/2 - 50		ns

Caution 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Caution 2. Use it with V_{DD} \geq V_b.

Remark 1. R_b[Ω]: Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

Remark 3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

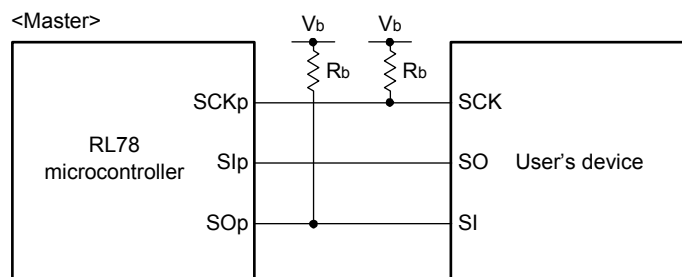
4.0 V \leq V_{DD} \leq 5.5 V, 2.7 V \leq V_b \leq 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

2.7 V \leq V_{DD} < 4.0 V, 2.3 V \leq V_b \leq 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

(8) Communication at different potential (2.5 V, 3 V) (fmck/4) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) Note 1	tsIK1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	81		479		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		ns
		2.7 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	479		479		ns
Slp hold time (from SCKp↑) Note 1	tkSI1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		ns
		2.7 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	19		19		ns
Delay time from SCKp↓ to SOp output Note 1	tkSO1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		100		100	ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195	ns
		2.7 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ		483		483	ns
Slp setup time (to SCKp↓) Note 2	tsIK1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	44		110		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		110		ns
		2.7 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	110		110		ns
Slp hold time (from SCKp↓) Note 2	tkSI1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		ns
		2.7 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	19		19		ns
Delay time from SCKp↑ to SOp output Note 2	tkSO1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		25		25	ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25	ns
		2.7 V ≤ VDD < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ		25		25	ns

(Notes, Caution and Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution 1. Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Caution 2. Use it with $V_{DD} \geq V_b$.

Remark 1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage

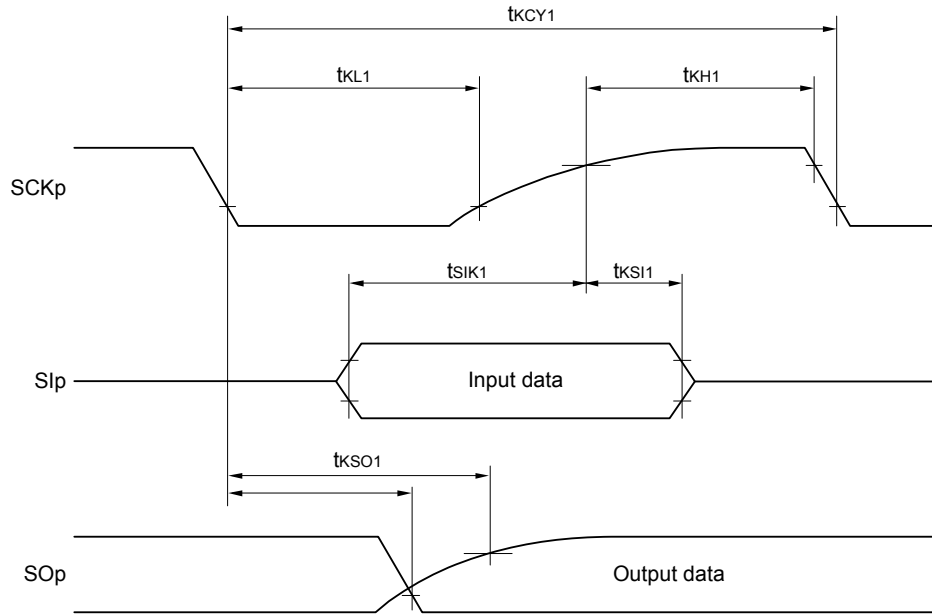
Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

Remark 3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

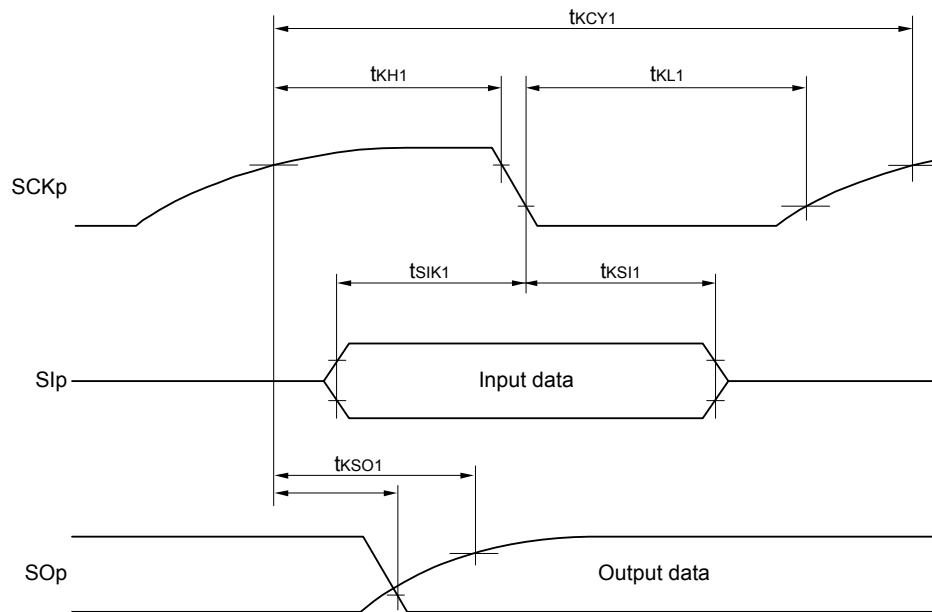
$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$: $V_{IH} = 2.2\text{ V}$, $V_{IL} = 0.8\text{ V}$

$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$: $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.5\text{ V}$

**CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



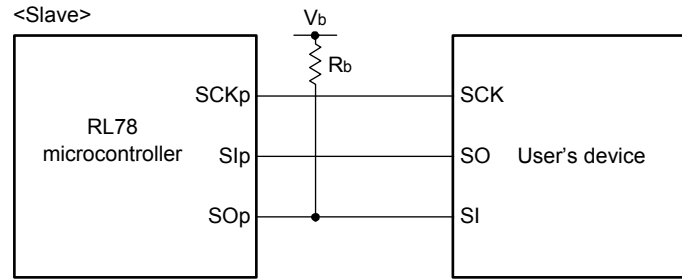
Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

(9) Communication at different potential (2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit	
			MIN.	MAX.	MIN.	MAX.		
SCKp cycle time ^{Note 1}	tkcy2	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$	$12/f_{MCK}$		—		ns
			$8\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$10/f_{MCK}$		—		ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$8/f_{MCK}$		$16/f_{MCK}$		ns
			$f_{MCK} \leq 4\text{ MHz}$	$6/f_{MCK}$		$10/f_{MCK}$		ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$	$16/f_{MCK}$		—		ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$14/f_{MCK}$		—		ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$12/f_{MCK}$		—		ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$8/f_{MCK}$		$16/f_{MCK}$		ns
		$2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$20\text{ MHz} < f_{MCK} \leq 24\text{ MHz}$	$36/f_{MCK}$		—		ns
			$16\text{ MHz} < f_{MCK} \leq 20\text{ MHz}$	$32/f_{MCK}$		—		ns
			$8\text{ MHz} < f_{MCK} \leq 16\text{ MHz}$	$26/f_{MCK}$		—		ns
			$4\text{ MHz} < f_{MCK} \leq 8\text{ MHz}$	$16/f_{MCK}$		$16/f_{MCK}$		ns
SCKp high-/low-level width	tkH2, tkL2	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	$tkcy2/2 - 12$		$tkcy2/2 - 50$		ns	
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	$tkcy2/2 - 18$		$tkcy2/2 - 50$		ns	
		$2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	$tkcy2/2 - 50$		$tkcy2/2 - 50$		ns	
Slp setup time (to SCKp \uparrow) ^{Note 2}	tsik2	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$1/f_{MCK} + 20$		$1/f_{MCK} + 30$		ns	
Slp hold time (from SCKp \uparrow) ^{Note 3}	tksl2		$1/f_{MCK} + 31$		$1/f_{MCK} + 31$		ns	
Delay time from SCKp \downarrow to SOp output ^{Note 4}	tkso2	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		$2/f_{MCK} + 120$		$2/f_{MCK} + 573$	ns	
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		$2/f_{MCK} + 214$		$2/f_{MCK} + 573$	ns	
		$2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_v = 5.5\text{ k}\Omega$		$2/f_{MCK} + 573$		$2/f_{MCK} + 573$	ns	

(Notes, Caution and Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and SCKp pin, and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. R_b[Ω]: Communication line (SO_p) pull-up resistance, C_b[F]: Communication line (SO_p) load capacitance, V_b[V]: Communication line voltage

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}).
m: Unit number, n: Channel number (mn = 00))

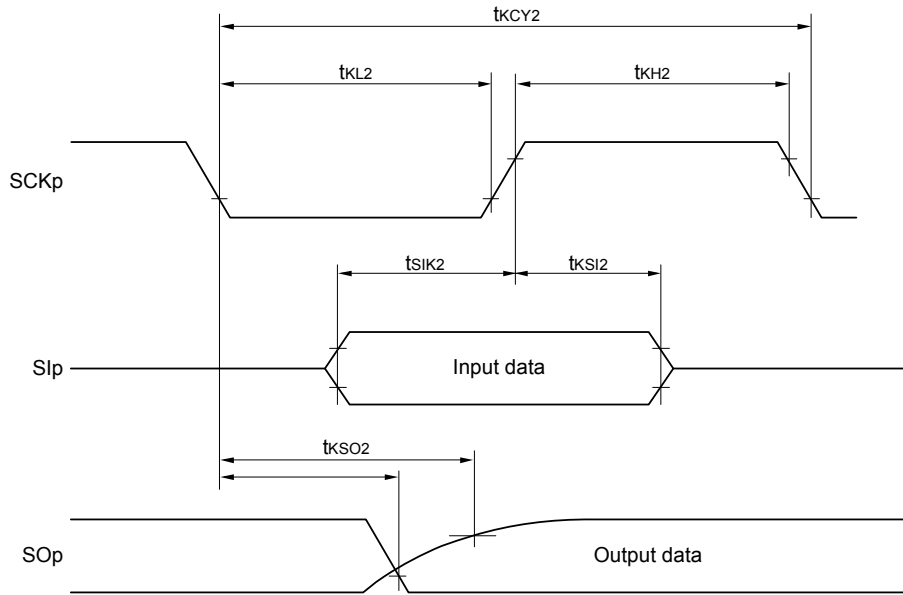
Remark 4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V

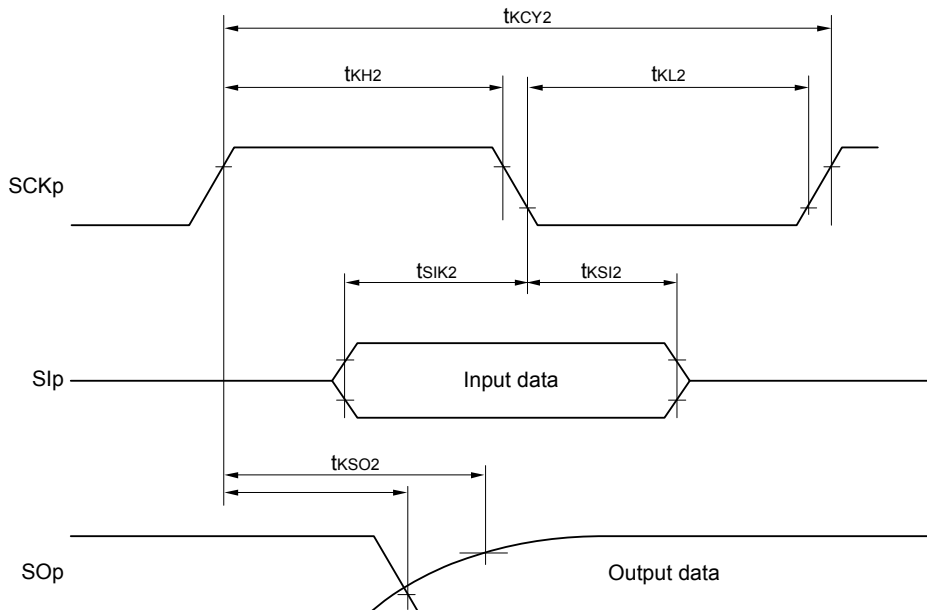
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Remark 5. Communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

Remark 2. Communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

(10) Communication at different potential (2.5 V, 3 V) (simplified I²C mode)**(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		300 Note 1	kHz
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		300 Note 1	kHz
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		400 Note 1		300 Note 1	kHz
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		400 Note 1		300 Note 1	kHz
		2.7 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b < 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1550		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1550		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1150		1550		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1150		1550		ns
		2.7 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b < 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ	1550		1550		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	245		610		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	200		610		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	675		610		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	600		610		ns
		2.7 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b < 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ	610		610		ns

(Notes, Caution and Remarks are listed on the next page.)

(10) Communication at different potential (2.5 V, 3 V) (simplified I²C mode)**(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)****(2/2)**

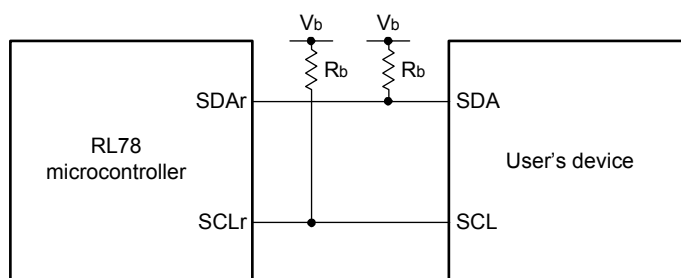
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 Note 3		1/f _{MCK} + 190 Note 3		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 Note 3		1/f _{MCK} + 190 Note 3		ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
		2.7 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b < 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
Data hold time (transmission)	t _{HD:DAT}	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	ns
		4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	355	0	355	ns
		2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	0	355	ns
		2.7 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b < 2.0 V Note 2, C _b = 100 pF, R _b = 5.5 kΩ	0	405	0	405	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.**Note 2.** Use it with V_{DD} ≥ V_b.**Note 3.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

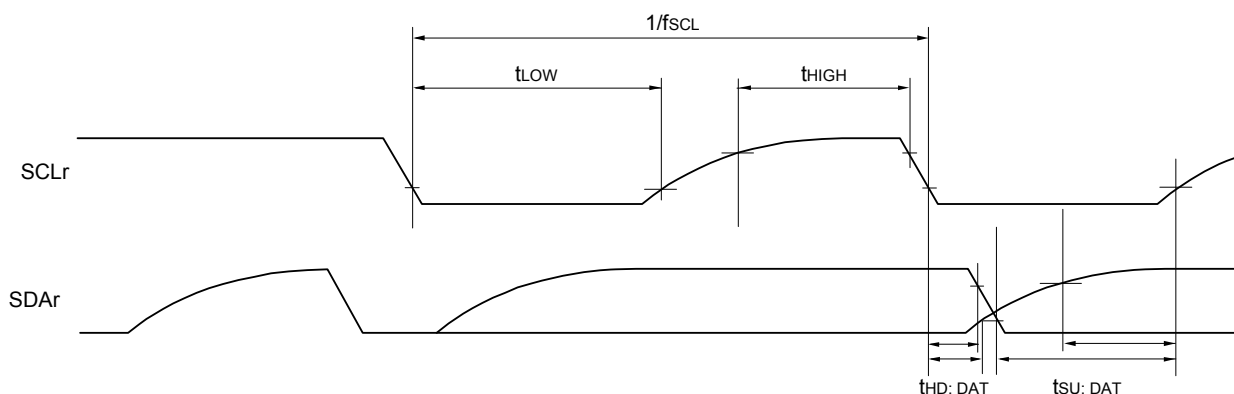
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. r: IIC number (r = 00), g: PIM, POM number (g = 3, 5)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0), mn = 00)

Remark 4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in simplified I²C mode.

$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$: $V_{IH} = 2.2\text{ V}$, $V_{IL} = 0.8\text{ V}$

$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$: $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.5\text{ V}$

2.7 Analog Characteristics

2.7.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage	Reference voltage (+) = AVREFP Reference voltage (-) = AVREFM	Reference voltage (+) = VDD Reference voltage (-) = VSS	Reference voltage (+) = VBGR Reference voltage (-) = AVREFM
ANI0 to ANI7		Refer to 2.7.1 (1).	Refer to 2.7.1 (3).	Refer to 2.7.1 (4).
ANI16 to ANI19		Refer to 2.7.1 (2).		
Internal reference voltage Temperature sensor output voltage		Refer to 2.7.1 (1).		—

(1) When AVREF (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin: ANI2 to ANI7

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	tCONV	10-bit resolution AVREFP = VDD	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V			±0.25	% FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V			±0.25	% FSR
Integral linearity error Note 1	ILE	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V			±2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V			±1.5	LSB
Reference voltage (+)	AVREFP			2.7		VDD	V
Analog input voltage	VAIN			0		AVREFP	V
	VBGR	Select internal reference voltage output, 2.7 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode		1.38	1.45	1.5	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

(2) When $AV_{REF} (+) = AV_{REFP}/ANI0$ ($ADREFP1 = 0, ADREFP0 = 1$), $AV_{REF} (-) = AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin: ANI16 to ANI19

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 5.0	LSB
Conversion time	tCONV	10-bit resolution $AV_{REFP} = V_{DD}$	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.35	% FSR
Full-scale error ^{Notes 1, 2}	EFS	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.35	% FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 3.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Reference voltage (+)	AV_{REFP}			2.7		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP}	V
	V_{BGR}	Select internal reference voltage output, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode		1.38	1.45	1.5	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

- (3) When $AV_{REF}(+) = V_{DD}$ ($ADREFP1 = 0$, $ADREFP0 = 0$), $AV_{REF}(-) = V_{SS}$ ($ADREFM = 0$),
target ANI pin: ANI0 to ANI7, ANI16 to ANI19

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
Conversion time	tCONV	10-bit resolution	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	% FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	% FSR
Integral linearity error Note 1	ILE	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Analog input voltage	VAIN	ANI0 to ANI7		0		V_{DD}	V
		ANI16 to ANI19		0		V_{DD}	V
	VBGR	Select internal reference voltage output, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode		1.38	1.45	1.5	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

(4) When $AV_{REF} (+)$ = Internal reference voltage ($ADREFP1 = 1$, $ADREFP0 = 0$), $AV_{REF} (-)$ = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin: ANI0 to ANI7, ANI16 to ANI19

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{BGR} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t _{CONV}	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error Notes 1, 2	EZS	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			±0.60	% FSR
Integral linearity error Note 1	ILE	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			±1.0	LSB
Reference voltage (+)	V _{BGR}			1.38	1.45	1.5	V
Analog input voltage	V _{AIN}			0		V _{BGR}	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

2.7.2 Temperature sensor characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Reference output voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		-3.6		$\text{mV}/^\circ\text{C}$
Operation stabilization wait time	t_{AMP}		5			μs

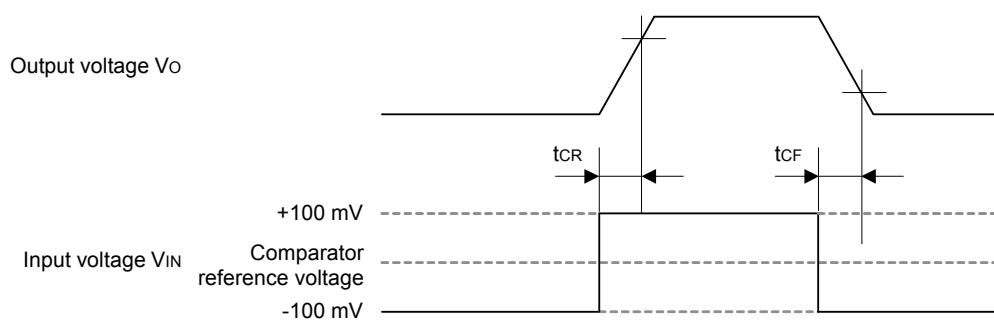
2.7.3 Comparator

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOCOMP}			± 5	± 40	mV
Input voltage range	V_{ICMP}		0		V_{DD}	V
Internal reference voltage deviation	ΔV_{IREF}	CmRVM register value: 7FH to 80H ($m = 0, 1$)			± 2	LSB
		Other than above			± 1	LSB
Response time	t_{CR}, t_{CF}	Input amplitude = $\pm 100\text{ mV}$		70	150	ns
Operation stabilization time Note 1	t_{CMP}	CMPnEN = 0 \rightarrow 1 $V_{DD} = 3.3$ to 5.5 V			1	μs
			$V_{DD} = 2.7$ to 3.3 V			
Reference voltage stabilization wait time	t_{VR}	CVRE: 0 \rightarrow 1 Note 2			20	μs

Note 1. Time required after the operation enable signal of the comparator has been changed (CMPnEN = 0 \rightarrow 1) until a state satisfying the DC and AC characteristics of the comparator is entered.

Note 2. Enable operation of internal reference voltage generation (CVREm bit = 1; $m = 0, 1$) and wait for the operation stabilization wait time before enabling the comparator output (CnOE bit = 1; $n = 0, 1$).



2.7.4 Programmable gain amplifier

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOPGA}			± 5	± 10	mV
Input voltage range	V_{IPGA}		0		$0.9 \times V_{DD}/\text{gain}$	V
Response time	V_{OHPGA}		$0.9 \times V_{DD}$			V
	V_{OLPGA}				$0.1 \times V_{DD}$	
Gain error	—	4, 8 times			± 1	%
		16 times			± 1.5	
		32 times			± 2	
Slew rate	SR_{RPGA}	Rising edge	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.4		V/ μs
			$2.7\text{ V} \leq V_{DD} \leq 4.0\text{ V}$	0.5		
	SR_{FPGA}	Falling edge	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.4		
			$2.7\text{ V} \leq V_{DD} \leq 4.0\text{ V}$	0.5		
Operation stabilization wait time Note	t_{PGA}	4, 8 times			5	μs
		16, 32 times			10	

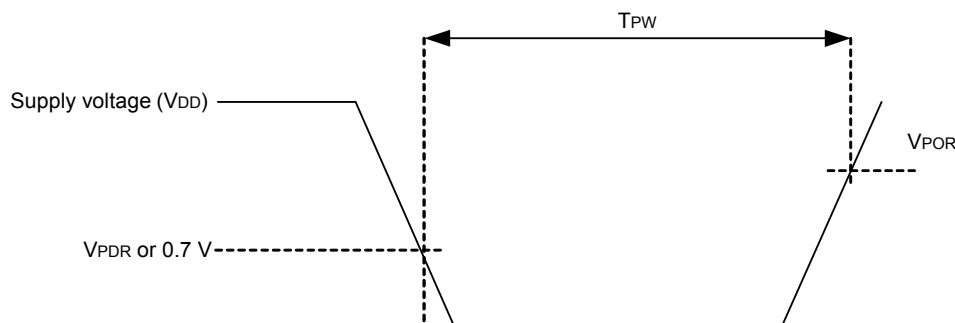
Note Time required after the PGA operation has been enabled ($PGAEN = 1$) until a state satisfying the DC and AC specifications of the PGA is entered.

2.7.5 POR circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width Note	t_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HISTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.7.6 LVD circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Detection voltage	Supply voltage level	VLVD0	Power supply rise time	3.98	4.06	4.14	V		
			Power supply fall time	3.90	3.98	4.06	V		
		VLVD1	Power supply rise time	3.68	3.75	3.82	V		
			Power supply fall time	3.60	3.67	3.74	V		
		VLVD2	Power supply rise time	3.07	3.13	3.19	V		
			Power supply fall time	3.00	3.06	3.12	V		
		VLVD3	Power supply rise time	2.96	3.02	3.08	V		
			Power supply fall time	2.90	2.96	3.02	V		
		VLVD4	Power supply rise time	2.86	2.92	2.97	V		
			Power supply fall time	2.80	2.86	2.91	V		
		VLVD5	Power supply rise time	2.76	2.81	2.87	V		
			Power supply fall time	2.70	2.75	2.81	V		
		Minimum pulse width		t _{LW}		300			μs
		Detection delay time		t _{LD}				300	μs

Remark VLVD_(n-1) > VLVD_n: n = 1 to 5

LVD Detection Voltage of Interrupt & Reset Mode**($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Interrupt and reset mode	V _{LVD5}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage: 2.7 V	2.70	2.75	2.81	V	
	V _{LVD4}	LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVD3}	LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V _{LVD0}	LVIS1, LVIS0 = 0, 0 (+1.2 V)	Rising release reset voltage	3.98	4.06	4.14	V
Falling interrupt voltage			3.90	3.98	4.06	V	

2.7.7 Power supply voltage rising slope characteristics**($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S _{VDD}				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.5 AC Characteristics.

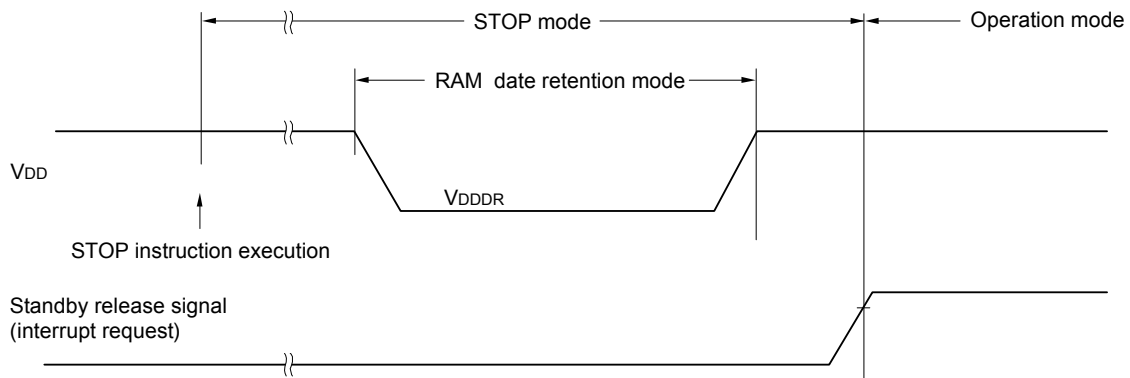
2.8 RAM Data Retention Characteristics

($T_A = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 Note		5.5	V

<R>

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



2.9 Flash Memory Programming Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	fCLK	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		24	MHz
Number of code flash rewrites ^{Notes 1, 2, 3}	C _{erwr}	Retained for 20 years $T_A = 85^\circ\text{C}$ ^{Note 3}	1,000			Times

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self programming library.

Note 3. These specifications show the characteristics of the flash memory and the results obtained from Renesas Electronics reliability testing.

Remark When updating data multiple times, use the flash memory as one for updating data.

2.10 Dedicated Flash Memory Programmer Communication (UART)

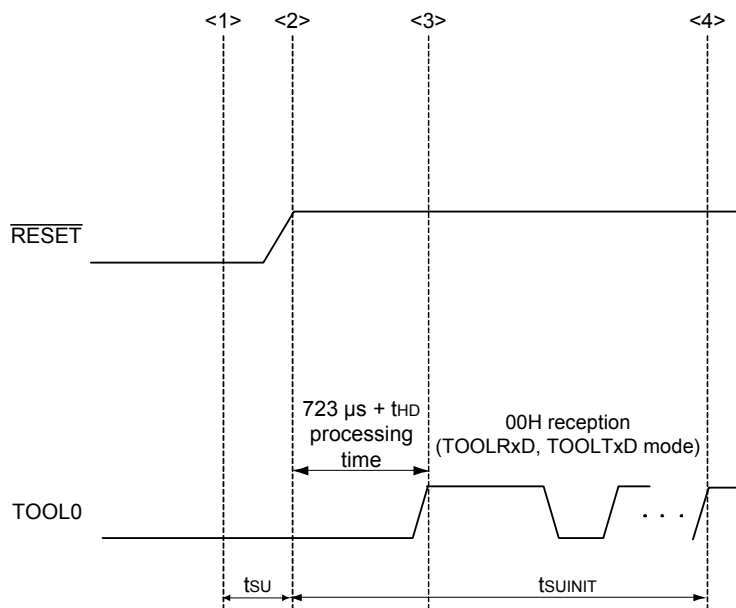
($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115.2 k		1 M	bps

2.11 Timing for Switching Flash Memory Programming Modes

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	tsuINIT	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	tsu	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	tHD	POR and LVD reset must end before the external reset ends.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset ends (POR and LVD reset must end before the external reset ends.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsuINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

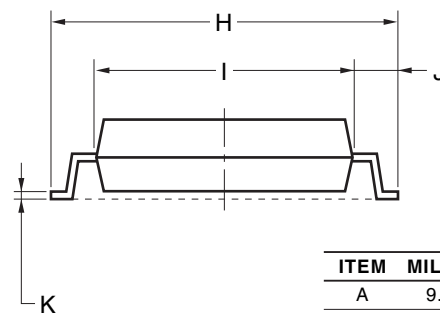
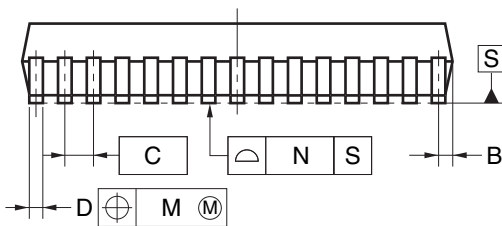
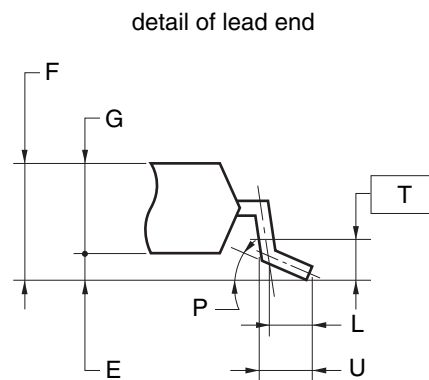
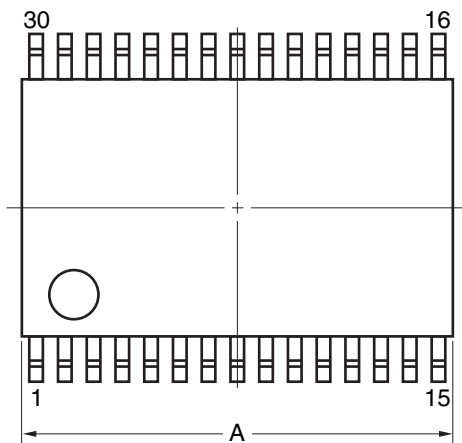
tHD: How long to keep the TOOL0 pin at the low level from when the external resets end (the flash firmware processing time is excluded)

3. PACKAGE DRAWINGS

3.1 30-pin Products

R5F11EA8ASP, R5F11EAAASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



NOTE

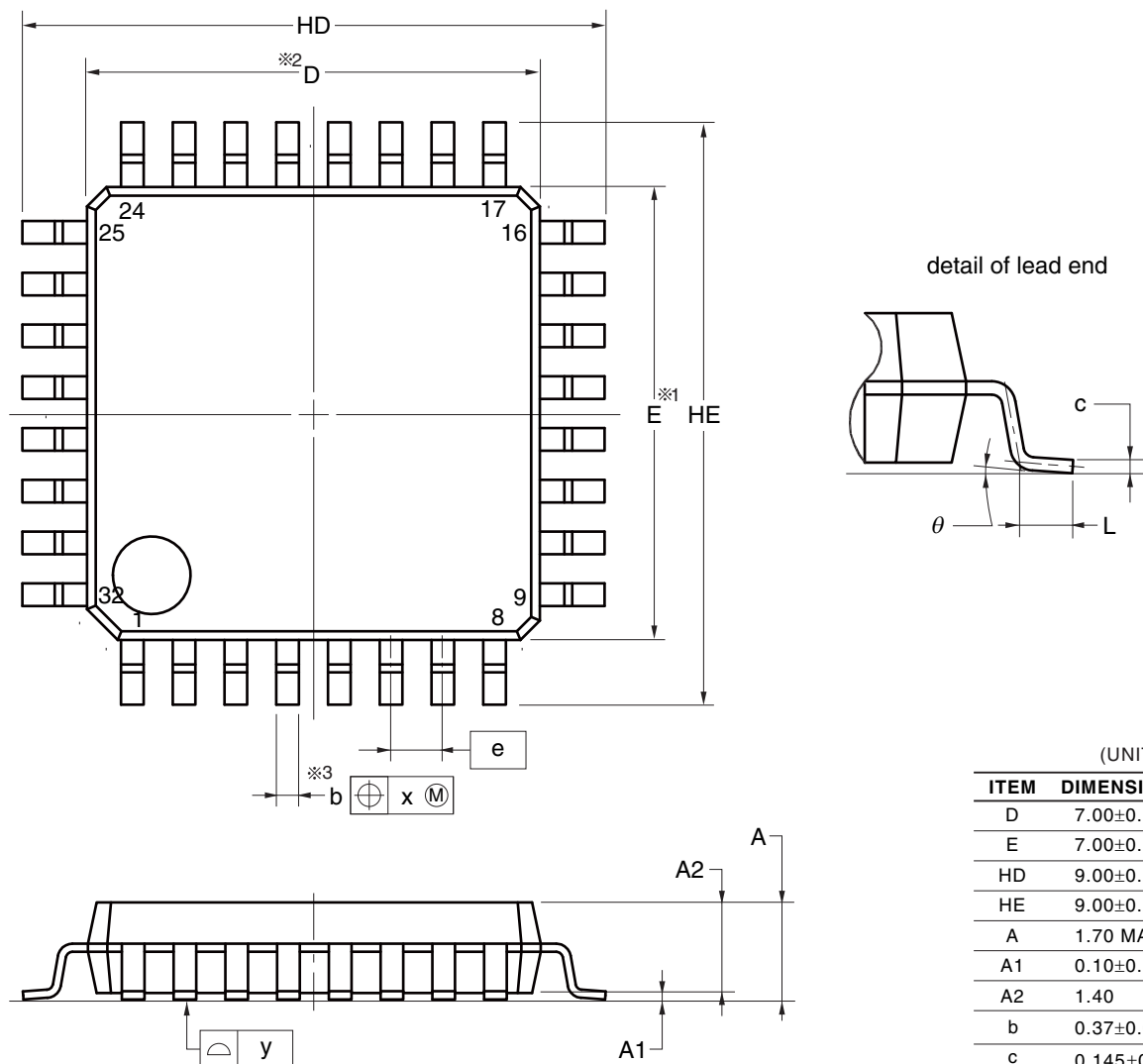
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15

3.2 32-pin Products

R5F11EB8AFP, R5F11EBAAFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

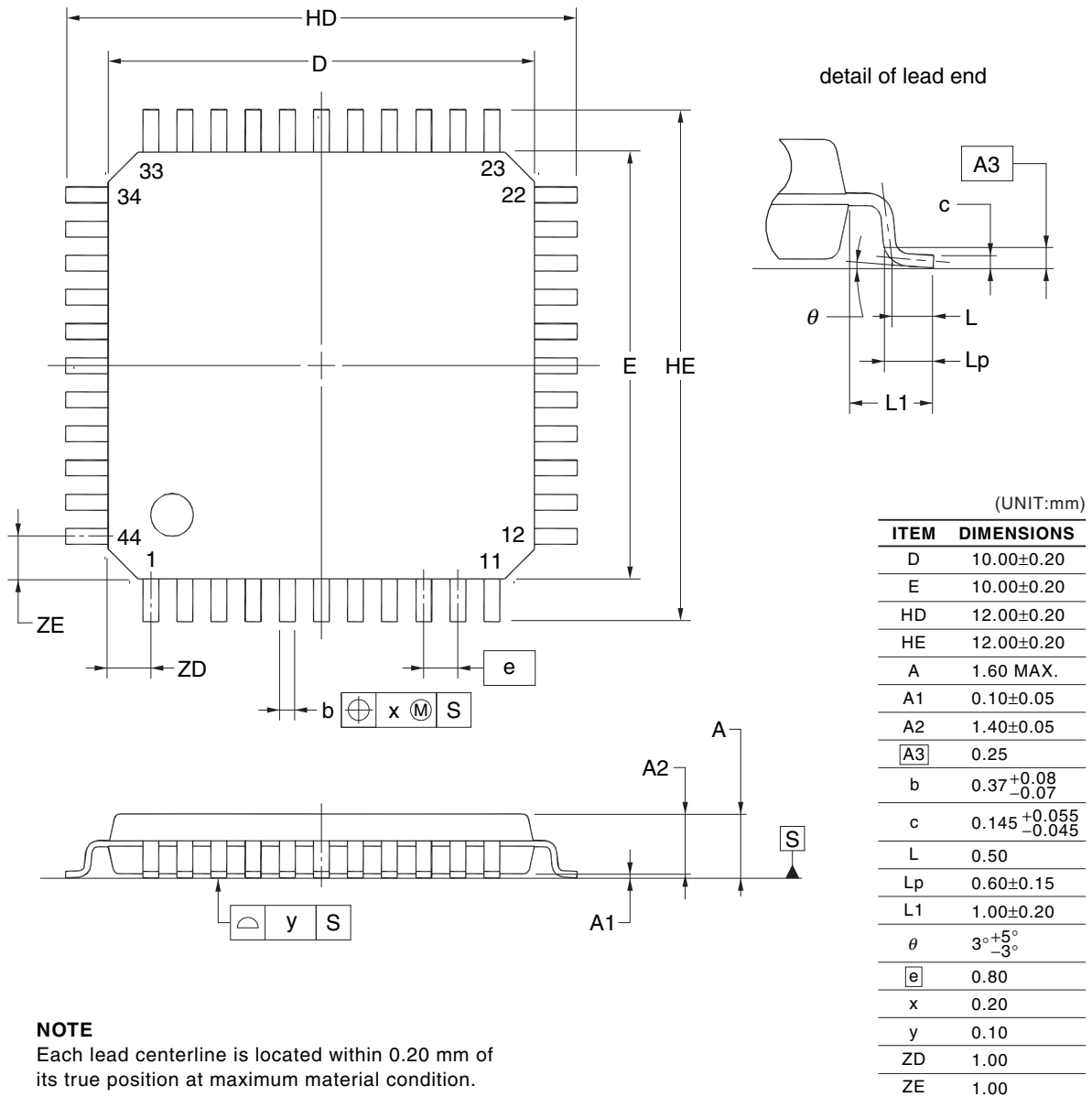
NOTE

1. Dimensions “ $\times 1$ ” and “ $\times 2$ ” do not include mold flash.
2. Dimension “ $\times 3$ ” does not include trim offset.

3.3 44-pin Products

R5F11EF8AFP, R5F11EFAAFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



NOTE
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

REVISION HISTORY	RL78/G1G Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Jul 31, 2014	—	First Edition issued
1.20	Mar 25, 2015	1	Change of description in 1.1 Features
		3	Change of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1G
		3	Change of Table 1 - 1 Orderable Part Numbers
		11	Change of 1.6 Outline of Functions
1.30	Sep 30, 2016	1	Addition of Note to 1.1 Features
		4	Modification of Pin configuration in 1.3.1 30-pin products
		5	Modification of Pin configuration in 1.3.2 32-pin products
		6	Modification of Pin configuration in 1.3.3 44-pin products
		63	Change of Note in 2.8 RAM Data Retention Characteristics

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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