

MC33078, MC33079, NCV33078, NCV33079

Low Noise Dual/Quad Operational Amplifiers

The MC33078/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input voltage noise with high gain bandwidth product and slew rate. The all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source and sink AC frequency performance.

The MC33078/9 family offers both dual and quad amplifier versions and is available in the plastic DIP and SOIC packages (P and D suffixes).

Features

- Dual Supply Operation: ± 5.0 V to ± 18 V
- Low Voltage Noise: 4.5 nV/ $\sqrt{\text{Hz}}$
- Low Input Offset Voltage: 0.15 mV
- Low T.C. of Input Offset Voltage: 2.0 $\mu\text{V}/^\circ\text{C}$
- Low Total Harmonic Distortion: 0.002%
- High Gain Bandwidth Product: 16 MHz
- High Slew Rate: 7.0 V/ μs
- High Open Loop AC Gain: 800 @ 20 kHz
- Excellent Frequency Stability
- Large Output Voltage Swing: $+14.1$ V/ -14.6 V
- ESD Diodes Provided on the Inputs
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

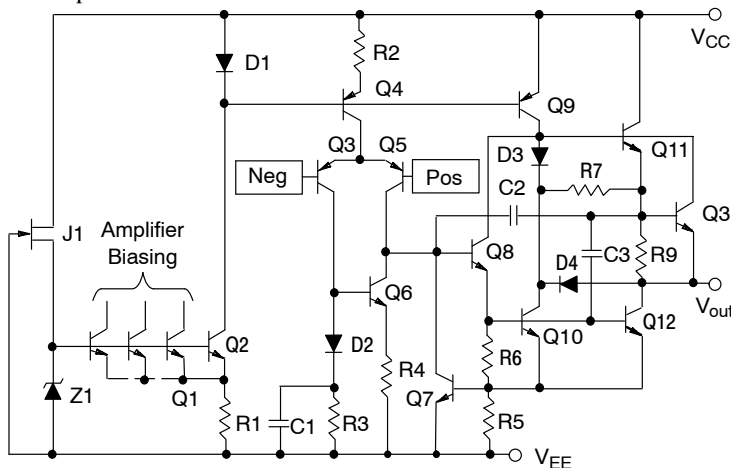


Figure 1. Representative Schematic Diagram
(Each Amplifier)



ON Semiconductor®

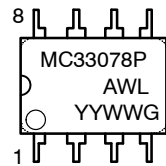
<http://onsemi.com>

MARKING DIAGRAMS

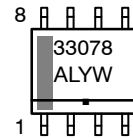
DUAL



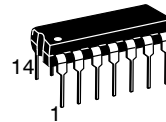
PDIP-8
P SUFFIX
CASE 626



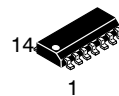
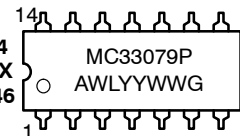
SOIC-8
D SUFFIX
CASE 751



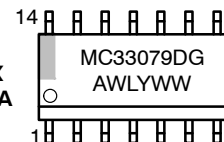
QUAD



PDIP-14
P SUFFIX
CASE 646



SOIC-14
D SUFFIX
CASE 751A



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	-60 to +150	°C
ESD Protection at any Pin MC33078/NCV33078 MC33079/NCV33079	V_{esd}	600 200 550 150	V
Maximum Power Dissipation	P_D	Note 2	mW
Operating Temperature Range	T_A	-40 to +85	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE} .
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

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DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 10\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) (MC33078) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$ (MC33079) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$	$ V_{IO} $	-	0.15	2.0	mV
Average Temperature Coefficient of Input Offset Voltage $R_S = 10\ \Omega$, $V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$, $T_A = T_{low}$ to T_{high}	$\Delta V_{IO}/\Delta T$	-	2.0	-	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$	I_{IB}	-	300	750	nA
Input Offset Current ($V_{CM} = 0\text{ V}$, $V_O = 0\text{ V}$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$	I_{IO}	-	25	150	nA
Common Mode Input Voltage Range ($\Delta V_{IO} = 5.0\text{ mV}$, $V_O = 0\text{ V}$)	V_{ICR}	± 13	± 14	-	V
Large Signal Voltage Gain ($V_O = \pm 10\text{ V}$, $R_L = 2.0\text{ k}\Omega$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$	A_{VOL}	90	110	-	dB
Output Voltage Swing ($V_{ID} = \pm 1.0\text{ V}$) $R_L = 600\ \Omega$ $R_L = 600\ \Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 2.0\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$	V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-}	-	+10.7	-	V
Common Mode Rejection ($V_{in} = \pm 13\text{ V}$)	CMR	80	100	-	dB
Power Supply Rejection (Note 3) $V_{CC}/V_{EE} = +15\text{ V}/-15\text{ V}$ to $+5.0\text{ V}/-5.0\text{ V}$	PSR	80	105	-	dB
Output Short Circuit Current ($V_{ID} = 1.0\text{ V}$, Output to Ground) Source Sink	I_{SC}	+15	+29	-	mA
Power Supply Current ($V_O = 0\text{ V}$, All Amplifiers) (MC33078) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$ (MC33079) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ\text{ to }+85^\circ\text{C}$	I_D	-	4.1	5.0	mA

3. Measured with V_{CC} and V_{EE} differentially varied simultaneously.

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AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V to } +10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1.0$)	SR	5.0	7.0	-	V/ μs
Gain Bandwidth Product ($f = 100\text{ kHz}$)	GBW	10	16	-	MHz
Unity Gain Bandwidth (Open Loop)	BW	-	9.0	-	MHz
Gain Margin ($R_L = 2.0\text{ k}\Omega$ $C_L = 0\text{ pF}$ $C_L = 100\text{ pF}$)	A_m	-	-11	-	dB
Phase Margin ($R_L = 2.0\text{ k}\Omega$ $C_L = 0\text{ pF}$ $C_L = 100\text{ pF}$)	ϕ_m	-	55	-	Deg
Channel Separation ($f = 20\text{ Hz to } 20\text{ kHz}$)	CS	-	-120	-	dB
Power Bandwidth ($V_O = 27\text{ V}_{pp}$, $R_L = 2.0\text{ k}\Omega$, THD $\pm 1.0\%$)	BW_p	-	120	-	kHz
Total Harmonic Distortion ($R_L = 2.0\text{ k}\Omega$, $f = 20\text{ Hz to } 20\text{ kHz}$, $V_O = 3.0\text{ V}_{rms}$, $A_V = +1.0$)	THD	-	0.002	-	%
Open Loop Output Impedance ($V_O = 0\text{ V}$, $f = 9.0\text{ MHz}$)	$ Z_O $	-	37	-	Ω
Differential Input Resistance ($V_{CM} = 0\text{ V}$)	R_{in}	-	175	-	$\text{k}\Omega$
Differential Input Capacitance ($V_{CM} = 0\text{ V}$)	C_{in}	-	12	-	pF
Equivalent Input Noise Voltage ($R_S = 100\ \Omega$, $f = 1.0\text{ kHz}$)	e_n	-	4.5	-	$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current ($f = 1.0\text{ kHz}$)	i_n	-	0.5	-	$\text{Hz}\sqrt{\text{pA}}$

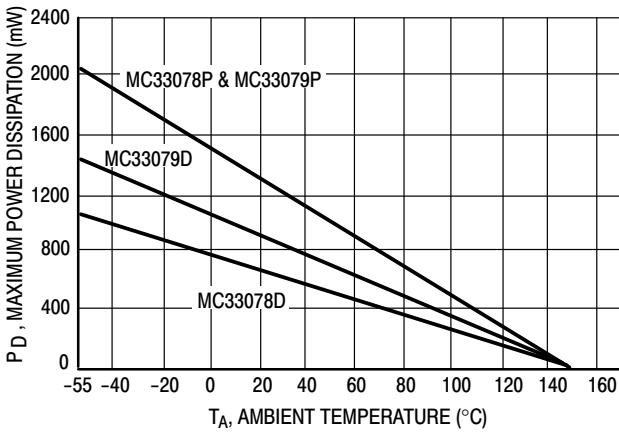


Figure 2. Maximum Power Dissipation versus Temperature

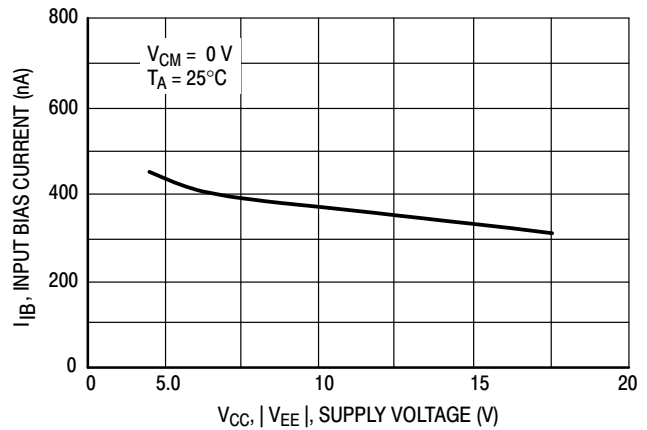


Figure 3. Input Bias Current versus Supply Voltage

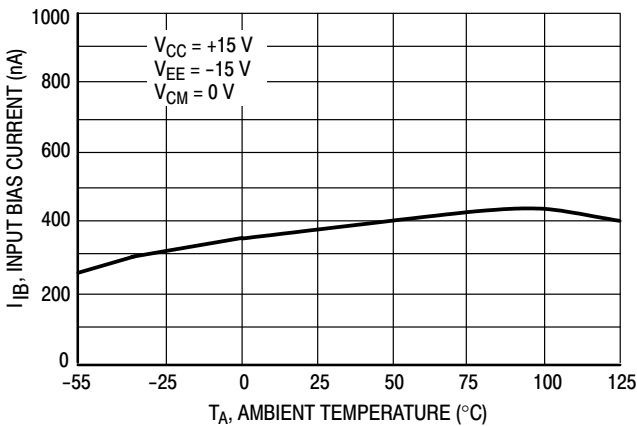


Figure 4. Input Bias Current versus Temperature

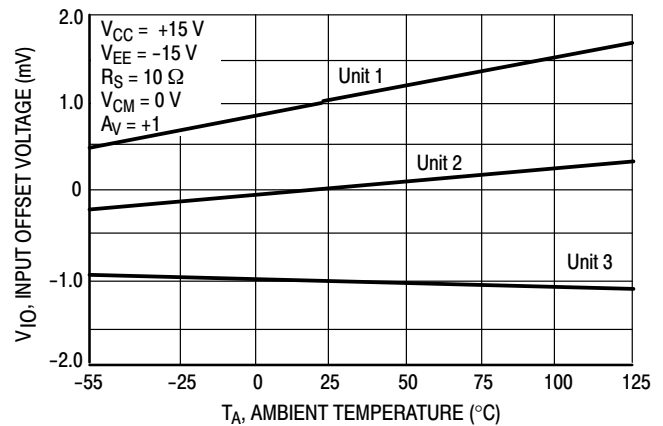


Figure 5. Input Offset Voltage versus Temperature

MC33078, MC33079, NCV33078, NCV33079



Figure 6. Input Bias Current versus Common Mode Voltage



Figure 7. Input Common Mode Voltage Range versus Temperature



Figure 8. Output Saturation Voltage versus Load Resistance to Ground



Figure 9. Output Short Circuit Current versus Temperature



Figure 10. Supply Current versus Temperature



Figure 11. Common Mode Rejection versus Frequency

MC33078, MC33079, NCV33078, NCV33079

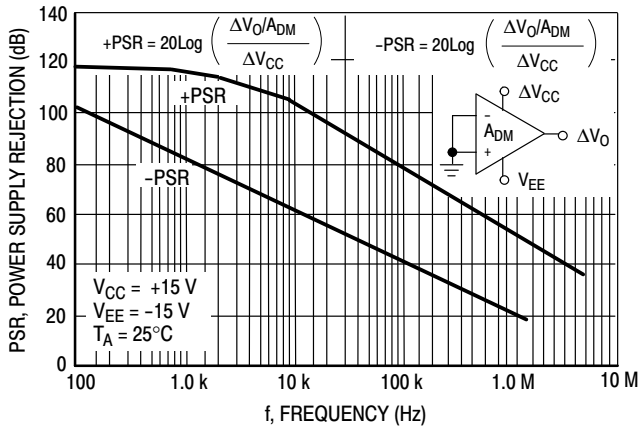


Figure 12. Power Supply Rejection versus Frequency

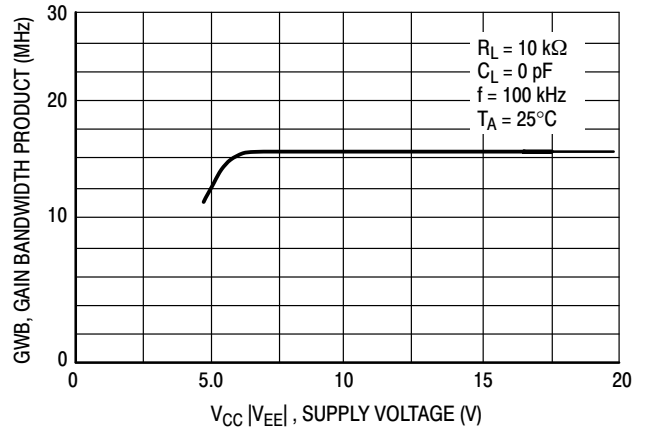


Figure 13. Gain Bandwidth Product versus Supply Voltage

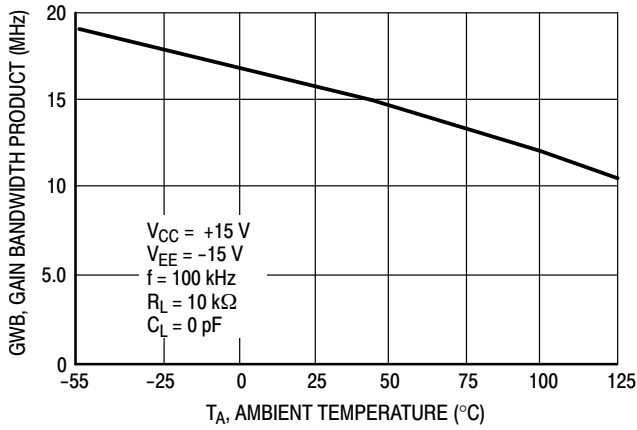


Figure 14. Gain Bandwidth Product versus Temperature

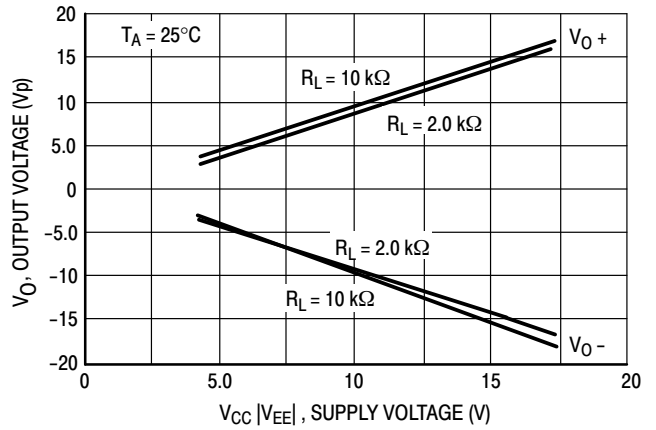


Figure 15. Maximum Output Voltage versus Supply Voltage



Figure 16. Output Voltage versus Frequency

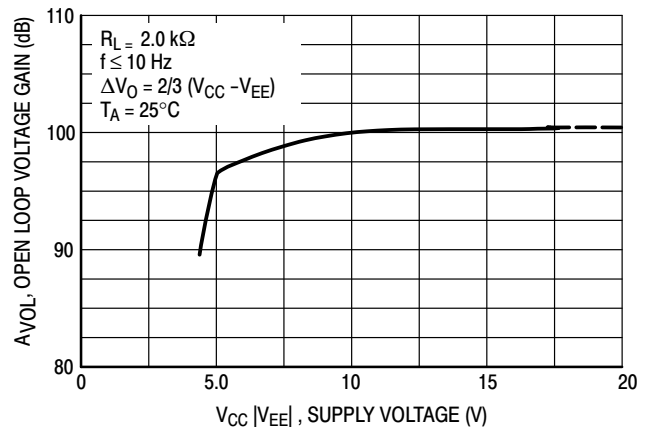


Figure 17. Open Loop Voltage Gain versus Supply Voltage

MC33078, MC33079, NCV33078, NCV33079



Figure 18. Open Loop Voltage Gain versus Temperature



Figure 19. Output Impedance versus Frequency



Figure 20. Channel Separation versus Frequency



Figure 21. Total Harmonic Distortion versus Frequency

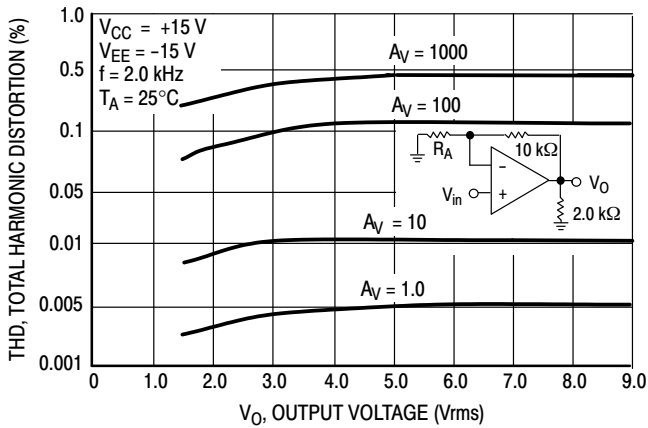


Figure 22. Total Harmonic Distortion versus Output Voltage



Figure 23. Slew Rate versus Supply Voltage

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Figure 24. Slew Rate versus Temperature

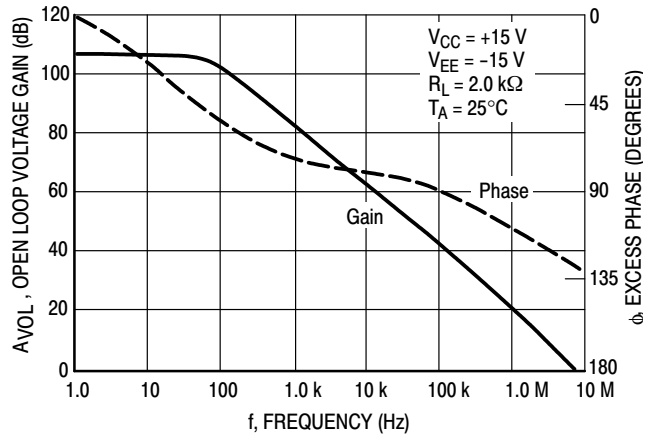


Figure 25. Voltage Gain and Phase versus Frequency



Figure 26. Open Loop Gain Margin and Phase Margin versus Load Capacitance



Figure 27. Overshoot versus Output Load Capacitance



Figure 28. Input Referred Noise Voltage and Current versus Frequency



Figure 29. Total Input Referred Noise Voltage versus Source Resistance

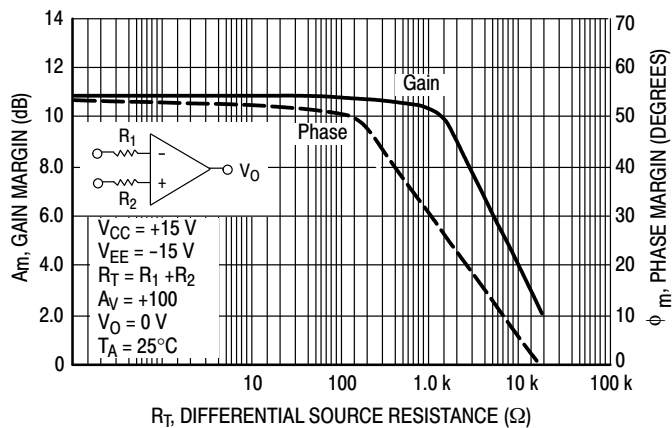


Figure 30. Phase Margin and Gain Margin versus Differential Source Resistance

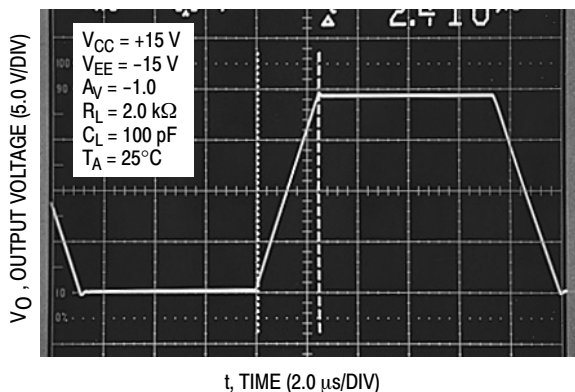


Figure 31. Inverting Amplifier Slew Rate

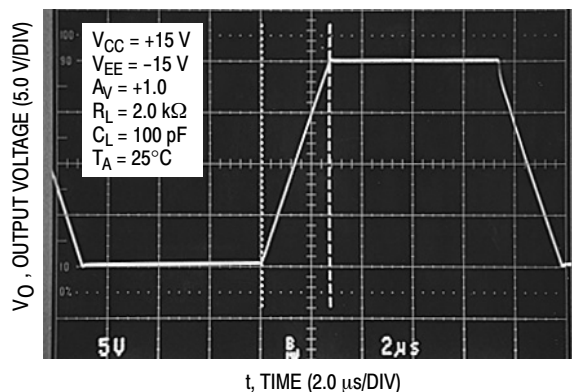


Figure 32. Non-inverting Amplifier Slew Rate

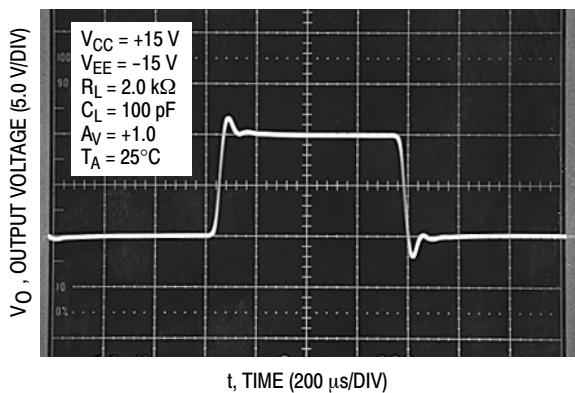


Figure 33. Non-inverting Amplifier Overshoot

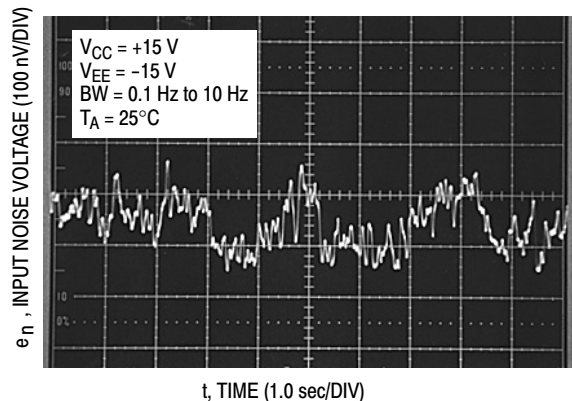
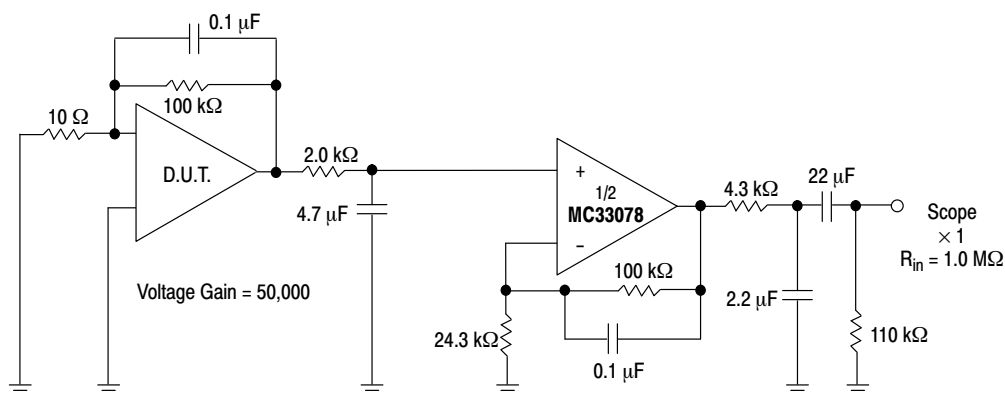


Figure 34. Low Frequency Noise Voltage versus Time

MC33078, MC33079, NCV33078, NCV33079



Note: All capacitors are non-polarized.

**Figure 35. Voltage Noise Test Circuit
(0.1 Hz to 10 Hz_{p-p})**

ORDERING INFORMATION

Device	Package	Shipping [†]
MC33078DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC33078DR2G		2500 / Tape & Reel
NCV33078DR2G*		
MC33078P	PDIP-8	50 Units / Rail
MC33078PG	PDIP-8 (Pb-Free)	
MC33079DG	SOIC-14 (Pb-Free)	55 Units / Rail
MC33079DR2G	SOIC-14 (Pb-Free)	2500 / Tape & Reel
NCV33079DR2G*		
MC33079P	PDIP-14	25 Units / Rail
MC33079PG	PDIP-14 (Pb-Free)	

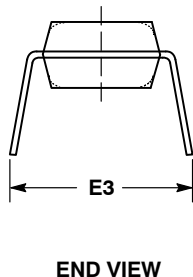
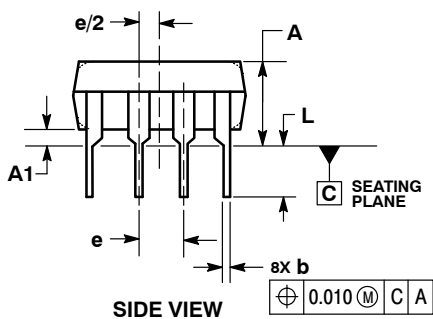
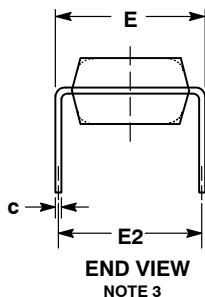
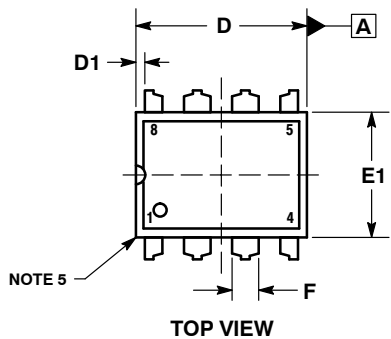
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV devices are qualified for automotive use.

MC33078, MC33079, NCV33078, NCV33079

PACKAGE DIMENSIONS

**PDIP-8
N SUFFIX
CASE 626-05
ISSUE M**



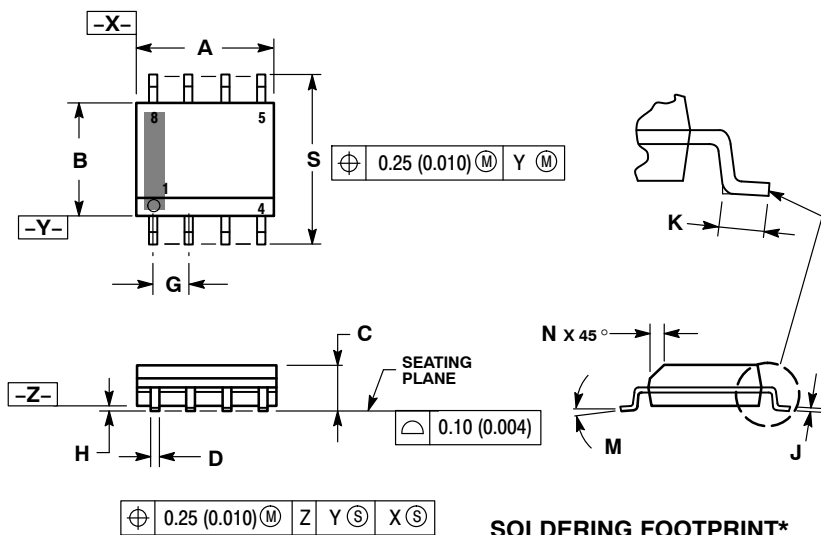
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION E IS MEASURED WITH THE LEADS RESTRAINED PARALLEL AT WIDTH E2.
4. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	----	----	0.210	----	----	5.33
A1	0.015	----	----	0.38	----	----
b	0.014	0.018	0.022	0.35	0.46	0.56
C	0.008	0.010	0.014	0.20	0.25	0.36
D	0.355	0.365	0.400	9.02	9.27	10.02
D1	0.005	----	----	0.13	----	----
E	0.300	0.310	0.325	7.62	7.87	8.26
E1	0.240	0.250	0.280	6.10	6.35	7.11
E2	0.300 BSC			7.62 BSC		
E3	----	----	0.430	----	----	10.92
e	0.100 BSC			2.54 BSC		
L	0.115	0.130	0.150	2.92	3.30	3.81

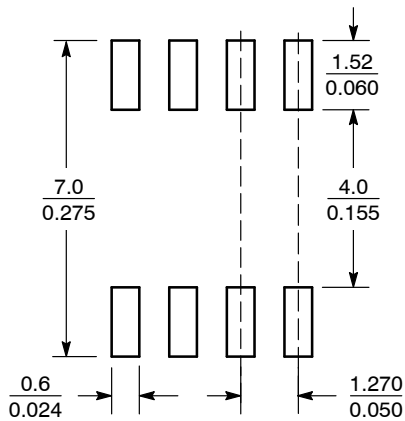
PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AK



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244



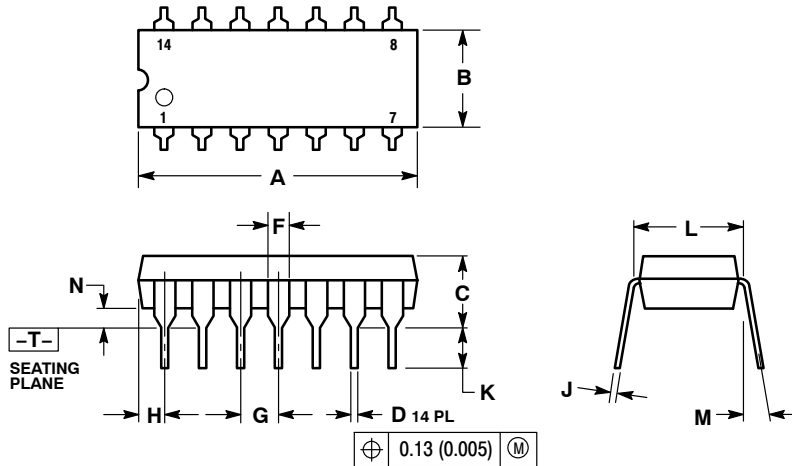
SCALE 6:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC33078, MC33079, NCV33078, NCV33079

PACKAGE DIMENSIONS

PDIP-14
CASE 646-06
ISSUE P



NOTES:

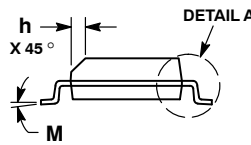
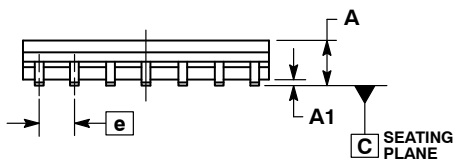
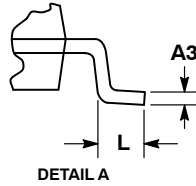
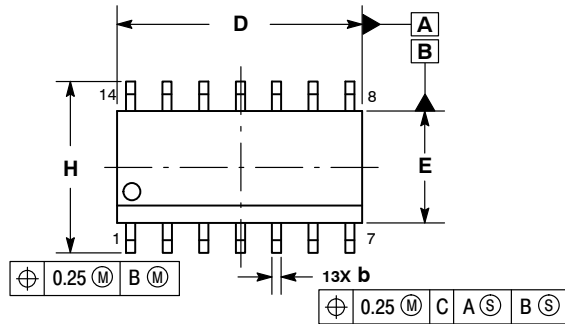
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	--- 10°		--- 10°	
N	0.015	0.039	0.38	1.01

MC33078, MC33079, NCV33078, NCV33079

PACKAGE DIMENSIONS

SOIC-14 NB
CASE 751A-03
ISSUE K

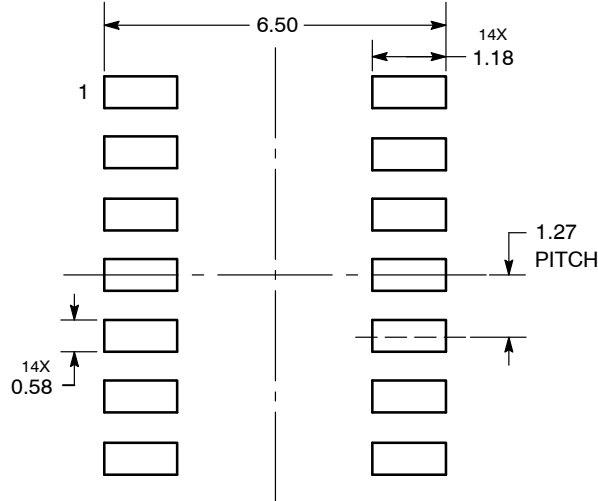


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0°	7°	0°	7°

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.