900 MHz Low Voltage LVPECL Clock Synthesizer

MPC9239

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DATASHEET

The MPC9239 is a 3.3 V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking, and computing applications. With output frequencies from 3.125 MHz to 900 MHz and the support of differential LVPECL output signals the device meets the needs of the most demanding clock applications.

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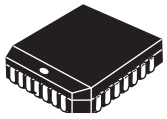
900 MHz LOW VOLTAGE CLOCK SYNTHESIZER



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776-02

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

Features

- 3.125 MHz to 900 MHz synthesized clock output signal
- Differential LVPECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference input
- 3.3 V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 28 PLCC and 32 LQFP packaging
- SiGe Technology
- Ambient temperature range 0°C to + 70°C
- Pin and function compatible to the MC12439

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator or external reference clock signal is multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1800 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50 Ω to V_{CC} – 2.0 V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the $\overline{\text{P\_LOAD}}$ input LOW until power becomes valid. On the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating. The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. Refer to PROGRAMMING INTERFACE for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output. The PWR_DOWN pin, when asserted, will synchronously divide the f_{OUT} by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de-assertion of the PWR_DOWN pin, the f_{OUT} input will step back up to its programmed frequency in four discrete increments.

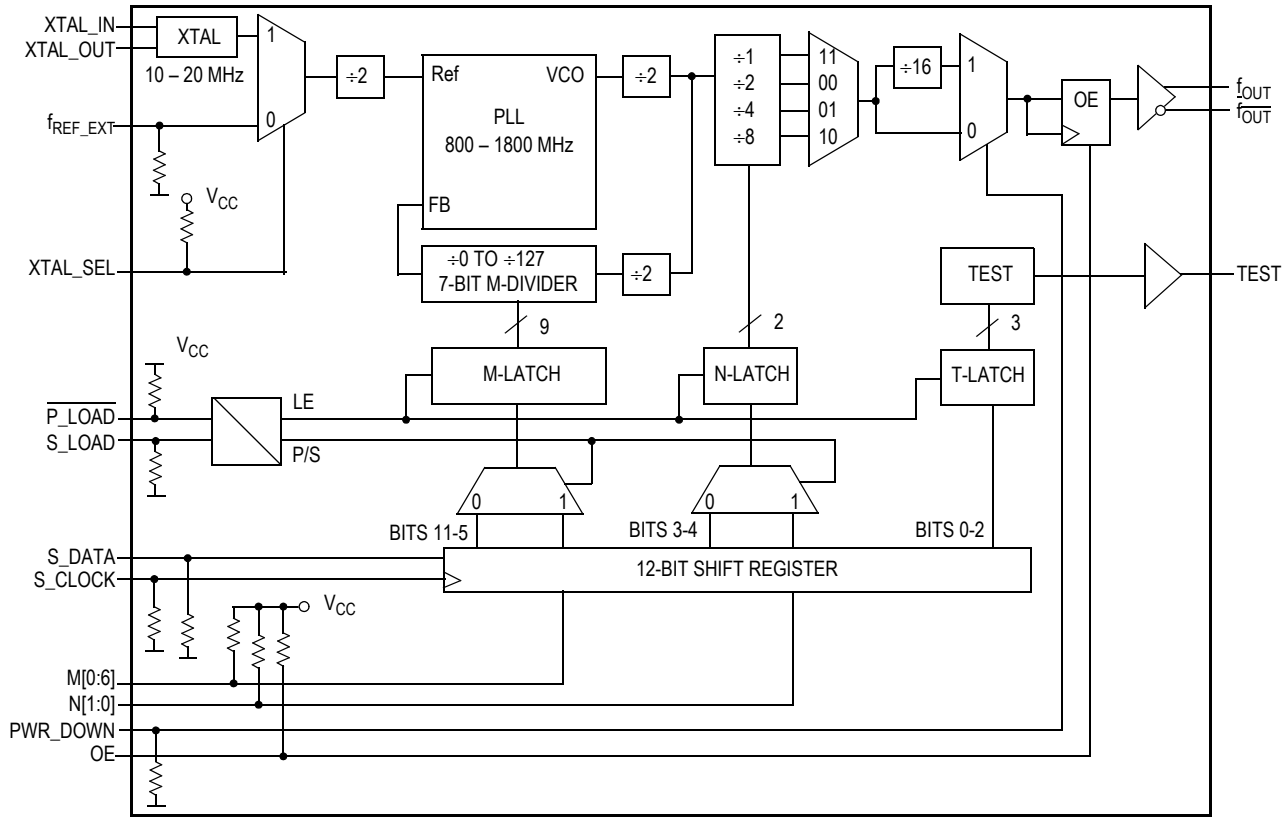


Figure 1. MPC9239 Logic Diagram

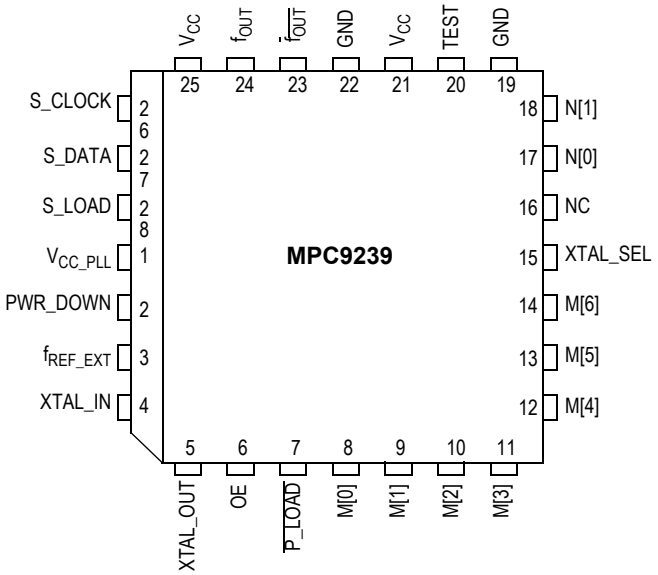


Figure 2. MPC9239 28-Lead PLCC Pinout
(Top View)

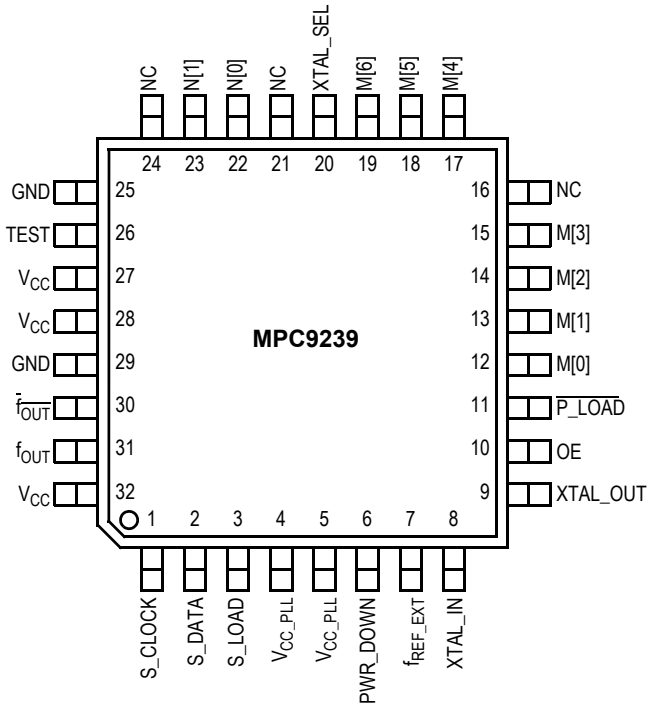


Figure 3. MPC9239 32-Lead LQFP Pinout
(Top View)

Table 1. Pin Configurations

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface.
f_{REF_EXT}	Input	0	LVCMOS	Alternative PLL reference input.
f_{OUT}, $\overline{f_{OUT}}$	Output		LVPECL	Differential clock output.
TEST	Output		LVCMOS	Test and device diagnosis output.
XTAL_SEL	Input	1	LVCMOS	PLL reference select input.
PWR_DOWN	Input	0	LVCMOS	Configuration input for power down mode. Assertion (deassertion) of power down will decrease (increase) the output frequency by a ratio of 16 in 4 discrete steps. PWR_DOWN assertion (deassertion) is synchronous to the input reference clock.
S_LOAD	Input	0	LVCMOS	Serial configuration control input. This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
$\overline{P\_LOAD}$	Input	1	LVCMOS	Parallel configuration control input. this input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of $\overline{P\_LOAD}$. $\overline{P\_LOAD}$ is state sensitive.
S_DATA	Input	0	LVCMOS	Serial configuration data input.
S_CLOCK	Input	0	LVCMOS	Serial configuration clock input.
M[0:6]	Input	1	LVCMOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of $\overline{P\_LOAD}$.
N[1:0]	Input	1	LVCMOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of $\overline{P\_LOAD}$.
OE	Input	1	LVCMOS	Output enable (active high). The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the f_{OUT} output. OE = L low stops f_{OUT} in the logic low stat (f_{OUT} = L, $\overline{f_{OUT}}$ = H).
GND	Supply		Ground	Negative power supply (GND).
V_{CC}	Supply		V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation.
V_{CC_PLL}	Supply		V_{CC}	PLL positive power supply (analog power supply).
NC				Do not connect.

Table 2. Output Frequency Range and PLL Post-Divider N

PWR_DOWN	N		VCO Output Frequency Division	f_{OUT} Frequency Range
	1	0		
0	0	0	2	200 – 450 MHz
0	0	1	4	100 – 225 MHz
0	1	0	8	50 – 112.5 MHz
0	1	1	1	400 – 900 MHz
1	0	0	32	12.5 – 28.125 MHz
1	0	1	64	6.25 – 14.0625 MHz
1	1	0	128	3.125 – 7.03125 MHz
1	1	1	16	25 – 56.25 MHz

Table 3. Function Table

Input	0	1
XTAL_SEL	f_{REF_EXT}	XTAL interface
OE	Outputs disabled. f_{OUT} is stopped in the logic low state (f_{OUT} = L, $\bar{f}_{\overline{OUT}}$ = H)	Outputs enabled
PWR_DOWN	Output divider ÷ 1	Output divider ÷ 16

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs (f_{REF_EXT}, PWR_DOWN, XTAL_SEL, $\overline{P\_LOAD}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1]. OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[1]			±200	µA	V_{IN} = V_{CC} or GND
Differential Clock Output f_{OUT}[2]						
V_{OH}	Output High Voltage[3]	V_{CC}–1.02		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage[3]	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage[3]	2.0			V	I_{OH} = –0.8 mA
V_{OL}	Output Low Voltage[3]			0.55	V	I_{OL} = 0.8 mA
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current		62	100	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50 Ω to V_{TT} = V_{CC} – 2 V.
3. The MPC9239 TEST output levels are compatible to the MC12429 output levels. The MPC9239 is capable of driving 25 Ω loads.

Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range		10		20	MHz	
f_{VCO}	VCO Frequency Range[2]		800		1800	MHz	
f_{MAX}	Output Frequency	N = 11 (÷ 1)	400		900	MHz	PWR_DOWN = 0
		N = 00 (÷ 2)	300		450	MHz	
		N = 01 (÷ 4)	100		225	MHz	
		N = 10 (÷ 8)	50		112.5	MHz	
f_{S_CLOCK}	Serial Interface Programming Clock Frequency[3]		0		10	MHz	
$t_{P,MIN}$	Minimum Pulse Width	(S_LOAD, $\overline{P\_LOAD}$)	50			ns	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.05		0.3	ns	20% to 80%
t_S	Setup Time	S_DATA to S_CLOCK	20			ns	
		S_CLOCK to $\overline{S\_LOAD}$	20			ns	
		M, N to $\overline{P\_LOAD}$	20			ns	
t_S	Hold Time	S_DATA to $\overline{S\_CLOCK}$	20			ns	
		M, N to $\overline{P\_LOAD}$	20			ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	N = 11 (÷ 1)			60	ps	
		N = 00 (÷ 2)			90	ps	
		N = 01 (÷ 4)			120	ps	
		N = 10 (÷ 8)			160	ps	
$t_{JIT(PER)}$	Period Jitter	N = 11 (÷ 1)			40	ps	
		N = 00 (÷ 2)			65	ps	
		N = 01 (÷ 4)			90	ps	
		N = 10 (÷ 8)			120	ps	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot 2 \cdot M$.
3. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. Refer to APPLICATIONS INFORMATION for more details.

Table 8. MPC9239 Frequency Operating Range (in MHz)

M	M[6:0]	VCO frequency for a crystal interface frequency of						Output frequency for f_{XTAL}=16 MHz and for N =			
		10 MHz	12 MHz	14 MHz	16 MHz	18 MHz	20 MHz	1	2	4	8
20	0010100						800				
21	0010101						840				
22	0010110						880				
23	0010111					828	920				
24	0011000					864	960				
25	0011001				800	900	1000	400	200	100	50
26	0011010				832	936	1040	416	208	104	52
27	0011011				864	972	1080	432	216	108	54
28	0011100			812	896	1008	1120	448	224	112	56
29	0011101			840	928	1044	1160	464	232	116	58
30	0011110			875	960	1080	1200	480	240	120	60
31	0011111			868	992	1116	1240	496	248	124	62
32	0100000			896	1024	1152	1280	512	256	128	64
33	0100001			924	1056	1188	1320	528	264	132	66
34	0100010		816	952	1088	1224	1360	544	272	136	68
35	0100011		840	980	1120	1260	1400	560	280	140	70
36	0100100		864	1008	1152	1296	1440	576	288	144	72
37	0100101		888	1036	1184	1332	1480	592	296	148	74
38	0100110		912	1064	1216	1368	1520	608	304	152	76
39	0100111		936	1092	1248	1404	1560	624	312	156	78
40	0101000	800	960	1120	1280	1440	1600	640	320	160	80
41	0101001	820	984	1148	1312	1476	1640	656	328	164	82
42	0101010	840	1008	1176	1344	1512	1680	672	336	168	84
43	0101011	860	1032	1204	1376	1548	1720	688	344	172	86
44	0101100	880	1056	1232	1408	1584	1760	704	352	176	88
45	0101101	900	1080	1260	1440	1620	1800	720	360	180	90
46	0101110	920	1104	1288	1472	1656		736	368	184	92
47	0101111	940	1128	1316	1504	1692		752	376	188	94
48	0110000	960	1152	1344	1536	1728		768	384	192	96
49	0110001	980	1176	1372	1568	1764		784	392	196	98
50	0110010	1000	1200	1400	1600	1800		800	400	200	100
51	0110011	1020	1224	1428	1632			816	408	204	102
52	0110100	1040	1248	1456	1664			832	416	208	104
53	0110101	1060	1272	1484	1696			848	424	212	106
54	0110110	1080	1296	1512	1728			864	432	216	108
55	0110111	1100	1320	1540	1760			880	440	220	110
56	0111000	1120	1344	1568	1792			896	448	224	112
57	0111001	1140	1368	1596							
58	0111010	1160	1392	1624							
59	0111011	1180	1416	1652							
60	0111100	1200	1440	1680							
61	0111101	1220	1488	1736							
62	0111110	1260	1512	1764							
63	0111111	1260	1512	1764							
64	1000000	1280	1536	1792							

PROGRAMMING INTERFACE

Programming the MPC9239

Programming the MPC9239 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$f_{OUT} = (f_{XTAL} \div 2) \cdot (M \cdot 4) \div (N \cdot 2) \text{ or} \quad (1)$$

$$f_{OUT} = f_{XTAL} \cdot M \div N \quad (2)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 800 to 1800 MHz in order to achieve stable PLL operation:

$$M_{MIN} = f_{VCO,MIN} \div (2 \cdot f_{XTAL}) \text{ and} \quad (3)$$

$$M_{MAX} = f_{VCO,MAX} \div (2 \cdot f_{XTAL}) \quad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M = 25 and M = 56. Table 8 shows the usable VCO frequency and M divider range for other example input frequencies.

Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$$f_{OUT} = 16\ M \div N$$

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 9. Output Frequency Range for f_{XTAL} = 10 MHz

N			f_{OUT}	f_{OUT} Range	f_{OUT} Step
1	0	Value			
0	0	2	8·M	200–450 MHz	8 MHz
0	1	4	4·M	100–225 MHz	4 MHz
1	0	8	2·M	50–112.5 MHz	2 MHz
1	1	1	16·M	400–900 MHz	16 MHz

Example Calculation for an 16 MHz Input Frequency

For example, if an output frequency of 384 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 384 MHz falls within the frequency range set by an N value of 2, so N[1:0]=00. For N = 2, f_{OUT} = 8·M, and M = $f_{OUT} \div 8$. Therefore, M = 384 ÷ 8 = 48, so M[6:0] = 0110000. Following this procedure a user can generate any whole frequency between 50 MHz and 900 MHz. The size of the programmable frequency steps will be equal to:

$$f_{STEP} = f_{XTAL} \div N$$

APPLICATIONS INFORMATION

Using the Parallel and Serial Interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW to HIGH transition will latch the information present on the M[6:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[6:0] and N[1:0] inputs will affect the f_{OUT} output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two, and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1, and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC9239 synthesizer.

M[6:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the Test and Diagnosis Output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents f_{OUT}, the LVCMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis.

The T2, T1, and T0 control bits are preset to ‘000' when P_LOAD is LOW so that the PECL f_{OUT} outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9239 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC9239 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the f_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving f_{OUT} directly gives the user more control on the test clocks sent through the clock tree shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the f_{OUT} pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 10. Test and Debug Configuration for TEST

T[2:0]			TEST Output
T2	T1	T0	
0	0	0	12-bit shift register out[1]
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 2$
0	1	1	M-Counter out
1	0	0	f_{OUT}
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	$f_{OUT} \div 4$

1. Clocked out at the rate of S_CLOCK.

Table 11. Debug Configuration for PLL Bypass[1]

Output	Configuration
f_{OUT}	S_CLOCK ÷ N
TEST	M-Counter out[2]

1. T[2:0] = 110. AC specifications do not apply in PLL bypass mode.
2. Clocked out at the rate of S_CLOCK ÷ (2 · N)

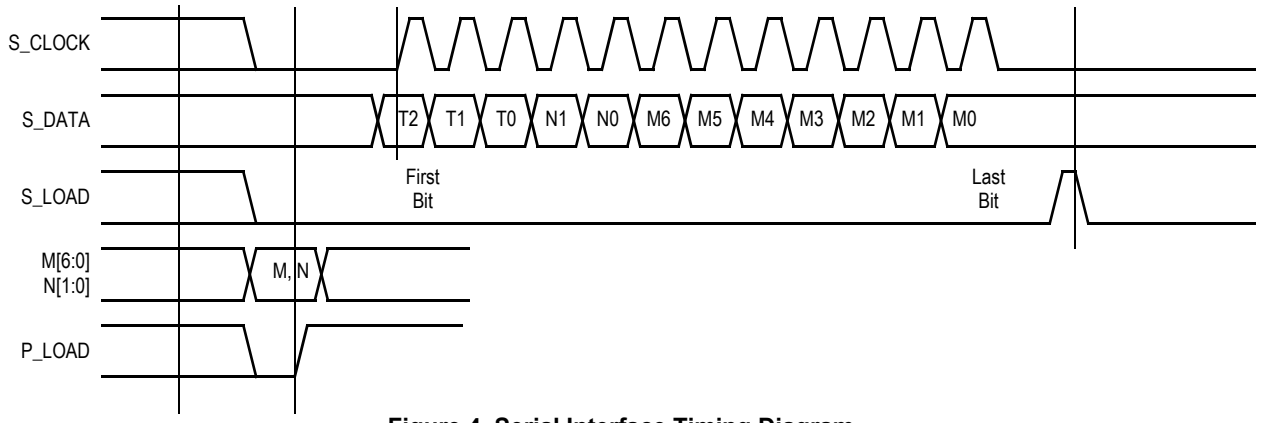


Figure 4. Serial Interface Timing Diagram

Power Supply Filtering

The MPC9239 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device characteristics. The MPC9239 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9239. Figure 5 illustrates a typical power supply filter scheme. The MPC9239 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the MPC9239 pin of the MPC9239. From the data sheet, the V_{CC_PLL}current (the current sourced through the V_{CC_PLL} pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 5 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the V_{CC_PLL} pin, a low DC resistance inductor is required (less than 15 Ω).

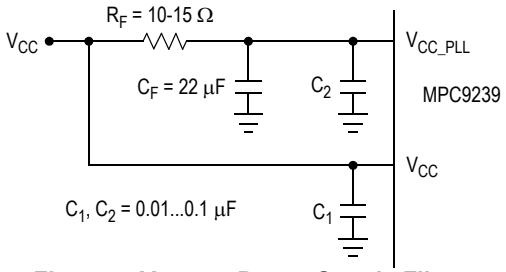


Figure 5. V_{CC_PLL} Power Supply Filter

Layout Recommendations

The MPC9239 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC9239. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC9239 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on—board oscillator. Although the MPC9239 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

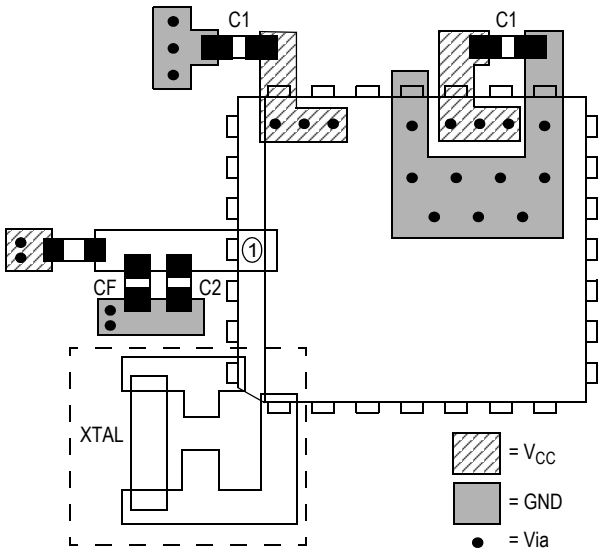


Figure 6. PCB Board Layout Recommendation for the PLCC28 Package

Using the On-Board Crystal Oscillator

The MPC9239 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC9239 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the XTAL terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1KΩ.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MPC9239 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 12 below specifies the performance requirements of the crystals to be used with the MPC9239.

Table 12. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance[1]
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5-7pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μW
Aging	5ppm/Yr (First 3 Years)

1. See accompanying text for series versus parallel resonant discussion.

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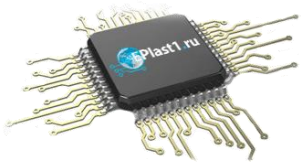

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