Data Sheet, Aug. 2010

# Control Integrated POwer System (CIPOS™)

## IGCM10F60GA

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For Power Management Application

LS Power Semitech
A joint venture with infineon

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# Table of Contents

# CIPOS™
# Control Integrated POwer System

## *Dual In-Line Intelligent Power Module*

## *3Φ-bridge 600V / 10A*

## Features

Fully isolated Dual In-Line molded module

- Infineon reverse conducting IGBTs with monolithic body diode
- Rugged SOI gate driver technology with stability against transient and negative voltage
- Allowable negative VS potential up to -11V for signal transmission at VBS=15V
- Integrated bootstrap functionality
- Over current shutdown
- Temperature monitor
- Under-voltage lockout at all channels
- Low side emitter pins accessible for all phase current monitoring (open emitter)
- Cross-conduction prevention
- All of 6 switches turn off during protection
- Minimum deadtime built in driver IC
- Lead-free terminal plating; RoHS compliant

## Target Applications

- Dish washers
- Refrigerators
- Washing machines
- Air-conditioners
- Fans
- Low power motor drives

## Description

The CIPOS™ module family offers the chance for integrating various power and control components to increase reliability, optimize PCB size and system costs.

It is designed to control three phase AC motors and permanent magnet motors in variable speed drives for applications like air conditioning, refrigerator and washing machine. The package concept is specially adapted to power applications, which need good thermal conduction and electrical isolation, but also EMI-save control and overload protection. The features of Infineon reverse conducting IGBT are combined with an optimized SOI gate driver for excellent electrical performance.

## System Configuration

- 3 half bridges with reverse conducting IGBT
- 3Φ SOI gate driver
- Thermistor
- Pin-to-heasink creepage distance typ. 1.6mm

## Pin Configuration

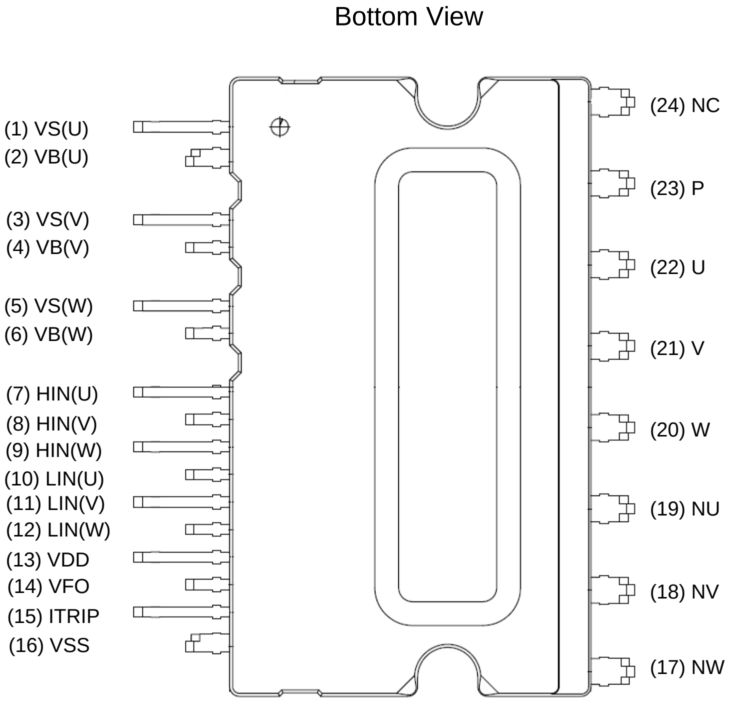

**Figure 1: Pin configuration**

## Internal Electrical Schematic

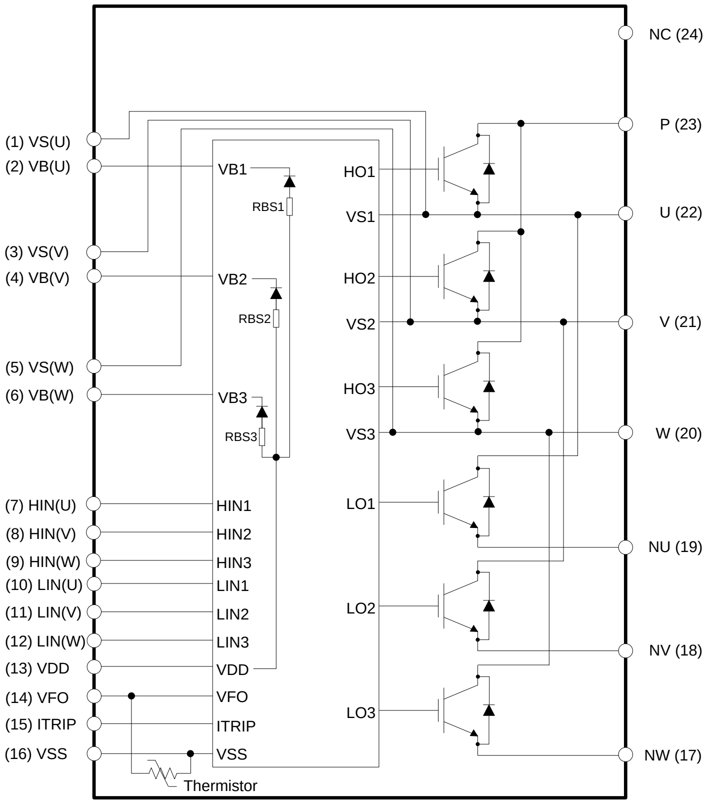

**Figure 2: Internal schematic**

## Pin Assignment

| Pin Number | Pin Name | Pin Description |
|---|---|---|
| 1 | VS(U) | U-phase high side floating IC supply offset voltage |
| 2 | VB(U) | U-phase high side floating IC supply voltage |
| 3 | VS(V) | V-phase high side floating IC supply offset voltage |
| 4 | VB(V) | V-phase high side floating IC supply voltage |
| 5 | VS(W) | W-phase high side floating IC supply offset voltage |
| 6 | VB(W) | W-phase high side floating IC supply voltage |
| 7 | HIN(U) | U-phase high side gate driver input |
| 8 | HIN(V) | V-phase high side gate driver input |
| 9 | HIN(W) | W-phase high side gate driver input |
| 10 | LIN(U) | U-phase low side gate driver input |
| 11 | LIN(V) | V-phase low side gate driver input |
| 12 | LIN(W) | W-phase low side gate driver input |
| 13 | VDD | Low side control supply |
| 14 | VFO | Fault output / Temperature monitor |
| 15 | ITRIP | Over current shutdown input |
| 16 | VSS | Low side control negative supply |
| 17 | NW | W-phase low side emitter |
| 18 | NV | V-phase low side emitter |
| 19 | NU | U-phase low side emitter |
| 20 | W | Motor W-phase output |
| 21 | V | Motor V-phase output |
| 22 | U | Motor U-phase output |
| 23 | P | Positive bus input voltage |
| 24 | NC | No Connection |

## Pin Description

### HIN(U,V,W) and LIN(U,V,W) (Low side and high side control pins, Pin 7 - 12)

These pins are positive logic and they are responsible for the control of the integrated IGBT. The Schmitt-trigger input threshold of them are such to guarantee LSTTL and CMOS compatibility down to 3.3V controller outputs. Pull-down resistor of about 5kΩ is internally provided to pre-bias inputs during supply start-up and a zener clamp is provided for pin protection purposes. Input schmitt-trigger and noise filter provide beneficial noise rejection to short input pulses.

The noise filter suppresses control pulses which are below the filter time $t_{FILIN}$. The filter acts according to Figure 4.

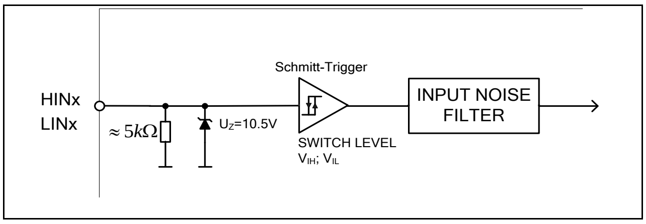

Figure 3: Input pin structure

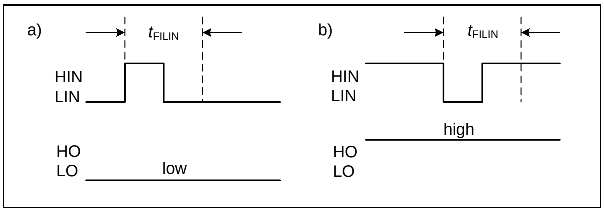

Figure 4: Input filter timing diagram

It is recommended for proper work of CIPOS™ not to provide input pulse-width lower than 1us.

The integrated gate drive provides additionally a shoot through prevention capability which avoids the simultaneous on-state of two gate drivers of the same leg (i.e. HO1 and LO1, HO2 and LO2, HO3 and LO3). When two inputs of a same leg are activated, only former activated one is activated so that the leg is kept steadily in a safe state.

A minimum deadtime insertion of typ 380ns is also provided by driver IC, in order to reduce cross-conduction of the external power switches.

### VFO (Fault-output and NTC, Pin 14)

The VFO pin indicates a module failure in case of under voltage at pin VDD or in case of triggered over current detection at ITRIP. A pull-up resistor is externally required to bias the NTC.

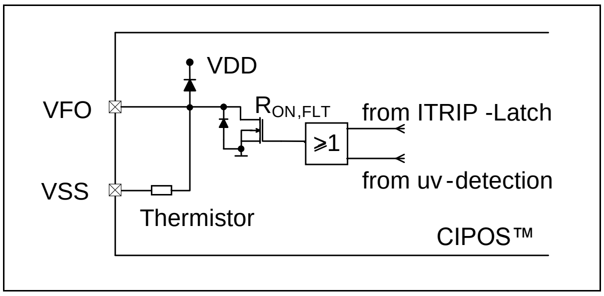

**Figure 5: Internal circuit at pin VFO**

The same pin provides direct access to the NTC, which is referenced to VSS. An external pull-up resistor connected to +5V ensures, that the resulting voltage can be directly connected to the microcontroller

### ITRIP (Over current detection function, Pin 15)

CIPOS™ provides an over current detection function by connecting the ITRIP input with the motor current feedback. The ITRIP comparator threshold (typ 0.47V) is referenced to VSS ground. A input noise filter (typ: $t_{ITRIPMIN}$ = 530ns) prevents the driver to detect false over-current events.

Over current detection generates a shut down of all outputs of the gate driver after the shutdown propagation delay of typically 1000ns.

The fault-clear time is set to typical 65us.

### VDD, VSS (Low side control supply and reference, Pin 13, 16)

VDD is the low side supply and it provides power both to input logic and to low side output power stage. Input logic is referenced to VSS ground.

The under-voltage circuit enables the device to operate at power on when a supply voltage of at least a typical voltage of $V_{DDUV+}$ = 12.1V is present.

The IC shuts down all the gate drivers power outputs, when the VDD supply voltage is below $V_{DDUV-}$ = 10.4V. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.

### VB(U,V,W) and VS(U,V,W) (High side supplies, Pin 1, 2, 3, 4, 5, 6)

VB to VS is the high side supply voltage. The high side circuit can float with respect to VSS following the external high side power device emitter voltage.

Due to the low power consumption, the floating driver stage is supplied by integrated bootstrap circuit.

The under-voltage detection operates with a rising supply threshold of typical $V_{BSUV+}$ = 12.1V and a falling threshold of $V_{DDUV-}$ = 10.4V.

VS(U,V,W) provide a high robustness against negative voltage in respect of VSS of -50V transiently. This ensures very stable designs even under rough conditions.

### NU, NV, NW (Low side emitter, Pin 17, 18, 19)

The low side emitters are available for current measurements of each phase leg. It is recommended to keep the connection to pin VSS as short as possible in order to avoid unnecessary inductive voltage drops.

### P (Positive bus input voltage, Pin 23)

The high side IGBT are connected to the bus voltage. It is recommended that the bus voltage does not exceed 400 V.

## Absolute Maximum Ratings

($V_{DD}$ = 15V and $T_C$ = 25°C, if not stated otherwise)

### Module Section

| Description | Condition | Symbol | Value | | Unit |
|---|---|---|---|---|---|
| | | | min | max | |
| Storage temperature range | | $T_{stg}$ | -40 | 125 | °C |
| Insulation test voltage | RMS, f=60Hz, t =1min | $V_{ISOL}$ | 2000 | - | V |
| Operating case temperature range | Refer to Figure 6 | $T_C$ | -40 | 100 | °C |

### RC-IGBT Section

| Description | Condition | Symbol | Value | | Unit |
|---|---|---|---|---|---|
| | | | min | max | |
| Max. blocking voltage | $I_C$=250µA | $V_{CES}$ | 600 | - | V |
| Output current | $T_C$ = 25°C, $T_J$<150°C<br>$T_C$ = 100°C, $T_J$<150°C | $I_C$ | -10<br>-6 | 10<br>6 | A |
| Maximum peak output current | less than 1ms | $I_C$ | -20 | 20 | A |
| Short circuit withstand time | $V_{DC} \leq$ 400V | $t_{SC}$ | - | 5 | µs |
| Power dissipation per IGBT | | $P_{tot}$ | - | 26 | W |
| Operating junction temperature range | | $T_J$ | -40 | 150 | °C |
| Single IGBT thermal resistance, junction-case | | $R_{thJC}$ | - | 4.79 | K/W |

### Control Section

| Description | Condition | Symbol | Value | | Unit |
|---|---|---|---|---|---|
| | | | min | max | |
| Module supply voltage | | $V_{DD}$ | -1 | 20 | V |
| High side floating supply voltage (VB vs. VS) | | $V_{BS}$ | -1 | 20 | V |
| Input voltage | LIN, HIN, ITRIP | $V_{IN}$<br>$V_{ITRIP}$ | -1<br>-1 | 10<br>10 | V |
| Switching frequency | | $f_{PWM}$ | - | 20 | kHz |

## Recommended Operation Conditions

All voltages are absolute voltages referenced to $V_{SS}$ -potential unless otherwise specified.

| Description | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| DC link supply voltage | $V_{DC}$ | 0 | - | 400 | V |
| High side floating supply voltage ($V_B$ vs. $V_S$) | $V_{BS}$ | 13.5 | - | 18.5 | V |
| Low side supply voltage | $V_{DD}$ | 14.0 | 16 | 18.5 | V |
| Control supply variation | $\Delta V_{BS,}$<br>$\Delta V_{DD}$ | -1<br>-1 | - | 1<br>1 | V/µs |
| Logic input voltages LIN,HIN,ITRIP | $V_{IN}$<br>$V_{ITRIP}$ | 0<br>0 | - | 5<br>5 | V |
| Between VSS - N (including surge) | $V_{SS}$ | -5 | - | 5 | V |

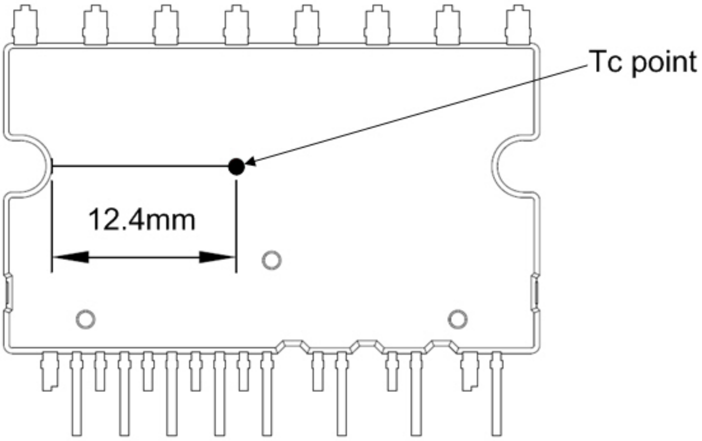

**Figure 6: $T_C$ measurement point**

## Static Parameters

($V_{DD}$ = 15V and $T_C$ = 25°C, if not stated otherwise)

| Description | Condition | Symbol | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Collector-Emitter saturation voltage | $I_{out}$ = 6A<br>$T_J$ = 25°C<br>150°C | $V_{CE(sat)}$ | -<br>- | 1.6<br>1.8 | 2.0<br>- | V |
| Emitter-Collector forward voltage | $I_{out}$ = -6A<br>$T_J$ = 25°C<br>150°C | $V_F$ | -<br>- | 1.75<br>1.8 | 2.2 | V |
| Collector-Emitter leakage current | $V_{CE}$ = 600V | $I_{CES}$ | - | - | 1 | mA |
| Logic "1" input voltage (LIN,HIN) | | $V_{IH}$ | - | 2.1 | 2.5 | V |
| Logic "0" input voltage (LIN,HIN) | | $V_{IL}$ | 0.7 | 0.9 | - | V |
| ITRIP positive going threshold | | $V_{IT,TH+}$ | 400 | 470 | 540 | mV |
| ITRIP input hysteresis | | $V_{IT,HYS}$ | 40 | 70 | - | mV |
| $V_{DD}$ and $V_{BS}$ supply under voltage positive going threshold | | $V_{DDUV+}$<br>$V_{BSUV+}$ | 10.8 | 12.1 | 13.0 | V |
| $V_{DD}$ and $V_{BS}$ supply under voltage negative going threshold | | $V_{DDUV-}$<br>$V_{BSUV-}$ | 9.5 | 10.4 | 11.2 | V |
| $V_{DD}$ and $V_{BS}$ supply under voltage lockout hysteresis | | $V_{DDUVH}$<br>$V_{BSUVH}$ | 1.0 | 1.7 | - | V |
| Input clamp voltage (HIN, LIN, ITRIP) | Iin=4mA | $V_{INCLAMP}$ | 9.0 | 10.1 | 12.5 | V |
| Quiescent $VB_x$ supply current ($VB_x$ only) | $H_{IN}$ = 0V | $I_{QBS}$ | - | 300 | 500 | µA |
| Quiescent *V*DD supply current (VDD only) | $L_{IN}$ = 0V, $H_{INX}$=5V | $I_{QDD}$ | - | 370 | 900 | µA |
| Input bias current | $V_{IN}$ = 5V | $I_{IN+}$ | - | 1 | 1.5 | mA |
| Input bias current | $V_{IN}$ = 0V | $I_{IN-}$ | - | 2 | - | µA |
| ITRIP input bias current | $V_{ITRIP}$ = 5V | $I_{ITRIP+}$ | - | 65 | 150 | µA |
| VFO input bias current | VFO = 5V, $V_{ITRIP}$ = 0V | $I_{FO}$ | - | 60 | - | µA |
| VFO output voltage | $I_{FO}$ = 10mA, $V_{ITRIP}$ = 1V | $V_{FO}$ | - | 0.5 | - | V |

## Dynamic Parameters

($V_{DD}$ = 15V and $T_C$ = 25°C, if not stated otherwise)

| Description | Condition | Symbol | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Turn-on propagation delay | $V_{LIN,HIN}$ = 5V; $I_{out}$ = 6A,<br>$V_{DC}$ = 300V | $t_{d(on)}$ | - | 650 | - | ns |
| Turn-on rise time | $V_{LIN,HIN}$ = 5V; $I_{out}$ = 6A,<br>$V_{DC}$ = 300V | $t_r$ | - | 20 | - | ns |
| Turn-off propagation delay | $V_{LIN,HIN}$ = 0V; $I_{out}$ = 6A,<br>$V_{DC}$ = 300V | $t_{d(off)}$ | - | 650 | - | ns |
| Turn-off fall time | $V_{LIN,HIN}$ = 0V; $I_{out}$ = 6A,<br>$V_{DC}$ = 300V | $t_f$ | - | 170 | - | ns |
| Short circuit propagation delay | From $V_{IT,TH+}$ to 10% $I_{SC}$ | $t_{SCP}$ | - | 1250 | - | ns |
| Input filter time ITRIP | $V_{ITRIP}$ = 1V | $t_{ITRIPmin}$ | - | 530 | - | ns |
| Input filter time at LIN, HIN for turn on and off | $V_{LIN,HIN}$ = 0V & 5V | $t_{FILIN}$ | - | 290 | - | ns |
| Fault clear time after ITRIP-fault | $V_{ITRIP}$ = 1V | $t_{FLTCLR}$ | 40 | 65 | 130 | µs |
| Deadtime between low side and high side | | $DT_{PWM}$ | 1.5 | - | - | µs |
| Deadtime of gate drive circuit | | $DT_{IC}$ | | 380 | | ns |
| IGBT turn-on energy (includes reverse recovery of diode) | $V_{DC}$ = 300V, $I_C$ = 6A,<br>$T_J$ = 25°C<br>150°C | $E_{on}$ | -<br>- | 110<br>155 | -<br>- | µJ |
| IGBT turn-off energy | $V_{DC}$ = 300V, $I_C$ = 6A,<br>$T_J$ = 25°C<br>150°C | $E_{off}$ | -<br>- | 155<br>220 | -<br>- | µJ |
| Diode recovery energy | $V_{DC}$ = 300V, $I_C$ = 6A,<br>$T_J$ = 25°C<br>150°C | $E_{rec}$ | -<br>- | 45<br>75 | -<br>- | µJ |

## Bootstrap Parameters

($T_C$ = 25°C, if not stated otherwise)

| Description | Condition | Symbol | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Repetitive peak reverse voltage | | $V_{RRM}$ | 600 | | | V |
| Bootstrap resistance of U-phase[1] | VS2 or VS3=300V, $T_J$=25°C<br>VS2 and VS3=0V, $T_J$=25°C<br>VS2 or VS3=300V, $T_J$=125°C<br>VS2 and VS3=0V, $T_J$=125°C | $R_{BS1}$ | | 35<br>40<br>50<br>65 | | Ω |
| Reverse recovery time | $I_F$=0.6A, di/dt=80A/µs | $t_{rr\_BS}$ | | 50 | | ns |
| Forward voltage drop | $I_F$=20mA, VS2 and VS3=0V | $V_{F\_BS}$ | | 2.6 | | V |

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[1] $R_{BS2}$ and $R_{BS3}$ have same values to $R_{BS1}$.

## Thermistor

| Description | Condition | Symbol | Value |  |  | Unit |
|---|---|---|---|---|---|---|
|  |  |  | min | typ | max |  |
| Resistor | $T_{NTC}$ = 25°C | $R_{NTC}$ | - | 85 | - | kΩ |
| B-constant of NTC<br>(Negative temperature coefficient) |  | B(25/100) | - | 4092 | - | K |

## Mechanical Characteristics and Ratings

| Description | Condition | Value |  |  | Unit |
|---|---|---|---|---|---|
|  |  | min | typ | max |  |
| Mounting torque | M3 screw and washer | 0.59 | 0.69 | 0.78 | Nm |
| Flatness | Refer to Figure 7 | -50 | - | 100 | µm |
| Weight |  | - | 6.15 | - | g |

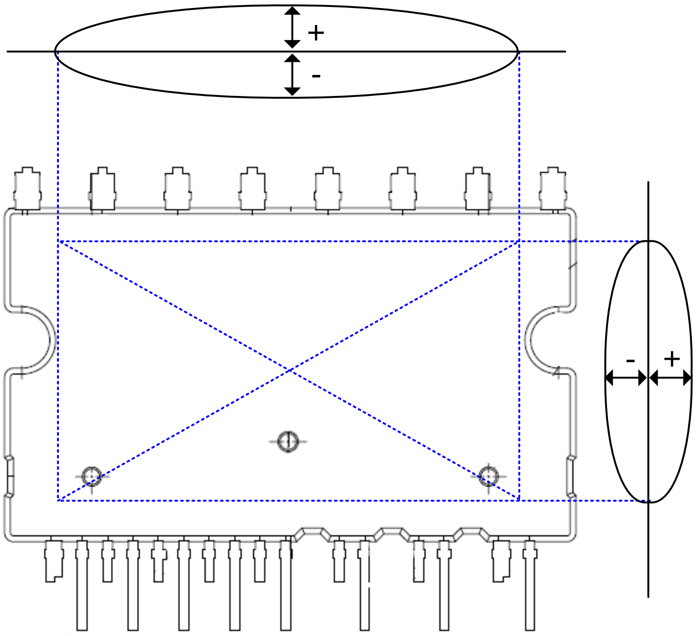


**Figure 7: Flatness measurement position**

## Circuit of a Typical Application

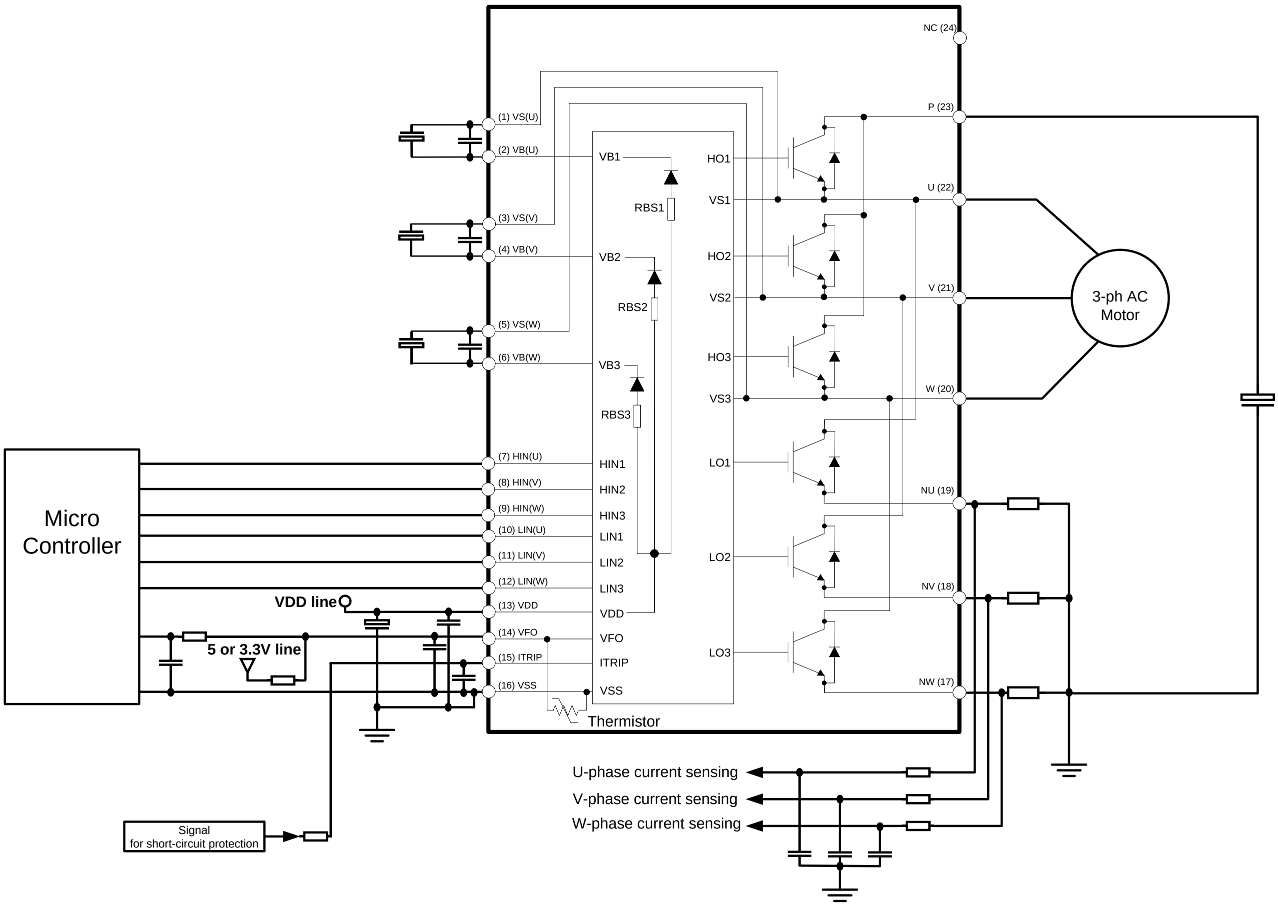


Figure 8: Application circuit

## Switching Times Definition

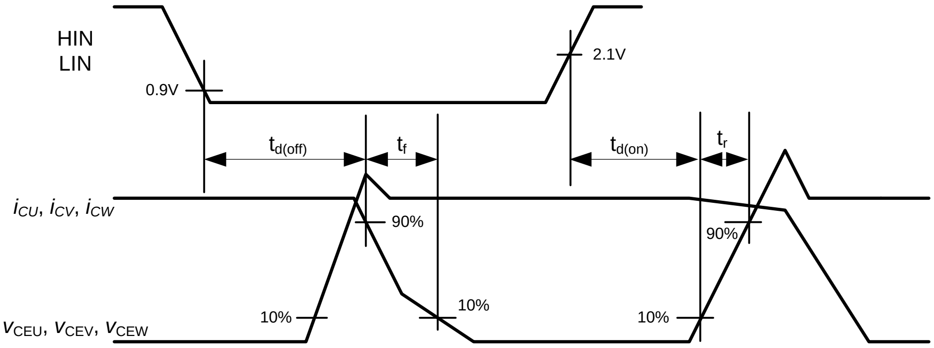
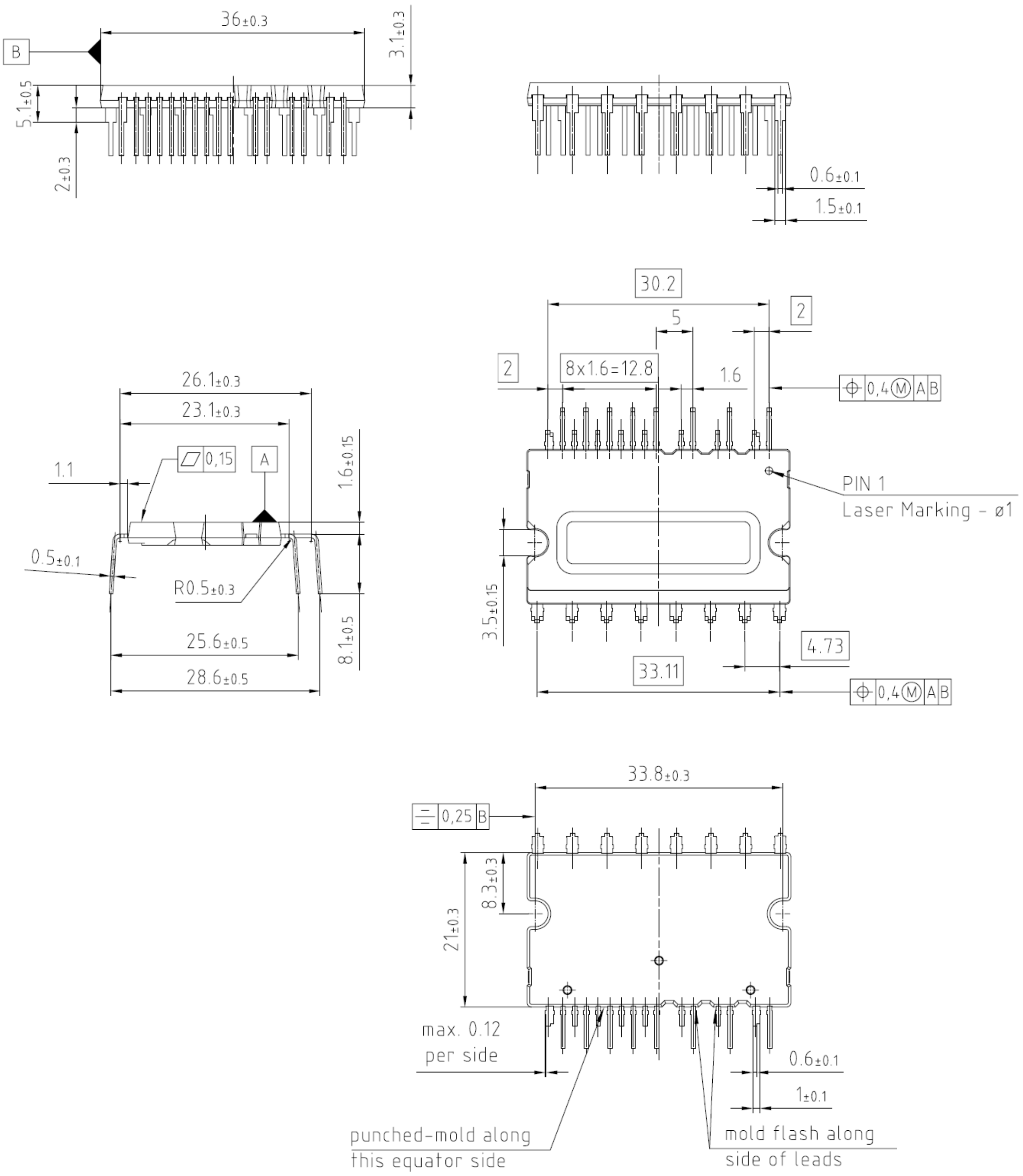


Figure 9: Switching times definition

## Package Outline



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
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- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

### Как с нами связаться

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