LMK04821EVM User's Guide

These evaluation board instructions describe how to set up and operate the LMK04821EVM evaluation module (EVM).

Topic **Page**

1 Evaluation Board Kit Contents

The evaluation board kit includes:

- Evaluation Board, SV600788-004
- USB2ANY interface

2 Quick Start

The LMK04821EVM allows full verification of the device functionality and performance specifications. To quickly set up and operate the board with basic equipment, refer to the quick start procedure below and test setup shown in Figure 1.

1. Connect a voltage of **4.5** volts to the Vcc SMA connector or terminal block. Device operates at 3.3 V using onboard LP3878-ADJ LDO. VCXO operates at 3.3 V using onboard LP5900 LDO.
2. Connect a reference clock to the CLKin1 port from a signal generator or other source. Use **122.88 MHz** for default. Exact frequency and input port (CLKin0/CLKin1) depends on programming.
3. Connect the SPI header to a computer using USB2ANY.
4. Program the device with CodeLoader. CodeLoader is available for download at: http://www.ti.com/tool/codeloader.
   (a) Select LMK04821 from “Select Device → Clock Conditioners” Menu.
   (b) **Select USB mode** from the Port Setup tab. Confirm that USB device being used to communicate with EVM is chosen from list of available USB devices.
   (c) Select a default mode from the “Mode” Menu. For the quick start use, “**CLKin1 122.88 MHz, OSCin 122.88 MHz**”
   (d) **Ctrl-L** must be pressed at least once to load all registers. Alternatively click menu Keyboard Controls → Load Device.
5. Measurements may be made at an active CLKout port via its SMA connector.

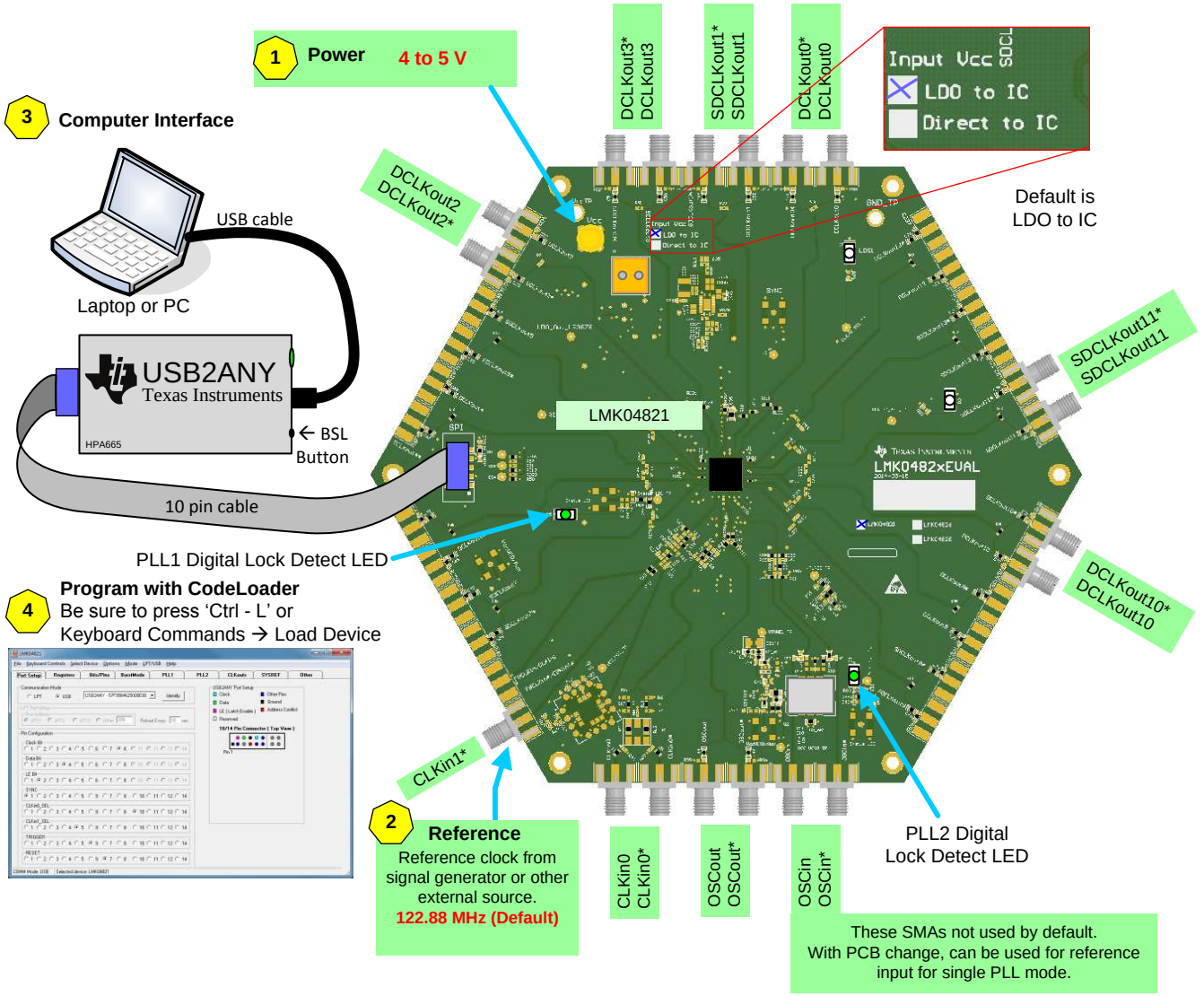

Figure 1. Quick Start Diagram

2.1 CLKout Tab Description

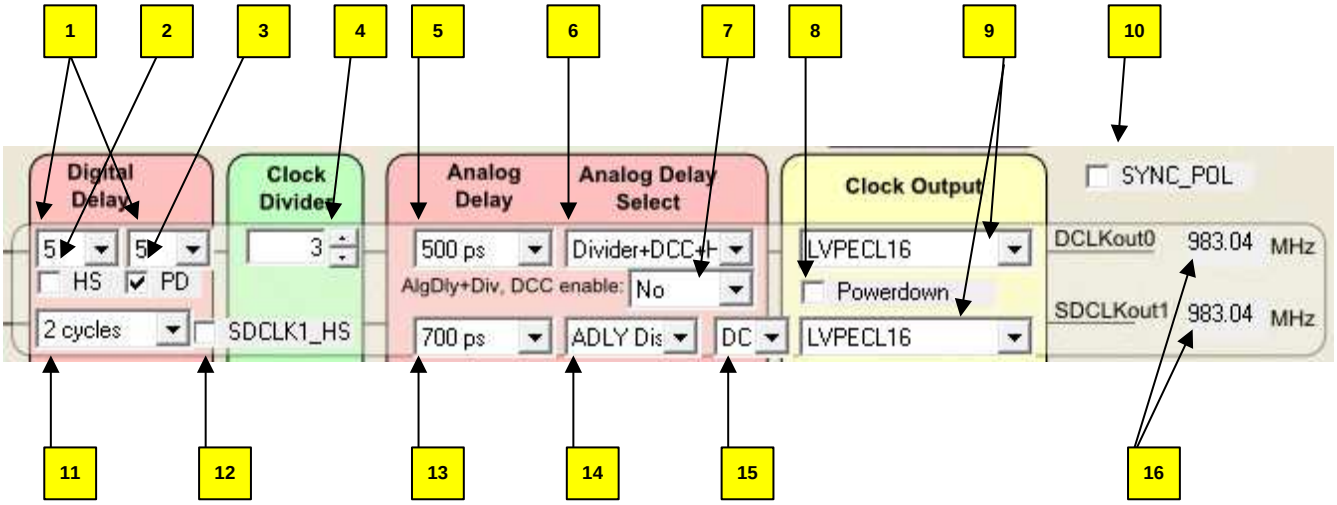

Figure 2. CLKout Tab Description Diagram

Device Clock Controls

1. DCLKoutX_DDLY_CNTL and DCLKoutX_DDLY_CNTH for controlling digital delay.
2. DCLKoutX_HS, Half step bit (must have a HS mode selected by #6 or #7).
3. DCLKoutX_DDLY_PD, Power down digital delay for DCLKoutX.
4. DCLKoutX_DIV, divider for the output channel.
5. DCLKoutX_ADLY, analog delay (if enabled with #6).
6. DCLKoutX_MUX, select source for output. Can be divider only, divider w/ DCC+HS (duty cycle correction and half step), bypass, or analog delay w/ Divider (and DCC/HS if selected by #7).
7. DCLKoutX_ADLY_MUX, Select DCC/HS or not when using analog delay mode.
8. CLKoutX_Y_PD, powerdown the entire CLKoutX_Y block. Both outputs will be off.

Device Clock/SYSREF Controls

9. DCLKoutX_FMT or SDCLKoutY_FMT, select output type for each output.
10. SYNC_POL bit, will allow SYNC when in default configuration (SYNC_MODE / SYSREF_MUX setup for normal SYNC).

SYSREF Controls

11. SDCLKoutY_DDLY, Local SYSREF clock digital delay.
12. SDCLKoutY_HS, SYSREF clock half step
13. SDCLKoutY_ADLY, SYSREF analog delay (if enabled by #14)
14. SDCLKoutY_ADLY_EN, enable analog delay
15. SDCLKoutY_MUX, select Device Clock or SYSREF clock for output to SDCLKoutY clock.
16. Calculated output frequency.

2.2 CodeLoader Tips

- On Bits/Pins tab right-clicking any register name in the Bits/Pins tab will display a Help prompt with the register address, data bit location/length, and a brief register description.
- On PLL tabs clicking Show Bits will show register info.
- On other tabs, pressing the ~ key with a control focused will show a help prompt.

2.3 SYSREF Quick Start

The LMK04821 EVM allows for verification of the LMK04821's implementation of JESD204B SYSREF functionality. To quickly setup and operate the SYSREF functions refer to the following procedures.

2.3.1 Continuous SYSREF

1. On SYSREF Tab set SYNC_MODE = 1 (SYNC Pin) and SYSREF_MUX = 0 (Normal SYNC)
2. On SYSREF Tab set SDCLKoutY_PD = 0 (where Y is the desired SDCLKout)
3. On CLKouts Tab set SDCLKoutY_MUX = 1 (Set to "SR" for desired SDCLKout)
4. On SYSREF Tab set SYSREF_PD and on CLKouts Tab SYSREF_DDLY_PD = 0
5. On CLKouts Tab set DCLKoutX_DDLY_PD = 0 and on SYSREF Tab set SYNC_DISX and SYNC_DISSYSREF = 0 (where X is the desired DCLKout)
6. Perform a SYNC event (toggle SYNC_POL on/off/on)
7. On SYSREF Tab set SYNC_DISX = 1 (for desired DCLKout's) and SYNC_DISSYSREF = 1
8. On SYSREF Tab set SYSREF_MUX = 3 (SYSREF Continuous)
9. On SYSREF Tab ensure SYSREF_CLR = 0 (SYSREF tab, location: right side, below clock output pic)

In Figure 3 and Figure 4 the Blue trace is DCLKout6 at 245.76 MHz and the Green trace is SDCLKout7 (SYSREF) at 24.475 MHz. Figure 5 shows the configuration of the LMK04821 outputs.

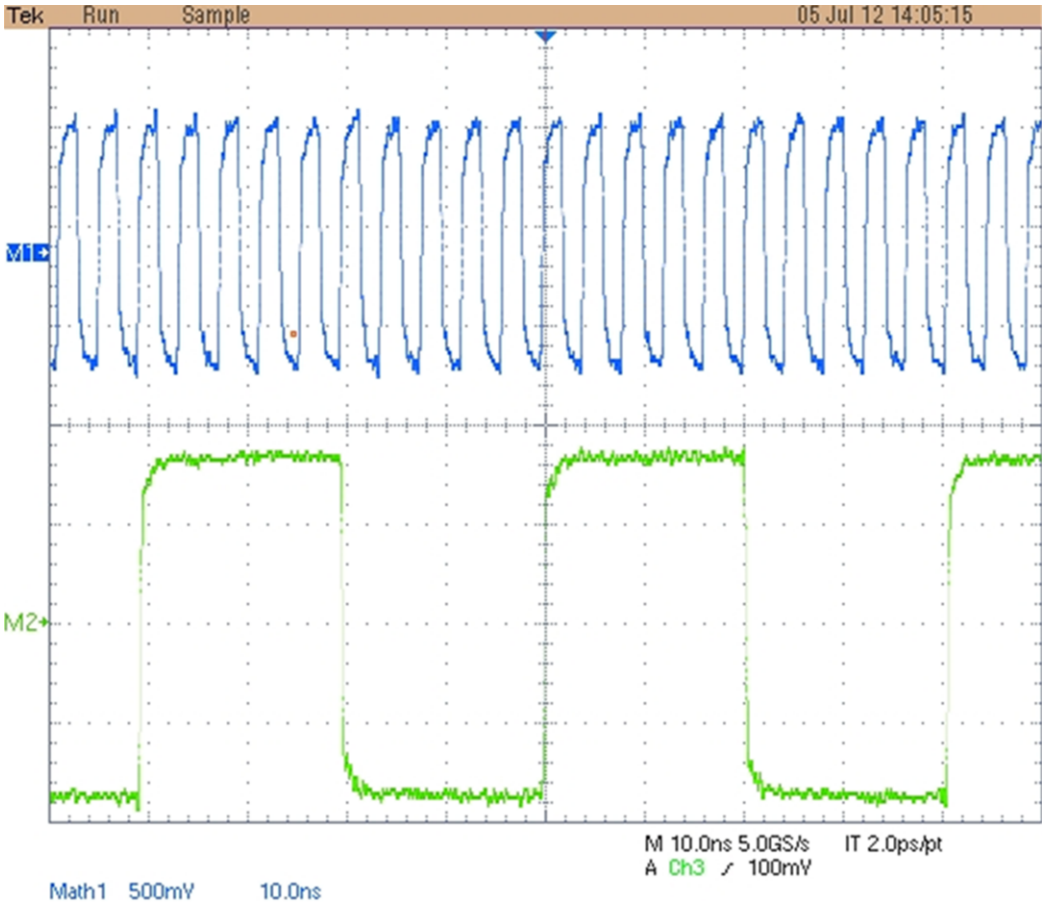

Figure 3. Continuous SYSREF Output

2.3.2 Pulsed SYSREF

1. On SYSREF tab set SDCLKoutY_PD = 0 (where Y is the desired SDCLKout)
2. On CLKouts tab set SDCLKoutY_MUX = 1 (Set to “SR” for desired SDCLKout)
3. On SYSREF tab set SYSREF_PD and on CLKouts tab SYSREF_DDLY_PD = 0
4. On SYSREF tab set SYNC_DISX and SYNC_DISSYSREF = 0 (where X is the desired DCLKout)
5. Perform a SYNC event (toggle SYNC_POL on/off/on)
6. On SYSREF tab set SYNC_DISX = 1 (for desired DCLKout’s) and SYNC_DISSYSREF = 1
7. On SYSREF tab set SYSREF_MUX = 2 (SYSREF Pulses)
8. On SYSREF tab set SYSREF_PULSE_CNT = 1, 2, 4, or 8 as desired
9. Generate a SYNC event (i.e. toggle SYNC_POL on/off/on)
10. On SYSREF tab ensure SYSREF_CLR = 0 (SYSREF tab, location: right side, below clock output pic)

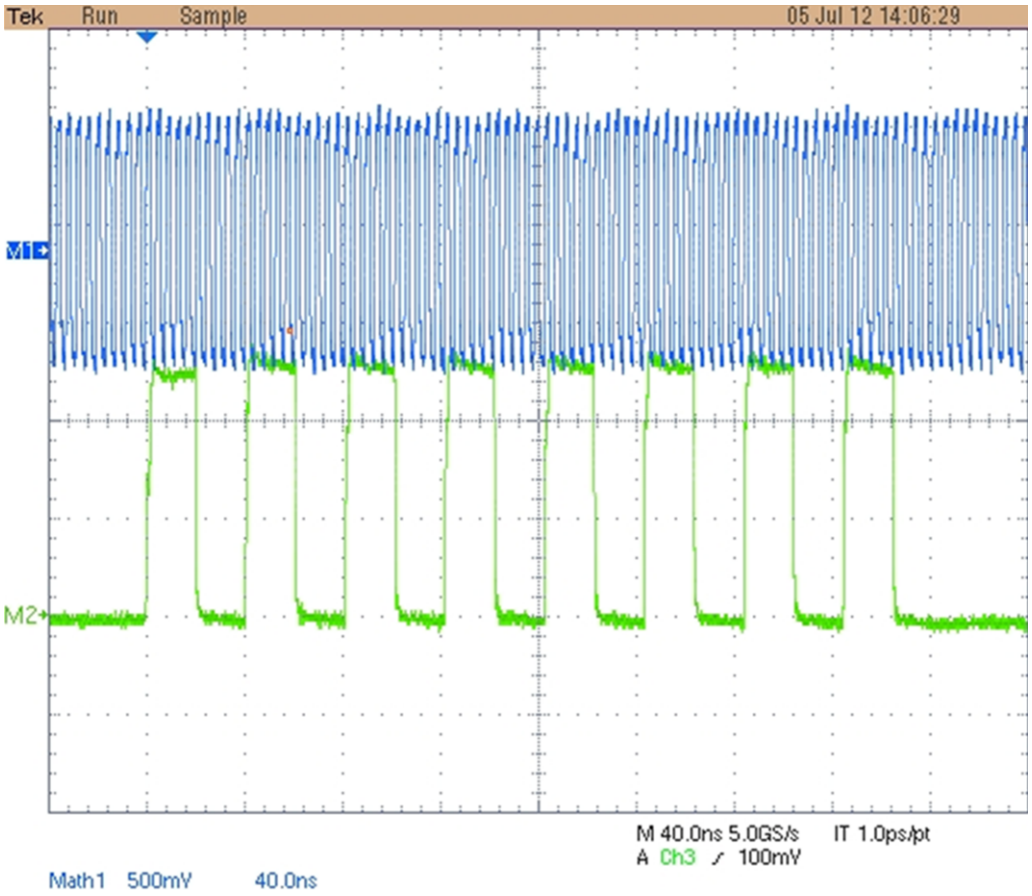

Figure 4. Pulsed SYSREF Output

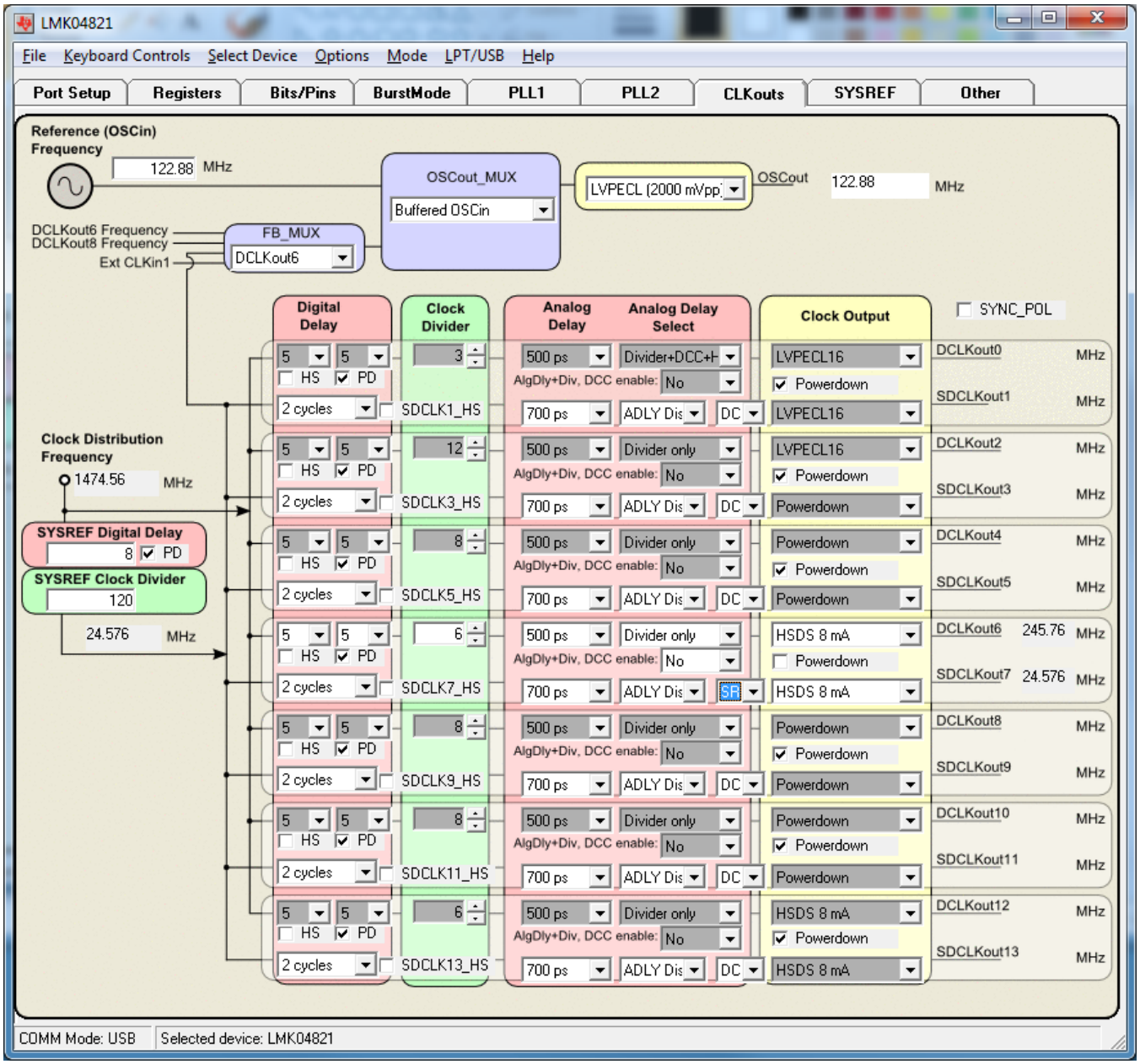

Figure 5. Clock Outputs Tab Setup for SYSREF Output on SDCLKout7

3 PLL Loop Filters and Loop Parameters

In jitter cleaning applications that use a cascaded or dual PLL architecture, the first PLL's purpose is to substitute the phase noise of a low-noise oscillator (VCXO or crystal resonator) for the phase noise of a "dirty" reference clock. The first PLL is typically configured with a narrow loop bandwidth in order to minimize the impact of the reference clock phase noise. The reference clock consequently serves only as a frequency reference rather than a phase reference.

The loop filters on the LMK04821 evaluation board are setup using the approach above. The loop filter for PLL1 has been configured for a narrow loop bandwidth (< 100 Hz). The specific loop bandwidth values depend on the phase noise performance of the oscillator mounted on the board. The following tables (Table 1 and Integrated VCO PLL(1)) contain the parameters for PLL1 and PLL2 for each oscillator option.

TI's Clock Design Tool can be used to optimize PLL phase noise/jitter for given specifications. See: http://www.ti.com/tool/clockdesigntool

3.1 PLL1 Loop Filter

Table 1. PLL1 Loop Filter Parameters for Crystek 122.88 MHz VCXO

122.88 MHz VCXO PLL			
Phase Margin	50°	**Charge Pump Current, Kφ**	450 uA
Loop Bandwidth	14 Hz	**Phase Detector Freq**	1.024 MHz
		VCO Gain	2.5 kHz/V
Reference Clock Frequency	122.88 MHz	**Output Frequency**	122.88 MHz (To PLL 2)
Loop Filter Components	C1_A1 = 100 nF	C2_A1 = 680 nF	R2_A1 = 39 kΩ

3.2 PLL2 Loop Filter

Integrated VCO PLL(1)

	LMK04821		Units
	VCO0	VCO1	
C1_A2	0.047		nF
C2_A2	3.9		nF
C3 (internal)	0.01		nF
C4 (internal)	0.01		nF
R2_A2	0.62		kΩ
R3 (internal)	0.2		kΩ
R4 (internal)	0.2		kΩ
Charge Pump Current, Kφ	3.2		mA
Phase Detector Frequency	122.88		MHz
VCO Frequency	1966.08	2949.12	MHz
Kvco	14.5	16.4	MHz/V
N	16	24	
Phase Margin	72	70	degrees
Loop Bandwidth	288	221	kHz

1. PLL Loop Bandwidth is a function of Kφ, Kvco, N, as well as loop filter components. Changing Kφ and N will change the loop bandwidth

4 Default CodeLoader Modes for the LMK0482x

CodeLoader saves the state of the selected LMK04821 device when exiting the software. To ensure a common starting point, the following modes listed in Table 2 may be restored by clicking “Mode” and selecting the appropriate device configuration.

NOTE: VCO1 Divider may need to be manually set as it state is not directly saved.

Table 2. Default CodeLoader Modes for the LMK0482x

Default CodeLoader Mode	Device Mode	CLKin Frequency	OSCin Frequency
CLKin1 122.88 MHz, OSCin 122.88 MHz	Dual PLL, Internal VCO	122.88 MHz	122.88 MHz

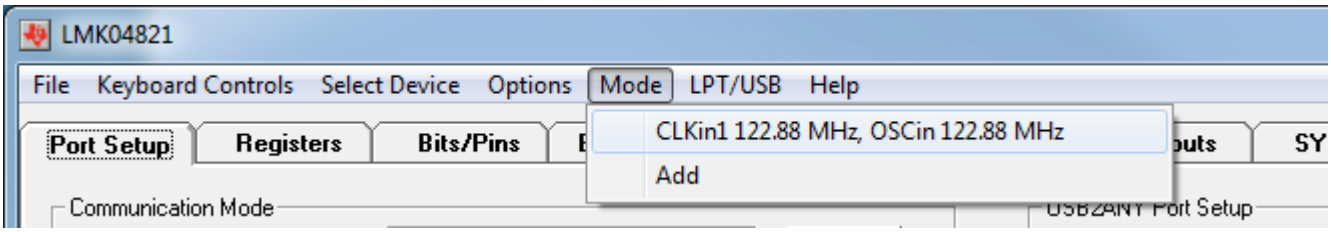

Figure 6. Selecting a Default Mode for the LMK04828 Device

5 Using CodeLoader to Program the LMK04821

The purpose of this section is to walk the user through using CodeLoader 4 to make some measurements with the LMK04821 device as an example. For more information on CodeLoader refer to CodeLoader 4 instructions located at http://www.ti.com/tool/codeloader

Before proceeding, be sure to follow the Section 2 section above to ensure proper connections.

5.1 Start CodeLoader Application

Click “Start” → “Programs” → “CodeLoader 4” → “CodeLoader 4”

The CodeLoader 4 program is installed by default to the CodeLoader 4 application group.

5.2 Select Device

Click “Select Device” → “Clock Conditioners” → “LMK04821”

Once started CodeLoader 4 will load the last used device. To load a new device click “Select Device” from the menu bar, then select the subgroup and finally device to load. Selecting the device does cause the device to be programmed.

5.3 Program/Load Device

Assuming the Port Setup settings are correct, press the “Ctrl+L” shortcut or click “Keyboard Controls” → “Load Device” from the menu to program the device to the current state of the newly loaded LMK04821 file.

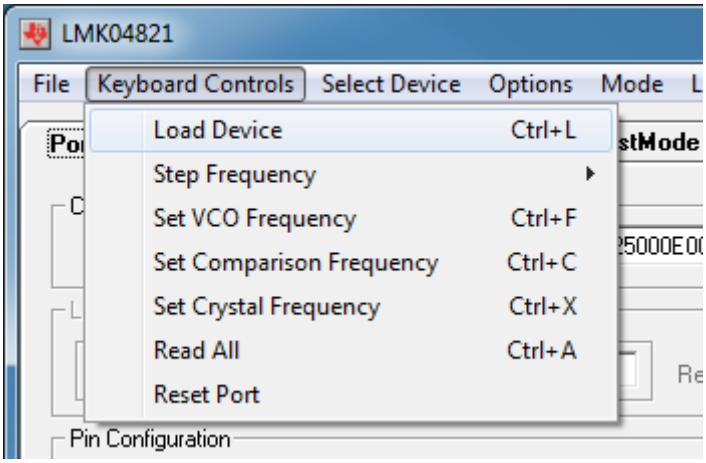

Figure 7. Loading the Device

Once the device has been initially loaded, CodeLoader will automatically program changed registers so it is not necessary to re-load the device upon subsequent changes in the device configuration. It is possible to disable this functionality by ensuring there is no checkmark by the “Options” → “AutoReload with Changes.”

Because a default mode will be restored in the next step, this step isn’t completely necessary but included to emphasize the importance of pressing “Ctrl+L” to load the device at least once after starting CodeLoader, restoring a mode, or restoring a saved setup using the File menu.

See CodeLoader 4 instructions located at http://www.ti.com/tool/codeloader/ for more information on Port Setup. This contains information on troubleshooting communications.

5.4 Restoring a Default Mode

Click “Mode” → “CLKin1 122.88 MHz, OSCin 122.88 MHz”; then press Ctrl+L.

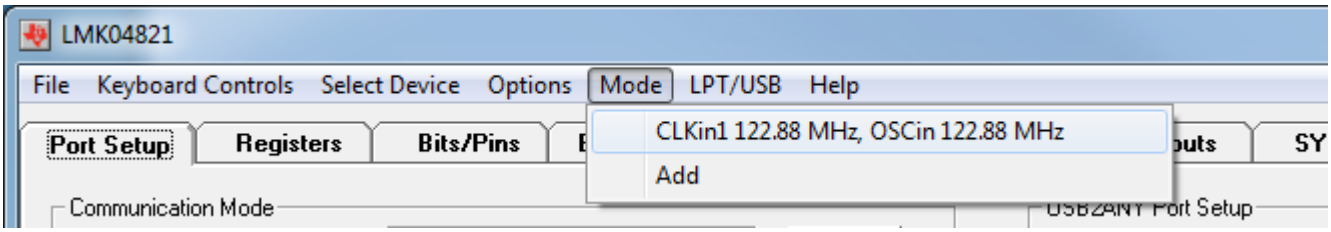

Figure 8. Setting the Default Mode for LMK04828

For the purpose of this walkthrough, a default mode will be loaded to ensure a common starting point. This is important because when CodeLoader is closed, it remembers the last settings used for a particular device. Again, remember to press Ctrl+L as the first step after loading a default mode.

5.5 Visual Confirmation of Frequency Lock

After a default mode is restored and loaded, LED D4, and D5 should illuminate when PLL1 and PLL2 are locked to the reference clock applied to CLKin1. This assumes PLL1_LD_MUX = PLL1_DLD, PLL2_LD_MUX = PLL2_DLD and PLLX_LD_TYPE = Output (Push-Pull).

5.6 Enable Clock Outputs

While the LMK04821 offers programmable clock output buffer formats, the evaluation board is shipped with pre-configured output terminations to match the default buffer type for each output.

To measure Phase noise at one of the clock outputs, for example DCLKout0:

1. 1. Click on the Distribution tab,
2. 2. Uncheck “Powerdown” in the Clock output box to enable the channel,
3. 3. Set the following settings as needed:
   (a) Digital Delay value
   (b) Clock Divider value
   (c) Analog delay select and Analog Delay value (if not “Analog Delay and Divider” is selected in the Analog Delay Select box,

Figure 9. Setting Digital Delay, Clock Divider, Analog Delay and Output Format

4. Depending on the configured output type, the clock output SMAs can be interfaced to a test instrument with a single-ended 50-ohm input as follows.
   (a) For LVDS:
      (i) A balun (like ADT2-1T or high quality Prodyn BIB-100G) is recommended for differential-to-single-ended conversion.
   (b) For LVPECL:
      (i) A balun can be used, or
      (ii) One side of the LVPECL signal can be terminated with a 50-ohm load and the other side can be run single-ended to the instrument.
   (c) For HSDS:
      (i) A balun (like ADT2-1T or high quality Prodyn BIB-100G) is recommended for differential-to-single-ended conversion.
5. The phase noise may be measured with a spectrum analyzer or signal source analyzer.

TI’s Clock Design Tool can be used to calculate divider values to achieve desired clock output frequencies. See: http://www.ti.com/tool/clockdesigntool

6 Evaluation Board Inputs and Outputs

The following table (Table 3) contains descriptions of the inputs and outputs for the evaluation board. Unless otherwise noted, the connectors described can be assumed to be populated by default. Additionally, some applicable CodeLoader programming controls are noted for convenience.

Table 3. Description of Evaluation Board Inputs and Outputs

<table>
<tr><th>Connector Name</th><th>Signal Type, Input/Output</th><th colspan="2">Description</th></tr>
<tr><td rowspan="19">Populated:
DCLKout0,
DCLKout0*,
SDCLKout1,
SDCLKout1*,
DCLKout2,
DCLKout2*,
SDCLKout3,
SDCLKout3*,
DCLKout10,
DCLKout10*
SDCLKout11,
SDCLKout11*</td><td rowspan="19">Analog,
Output</td><td colspan="2">Clock outputs with programmable output buffers.

The output terminations by default on the evaluation board are shown below:</td></tr>
<tr><td>Clock Output Pair</td><td>Default Board Termination</td></tr>
<tr><td>DCLKout0</td><td rowspan="4">240 Ω emitter resistor
(LVPECL16/LVPECL20/LCPECL)</td></tr>
<tr><td>SDCLKout1</td></tr>
<tr><td>DCLKout2</td></tr>
<tr><td>SDCLKout3</td></tr>
<tr><td>DCLKout4</td><td rowspan="10">560 Ω across output
(LVDS / HSDS 6 mA / HSDS 8 mA /
HSDS 10 mA)</td></tr>
<tr><td>SDCLKout5</td></tr>
<tr><td>DCLKout6</td></tr>
<tr><td>SDCLKout7</td></tr>
<tr><td>DCLKout8</td></tr>
<tr><td>SDCLKout9</td></tr>
<tr><td>DCLKout10</td></tr>
<tr><td>SDCLKout11</td></tr>
<tr><td>DCLKout12</td></tr>
<tr><td>SDCLKout13</td></tr>
<tr><td colspan="2">Each CLKout pair has a programmable LVDS, LVPECL, or HSDS buffer. The output buffer type can be selected in CodeLoader in the Clock Outputs tab via the CLKoutX_TYPE control.

All clock outputs are AC-coupled to allow safe testing with RF test equipment.

All LVPECL clock outputs are terminated using 240 Ω emitter-resistors.

All HSDS clock outputs have 560 Ω resistor across output.

If an output pair is programmed to LVCMOS, each output can be independently configured (normal, inverted, or off/tri-state).</td></tr>
<tr><td rowspan="5">Populated:
OSCout, OSCout*</td><td rowspan="5">Analog,
Output</td><td colspan="2">Buffered outputs of OSCin port.</td></tr>
<tr><td colspan="2">The output terminations on the evaluation board are shown below.:</td></tr>
<tr><td>OSC output pair</td><td>Default Board Termination</td></tr>
<tr><td>OSCout</td><td>240 Ω emitter resistor
LVPECL</td></tr>
<tr><td colspan="2">OSCout has a programmable LVDS, LVPECL, or LVCMOS output buffer. The OSCout buffer type can be selected in CodeLoader on the Distribution tab via the OSCout_FMT control.

OSCout is AC-coupled to allow safe testing with RF test equipment.

The OSCout output is terminated using 240 Ω emitter-resistors.

If OSCout is programmed as LVCMOS, each output can be independently configured (normal, inverted, inverted, and off/tri-state).

Best performance/EMI reduction is achieved by using a complementary output mode like Norm/Inv. It is NOT recommended to use Norm/Norm or Inv/Inv mode.</td></tr>
</table>

Table 3. Description of Evaluation Board Inputs and Outputs (continued)

Connector Name	Signal Type, Input/Output	Description
Populated: Vcc	Power, Input	Main power supply input for the evaluation board. The LMK04821 contains internal voltage regulators for the VCO, PLL and other internal blocks. The clock outputs do not have an internal regulator, so a clean power supply with sufficient output current capability is required for optimal performance. On-board LDO regulators and 0 Ω resistor options provide flexibility to supply and route power to various devices. See the schematics in section Section 10 for more details.
Populated: J1	Power, Input	Alternative power supply input for the evaluation board using two unshielded wires (Vcc and GND). Apply power to either Vcc SMA or J1, but not both.
Not Populated: VccVCXO/Aux	Power, Input	Optional Vcc input to power the VCXO circuit if separated voltage rails are needed. The VccVCXO/Aux input can power these circuits directly or supply the on-board LDO regulators. 0 Ω resistor options provide flexibility to route power.
Populated: CLKin0, CLKin0*, CLKin1* Not Populated: CLKin1	Analog, Input	Reference Clock Inputs for PLL1 (CLKin0, 1). CLKin1 can alternatively be used as an External Feedback Clock Input (FBCLKin) in 0-delay mode or an RF Input (Fin) in External VCO mode. **Reference Clock Inputs for PLL1 (CLKin0, 1)** FBCLKin/CLKin1* is configured by default for a single-ended reference clock input from a 50-ohm source.The non-driven input pin (FBCLKin/CLKin1) is connected to GND with a 0.1 uF. CLKin0/CLKin0* is configured by default for a differential reference clock input from a 50-ohm source. CLKin1* is the default reference clock input selected in CodeLoader. The clock input selection mode can be programmed on the **Bits/Pins** tab via the Clock Inputs control. **External Feedback Input (FBCLKin) for 0-Delay** CLKin1 is shared for use with FBCLKin as an external feedback clock input to PLL1 for 0-delay mode. See the LMK0482x family datasheet (literature number SNAS605) for more details on using 0-delay mode with the evaluation board and the evaluation board software.
Populated: OSCin, OSCin*	Analog, Input	Feedback VCXO clock input to PLL1 and Reference clock input to PLL2. The single-ended output of the onboard VCXO (U4) drives the OSCin* input of the device and the OSCin input of the device is connected to GND with 0.1 uF. A VCXO add-on board may be optionally attached via these SMA connectors with minor modification to the components going to the OSCin/OSCin* pins of device. This is useful if the VCXO footprint does not accommodate the desired VCXO device or if the user desires to use the LMK04821 in single loop mode. A single-ended or differential signal may be used to drive the OSCin/OSCin* pins and must be AC coupled. If operated in single-ended mode, the unused input must be connected to GND with 0.1 uF. Refer to the LMK0482x family datasheet section “Electrical Characteristics” for PLL2 Reference Input (OSCin) specifications (literature number SNAS605).
Test point: VTUNE1_TP	Analog, Input	Tuning voltage output from the loop filter for PLL1. If a VCXO add-on board is used, this tuning voltage can be connected to the voltage control pin of the external VCXO when this SMA connector is installed and connected through R72 by the user.
Test point: VTUNE2_TP	Analog, Input	Tuning voltage output from the loop filter for PLL2.
Test points: SDIO SCK CS*	CMOS, Input/Output	10-pin header for SPI programming interface and programmable logic I/O pins for the LMK04821.

Table 3. Description of Evaluation Board Inputs and Outputs (continued)

<table>
<tr><th>Connector Name</th><th>Signal Type, Input/Output</th><th>Description</th></tr>
<tr><td>Populated:
SPI</td><td></td><td>10-pin header for SPI programming interface and programmable logic I/O pins for the LMK04821.

The programmable logic I/O signals accessible through this header include: RESET, SYNC, Status_LD1, Status_LD2, CLKin_SEL0, and CLKin_SEL1. These logic I/O signals also have dedicated SMAs and test points.</td></tr>
<tr><td>Test point:
Status_LD1_TP

Status_LD</td><td>CMOS,
Input/Output</td><td>Programmable status output pin. By default, set to output the digital lock detect status signal for PLL1.

In the default CodeLoader modes, LED D5 will illuminate green when PLL1 lock is detected by the LMK04821 (output is high) and turn off when lock is lost (output is low).

The status output signal for the Status_LD1 pin can be selected on the Bits/Pins tab via the PLL1_LD_MUX control.</td></tr>
<tr><td>Test point:
Status_LD2_TP

Status_LD2</td><td>CMOS,
Input/Output</td><td>Programmable status output pin. By default, set to output the digital lock detect status signal for PLL2.

In the default CodeLoader modes, LED D4 will illuminate green when PLL1 lock is detected by the LMK04821 (output is high) and turn off when lock is lost (output is low).

The status output signal for the Status_LD1 pin can be selected on the Bits/Pins tab via the PLL2_LD_MUX control.</td></tr>
<tr><td>Test points:
CLKin0_SEL_TP
CLKin1_SEL_TP</td><td>CMOS,
Input/Output</td><td>Programmable status I/O pins. By default, set as input pins for controlling input clock switching of CLKin0 and CLKin1.

These inputs will not be functional because CLKin_SEL_MODE is set to 0 (CLKin0 Manual) by default in the Bits/Pins tab in CodeLoader. To enable input clock switching, CLKin_SEL_MODE must be 3 and Status_CLKinX_TYPE must be 0 to 3 (pin enabled as an input).

Input Clock Switching – Pin Select Mode
When CLKin_SEL_MODE is 3, the Status_CLKinX pins select which clock input is active as follows:
<table>
<tr><th>Status_CLKin1</th><th>Status_CLKin0</th><th>Active Clock</th></tr>
<tr><td>0</td><td>0</td><td>CLKin0</td></tr>
<tr><td>0</td><td>1</td><td>CLKin1</td></tr>
<tr><td>1</td><td>0</td><td>CLKin2</td></tr>
<tr><td>1</td><td>1</td><td>Holdover</td></tr>
</table></td></tr>
<tr><td>Test point:
SYNC_TP

Not Populated:
SYNC</td><td>CMOS,
Input/Output</td><td rowspan="2">Programmable status I/O pin. By default, set as an input pin for synchronize the clock outputs with a fixed and known phase relationship between each clock output selected for SYNC. A SYNC event also causes the digital delay values to take effect.

SYNC/SYSREF_REQ pin forces the SYSREF_MUX into SYSREF Continuous mode (0x03) when SYSREF_REQ_EN = 1.

SYNC/SYSREF_REQ pin can hold outputs in a low state, depending on system configuration. SYNC_POL adjusts for active low or active high control.

A SYNC event can also be programmed by toggling the SYNC_POL_INV bit in the Bits/Pins tab in CodeLoader.</td></tr>
<tr><td>Test point:
RESET_TP</td><td>CMOS,
Input/Output</td></tr>
</table>

7 Recommended Test Equipment

Power Supply

The Power Supply should be a low noise power supply, particularly when the devices on the board are being directly powered (onboard LDO regulators bypassed).

Phase Noise / Spectrum Analyzer

To measure phase noise and RMS jitter, an Agilent E5052 Signal Source Analyzer is recommended. An Agilent E4445A PSA Spectrum Analyzer with the Phase Noise option is also usable although the architecture of the E5052 is superior for phase noise measurements. At frequencies less than 100 MHz the local oscillator noise of the E4445A is too high and measurements will reflect the E4445A's internal local oscillator performance, not the device under test.

Oscilloscope

To measure the output clocks for AC performance, such as rise time or fall time, propagation delay, or skew, it is suggested to use a real-time oscilloscope with at least 1 GHz analog input bandwidth (2.5+ GHz recommended) with 50 ohm inputs and 10+ Gsps sample rate. To evaluate clock synchronization or phase alignment between multiple clock outputs, it's recommended to use phase-matched, 50-ohm cables to minimize external sources of skew or other errors/distortion that may be introduced if using oscilloscope probes.

8 Appendix A: CodeLoader Usage

CodeLoader is used to program the evaluation board with a USB port using the included USB2ANY.

8.1 Port Setup Tab

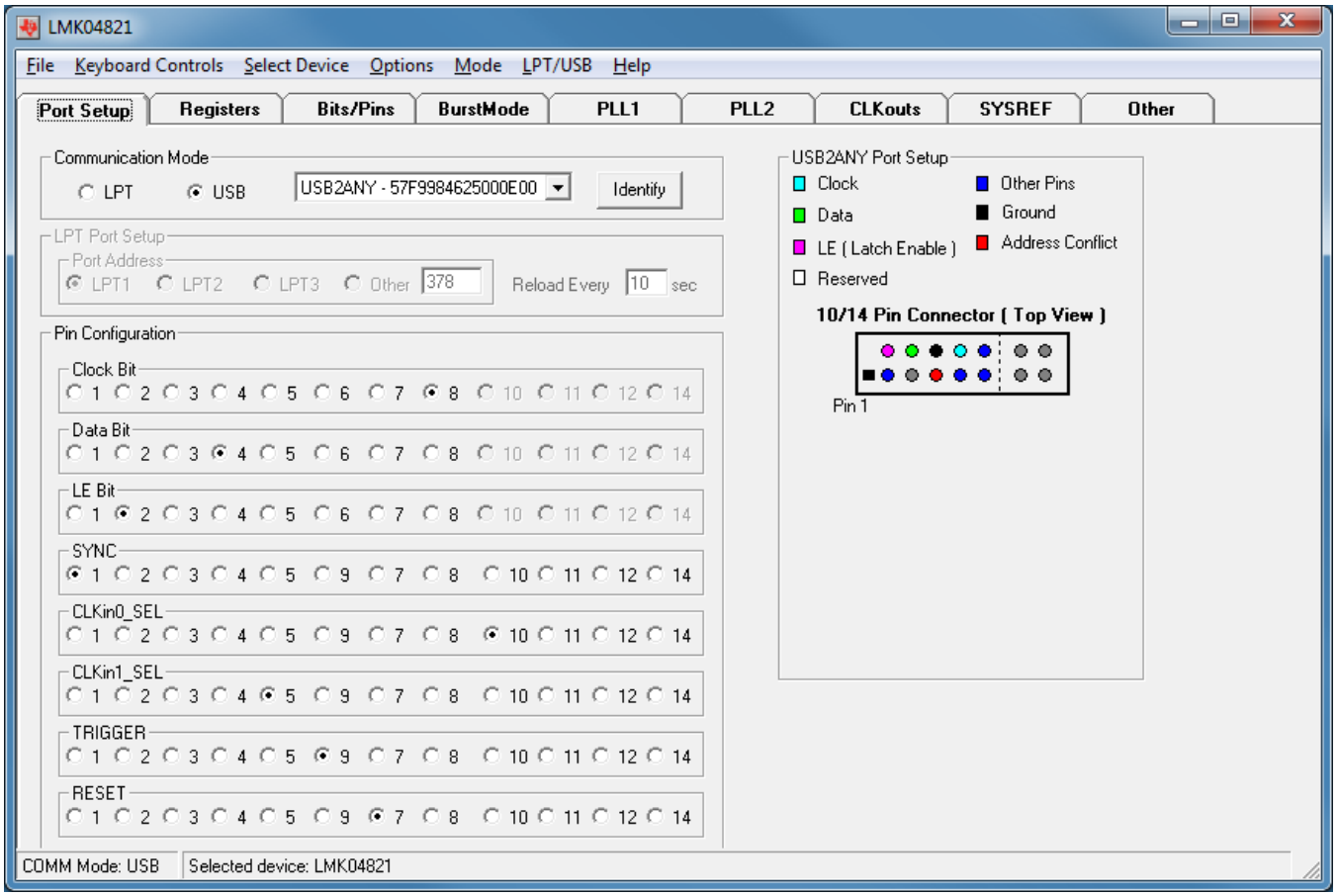

Figure 10. Port Setup Tab

On the Port Setup tab, the user may select the type of communication port (USB or Parallel) that will be used to program the device on the evaluation board. If parallel port is selected, the user should ensure that the correct port address is entered. If USB mode is selected, identify the correct target device by clicking the Identify button - the selected USB2ANY will blink the onboard LED 5 times.

The Pin Configuration field is hardware dependent and normally **does not** need to be changed by the user.

USB interface should be used for LMK04821. When using USB2ANY Clock Bit, Data Bit, and LE Bit positions have no effect.

8.2 PLL1 Tab

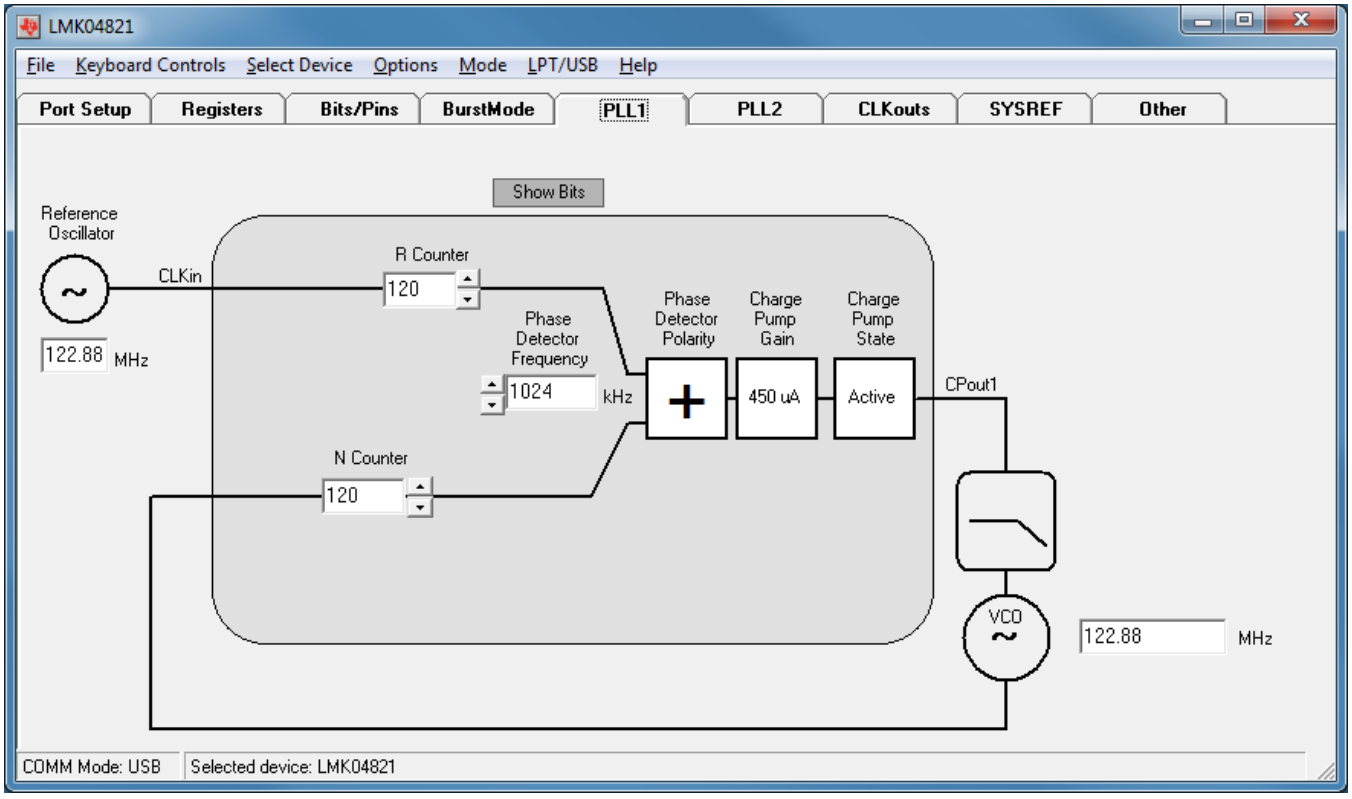

Figure 11. PLL1 Tab

The PLL1 tab allows the user to change the following parameters in Table 4.

Table 4. Registers Controls and Descriptions in PLL1 Tab

Control Name	Register Name	Description
Reference Oscillator Frequency (MHz)	n/a	CLKin frequency of the selected reference clock.
Phase Detector Frequency (MHz)	n/a	PLL1 Phase Detector Frequency (PDF). This value is calculated as: PLL1 PDF = CLKin Frequency / (PLL1_R)
VCO Frequency (MHz)	n/a	The VCO Frequency should be the OSCin frequency, except when operating in Dual PLL with 0-delay feedback. This value is calculated as: VCO Freq (OSCin freq) = PLL1 PDF * PLL1_N.
R Counter	PLL1_R	PLL1 R Counter value (1 to 16383).
N Counter	PLL1_N	PLL1 N Counter value (1 to 16383).
Phase Detector Polarity	PLL1_CP_POL	PLL1 Phase Detector Polarity. Click on the polarity sign to toggle polarity “+” or “–”.
Charge Pump Gain	PLL1_CP_GAIN	PLL1 Charge Pump Gain. Left-click/right-click to increase/decrease charge pump gain (50,150, 250, 1550 uA).
Charge Pump State	PLL1_CP_TRI	PLL1 Charge Pump State. Click to toggle between Active and Tri-State.

8.3 PLL2 Tab

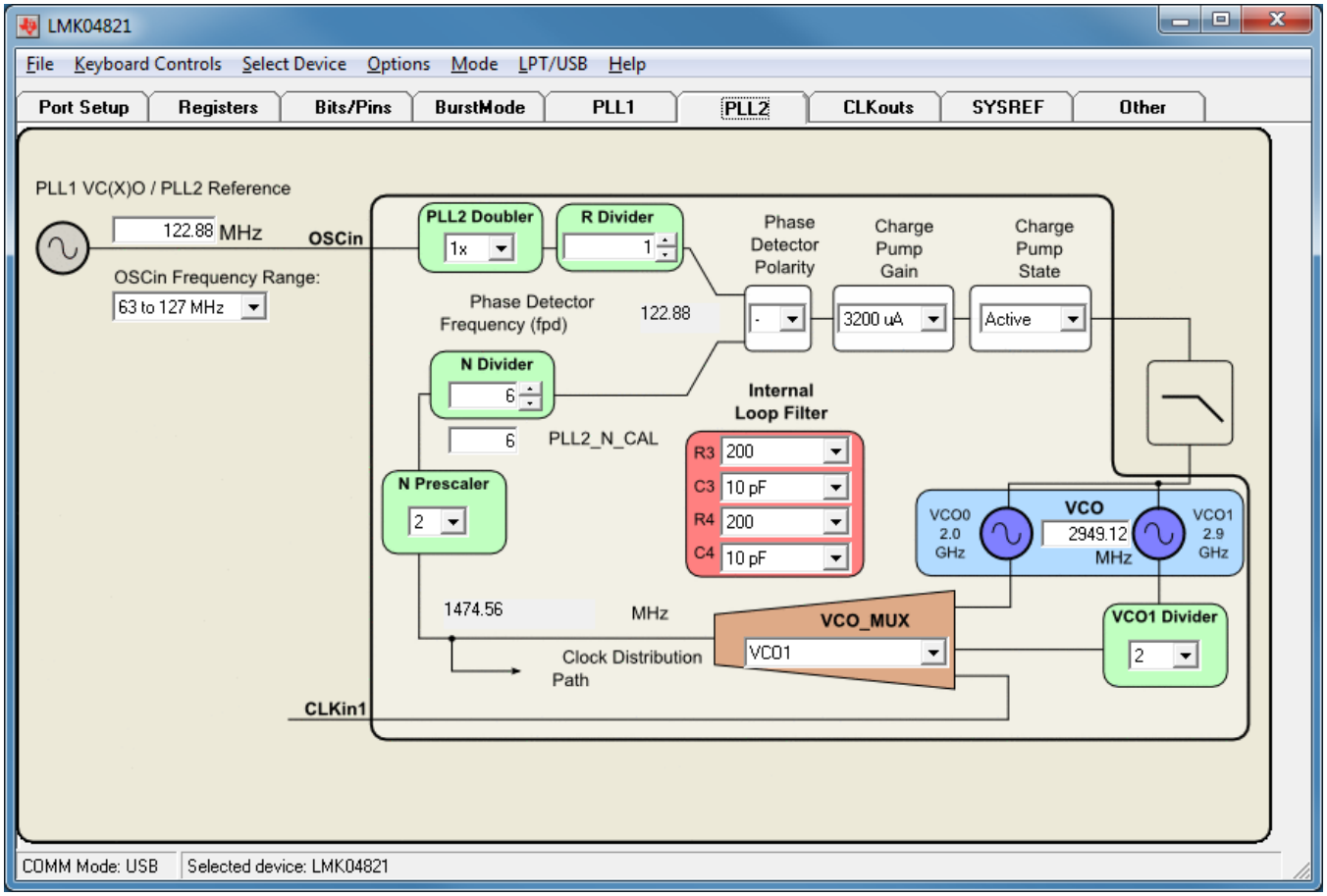

Figure 12. PLL2 Tab

Table 5. Registers Controls and Descriptions in PLL2 Tab[(1)]

Control Name	Register Name	Description
Reference Oscillator Frequency (MHz)	OSCin_FREQ	OSCin frequency from the External VCXO or Crystal.
Phase Detector Frequency (MHz)	n/a	PLL2 Phase Detector Frequency (PDF). Calculated as: PLL2 PDF = OSCin Freq *(2EN_PLL2_REF_2X) / PLL2_R.
VCO Frequency (MHz)	n/a	VCO Frequency of the LMK048xxB device. Calculated as: VCO Freq = PLL2 PDF * (PLL2_N * PLL2_P * VCO div value).
Doubler	EN_PLL2_REF_2X	PLL2 Doubler: 0 = Bypass Doubler, 1 = Enable Doubler
R Counter	PLL2_R	PLL2 R Counter value (1 to 4095).
N Counter	PLL2_N	PLL2 N Counter value (1 to 262143).
PLL Prescaler	PLL2_P	PLL2 N Prescaler value (2 to 8).
Phase Detector Polarity	PLL2_CP_POL	PLL2 Phase Detector Polarity. Click on the polarity sign to toggle polarity “+” or “–”.
Charge Pump Gain	PLL2_CP_GAIN	PLL2 Charge Pump Gain. Left-click/right-click to increase/decrease charge pump gain (100, 400, 1600, 3200 uA).
Charge Pump State	PLL2_CP_TRI	PLL2 Charge Pump State. Click to toggle.
VCO Mux	VCO_MUX	Allows user to select between VCO0, VCO1 with VCO1_DIV, or CLKin1 for external VCO or clock distribution mode.
VCO1 Divider	VCO1_DIV	Allows user to set the divide value used by VCO1 output. This will limit maximum output frequency possible.

(1) Changes made on this tab will be reflected in the **Clock Outputs** tab. The VCO Frequency should conform to the specified internal VCO frequency range.

8.4 Distribution Tab

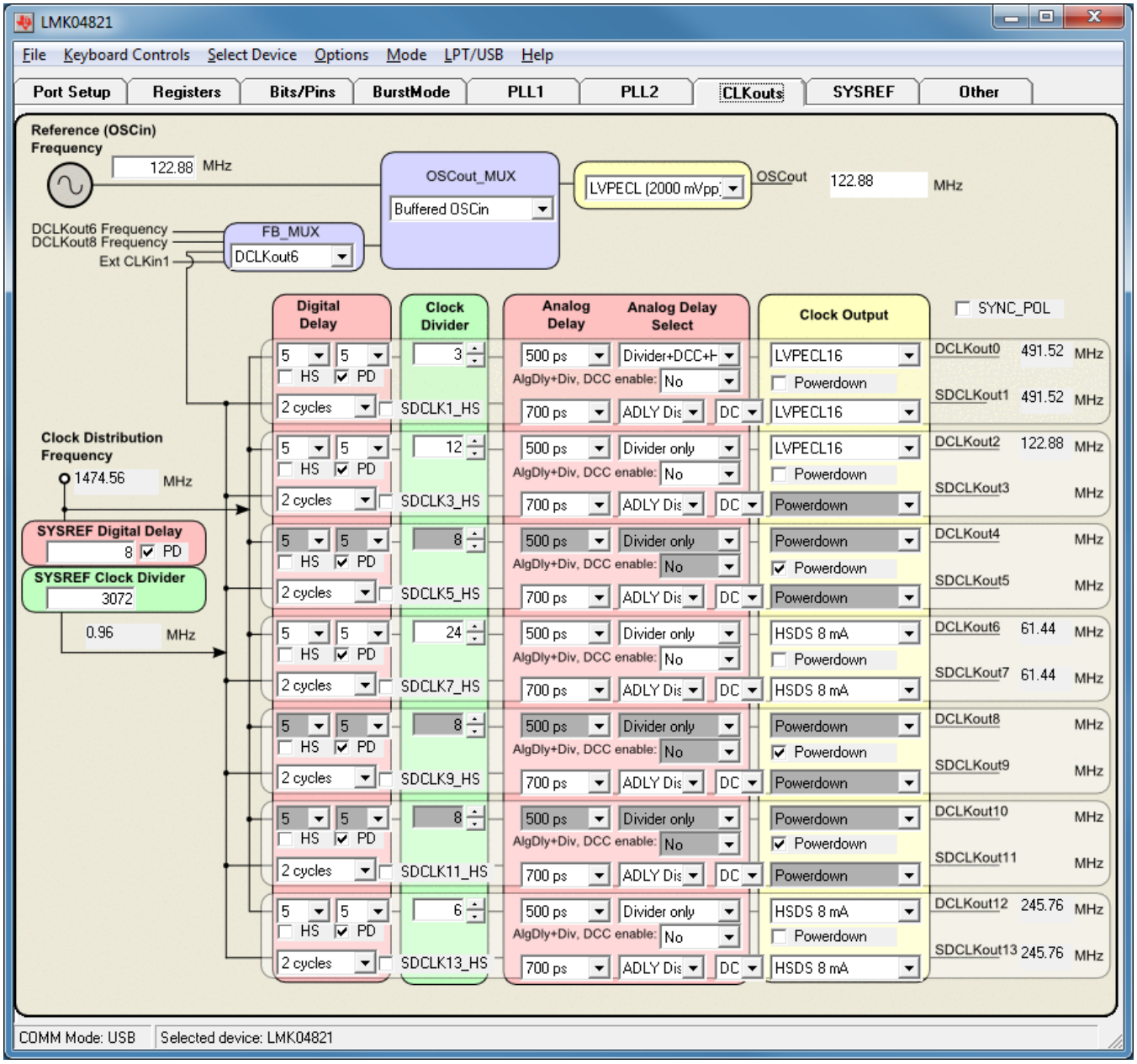

Figure 13. Distribution Tab

The **Distribution tab** allows the user to control the output channel blocks.

Note that the total PLL2 N divider value is the product of the VCO Divider value and the PLL N Prescaler and N Counter values (shown in the **PLL2** tab), and is given by:

PLL2 N Total = PLL2 N Prescaler * PLL2 N Counter (1)

8.5 SYSREF Tab

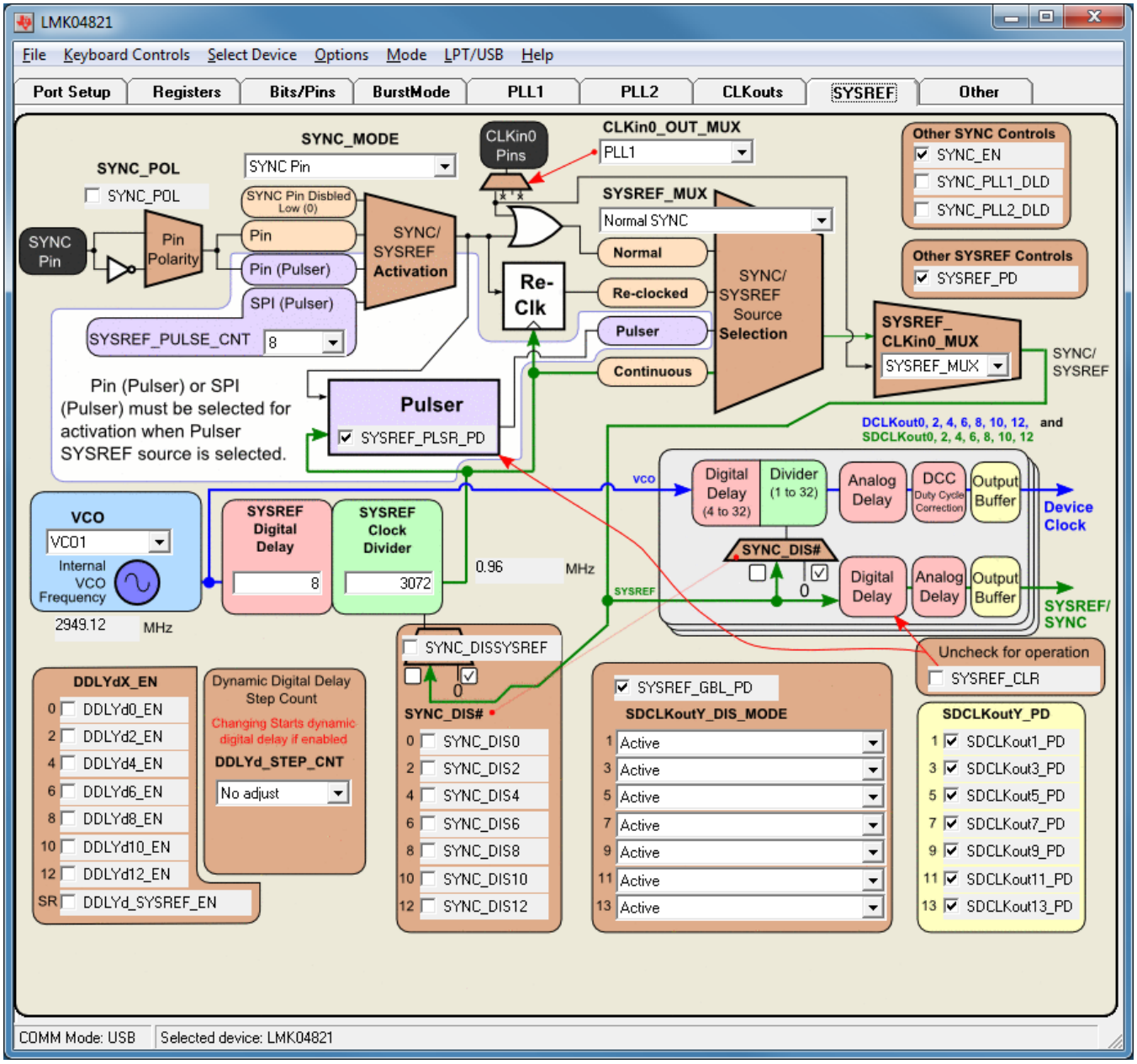

Figure 14. SYSREF Tab

The **SYSREF tab** show the controls for SYSREF functionality as well as Dynamic Digital Delay enable.

8.6 Bits/Pins Tab

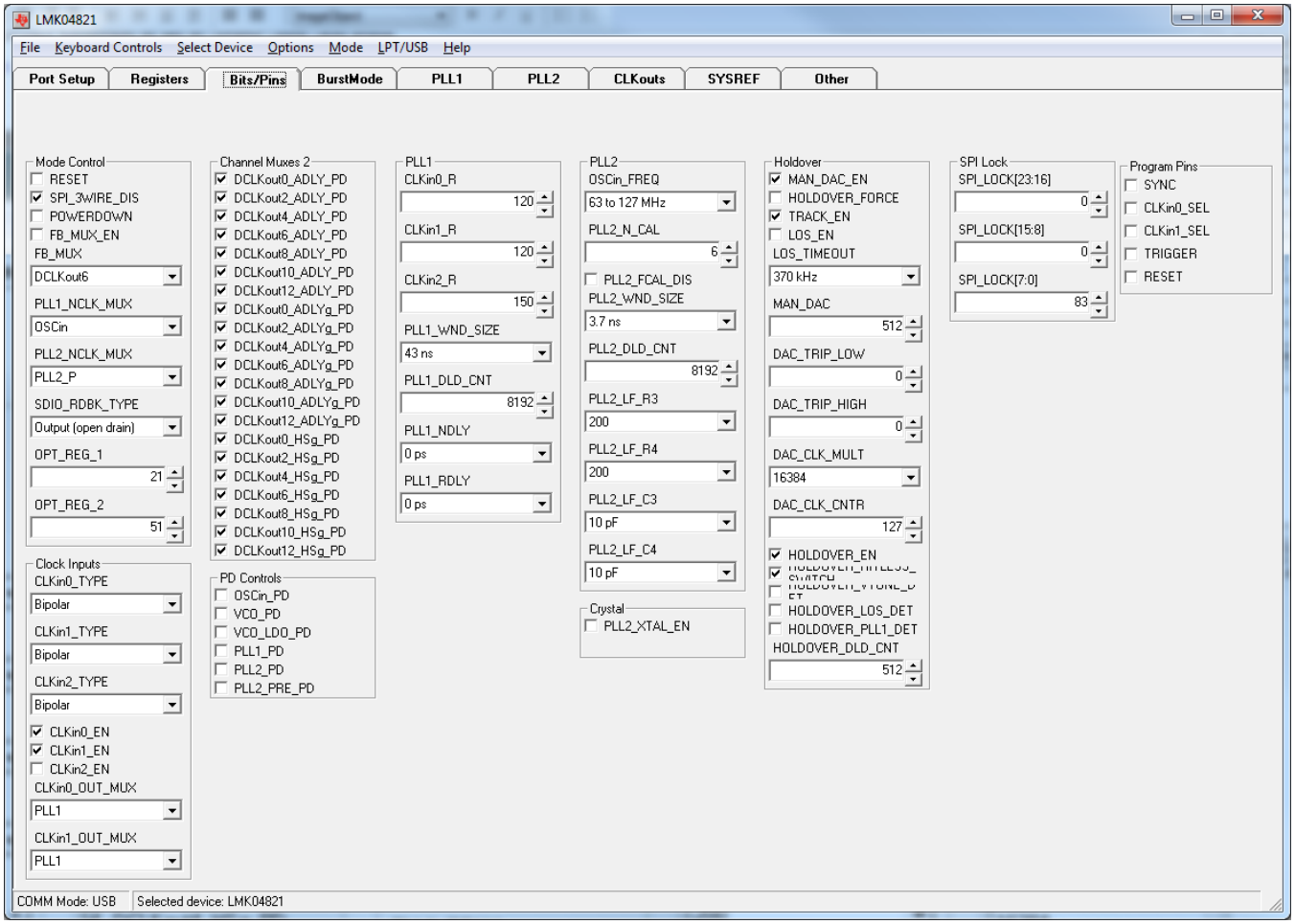

Figure 15. Bits/Pins Tab

The **Bits/Pins** tab allows the user to program bits not available on other tabs.

NOTE: Right-clicking any register name in the **Bits/Pins** tab will display a Help prompt with the register address, data bit location/length, and a brief register description.
On PLL2, CLKouts, SYSREF, and Other tabs pressing the ` key will provide help.

9 Appendix B: Typical Phase Noise Performance Plots

The LMK04821's dual PLL architecture achieves ultra low jitter and phase noise by allowing the external VCXO or Crystal's phase noise to dominate the final output phase noise at low offset frequencies and the internal VCO's phase noise to dominate the final output phase noise at high offset frequencies. This results in the best overall noise and jitter performance.

Table 6 lists the test conditions used for output clock phase noise measurements with the Crystek 122.88 MHz VCXO.

Table 6. LMK04821 Test Conditions

Parameter	Value
PLL1 Reference clock input	CLKin1* single-ended input, CLKin1 AC-coupled to GND
PLL1 Reference Clock frequency	122.88 MHz
PLL1 Phase detector frequency	1024 kHz
PLL1 Charge Pump Gain	450 uA
VCXO frequency	122.88 MHz
PLL2 phase detector frequency	122.88 MHz
PLL2 Charge Pump Gain	3200 uA
PLL2 REF2X mode	Enabled

9.1 122.88 MHz VCXO Phase Noise

The phase noise of the reference is masked by the phase noise of this VCXO by using a narrow loop bandwidth for PLL1 while retaining the frequency accuracy of the reference clock input. This VCXO sets the reference noise to PLL2. Figure 16 shows the open loop typical phase noise performance of the CVHD-950-122.88 Crystek VCXO.

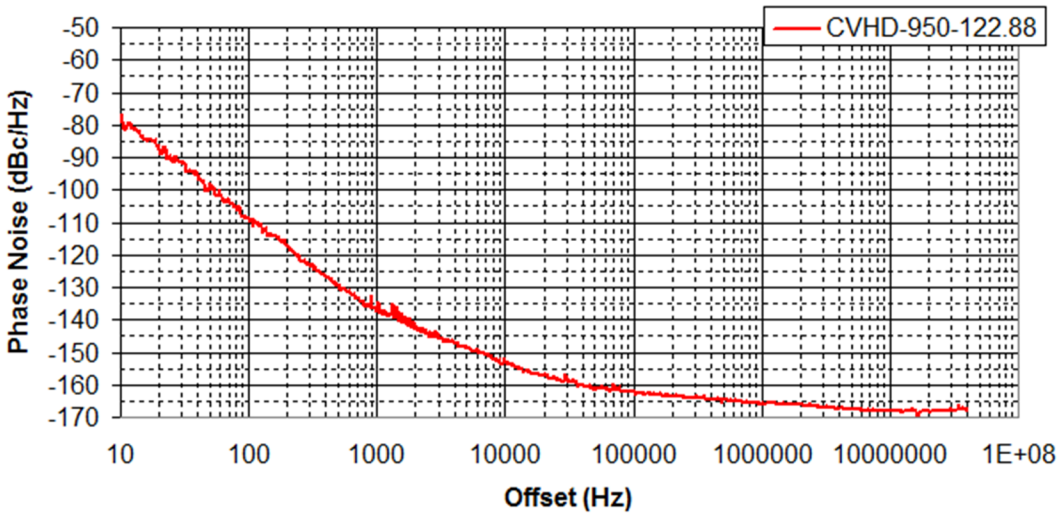

Figure 16. Crystek CVHD-950-122.88 MHz VCXO Phase Noise at 122.88 MHz

Table 7. VCXO Phase Noise and Jitter

Offset	VCXO Phase Noise at 122.88 MHz (dBc/Hz)	VCXO RMS Jitter to high offset of 20 MHz at 122.88 MHz (rms fs)
10 Hz	-76.6	60.5
100 Hz	-108.9	36.2
1 kHz	-137.4	35
10 kHz	-153.3	34.5
100 kHz	-162	32.9
1 MHz	-165.7	22.7
10 MHz	-168.1	515.4
40 MHz	-168.1	60.5

9.2 Output Measurement Technique

The same technique was used to measure phase noise for all three output types available on the programmable OSCout and CLKout buffers. This was achieved by terminating one side of the LVPECL, LVDS, or LVCMOS output with a 50-ohm load, and measuring the other side single-ended using an Agilent E5052B Source Signal Analyzer.

9.3 Clock Outputs (DCLKout and SDCLKout)

The LMK04821 features programmable HSDS, LVDS, LVPECL buffer modes for the DCLKoutX, SDCLKout pairs. Below is a phase noise measurement of DCLKout2 (best phase noise clock output) using a balun.

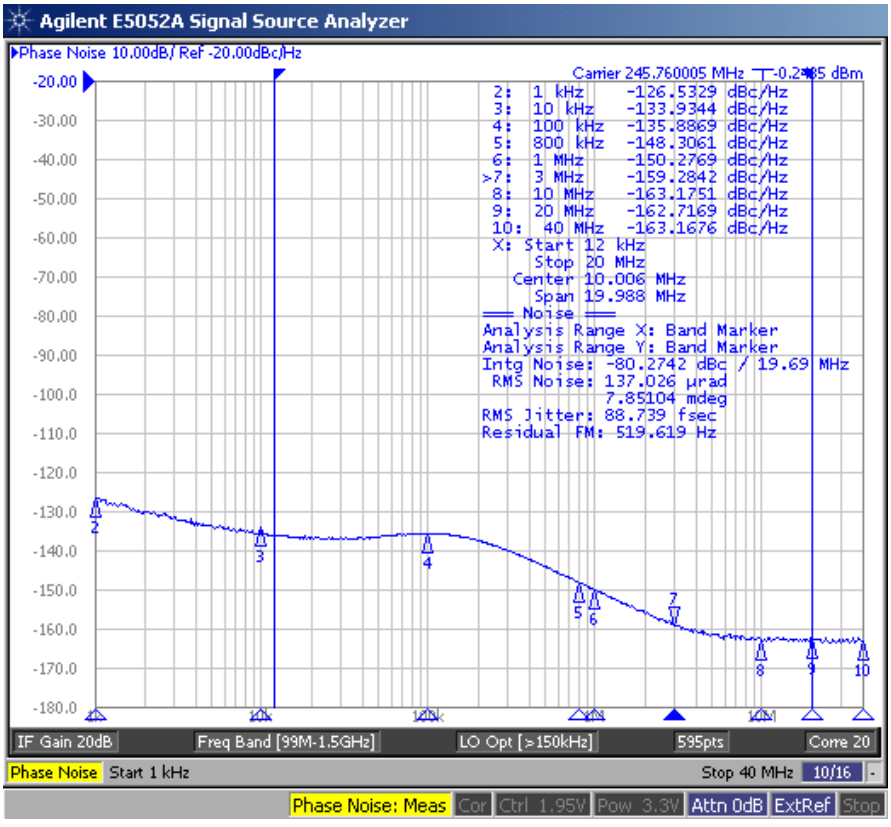

Figure 17. LMK04821 DCLKout2, VCO0, 245.76 MHz, Div8, LVPECL20 /w 240 ohm emitter resistor, DCLKoutX_MUX=Divider, IDL=1, ODL=0, Balun = Prodyn BIB-100G

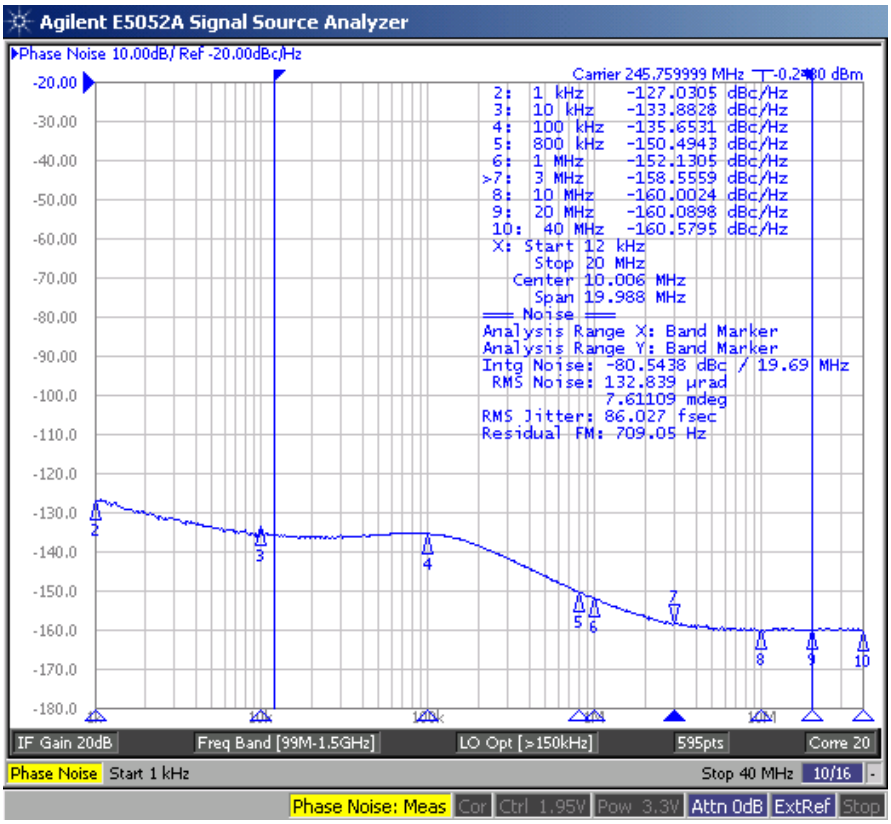

Figure 18. LMK04821 DCLKout2, VCO1, 245.76 MHz, VCO1_DIV = ÷2, CLKout2_DIV = ÷6 LVPECL20 /w 240 ohm emitter resistor, DCLKout2_MUX=Divider, IDL=1, ODL=0, Balun = Prodyn BIB-100G

Figure 19. LMK04821 DCLKout2, VCO1, 245.76 MHz, Div10 , LVPECL20 /w 240 ohm emitter resistor, DCLKoutX_MUX=Divider, IDL=1, ODL=0, Single Ended

10 Appendix C: Schematics

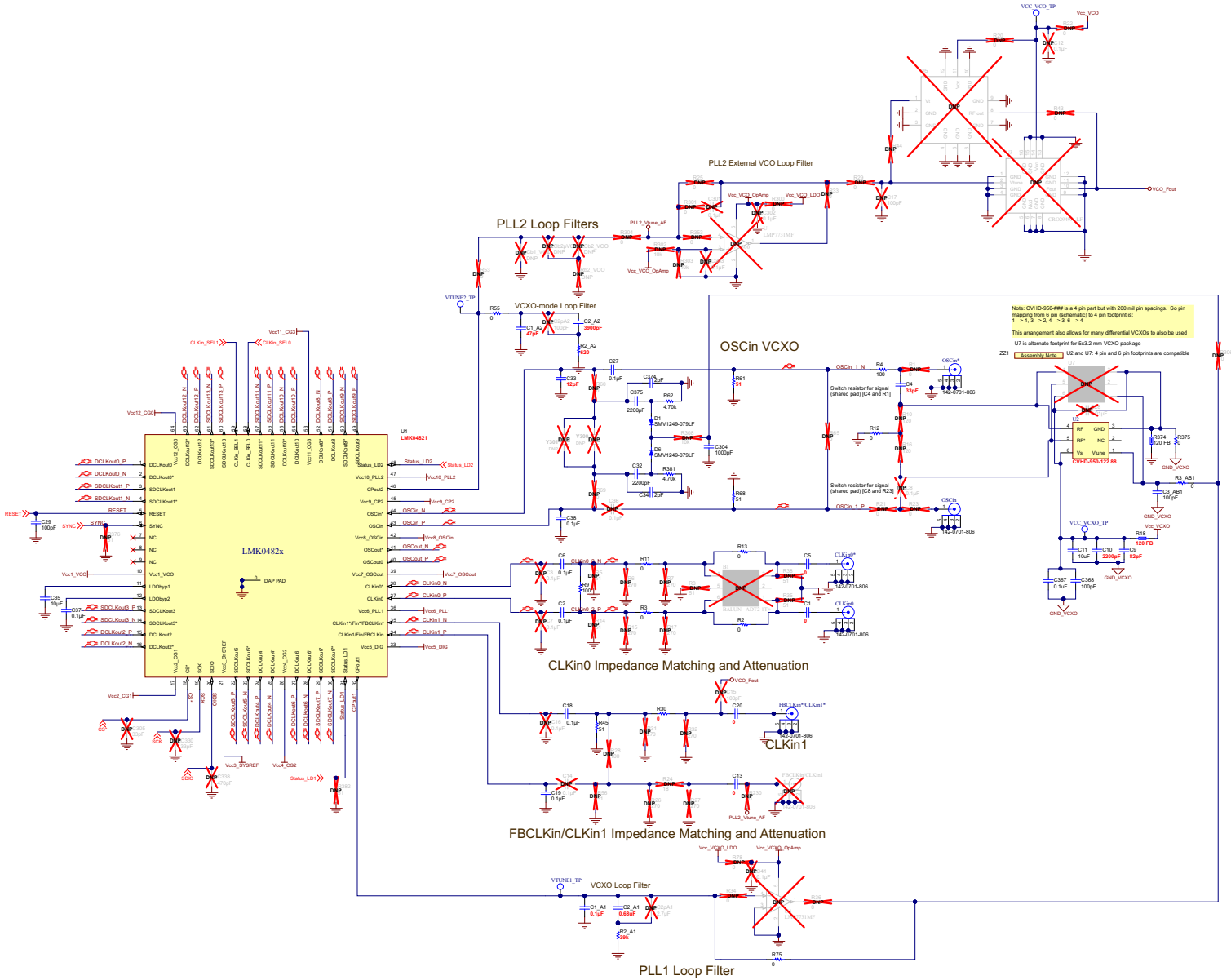

Figure 20. Power Supply

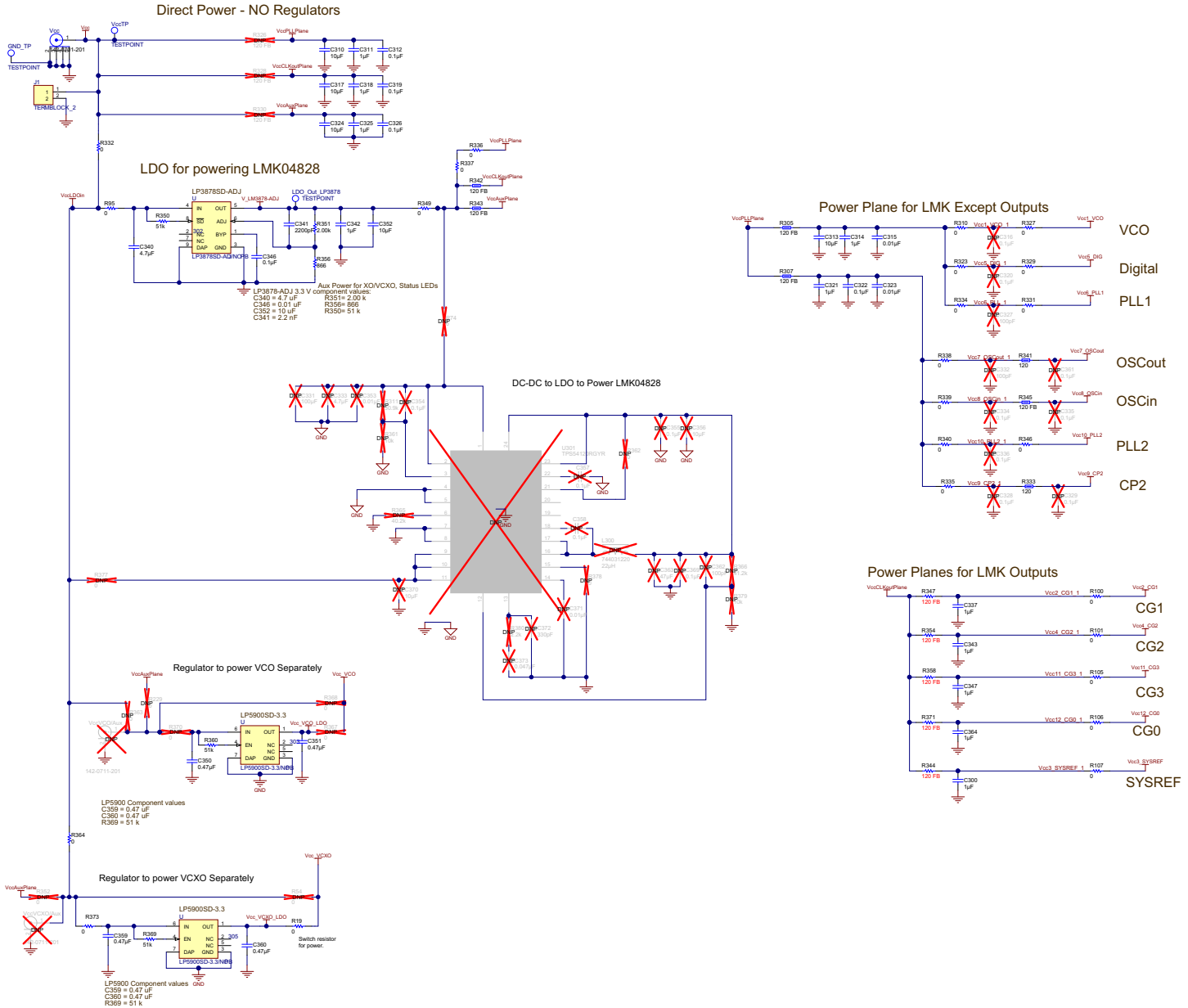

Figure 21. LMK04828B

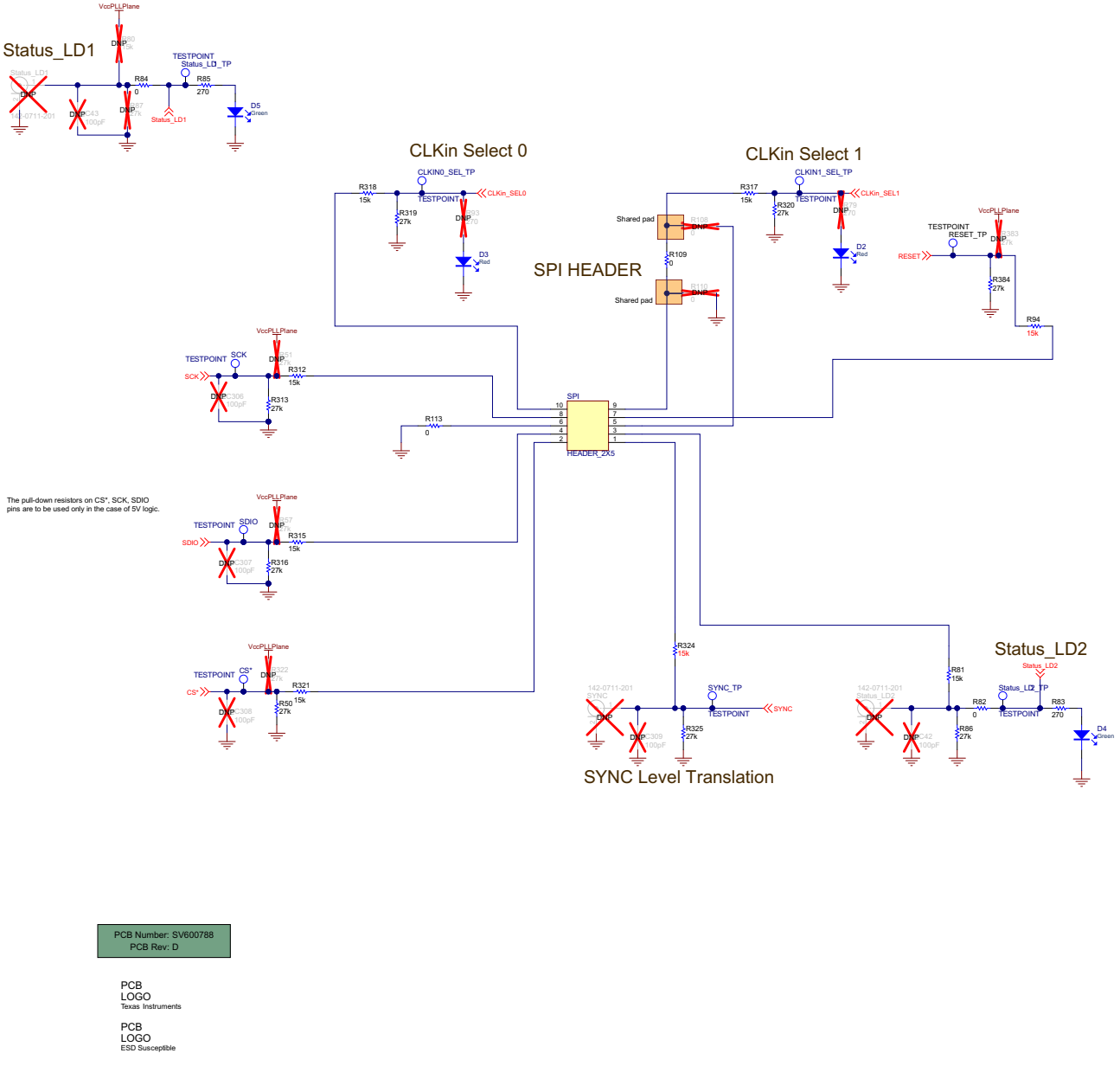

Figure 22. Digital

SYSREF CLOCK OUTPUTS

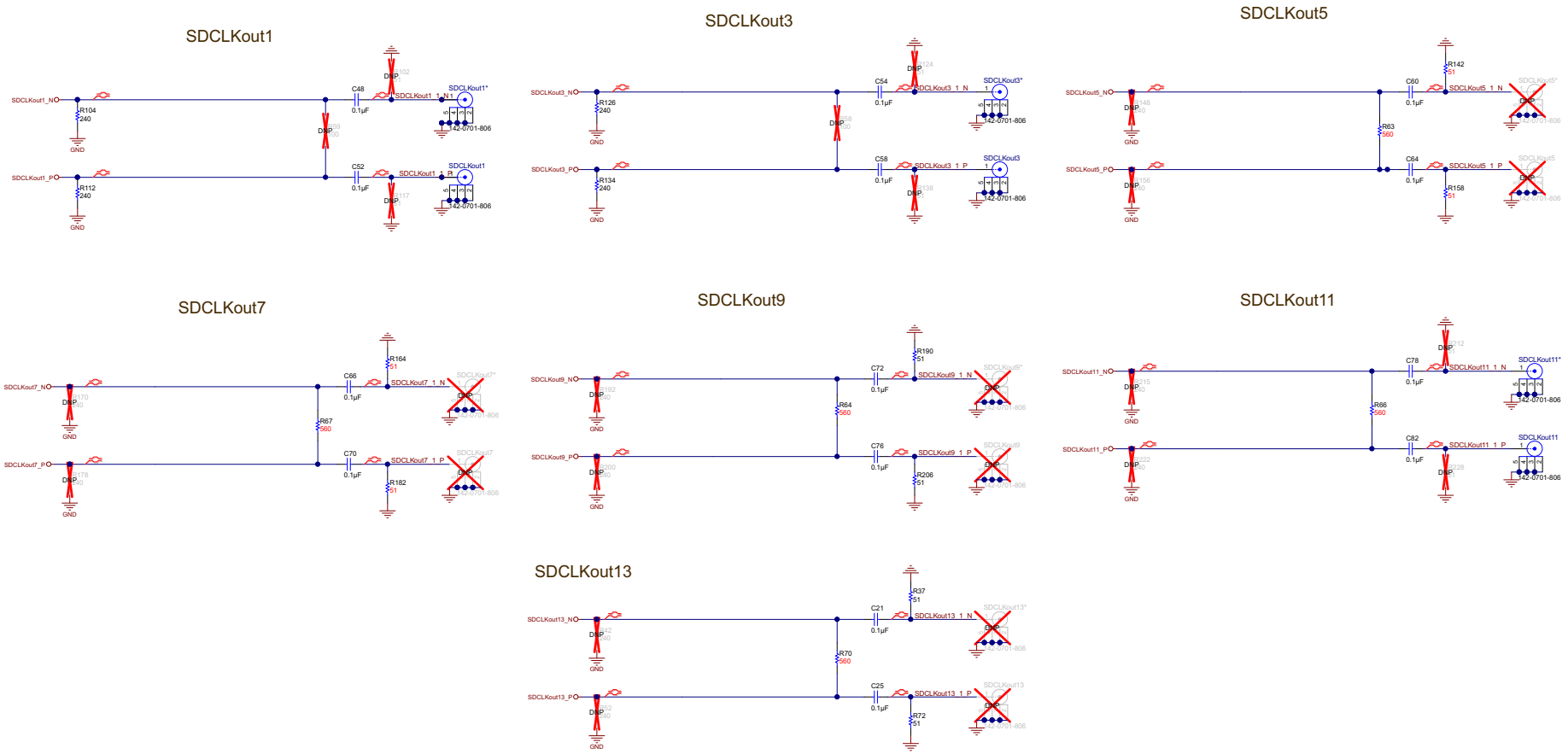

Figure 23. Clock Outputs 1 of 2

DEVICE CLOCK OUTPUTS AND OSCout

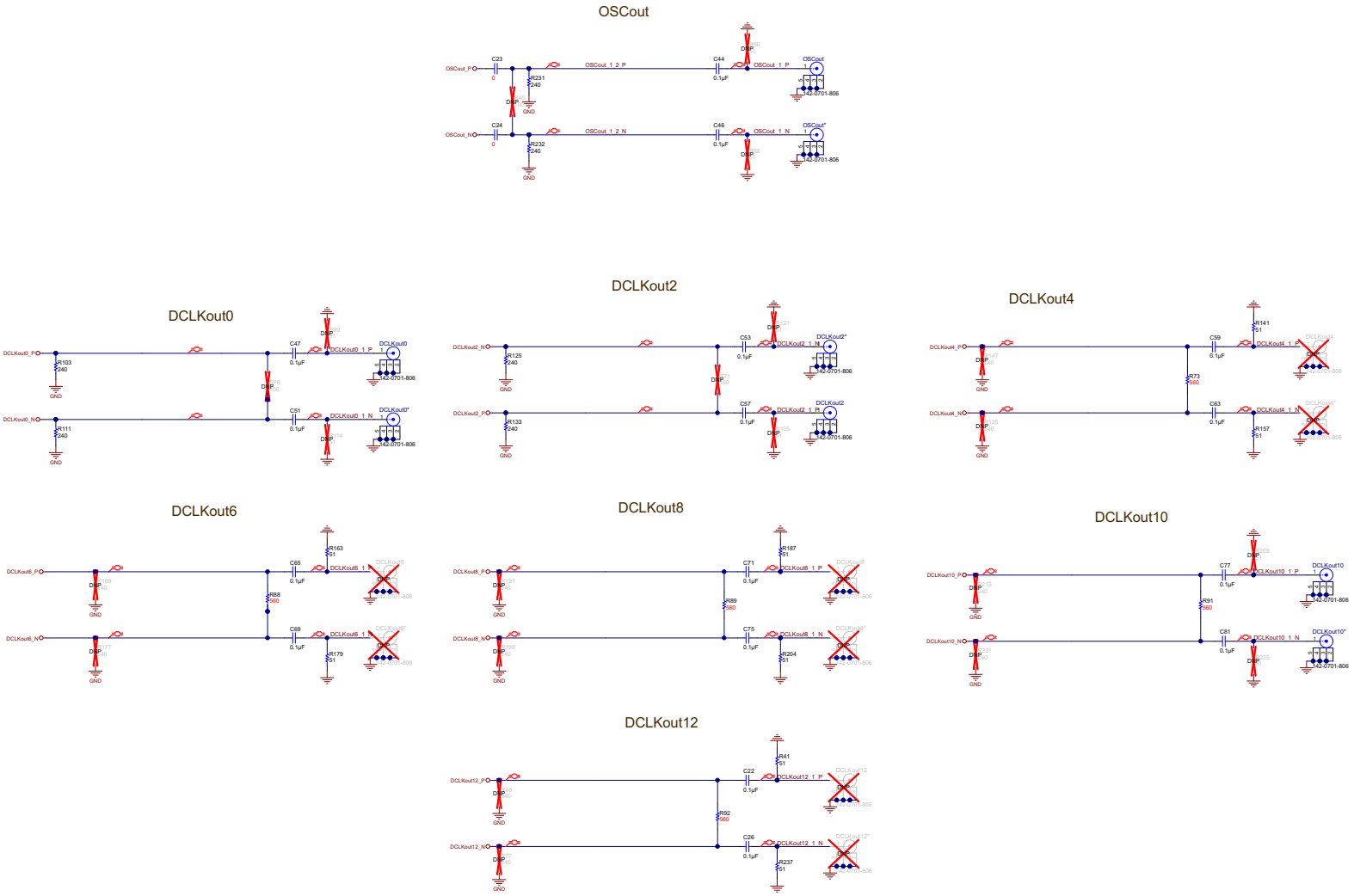

Figure 24. Clock Outputs 2 of 2

11 Appendix D: Bill of Materials

Table 8. Bill of Materials

Item	Designator	Description	Manufacturer	PartNumber	Qty.
1	PCB	Printed Circuit Board	Any	SV600788D	1
2	C1, C5, C13, C20, C23, C24, R3, R3_AB1, R11, R12, R19, R30, R55, R75, R82, R84, R95, R109, R113, R310, R323, R327, R329, R331, R334, R335, R336, R337, R338, R339, R340, R346, R349, R364, R373, R375	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	36
3	C1_A1, C2, C6, C18, C19, C21, C22, C25, C26, C27, C38, C37, C44, C46, C47, C48, C51, C52, C53, C54, C57, C58, C59, C60, C63, C64, C65, C66, C70, C71, C72, C75, C76, C77, C78, C81, C82, C312, C319, C346	CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	Kemet	C0603C104J3RACTU	40
4	C1_A2	CAP, CERM, 47pF, 50V, +/-5%, C0G/NP0, 0603	Kemet	C0603C470J5GACTU	1
5	C2_A1	CAP, CERM, 0.68uF, 10V, +/-10%, X5R, 0603	Kemet	C0603C684K8PACTU	1
6	C2_A2	CAP, CERM, 3900pF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H392KA01D	1
7	C3_AB1, C29, C368	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	Kemet	C0603C101J5GACTU	3
8	C4	CAP, CERM, 33pF, 100V, +/-5%, C0G/NP0, 0603	AVX	06031A330JAT2A	1
9	C9	CAP, CERM, 82pF, 50V, +/-10%, C0G/NP0, 0603	Kemet	C0603C820K5GACTU	1
10	C10, C32, C341, C375	CAP, CERM, 2200pF, 50V, +/-10%, X7R, 0603	Kemet	C0603C222K5RACTU	4
11	C11	CAP, CERM, 10uF, 10V, +/-20%, X5R, 0805	Kemet	C0805C106M8PACTU	1
12	C33	CAP, CERM, 12pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A120JAT2A	1
13	C34, C374	CAP, CERM, 2pF, 50V, +/-12.5%, C0G/NP0, 0603	Kemet	C0603C209C5GACTU	2
14	C35, C310, C317, C324, C352	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	Kemet	C0805C106K8PACTU	5
15	C69, C322, C326, C367	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	Kemet	C0603C104K3RACTU	4
16	C300, C311, C314, C318, C321, C325, C337, C342, C343, C347, C364	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603	Kemet	C0603C105K8PACTU	11
17	C304	CAP, CERM, 1000pF, 50V, +/-5%, C0G/NP0, 0603	Kemet	C0603C102J5GACTU	1
18	C313	CAP, CERM, 10uF, 6.3V, +/-20%, X5R, 0603	Kemet	C0603C106M9PACTU	1
19	C315, C323	CAP, CERM, 0.01uF, 100V, +/-10%, X7R, 0603	Kemet	C0603C103K1RACTU	2
20	C340	CAP, CERM, 4.7uF, 10V, +/-10%, X5R, 0603	Kemet	C0603C475K8PACTU	1
21	C350, C351, C359, C360	CAP, CERM, 0.47uF, 16V, +/-10%, X7R, 0603	Kemet	C0603C474K4RACTU	4

Table 8. Bill of Materials (continued)

Item	Designator	Description	Manufacturer	PartNumber	Qty.
22	CLKin0, CLKin0*, DCLKout0, DCLKout0*, DCLKout2, DCLKout2*, DCLKout10, DCLKout10*, FBCLKin*/CLKin1*, OSCin, OSCin*, OSCout, OSCout*, SDCLKout1, SDCLKout1*, SDCLKout3, SDCLKout3*, SDCLKout11, SDCLKout11*	Connector, SMT, End launch SMA 50 ohm	Emerson Network Power	142-0701-806	19
23	D1, D6	DIODE VARACTOR 15V 20MA SC-79	Skyworks Inc	SMV1249-079LF	2
24	D2, D3	LED 2.8X3.2MM 565NM RED CLR SMD	Lumex Opto/Components Inc.	SML-LX2832IC	2
25	D4, D5	LED 2.8X3.2MM 565NM GRN CLR SMD	Lumex Opto/Components Inc.	SML-LX2832GC	2
26	J1	CONN TERM BLK PCB 5.08MM 2POS OR	Weidmuller	1594540000	1
27	R2, R13, R332	RES, 0 ohm, 5%, 0.125W, 0805	Vishay-Dale	CRCW08050000Z0EA	3
28	R2_A1	RES, 39k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060339K0JNEA	1
29	R2_A2	RES, 620 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603620RJNEA	1
30	R4, R9	RES, 100 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603100RJNEA	2
31	R18, R305, R307, R342, R343, R344, R345, R347, R354, R358, R371, R374	FB, 120 ohm, 500 mA, 0603	Murata	BLM18AG121SN1D	12
32	R37, R41, R45, R61, R68, R72, R141, R142, R157, R158, R163, R164, R179, R182, R187, R190, R204, R206, R237	RES, 51 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060351R0JNEA	19
33	R50, R86, R313, R316, R319, R320, R325, R384	RES, 27k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060327K0JNEA	8
34	R62, R381	RES, 4.70k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-074K7L	2
35	R63, R64, R66, R67, R70, R73, R88, R89, R91, R92	RES, 560 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603560RJNEA	10
36	R81, R94, R312, R315, R317, R318, R321, R324	RES, 15k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060315K0JNEA	8
37	R83, R85	RES, 270 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603270RJNEA	2
38	R100, R101, R105, R106, R107	RES, 0 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04020000Z0ED	5
39	R103, R104, R111, R112, R125, R126, R133, R134, R231, R232	RES, 240 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603240RJNEA	10
40	R333, R341	FB, 120 ohm, 500 mA, 0402	TDK	MMZ1005Y121C	2
41	R350, R360, R369	RES, 51k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060351K0JNEA	3
42	R351	RES, 2.00k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06032K00FKEA	1
43	R356	RES, 866 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603866RFKEA	1
44	S1, S2, S3, S4, S5, S6	0.375" Standoff	VOLTREX	SPCS-6	6
45	SPI	Low Profile Vertical Header 2x5 0.100"	FCI	52601-G10-8LF	1
46	U1	LMK04821	Texas Instruments	LMK04821	1
47	U2	122.88 MHz VCXO	Crystek	CVHD-950-122.88	1
48	U302	Micropower 800mA Low Noise "Ceramic Stable" Adjustable Voltage Regulator for 1V to 5V Applications, 8-pin LLP, Pb-Free	Texas Instruments	LP3878SD-ADJ/NOPB	1
49	U303, U305	Ultra Low Noise, 150mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor, 6-pin LLP, Pb-Free	Texas Instruments	LP5900SD-3.3/NOPB	2

Table 8. Bill of Materials (continued)

Item	Designator	Description	Manufacturer	PartNumber	Qty.
50	Vcc	Connector, TH, SMA	Emerson Network Power	142-0701-201	1

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

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西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY WRITTEN DESIGN MATERIALS PROVIDED WITH THE EVM (AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS ANDCONDITIONS OR THE USE OF THE EVMS PROVIDED HEREUNDER, REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN ONE YEAR AFTER THE RELATED CAUSE OF ACTION HAS OCCURRED.

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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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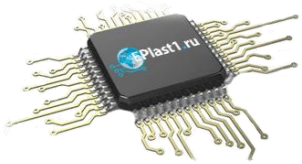

Как с нами связаться

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