DATASHEET

Intel® Enpirion® Power Solutions

EM2040N01QI 40A PowerSoC

Step-Down DC-DC Switching Converter with Integrated Inductor

Description

The EM2040 is a fully integrated 40A PowerSoC synchronous buck converter with digital non-linear control loop. It features an advanced controller, gate drivers, synchronous MOSFET switches, and a high performance inductor. Only input and output filter capacitors and a few small signal components are required for a complete solution. The digital loop enables a reduction in output bulk filter capacitors.

Differential remote sensing and ±0.5% set-point accuracy provides precise regulation over line, load and temperature variation. Very low ripple further reduces accuracy uncertainty to provide best in class static regulation for today's FPGAs, ASICs, processors, and DDR memory devices.

The EM2040 features high conversion efficiency and superior thermal performance to minimize thermal de-rating limitations, which is key to product reliability and longevity.

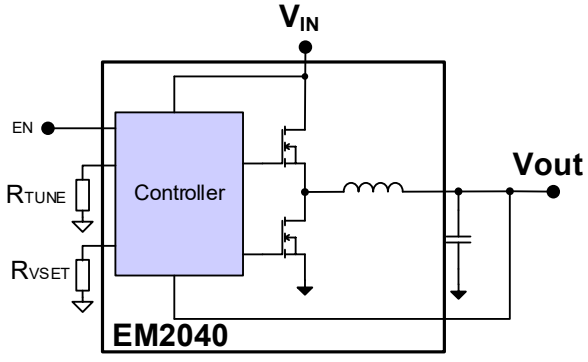
Features

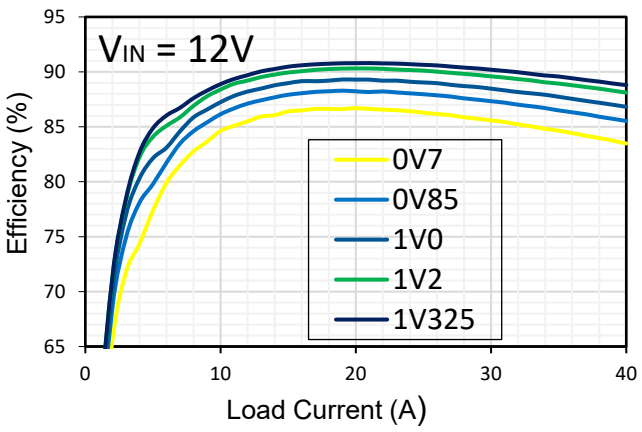
- Integrated inductor, FETs, and controller
- Wide 4.5V to 16V V_{IN} range
- 0.5V to 1.325V V_{OUT} range
- 11mm x 17mm x 6.76mm QFN package
  - 90% efficiency at V_{IN} = 12V, V_{OUT} = 1.2V
- Optimized total solution size of only 365 mm^2
- Meets all high performance FPGA requirements
  - 0.5% set-point over line, load, and temperature
  - Output ripple as low as 10 mV peak-peak
  - Differential remote sensing
- RVSET resistor for programmable V_{OUT}
- RTUNE resistor for single resistor compensation
- Tracking pin for complex sequencing
- RoHS compliant, MSL level 3, 260°C reflow

Applications

- High performance FPGA supply rails
- ASIC and processor supply rails
- High density double data rate (DDR) memory VDDQ rails

Simplifed Block Diagram





Ordering Information

Table 1

Part Number	Supported V_{OUT} Range	Package Markings	Package Description
EM2040N01QI	0.5V to 1.325V	M2040	17 mm x 11 mm x 6.76 mm QFN104 provided in 112 units per tray

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Pin Assignments

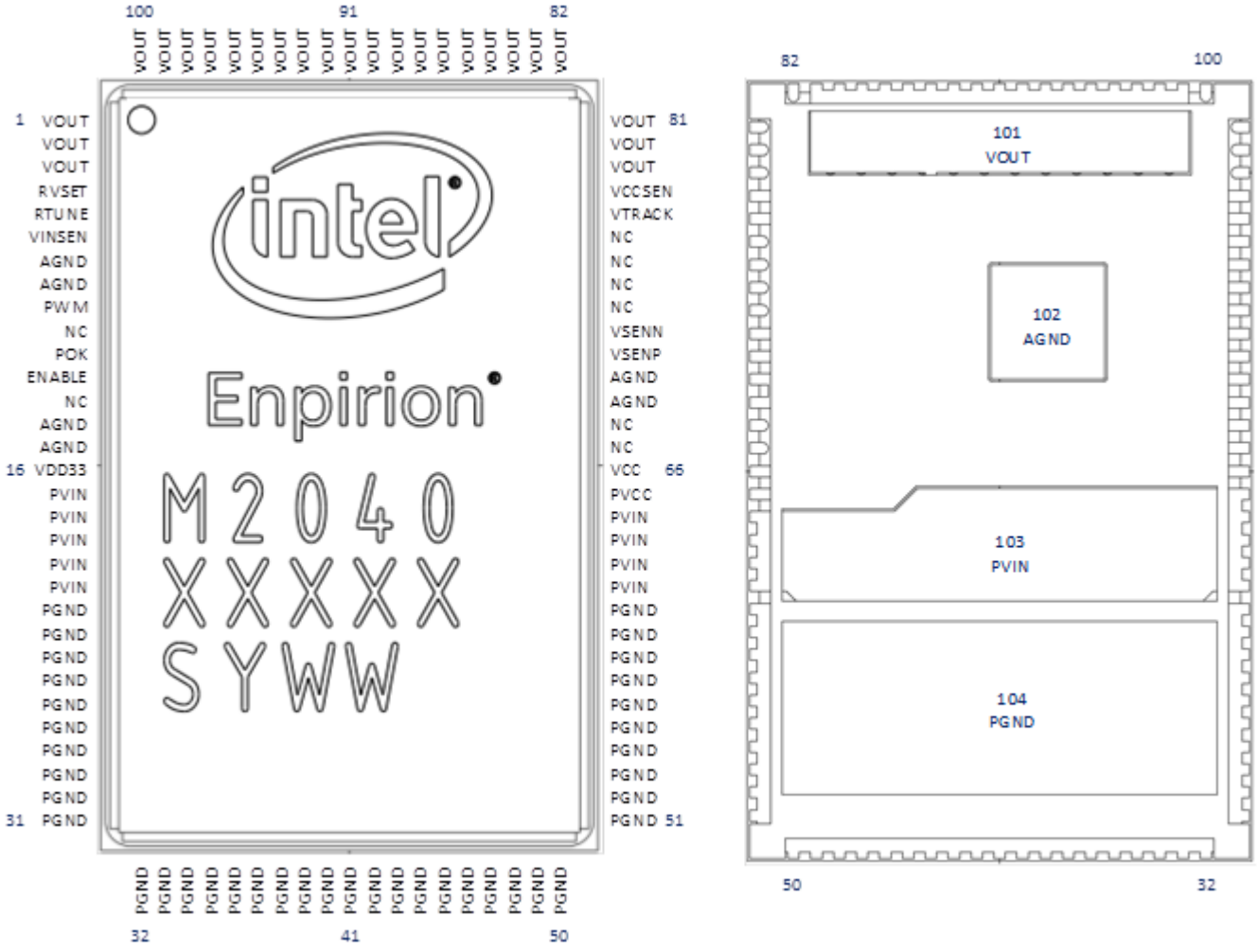


Figure 1: Pin Out Diagram

Pin Description

Table 2

PIN	NAME	I/O	FUNCTION
1,2,3, 79-101	VOUT	Regulated Output	Regulated output voltage. Decouple to PGND with appropriate filter capacitors
4	RVSET	Analog I/O	A resistor from RVSET to AGND; and can be used to program the V_{OUT} set-point. Using 1% tolerance or better resistor. See Table 8 for more information.
5	RTUNE	Analog I/O	A resistor from RTUNE to AGND; and can be used to tune the transient compensator for the amount of output capacitance. Using 1% tolerance or better resistor. See Table 9 for more information.
6	VINSEN	Analog Input	Single-ended input voltage sense (relative to AGND).
7, 8, 14, 15, 69, 70, 102	AGND	Ground	Analog ground. Connect to system ground plane. Refer to layout section for more details on grounding.
9	PWM	PWM	PWM signal test pin.
10, 13, 67,68, 73-76	NC	NC	No connect. Do not connect to any signal, supply, or ground.
11	POK	Input	Power OK signal. Open Drain Output
12	ENABLE	Input	A high on the ENABLE Pin will result in the Vout rising. ENABLE should never be left floating..
16	VDD33	Output	3.3V output of the internal LDO. May be used as pull-up supply ENABLE pin.
17-21, 61-64, 103	PVIN	Input Supply	Input supply for MOSFET switches. Decouple to PGND with appropriate filter capacitors. Refer to Recommended Application Circuit section for more details.
22-60, 104	PGND	Ground	Power ground. Ground for MOSFET switches.
65	PVCC	Input Supply	5.0V supply voltage for driver circuitry. Decouple to PGND using a 2.2µF MLCC high quality ceramic capacitor.
66	VCC	Input Supply	5.0V supply voltage for analog circuitry.
71	VSENP	Analog Input	Differential output voltage sense input (positive).
72	VSENN	Analog Input	Differential output voltage sense input (negative).
77	VTRACK	Analog Input	Voltage tracking reference input. Vout will track applied signal. If not used, it **cannot be left floating** but should be connected to VDD33 using a 10kΩ resistor.
78	VCCSEN	Analog Input	Single-ended VCC voltage sense (relative to AGND)

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Voltage measurements are referenced to AGND.

Absolute Maximum Pin Ratings

Table 3

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply voltage PVIN	PVIN	-0.3	18	V
Supply voltage VCC	VCC	-0.3	5.5	V
VCC ramp time	VCC		20	ms
VDD33	VDD33	-0.3	3.6	V
Power ground	PGND	-0.3	0.3	V
I/O pins	VINSEN, VCCSEN, RVSET, RTUNE, VTRACK	-0.3	2.0	V
I/O pin	ENABLE	-0.3	3.6	V
I/O pin	POK	-0.3	5.5	V
Voltage feedback	VSENP, VSENN	-0.3	2.0	V
PWM pin	PWM	-0.3	5.5	V
Output voltage pins	VOUT	-0.3	1.44	V
DC current on VOUT	VOUT		43	A

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Operating junction temperature			+125	°C
Storage temperature range		-65	+150	°C
Reflow peak body temperature	(10 Sec) MSL3		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBD	All pins; Except VINSEN 1000 V Max	2000		V
CDM; all pins		500		V

Recommended Operating Conditions

Table 4

PARAMETER	PINS	MIN	MAX	UNITS
PVIN supply voltage range	PVIN	4.5	16	V
Supply voltage V_{CC} & PV_{CC}	VCC, PVCC	4.75	5.25	V
Continuous load current	V_{OUT}		40	A
Junction Temperature *(Note 1)*		-40	125	°C

(Note 1): OTP default is set to 120°C for safety margin

Thermal Characteristics

Table 5

PARAMETER	PINS	TYPICAL	UNITS
Thermal shutdown	T_{SD}	120	°C
Thermal shutdown Hysteresis	T_{SDH}	18	°C
Thermal resistance: junction to ambient (0 LFM) *(Note1)*	θ_{JA}	8	°C/W
Thermal resistance: junction to case bottom (0 LFM)	θ_{JC}	1.5	°C/W

Note1: Based on 2 oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51 standards for high thermal conductivity boards. No top side cooling required.

Electrical Characteristics

PV_{IN} = 12V and V_{CC} = 5.0V. The minimum and maximum values are over the ambient temperature range (-40°C to 85°C) unless otherwise noted. Typical values are at T_A = 25°C.

Table 6

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CHARACTERISTICS						
PVIN supply voltage range	PVIN		4.5		16	V
PVIN supply quiescent current		Device switching; no load; V_{OUT} = 1.0V		40		mA
		Device not switching		1		
VCC supply voltage range	VCC		4.75	5.0	5.25	V
VCC UVLO rising				4.4		V
VCC UVLO falling				4.2		V
PVCC & VCC supply current		Normal operation; no load;		80 (Note 1)		mA
		Idle; no switching		30		mA
		Disabled (V_{CC} ≤ 2.8V)		900		µA
INTERNALLY GENERATED SUPPLY VOLTAGE						
VDD33 voltage range	VDD33		3.0	3.3	3.6	
VDD33 output current					2	mA
Open Drain PIN (POK)						
Input low voltage			0		0.8	V
Input leakage current					±1	µA
Output current - sink					2.0	mA
I/O PIN (ENABLE)						
Input high voltage			2.0		3.6	V
Input low voltage			-0.3		0.8	V
ENABLE response delay		Off - Low		150		µs
ENABLE response delay		On - High		250		µs
I/O PINS (VINSEN, VCCSEN)						
Input voltage			0		1.4	V
I/O PIN PWM						
PWM output voltage		High	2.4			V
PWM output voltage		Low			0.4	V

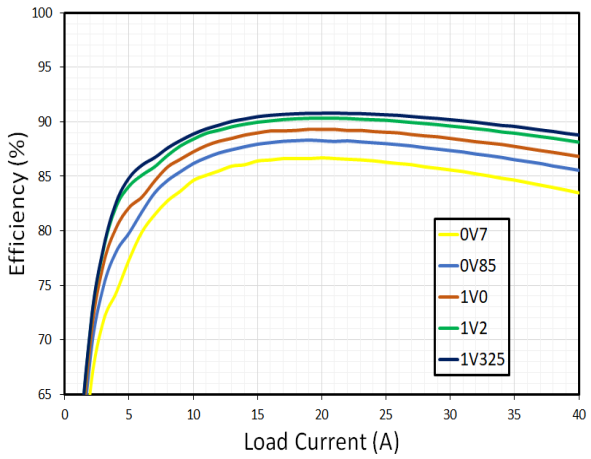
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM tristate leakage					±1	µA
PWM pulse width			30			ns
Resolution				163		ps
Switching frequency	f_{SW}			800		kHz
I/O PIN VTRACK						
VTRACK ramp rate					2.0	V/ms
VTRACK range			0		1.4	V
VTRACK offset voltage				±100		mV
OUTPUT VOLTAGE						
Output voltage adjustment range			0.5		1.325	V
Output voltage set-point accuracy		0˚C < T_A < 85˚C	-0.5		+0.5	%
		-40˚C < T_A < 85˚C	-1		+1	%
Output set-point resolution				1.5		mV
Line regulation				0.007		mV/V
Load regulation				0.07		mV/A
Output voltage startup delay		From V_{CC} valid, to start of output voltage ramp		5		ms
Rise Time		VTRACK not used (tied high)		0.18		V/ms
Fall Time		VTRACK not used (tied high)		0.18		V/ms
FAULT MANAGEMENT PROTECTION FEATURES						
PV_{IN} UV threshold				4		V
PVIN OV threshold				16.4		V
V_{OUT} OV threshold		Percentage of output voltage		120		%
V_{OUT} UV threshold		Percentage of output voltage		85		%
I_{OUT} OCP		DC Current Value	60		70	A
OTP threshold				120		°C
OTP hysteresis				102		°C
POK threshold		On level		95		%
POK threshold		Off level		90		%

Note 1: For 5V regulator design, allocate 150mA

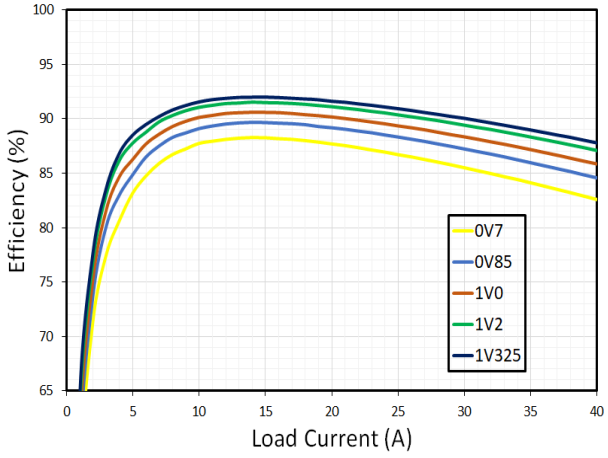
Typical Performance Characteristics

All the performance curves are measured with EM2040 evaluation board at 25°C ambient temperature unless otherwise noted. The output capacitors configuration for the evaluation board is 2 x 470 µF (3 mΩ ESR) + 4 x 100 µF (Ceramic) + 4 x 47 µF (Ceramic).

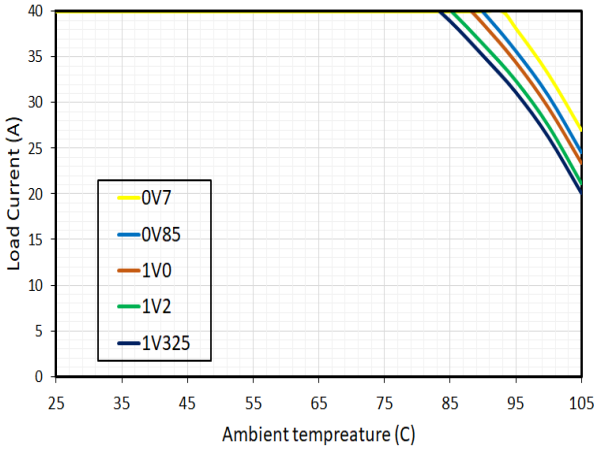
Efficiency, V_{IN} = 12V



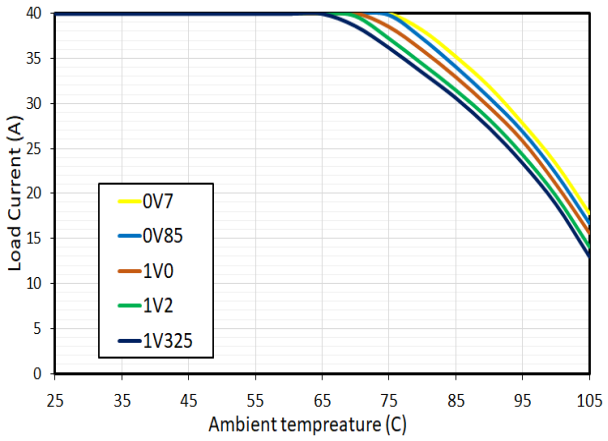
Efficiency, V_{IN} = 5V



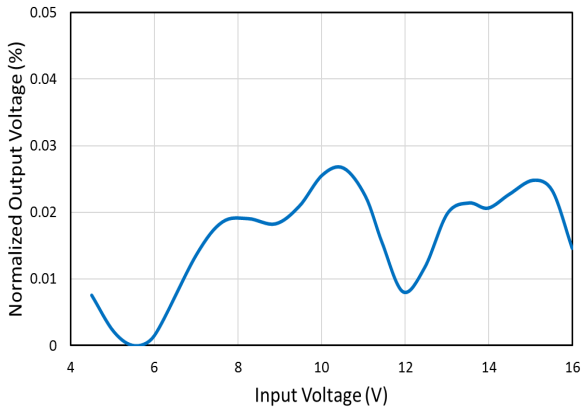
Thermal Derating, With Airflow 400 LFM



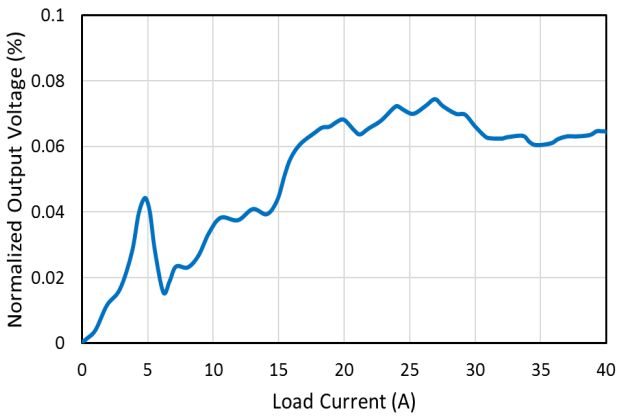
Thermal Derating, No Airflow



EM2040 Line Regulation, V_{OUT} = 0.9V

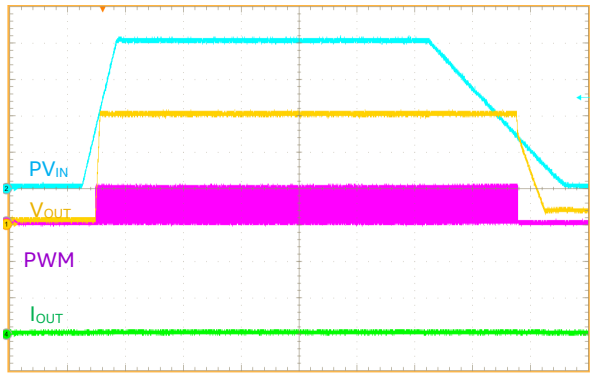


EM2040 Load Regulation, V_{OUT} = 0.9V



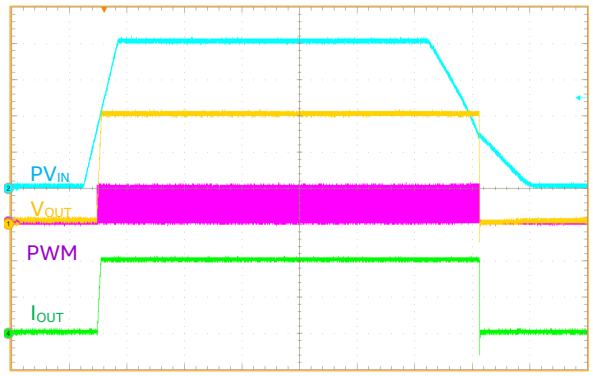
Typical Performance Characteristics (Continued)

Start-up/Shutdown, PVIN At No Load, 20 ms/div



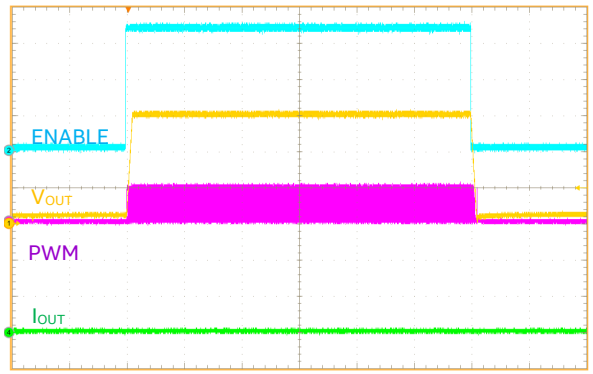
PV_{IN} and PWM: 3 V/div,
V_{OUT}: 300 mV/div, I_{OUT}: 20 A/div

Start-up/Shutdown, PVIN At 20A Load, 20 ms/div



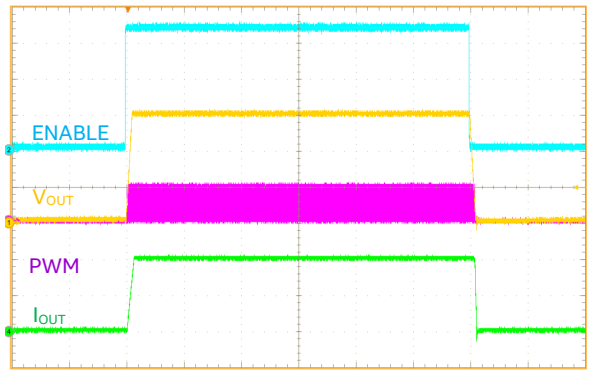
PV_{IN} and PWM: 3 V/div,
V_{OUT}: 300 mV/div, I_{OUT}: 20 A/div

Start-up/Shutdown, ENABLE At No Load, 10 ms/div



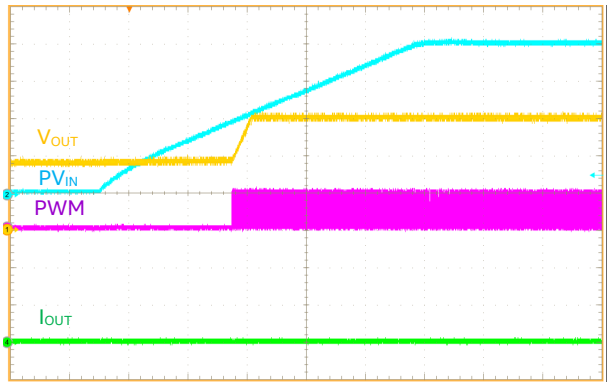
ENABLE: 1 V/div, PWM: 3 V/div,
V_{OUT}: 300 mV/div, I_{OUT}: 20 A/div

Start-up/Shutdown, ENABLE At 20A Load, 10 ms/div



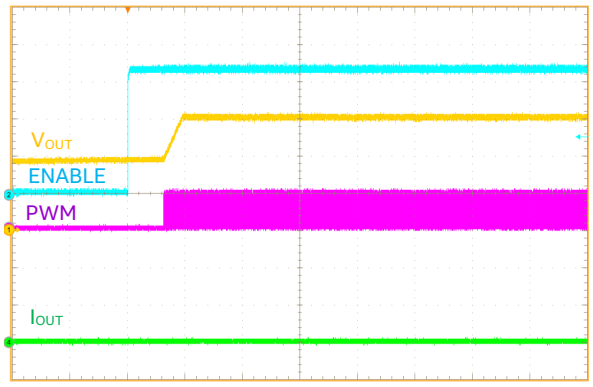
ENABLE: 1 V/div, PWM: 3 V/div,
V_{OUT}: 300 mV/div, I_{OUT}: 20 A/div

Start-up Into 0.6V Pre-Bias With PVIN, 2 ms/div



PV_{IN}: 3 V/div, PWM: 3 V/div,
V_{OUT}: 300 mV/div, I_{OUT}: 20 A/div

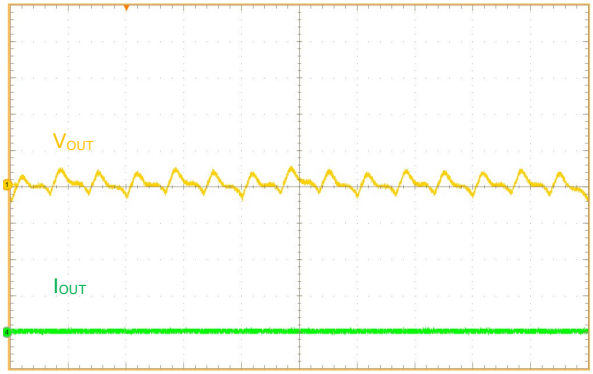
Start-up Into 0.6V Pre-Bias With ENABLE, 2 ms/div



ENABLE: 1 V/div, PWM: 3 V/div,
V_{OUT}: 300 mV/div, I_{OUT}: 20 A/div

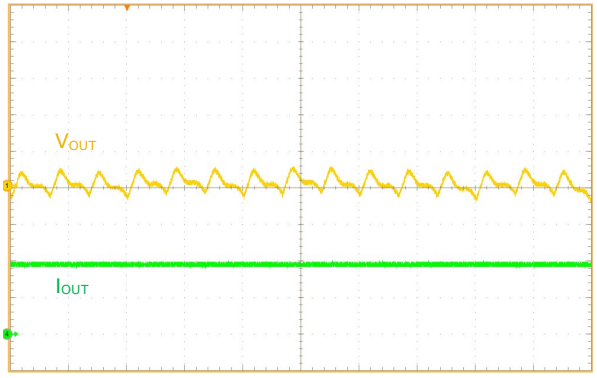
Typical Performance Characteristics (Continued)

Output Voltage Ripple, No Load



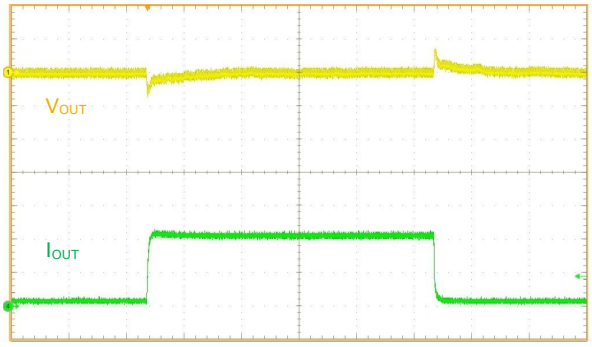
V_{IN} = 12V, V_{OUT} = 0.9V
2 µs/div, V_{OUT}: 10 mV/div, 20 MHz bandwidth

Output Voltage Ripple, 40A Load



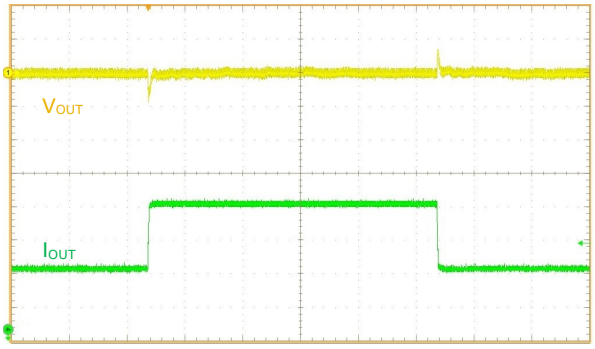
V_{IN} = 12V, V_{OUT} = 0.9V
2 µs/div, V_{OUT}: 10 mV/div, 20 MHz bandwidth

Output Voltage Transient Response, Load Step From 0A To 20A



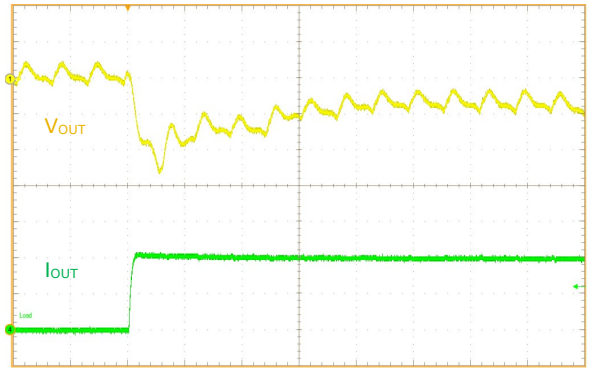
V_{IN} = 12V, V_{OUT} = 0.9V, 100µs/div
V_{OUT}: 30mV/div, I_{OUT}: 10A/div, 10A/µs

Output Voltage Transient Response, Load Step From 20A To 40A



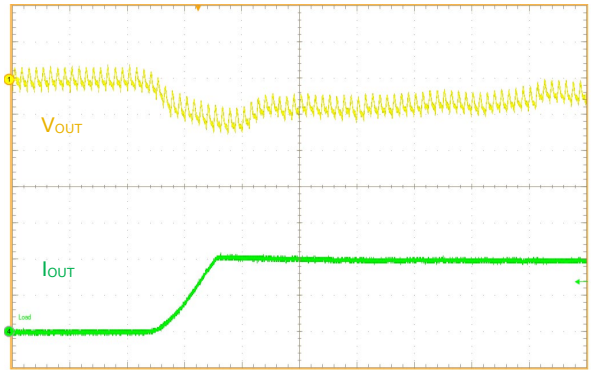
V_{IN} = 12V, V_{OUT} = 0.9V, 100µs/div
V_{OUT}: 30mV/div, I_{OUT}: 10A/div, 10A/µs

Output Voltage Transient Response, Load Step From 0A To 20A



V_{IN} = 12V, V_{OUT} = 0.9V, 2µs/div
V_{OUT}: 10mV/div, I_{OUT}: 10A/div, 10A/µs

Output Voltage Transient Response, Load Step From 0A To 20A



V_{IN} = 12V, V_{OUT} = 0.9V, 10µs/div
V_{OUT}: 10 mV/div, I_{OUT}: 10A/div, 1A/µs

Functional Block Diagram

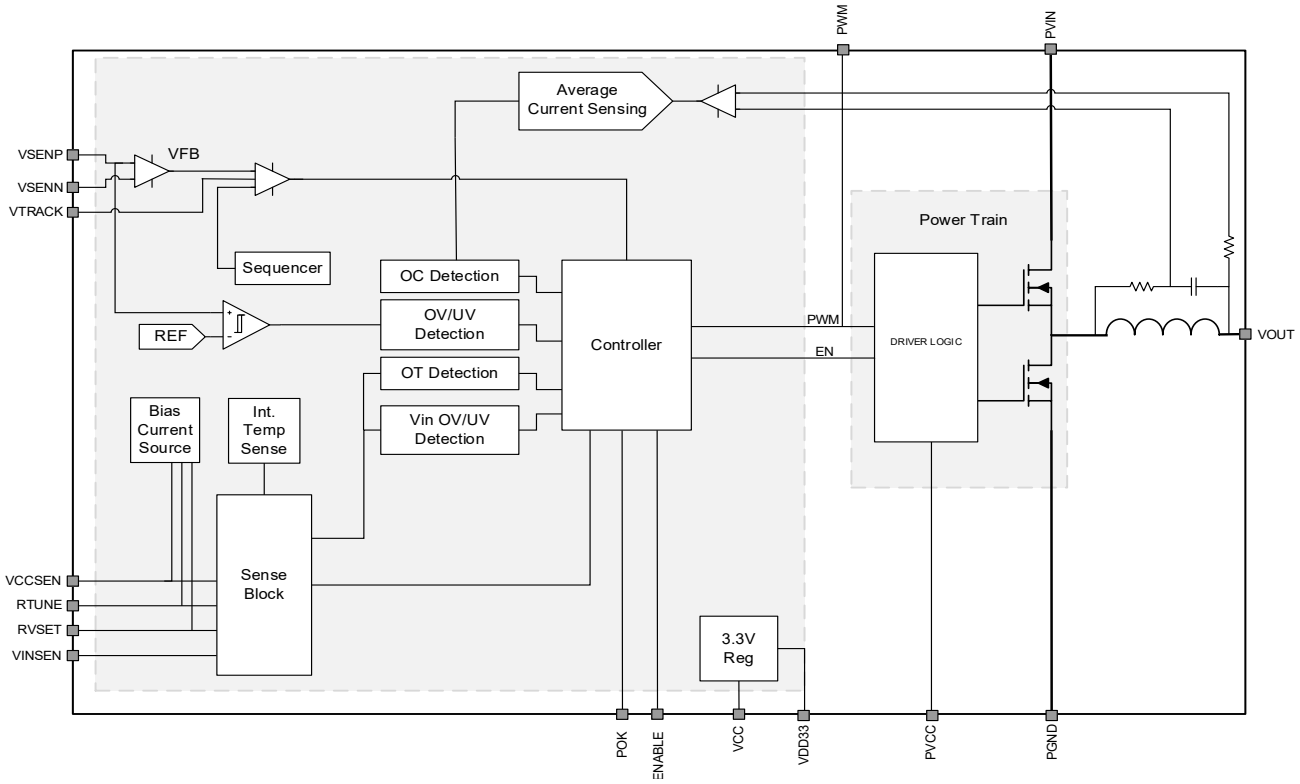


Figure 2: Functional Block Diagram

Functional Description

FUNCTIONAL DESCRIPTION

The EM2040 is a single output PowerSoC synchronous step-down converter capable of supplying up to 40A of continuous output current. The PowerSoC includes integrated power MOSFETs, a high-performance inductor and a digital controller.

The EM2040 requires only two resistors to set the output voltage and set the compensation. This easy-to-use set-up allows the user to tune the EM2040 to meet the most demanding accuracy and load transient requirements. The device switches at 800KHz, and is optimized for both efficiency and transient performance and uses a voltage-mode controller.

The EM2040 controller features two PID compensators for steady-state operation and fast transient operation. Fast, reliable switching between the different compensation modes ensures good transient performance and quiet steady state performance. The EM2040 has been designed with a selection of compensators which lets the user select the most suitbale one thereby giving the best transient response and stability for the output capacitance of the system. The compensator is chosen using the RTUNE resistor.

The EM2040 offers a complete suite of fault warnings and protections. Input and output Under Voltage Lock-Out (UVLO) and Over Voltage Lock-Out (OVLO) conditions are continuously monitored along with fast Over-

Current Protection (OCP). Over Temperature Protection (OTP) is accomplished by direct monitoring of the device's internal temperature.

POWER ON RESET

The EM2040 employs an internal power-on-reset (POR) circuit to ensure proper start-up and shut down with a changing supply voltage. Once the VCC supply voltage increases above the POR threshold voltage, the EM2040 begins the internal start-up process. Upon its completion, the device is ready for operation.

Two separate input voltage supplies are necessary to operate, PVIN (4.5V to 16V) and V_{CC} (4.75V to 5.25V). Both of these voltage rails are monitored for proper power-up and to protect the power MOSFETs under various input power fault conditions. A voltage divider on each input voltage supply connected to VINSEN for the power rail (PVIN) and VCCSEN for the supply rail (VC) is used for monitoring of both rails.

As illustrated in Figure 3, the values of resistors R1, R2, R3 and R4 are chosen so the internal monitoring circuitry is within the appropriate ranges. It is mandatory that the listed resistors values are used to ensure proper operation with the EM2040. The resistors used must be R1=11 kΩ, R2=1 kΩ, R3=10 kΩ and R4=3.3 kΩ, using 1% tolerance or better resistors.

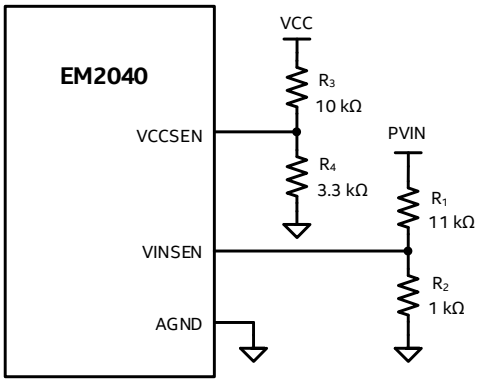


Figure 3: VINSEN And VCCSEN Input Resistor Dividers

The EM2040 also uses the PVIN monitor for input voltage feed-forward, which eliminates variations in the output voltage due to sudden changes in the input voltage supply. It does this by immediately changing the duty cycle to compensate for the input supply variation by normalizing the DC gain of the loop.

SETTING THE OUTPUT VOLTAGE

Differential remote sensing provides for precise regulation at the point of load. One of thirty output voltages may be selected, based on a resistor connected to the RVSET pin. At power-up, an internal current source biases the resistor and the voltage is measured to make the Vout selection. Use the RVSET tables (

Table 8) for the details of V_{OUT} selection and RVSET values

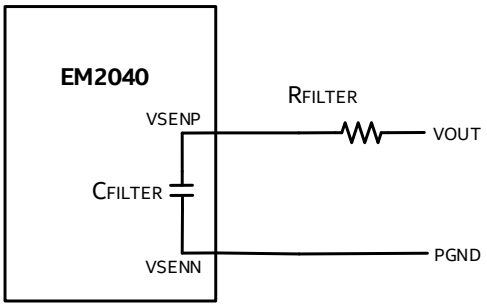


Figure 4: Output Voltage Sense Circuitry

The EM2040 supports direct output voltage feedback connection over the entire V_{OUT} range. The resistor RDIV2 may be used to adjust VOUT slightly or to get a VOUT value not supported by RVSET. Resistors with tight tolerances are recommended to maintain output voltage accuracy.

The resistor R_{FILTER} in the feedback path forms a low-pass filter with the internal capacitor, C_{FILTER}, to help remove any high-frequency disturbances from the sense signals. Place the resistor R_{FILTER} as close as possible to the EM2040 for best filtering performance.

Table 7: Output Voltage Feedback Component

Module	V_{OUT}	R_{FILTER}
EM2040	$0.7V \le V_{OUT} \le 1.325V$	2 kΩ

Table 8: Supported Configuration Voltage Values For EM2040 Output Voltage

RVSET Resistor	V_{OUT}
0kΩ	0.5V
0.392kΩ	0.55V
0.576kΩ	Reserved
0.787kΩ	Reserved
1.000kΩ	1.325V
1.240kΩ	1.3V
1.500kΩ	1.275V
1.780kΩ	1.25V
2.100kΩ	1.225V
2.430kΩ	1.2V
2.800kΩ	1.175V
3.240kΩ	1.15V
3.740kΩ	1.12V
4.220kΩ	1.1V
4.750kΩ	1.075V

RVSET Resistor	V_{OUT}
5.360kΩ	1.05V
6.040kΩ	1.03V
6.810kΩ	1.0V
7.680kΩ	0.975V
8.660kΩ	0.95V
9.530kΩ	0.925V
10.500kΩ	0.9V
11.800kΩ	0.875V
13.000kΩ	0.85V
14.300kΩ	0.825V
15.800kΩ	0.8V
17.400kΩ	0.775V
19.100kΩ	0.75V
21.000kΩ	0.725V
23.200kΩ	0.7V

ENABLE And OUTPUT START-UP BEHAVIOR

The ENABLE pin provides a means to enable normal operation or to shut down the device. When the ENABLE pin is asserted (high) the device will undergo a normal soft-start. A logic low on this pin will power the device down in a controlled manner. Dedicated pre-biased start-up logic ensures proper start-up of the power converter when the output capacitors are pre-charged to a non-zero output voltage. Closed-loop stability is ensured during this period.

The typical power sequencing, including ramp up/down and delays is shown in Figure 5.

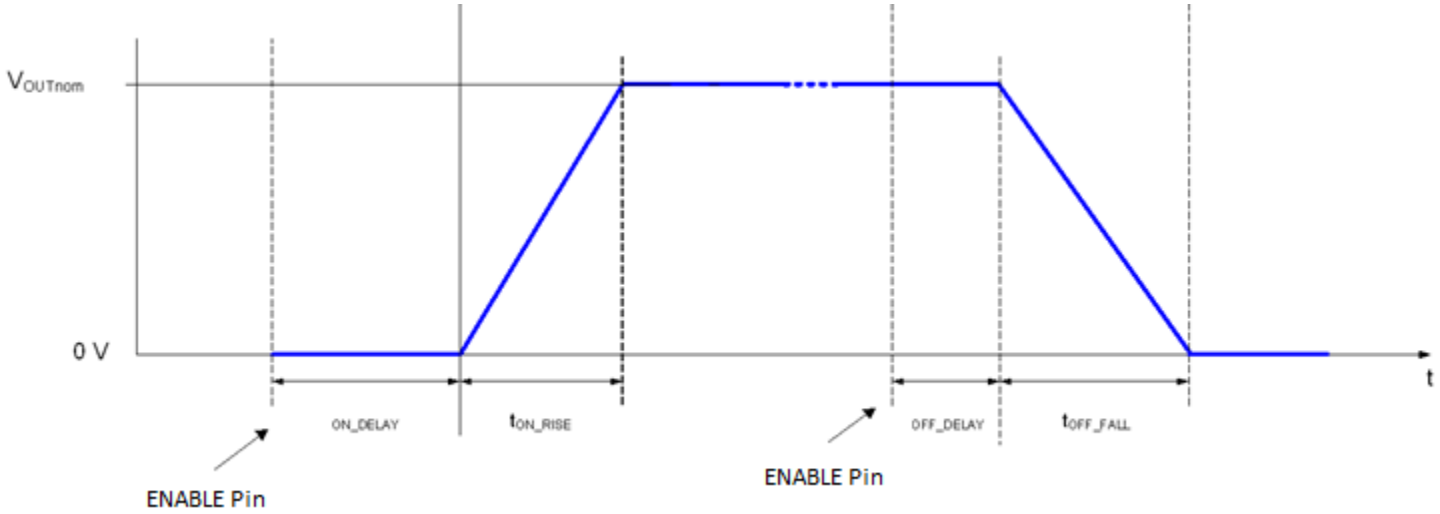


Figure 5: Power Sequencing

POWER OK

The EM2040 has a Power OK (POK) indicator at its output pin, which is Open Drain and therefore requires a pull-up resistor. The Pull-Up resistor may be connected to the VDD33 pin but it is not recommended to use the 5VCC supply. When de-asserted, POK indicates that the output voltage is below a certain threshold value. The POK on threshold is set to 95% of the programmed output voltage. When asserted, POK indicates that the output is in regulation, and no major faults are present. POK de-asserts (90%) during any serious fault condition where power conversion stops and re-asserts when the output voltage recovers.

In a noisy application, it is strongly recommended that a 100nf decoupling capacitor be placed between the POK pin and GND to act as a filter to unwanted external noise .

COMPENSATING THE CONTROL LOOP

To improve the transient performance for a typical point-of-load design, it is common to add output capacitance to the converter. This moves the output LC resonant frequency lower as capacitance increases which results in lower bandwidth, lower phase margin, and longer settling times unless the control loop is compensated for added capacitance.

However, with EM2040 the user does not need to be concerned with, or even understand, the details of control loop compensation techniques. RTUNE allows users to select from a number of PID control loop settings (known as compensators) through the use of pin-strapping. A single resistor from the RTUNE pin to AGND informs the EM2040 of the compensator selection.

The selection of the compensator is driven first by the type of output capacitors used, as the ESL and ESR of different capacitor types demands different PID coefficients to optimize transient deviation and recovery characteristics. An all ceramic output capacitor design requires a different compensator than a design with a combination of ceramic and polymer capacitors, i.e. POSCAP. **Table 10** shows several output capacitor part number recommendations.

The EM2040 supports three different compensators can then be subdivided into groups of six each whereby the initial capacitance value in the appropriate compensator can be scaled upwards by multiplication factor M to match the additional capacitance.

Table 9 :RTUNE configuration table for EM2040

Compensator Description	C_{OUT}	RTUNE Resistor	Multiplication factor (M)	Typical Deviation With 20A Load Step
Polymer Aluminum (SP-CAP) and Ceramic MLCC Output Capacitors Base capacitance = 1 x 470µF (Polymer) + 2 x 100µF (Ceramic) + 2 x 47µF (Ceramic)	Base	0kΩ	1	± 5%
	2 x Base	0.392kΩ	2	± 3%
	3 x Base	0.576kΩ	3	
	4 x Base	0.787kΩ	4	± 1.5%
	5 x Base	1.000kΩ	5	
	6 x Base	1.240kΩ	6	
All MLCC Ceramic Output Capacitors Base capacitance = 8 x 100µF	Base	1.500kΩ	1	± 5%
	1.5 x Base	1.780kΩ	1.5	
	2 x Base	2.100kΩ	2	± 3%
	3 x Base	2.430kΩ	3	
	4 x Base	2.800kΩ	4	
	4.5 x Base	3.240kΩ	4.5	± 1.5%
POSCAP and Ceramic MLCC Output Capacitors Base capacitance = 4 x 330 µF (POSCAP) + 2 x 100 µF (Ceramic)	Base	3.740kΩ	1	± 5%
	1.5 x Base	4.220kΩ	1.5	
	2 x Base	4.750kΩ	2	± 3%
	2.5 x Base	5.360kΩ	2.5	
	3 x Base	6.040kΩ	3	± 1.5%
	3.5 x Base	6.810kΩ	3.5	

Table **10: Recommended Output Capacitors**

Description	Manufacturer	P/N
470µF, 2.5V, ESR 3mΩ SP-CAP	Panasonic	EEFGX0E471R
330µF, 6.3V, ESR 9 mΩ POSCAP	Panasonic	6TPF330M9L
330µF, 2.5V, ESR 9 mΩ POSCAP	Kemet	T520B337M2R5ATE009
100µF, 6.3V, X5R, 1206 Ceramic	Kemet	C1206C107M9PACTU
47µF, 6.3V, X5R 1206 Ceramic	Murata	GRM31CR60J476ME19L

OUTPUT CAPACITOR RECOMMENDATION

EM2040 is designed for fast transient response and low output ripple noise. The output capacitors should be low ESR polymer, tantalum or ceramic capacitor. **Table 9** shows different output capacitor combinations to optimize the load transient deviation performance. With the Rtune feature, the user can simply scale up the total output capacitance to meet further stringent transient requirement.

Please consult the documentation for your particular FPGA, ASIC, processor, or memory block for the transient and the bulk decoupling capacitor requirements.

INPUT CAPACITOR RECOMMENDATION

The EM2040 input should be decoupled with at least three 22µF 1206 case size and one 10µF 0805 case size MLCC ceramic capacitors or four 22µF MLCC 1206 case size ceramic capacitors. More bulk capacitor may be needed only if there are long inductive traces at the input source or there is not enough source capacitance.

These input decoupling ceramic capacitors can be mounted on the PCB back-side to reduce the solution size. These input filter capacitors should have the appropriate voltage rating for the input voltage on PVIN, and use a X5R, X7R, or equivalent dielectric rating. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage.

The PVCC pin provides power to the gate drive of the internal high/low side power MOSFETs. The VCC pin provides power to the internal controller. These two power inputs share the same supply voltage (5V nominal), and should be bypassed with a single 2.2µF MLCC capacitor. To avoid switching noise injection from PVCC to VCC, it is recommended a ferrite bead is inserted between PVCC and VCC pins as shown Figure 12.

PROTECTION FEATURES

The EM2040 has a complete suite of fault protections. Input and output Under Voltage Lock-Out (UVLO) and Over Voltage Lock-Out (OVLO) conditions are continuously monitored along with the output current to provide fast Over-Current Protection (OCP) response.

To prevent damage to the load, the EM2040 also utilizes an output over-voltage protection circuit. The voltage at VSENP is continuously compared with a RVSET OVP threshold using a high-speed analog comparator. If the voltage exceeds the OVP threshold, a fault response is generated and the PWM output is turned off.

Over Temperature Protection (OTP) is based on direct monitoring of the modules internal temperature. If the temperature exceeds the OTP threshold, the device will enter a soft-stop mode slowly ramping the output voltage down until the temperature falls below the recovery temperature.

The fault response is for the output to latch off for most fault conditions. The ENABLE pin may be cycled to clear the latch. Table 11 summarizes the settings that have been implemented in the device.

Table 11: Fault Overview

Signal	Fault Level	Response Type	VOUT
Output Over-Voltage	Fault	High-impedance	Latched Off
Output Under-Voltage	Fault	High-impedance	Latched Off
Input Over-Voltage	Fault	High-impedance	Latched Off
Input Under-Voltage	Fault	High-impedance	Retry if Fault removed
Over-Current	Fault	High-impedance	Latched Off
Over-Temperature	Fault	Soft Off	Retry if Fault removed

The EM2040 monitors various signals during operation in order to detect fault conditions. Measured and filtered signals are compared to a fault threshold which when triggered generates a response as given in table Table 11

The EM2040 fault response depends on the fault type detected.

The EM2040 responds to an over temperature event by ramping down V_{OUT} in a controlled manner at a slew rate of approx. 0.18v/ms (Soft Off). For all other faults the EM2040 will respond by immediately turning off both the top-side MOSFET and low-side MOSFET (High-Impedance)

In the event of a Temperature Fault or a Low PVIN Fault the module will restart Vout automatically without user intervention once the fault is deemed to have been removed. For all other faults the module will remain off until the user either toggles the ENABLE pin or recycled the supply whereupon if the fault is removed the VOUT will restart.

PRE-BIASED START-UP AND SOFT-STOP

In systems with complex power architectures, there may be leakage paths from one supply domain which charge capacitors in another supply domain leading to a pre-biased condition on one or more power supplies. This condition is not ideal and can be avoided through careful design, but is generally not harmful. Attempting

to discharge the pre-bias is not advised as it may force high current though the leakage path. The EM2040 include a feature to allow it to be enabled into pre-biased output capacitors without discharging them.

If the output capacitors are pre-biased when the EM2040 is enabled, start-up logic in the EM2040 ensures that the output does not pull down the pre-biased voltage. Closed-loop stability is ensured during the entire start-up sequence under all pre-bias conditions.

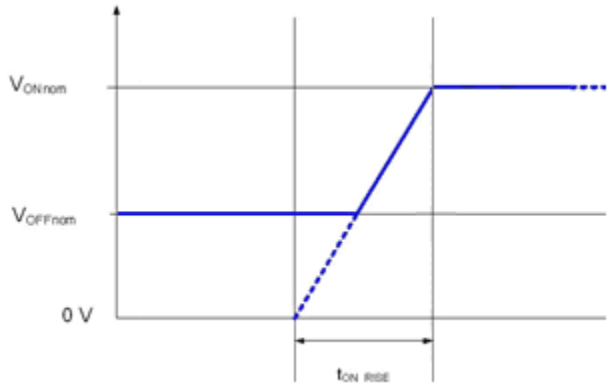


Figure 6: Power Sequencing With Non-Zero Off Voltage

VOLTAGE TRACKING

The EM2040 can control the output voltage based on the external voltage applied to the VTRACK pin, thus allowing sequencing of the output voltage from an external source. Pre-bias situations are also supported. The VTRACK pin voltage is a single-ended input referenced to analog ground.

If VTRACK is not intended to be used, the VTRACK pin must be tied high. (It cannot be tied low or left floating).

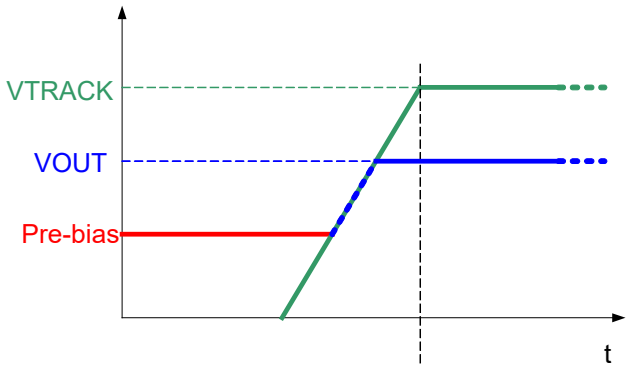


Figure 7: Power Sequencing Using VTRACK With Bias Voltage On VOUT

The set point voltage for the EM2040 is defined by the lower value of the V_{OUT} setting or an external voltage applied to the VTRACK pin. If the VTRACK voltage rises above the V_{OUT} set point voltage, then the final output voltage will be limited by the V_{OUT} setting. If the VTRACK pin is tied low or floating, then the output will never start as the VTRACK pin input is always the lower value and will always be in control. Conversely, if VTRACK is tied high, the output will start but will follow the V_{OUT} set point, not the VTRACK pin.

In the event of using VTRACK for sequencing, it is highly recommended that the VTRACK signal is kept greater than the V_{OUT} voltage. This ensures that the internal V_{OUT} set point is used as the final steady-state output voltage and accuracy is not a function of the externally applied VTARCK voltage.

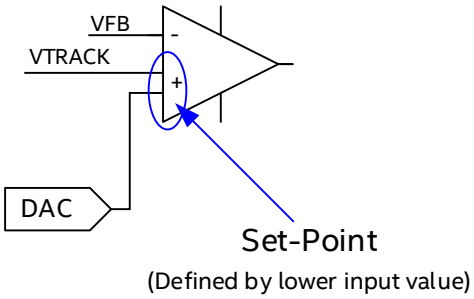


Figure 8: VTRACK Circuitry

The following figures demonstrate ratio-metric and simultaneous sequencing of the output voltage, which can be accomplished by applying an appropriate external voltage on the VTRACK pin.

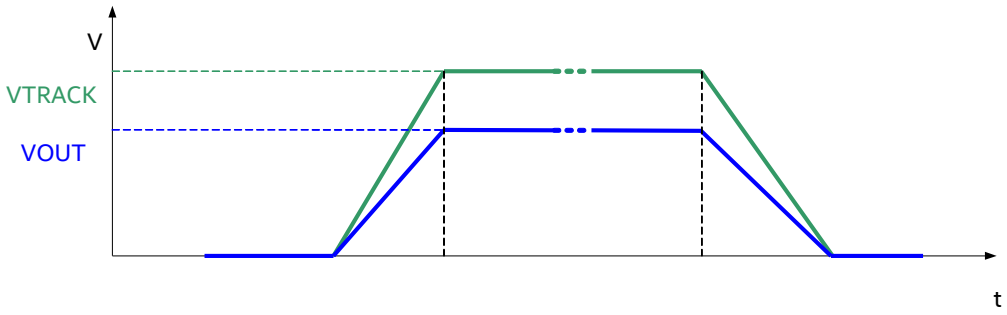


Figure 9: Ratiometric Sequencing Using VTRACK

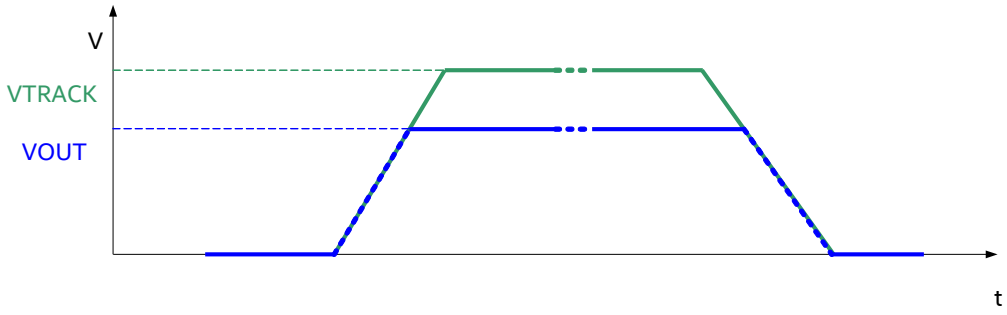


Figure 13: Simultaneous Sequencing Using VTRACK

When using the VTRACK feature, the sequencing will be ratio-metric as shown in Figure 9 if an external resistor network is used at the VTRACK pin as shown Figure 10. If no external resistors are used, the output sequence is simultaneous as shown in Figure 13.

In the event that a feedback divider is not required, but the tracking voltage applied to VTRACK is greater than 1.4V, then a 2kΩ resistor is required in series with the VTRACK pin to minimize leakage current as shown in Figure 11.

In applications where a voltage divider is required on the output voltage, a voltage divider consisting of the same values is also required for the VTRACK pin.

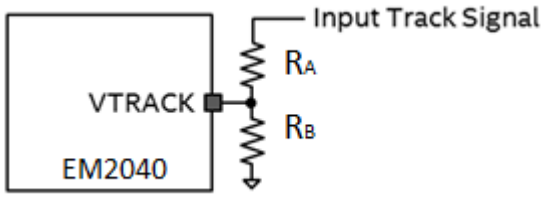


Figure 10: VTRACK Sense Circuitry with Resistor Divider

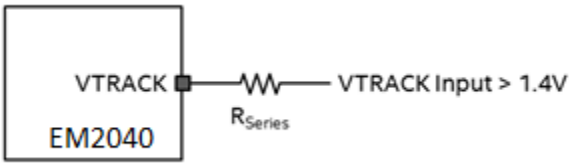


Figure 11: VTRACK Sense Circuitry (Input > 1.4V)

TEMPERATURE AND OUTPUT CURRENT MEASUREMENT

The EM2040 temperature sense block provides the device with precision temperature information over a wide range of temperatures (-40°C to +150°C). The temperature sense block measures the controller temperature, which will be slightly lower than the powertrain junction temperature.

The EM2040 monitors output current by real-time, temperature compensated DCR current sensing across the inductor. This real-time current waveform is then filtered and averaged for accurate fault warning and management.

Factory calibration has been performed for every EM2040 device to improve measurement accuracy over the full output current range. This allows the EM2040 to correct for DCR manufacturing variations.

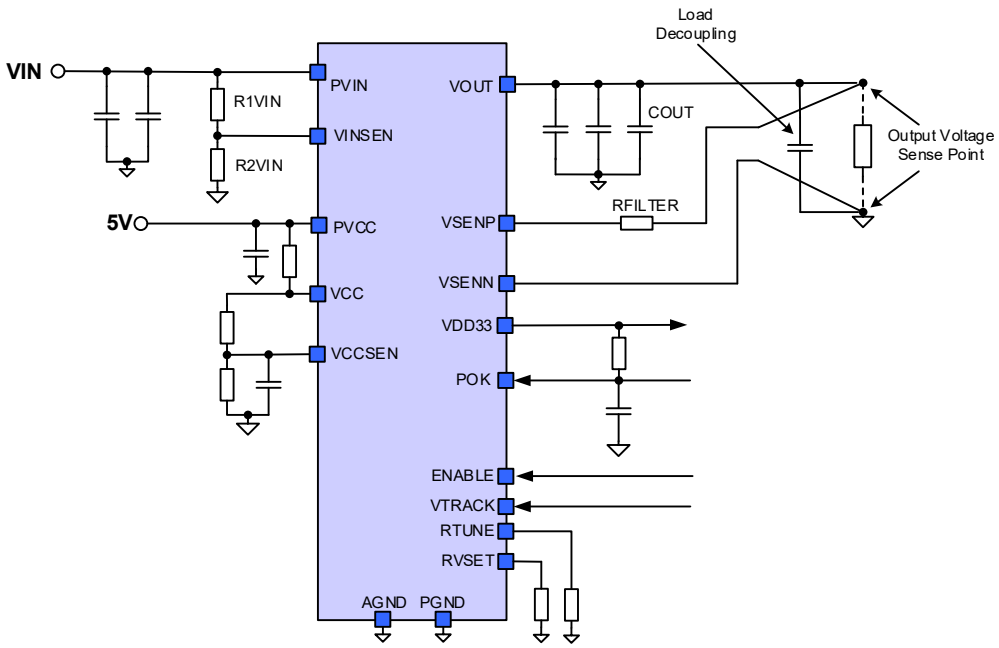


Figure 12: Recommended Application Circuit

Layout Recommendations

Recommendation 1: It is highly recommended to use separate nets for AGND and PGND and connecting them through a 0Ω resistor or a short. This method helps with ground management and prevents the noise from the Power Ground disturbing the more sensitive Analog (“Signal”) Ground.

Recommendation 2: It is good practice to minimize the PGND loop. Whenever possible the input and output loops should close to the same point, which is the ground of the EM2040 module. Module decoupling ceramic capacitors are to be placed as close as possible to the module in order to contain the switching noise in the smallest possible loops and to improve PVIN decoupling by minimizing the series parasitic inductance of the PVIN traces. For achieving this goal, it helps to place decoupling capacitors on the same side as the module since VIAs are generally more inductive, thus reducing the effectiveness of the decoupling. Of course, bulk and load high frequency decoupling should be placed closer to the load. If the input decoupling is placed on the back side, it is recommended to place small, low value capacitors on the topside right next to the EM2040, to help minimize the effect of via inductance.

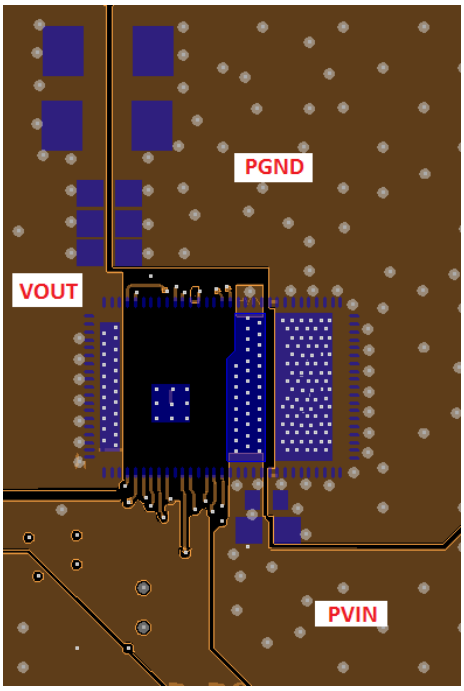


Figure 13: Top Layer Layout With Critical Components Only

Recommendation 3: It is good practice to place the other small components needed by the EM2040 on the opposite side of the board, in order to avoid cutting the power planes on the module side. Since the EM2040 heat is evacuated mostly through the PCB, this will also help with heat dissipation; wide copper planes under the module can also help with cooling. The PVIN copper plane should not be neglected as it helps spread the heat from the high side FET.

Recommendation 4: It is recommended that at least below the EM2040 module, the next layers to the surface (2 and n-1) be solid ground planes, which provides shielding and lower the ground impedance at the module level. AGND should be also routed as a copper plane, in order to reduce the ground impedance and reduce noise injection.

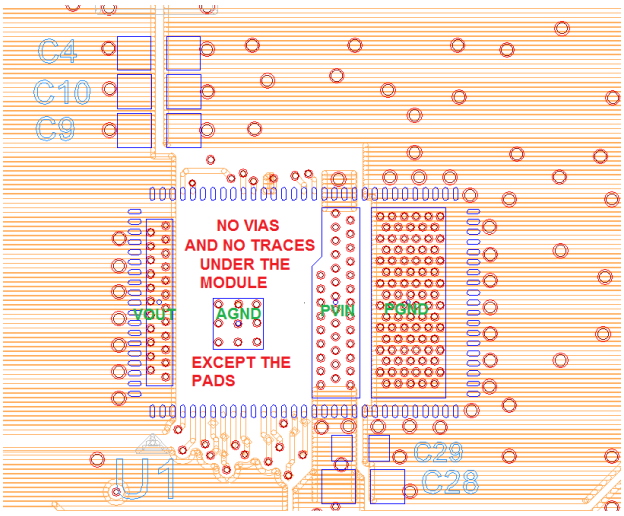


Figure 14: VIAs in The Power Pads

Recommendation 5: In order to better spread the current and the heat through the inner layers, arrays of VIAs should be placed in the power pads. 10mils diameter is a good size for the plated in-pad VIAs. It is critical that through VIAs should not be placed by any means elsewhere under the module; the non-pad area around AGND is VIA keep out area.

Recommendation 6: All other signal and LDO decoupling capacitors should be placed as close as possible to the terminal they are decoupling, while the AGND connection should be done through VIAs to the AGND plane.

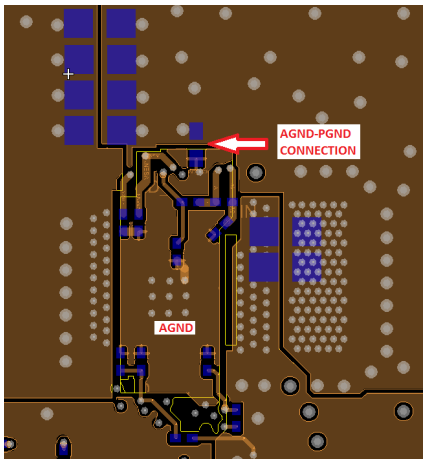


Figure 15: Backside Decoupling
All Signal Decoupling Go To The Bottom AGND Plane And Get Connected To The EM2040 Module AGND Through The AGND In-PAD VIAs (Again, No Other VIAs Are Allowed In That Area)

Recommendation 7: Figure 15 also shows the 0Ω resistor that connects AGND to PGND. The recommended connecting point, as shown, is to a quiet PGND → the output capacitors PGND.

Recommendation 8: Differential remote sense should be routed as much as possible as a differential pair, on an inner layer, preferably shielded by a ground plane.

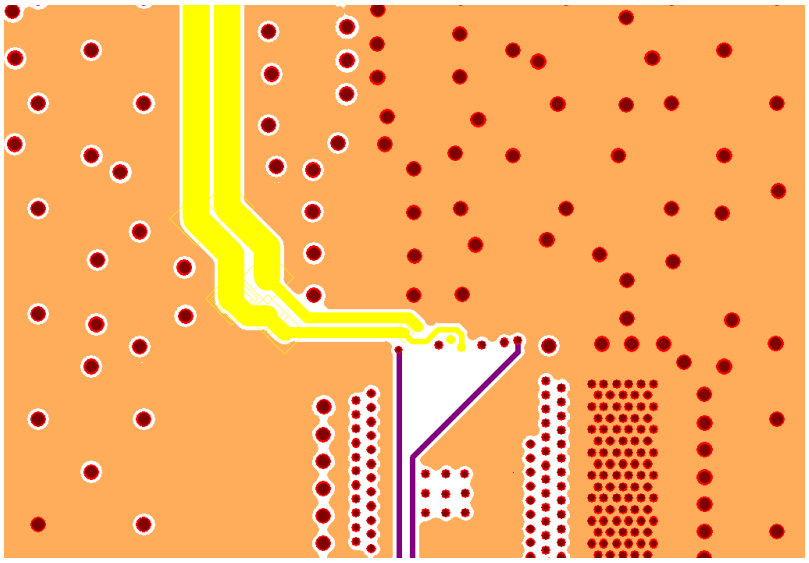


Figure 16: Remote Sense Routing On An Inner Layer (Highlighted, Yellow)

Recommendation 9: If the design allows it, stitching VIAs can be used on the power planes, close to the module in order to help with cooling. This is a thermal consideration and does not matter much for the electrical design.

Recommended PCB Footprint

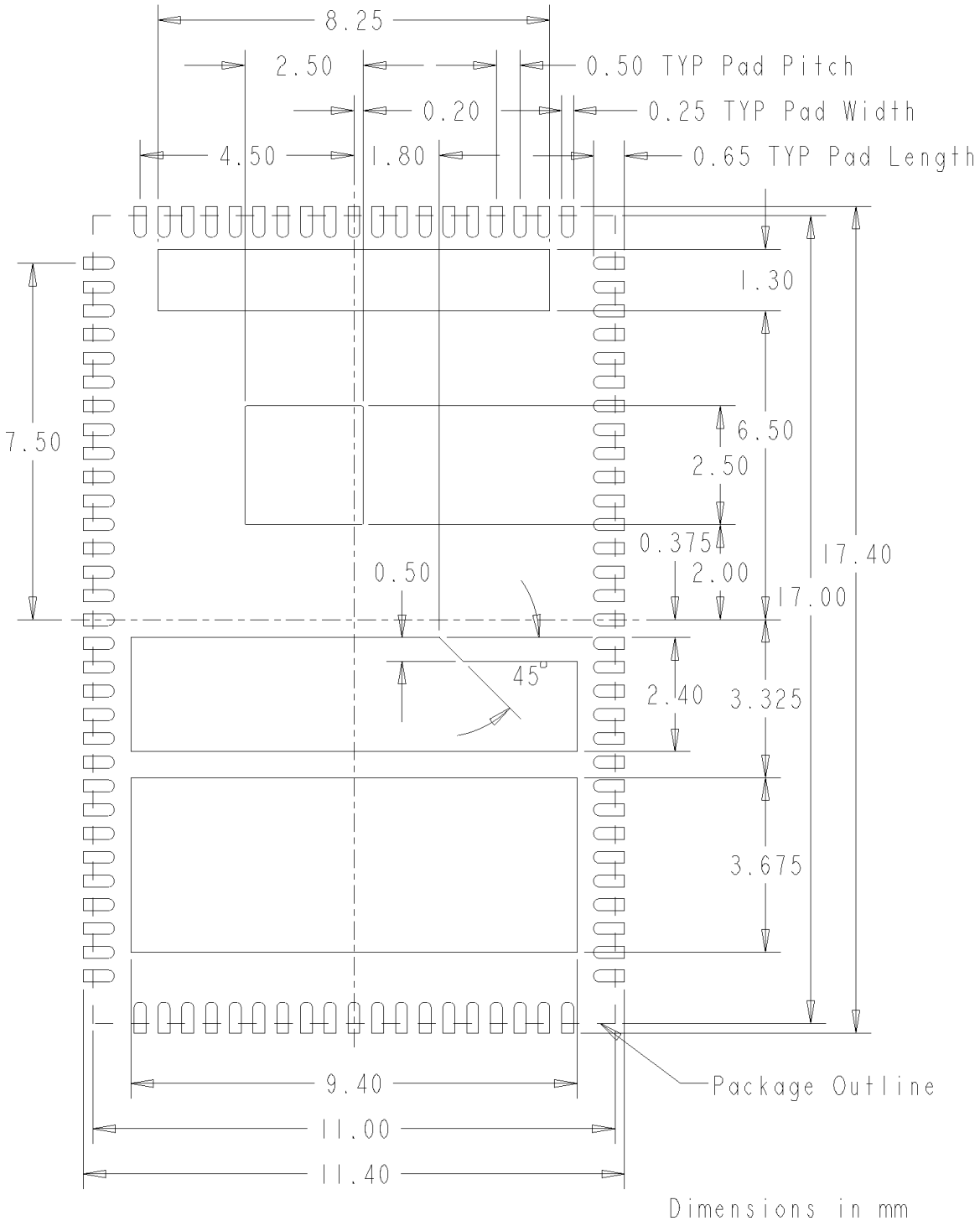


Figure 17: Recommended PCB Footprint

30% Solder Stencil Aperture (see note below)

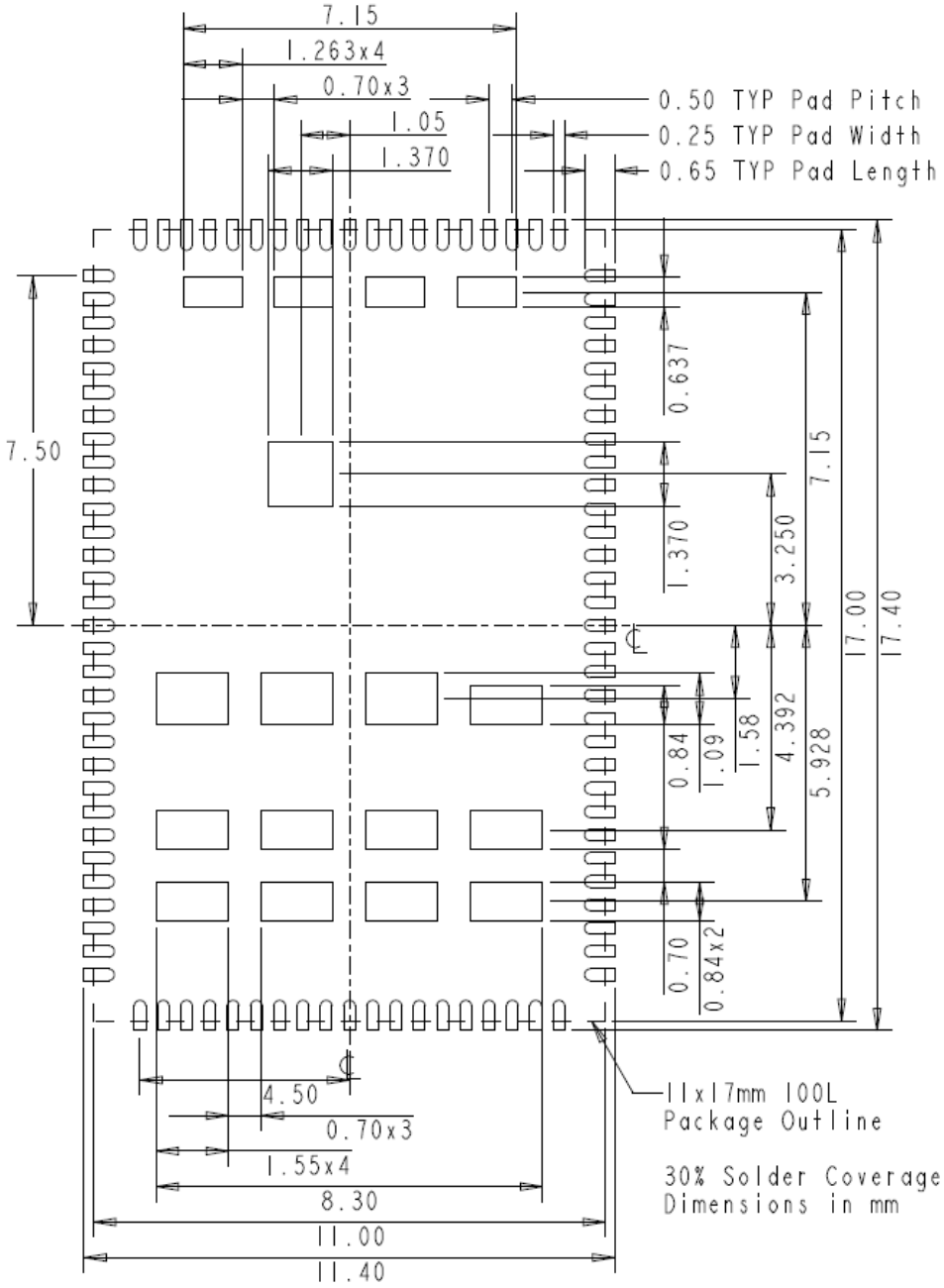


Figure 18: 30% Solder Stencil Aperture Dimensions

Notes:

- The solder stencil for each pad under the device is recommended to be up to 30% of the total pad size.
- The aperture dimensions are based on a 4mil stencil thickness

Package Dimensions

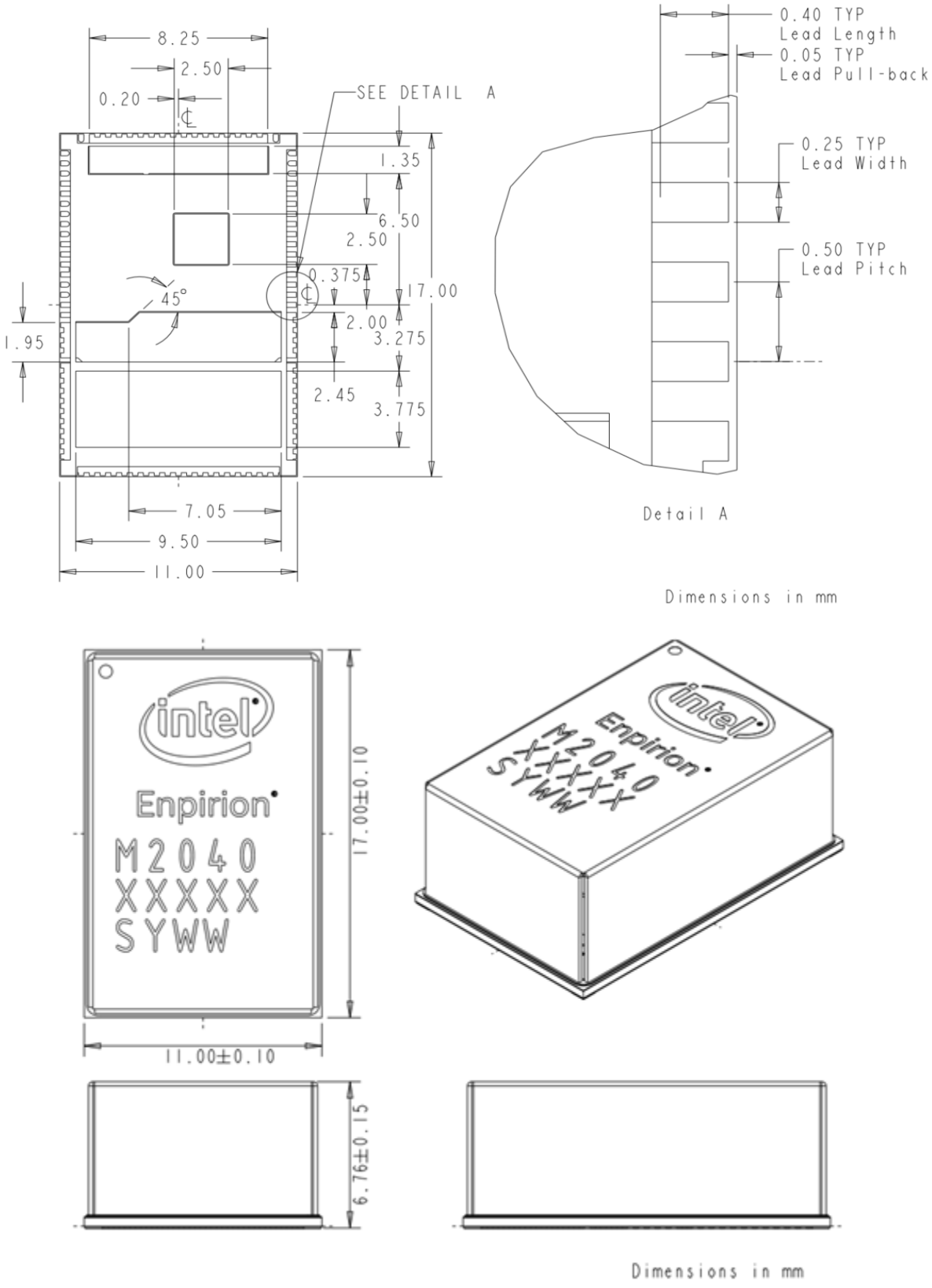


Figure 20: Package Dimensions

Tray Information

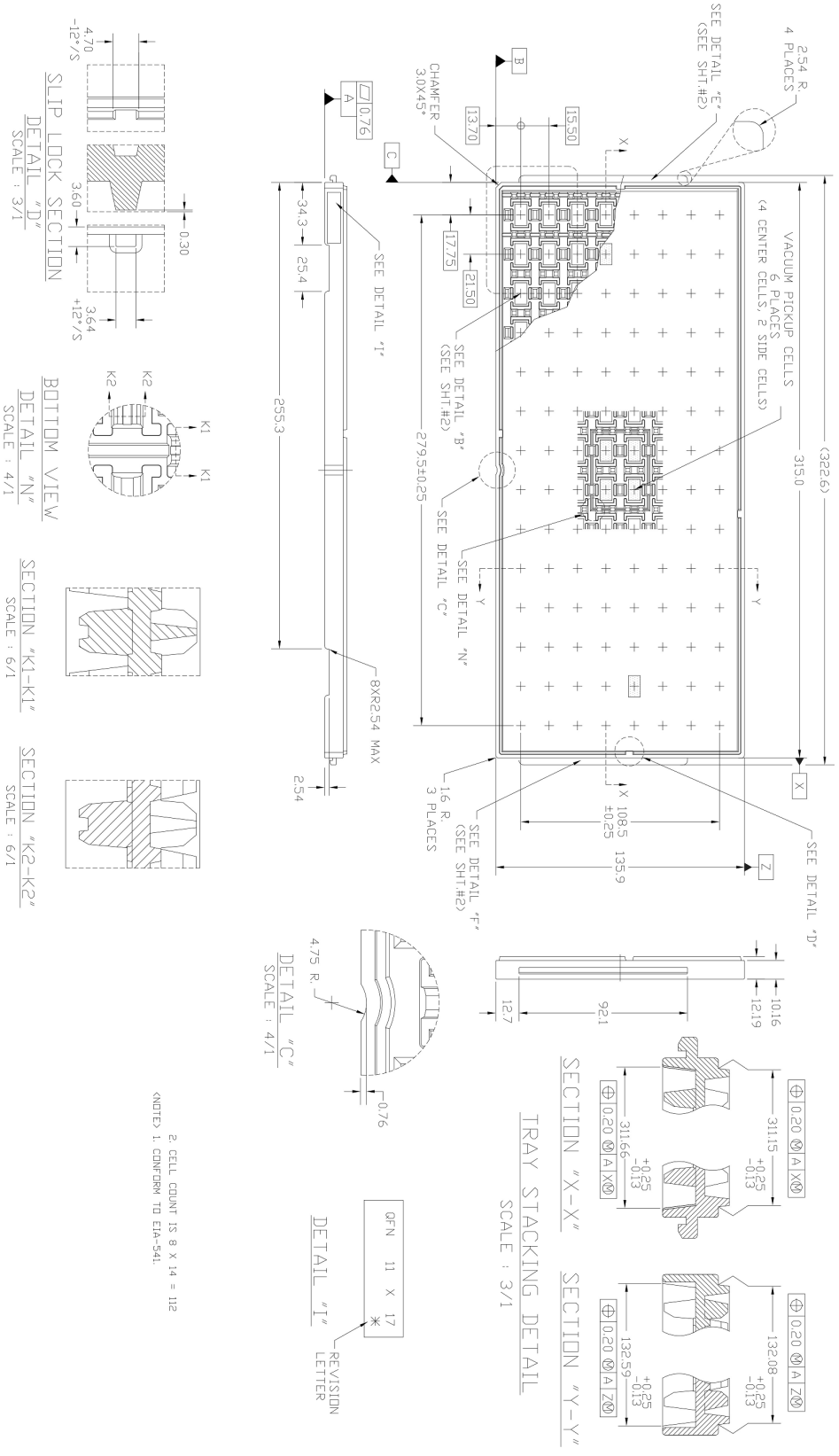


Figure 21: Tray Information 1/2

Tray Information (Continued)

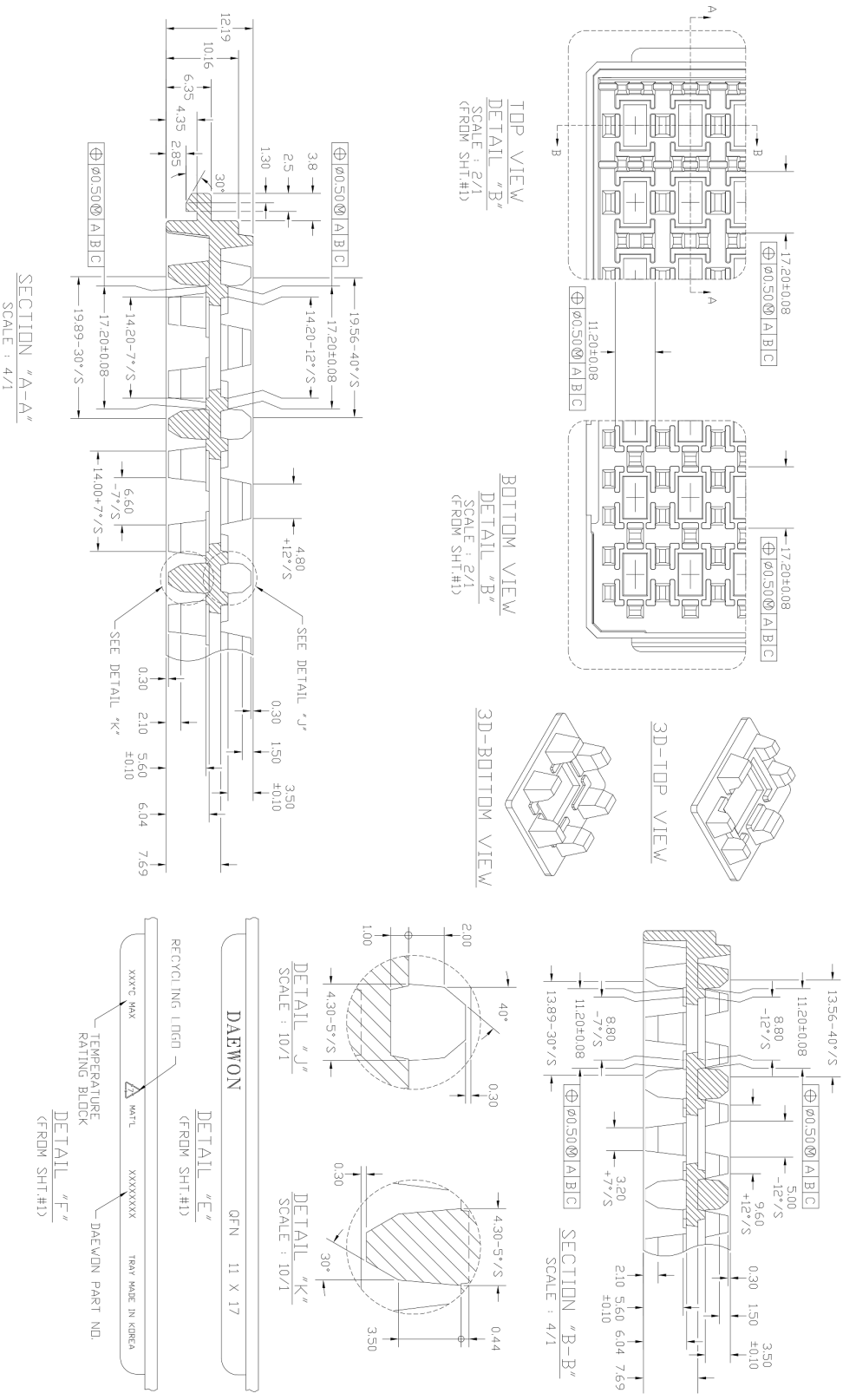


Figure 22: Tray Information 2/2

Revision History

Rev	Date	Change(s)
A	July-18	Initial Release
B	Mar-20	Removed stencil option for 45% opening

Where to Get More Information

For more information about Intel and Intel Enpirion PowerSoCs, visit **https://www.altera.com/enpirion**

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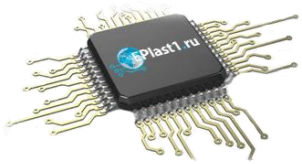
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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