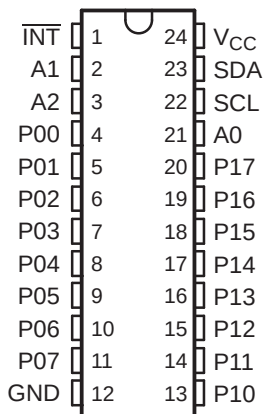


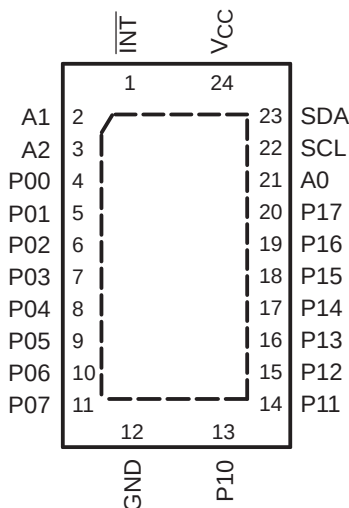
## FEATURES

- Low Standby-Current Consumption of 10  $\mu$ A Max
- I<sup>2</sup>C to Parallel-Port Expander
- Open-Drain Interrupt Output
- Compatible With Most Microcontrollers
- 400-kHz Fast I<sup>2</sup>C Bus
- Address by Three Hardware Address Pins for Use of up to Eight Devices
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

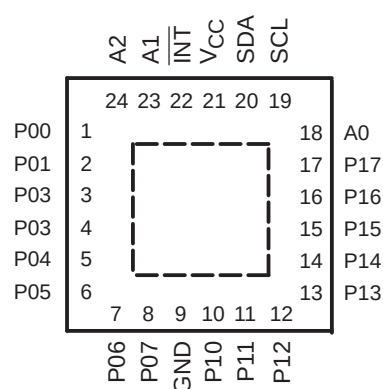
DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



RHL PACKAGE  
(TOP VIEW)



RGE PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

This 16-bit I/O expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 4.5-V to 5.5-V  $V_{CC}$  operation.

### ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|--------------|-----------------------|------------------|
| –40°C to 85°C | QSOP – DBQ             | Reel of 2500 | PCF8575CDBQR          | PCF8575C         |
|               | TVSOP – DGV            | Reel of 2000 | PCF8575CDGVR          | PF575C           |
|               | SOIC – DW              | Tube of 25   | PCF8575CDW            | PCF8575C         |
|               |                        | Reel of 2000 | PCF8575CDWR           |                  |
|               | SSOP – DB              | Tube of 60   | PCF8575CDB            | PF575C           |
|               |                        | Reel of 2000 | PCF8575CDBR           |                  |
|               | TSSOP – PW             | Tube of 60   | PCF8575CPW            | PF575C           |
|               |                        | Reel of 1200 | PCF8575CPWR           |                  |
|               |                        | Reel of 250  | PCF8575CPWT           |                  |
|               | QFN – RGE              | Reel of 3000 | PCF8575CRGER          | PF575C           |
|               | QFN – RHL              | Reel of 1000 | PCF8575CRHLR          | PREVIEW          |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# PCF8575C

## REMOTE 16-BIT I<sup>2</sup>C AND SMBus LOW-POWER I/O EXPANDER WITH INTERRUPT OUTPUT

SCPS123C – MARCH 2005 – REVISED JULY 2006

### DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The PCF8575C provides general-purpose remote I/O expansion for most microcontroller families via the I<sup>2</sup>C interface serial clock (SCL) and serial data (SDA).

The device features a 16-bit quasi-bidirectional input/output (I/O) port (P07–P00, P17–P10), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are in 3-state mode. The strong pullup to V<sub>CC</sub> allows fast-rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs. After power on, as all the I/Os are set to 3-state, all of them can be used as inputs. Any change in setting of the I/Os as either inputs or outputs can be done with the write mode. If a high is applied externally to an I/O that has been written earlier to low, a large current (I<sub>OL</sub>) flows to GND.

The PCF8575C provides an open-drain interrupt ( $\overline{\text{INT}}$ ) output, which can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time (t<sub>iv</sub>), the signal  $\overline{\text{INT}}$  is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting, or data is read from or written to the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal or in the write mode at the ACK bit after the falling edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short), due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as  $\overline{\text{INT}}$ . Reading from or writing to another device does not affect the interrupt circuit.

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports, without having to communicate via the I<sup>2</sup>C bus. Thus, the PCF8575C can remain a simple slave device.

Every data transmission to or from the PCF8575C must consist of an even number of bytes. The first data byte in every pair refers to port 0 (P07–P00), and the second data byte in every pair refers to port 1 (P17–P10). To write to the ports (output mode), the master first addresses the slave device, setting the last bit of the byte containing the slave address to logic 0. The PCF8575C acknowledges and the master sends the first data byte for P07–P00. After the first data byte is acknowledged by the PCF8575C, the second data byte (P17–P10) is sent by the master. Once again, the PCF8575C acknowledges the receipt of the data, after which this 16-bit data is presented on the port lines.

The number of data bytes that can be sent successively is not limited. After every two bytes, the previous data is overwritten. When the PCF8575C receives the pairs of data bytes, the first byte is referred to as P07–P00 and the second byte as P17–P10. The third byte is referred to as P07–P00, the fourth byte as P17–P10, and so on.

Before reading from the PCF8575C, all ports desired as input should be set to logic 1. To read from the ports (input mode), the master first addresses the slave device, setting the last bit of the byte containing the slave address to logic 1. The data bytes that follow on the SDA are the values on the ports. If the data on the input port changes faster than the master can read, this data may be lost.

When power is applied to V<sub>CC</sub>, an internal power-on reset holds the PCF8575C in a reset state until V<sub>CC</sub> has reached V<sub>POR</sub>. At that time, the reset condition is released, and the device I<sup>2</sup>C-bus state machine initializes the bus to its default state.

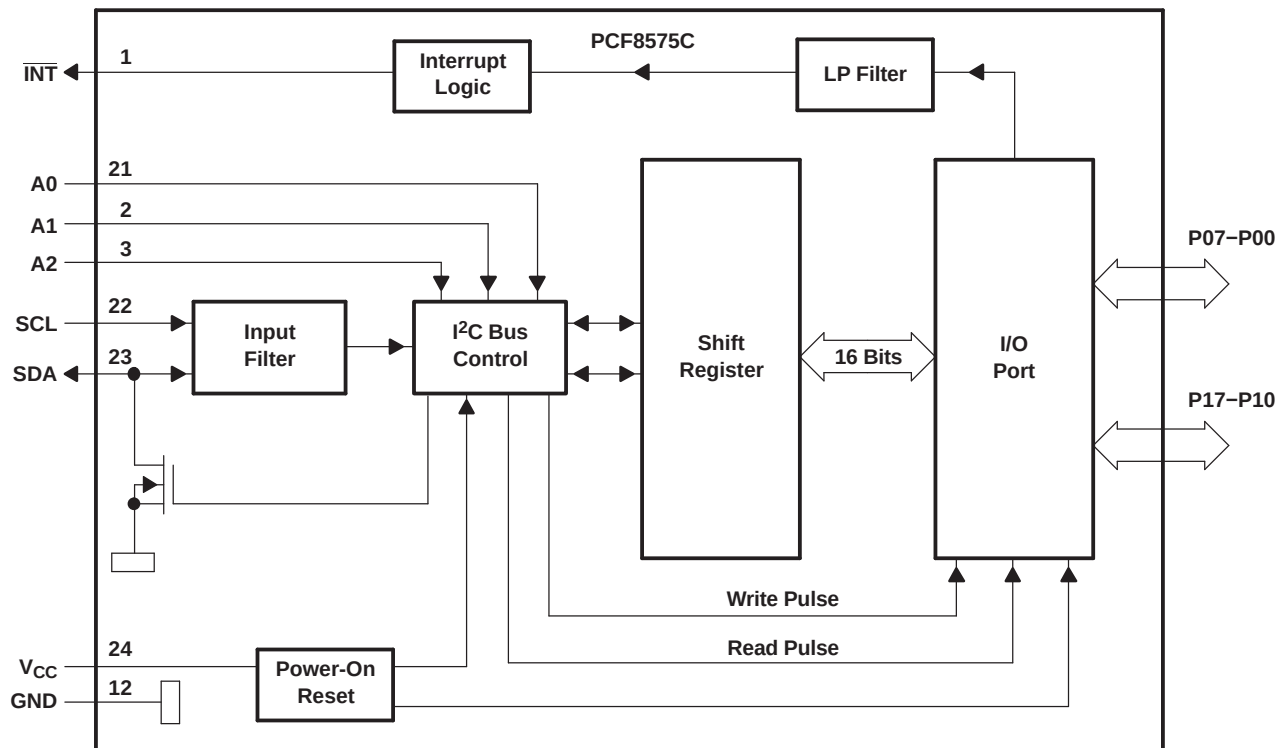
The hardware pins (A0, A1, and A2) are used to program and vary the fixed I<sup>2</sup>C address, and allow up to eight devices to share the same I<sup>2</sup>C bus or SMBus. The fixed I<sup>2</sup>C address of the PCF8575C is the same as the PCF8575, PCF8574, PCA9535, and PCA9555, allowing up to eight of these devices, in any combination, to share the same I<sup>2</sup>C bus or SMBus.

### TERMINAL FUNCTIONS

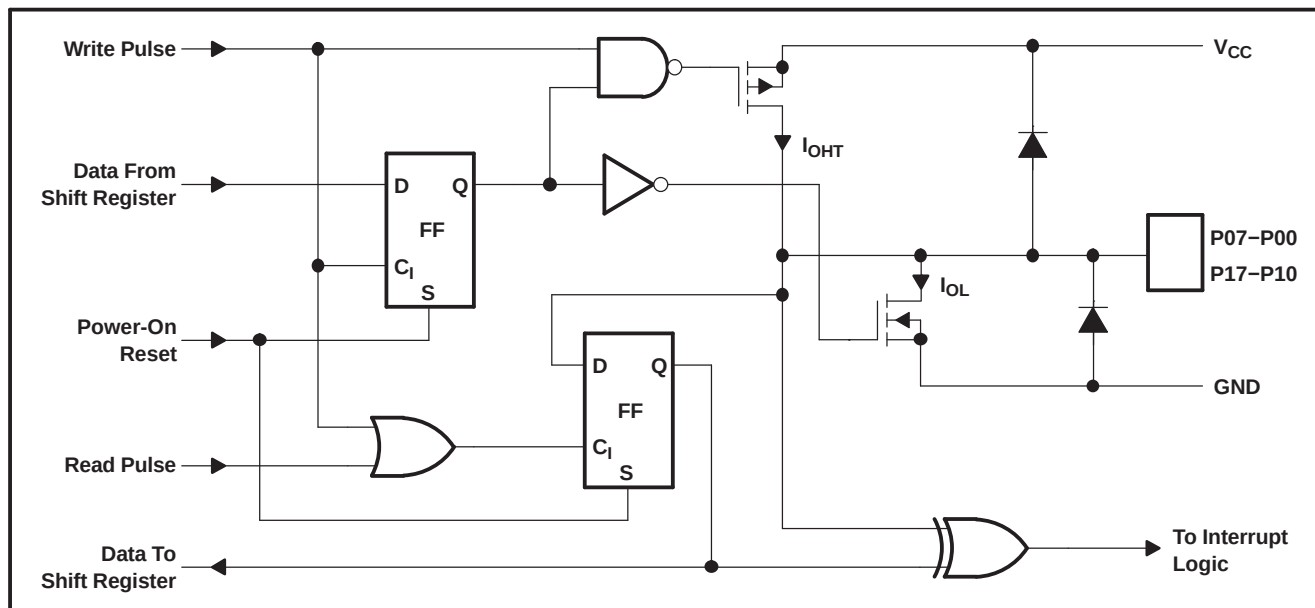
| NO.                                 |     | NAME            | FUNCTION                                                                                                |
|-------------------------------------|-----|-----------------|---------------------------------------------------------------------------------------------------------|
| DB, DBQ, DGV,<br>DW, PW, AND<br>RHL | RGE |                 |                                                                                                         |
| 1                                   | 22  | INT             | Interrupt output. Connect to V <sub>CC</sub> through a pullup resistor.                                 |
| 2                                   | 23  | A1              | Address input 1. Connect directly to V <sub>CC</sub> or ground. Pullup resistors are not needed.        |
| 3                                   | 24  | A2              | Address input 2. Connect directly to V <sub>CC</sub> or ground. Pullup resistors are not needed.        |
| 4                                   | 1   | P00             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 5                                   | 2   | P01             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 6                                   | 3   | P02             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 7                                   | 4   | P03             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 8                                   | 5   | P04             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 9                                   | 6   | P05             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 10                                  | 7   | P06             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 11                                  | 8   | P07             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 12                                  | 9   | GND             | Ground                                                                                                  |
| 13                                  | 10  | P10             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 14                                  | 11  | P11             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 15                                  | 12  | P12             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 16                                  | 13  | P13             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 17                                  | 14  | P14             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 18                                  | 15  | P15             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 19                                  | 16  | P16             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 20                                  | 17  | P17             | P-port input/output. Open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| 21                                  | 18  | A0              | Address input 0. Connect directly to V <sub>CC</sub> or ground. Pullup resistors are not needed.        |
| 22                                  | 19  | SCL             | Serial clock line. Connect to V <sub>CC</sub> through a pullup resistor                                 |
| 23                                  | 20  | SDA             | Serial data line. Connect to V <sub>CC</sub> through a pullup resistor.                                 |
| 24                                  | 21  | V <sub>CC</sub> | Supply voltage                                                                                          |

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### LOGIC DIAGRAM (POSITIVE LOGIC)



### SIMPLIFIED SCHEMATIC DIAGRAM OF EACH P-PORT INPUT/OUTPUT



## I<sup>2</sup>C Interface

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I<sup>2</sup>C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see [Figure 1](#)). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A2–A0) of the slave device must not be changed between the start and the stop conditions.

The data byte follows the address ACK. If the R/W bit is high, the data from this device are the values read from the P port. If the R/W bit is low, the data are from the master, to be output to the P port. The data byte is followed by an ACK sent from this device. If other data bytes are sent from the master, following the ACK, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time ( $t_{pv}$ ) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see [Figure 2](#)).

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see [Figure 1](#)).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see [Figure 3](#)). Setup and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

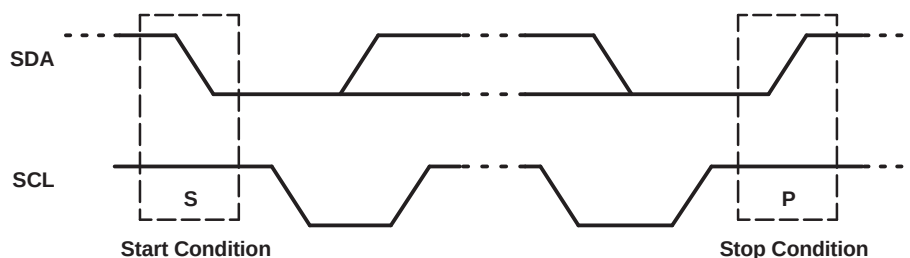


Figure 1. Definition of Start and Stop Conditions

# PCF8575C

## REMOTE 16-BIT I<sup>2</sup>C AND SMBus LOW-POWER I/O EXPANDER

### WITH INTERRUPT OUTPUT

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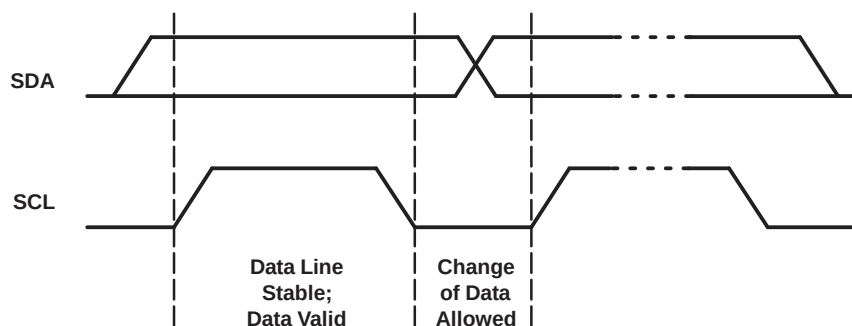


Figure 2. Bit Transfer

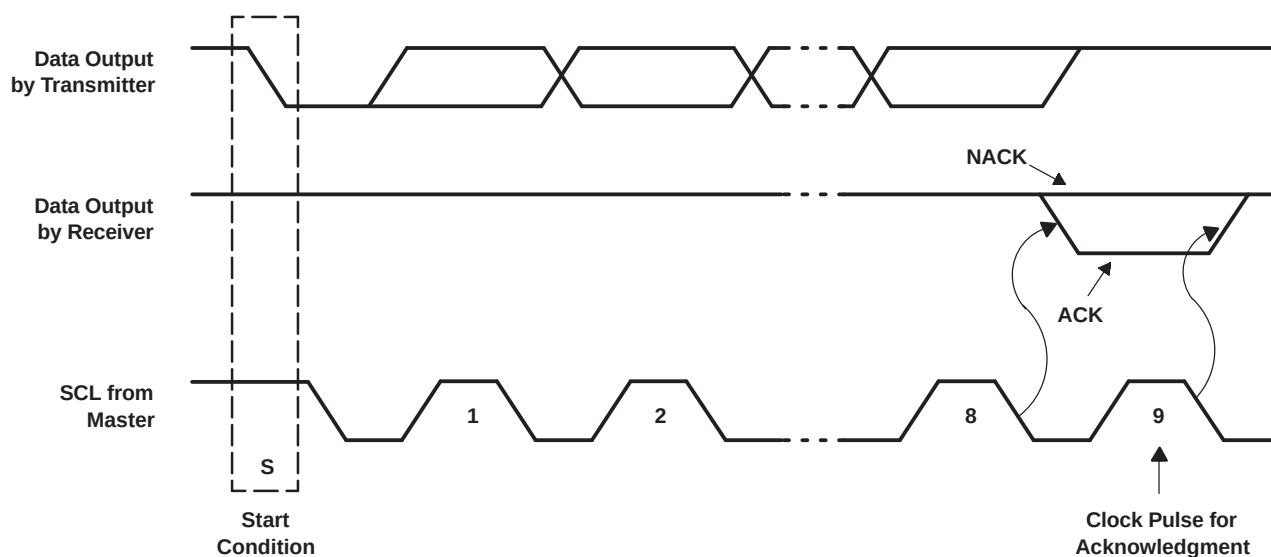


Figure 3. Acknowledgment on I<sup>2</sup>C Bus

#### Interface Definition

| BYTE                           | BIT     |     |     |     |     |     |     |         |
|--------------------------------|---------|-----|-----|-----|-----|-----|-----|---------|
|                                | 7 (MSB) | 6   | 5   | 4   | 3   | 2   | 1   | 0 (LSB) |
| I <sup>2</sup> C slave address | L       | H   | L   | L   | A2  | A1  | A0  | R/W     |
| P0x I/O data bus               | P07     | P06 | P05 | P04 | P03 | P02 | P01 | P00     |
| P1x I/O data bus               | P17     | P16 | P15 | P14 | P13 | P12 | P11 | P10     |

Figure 4 and Figure 5 show the address and timing diagrams for the write and read modes, respectively.

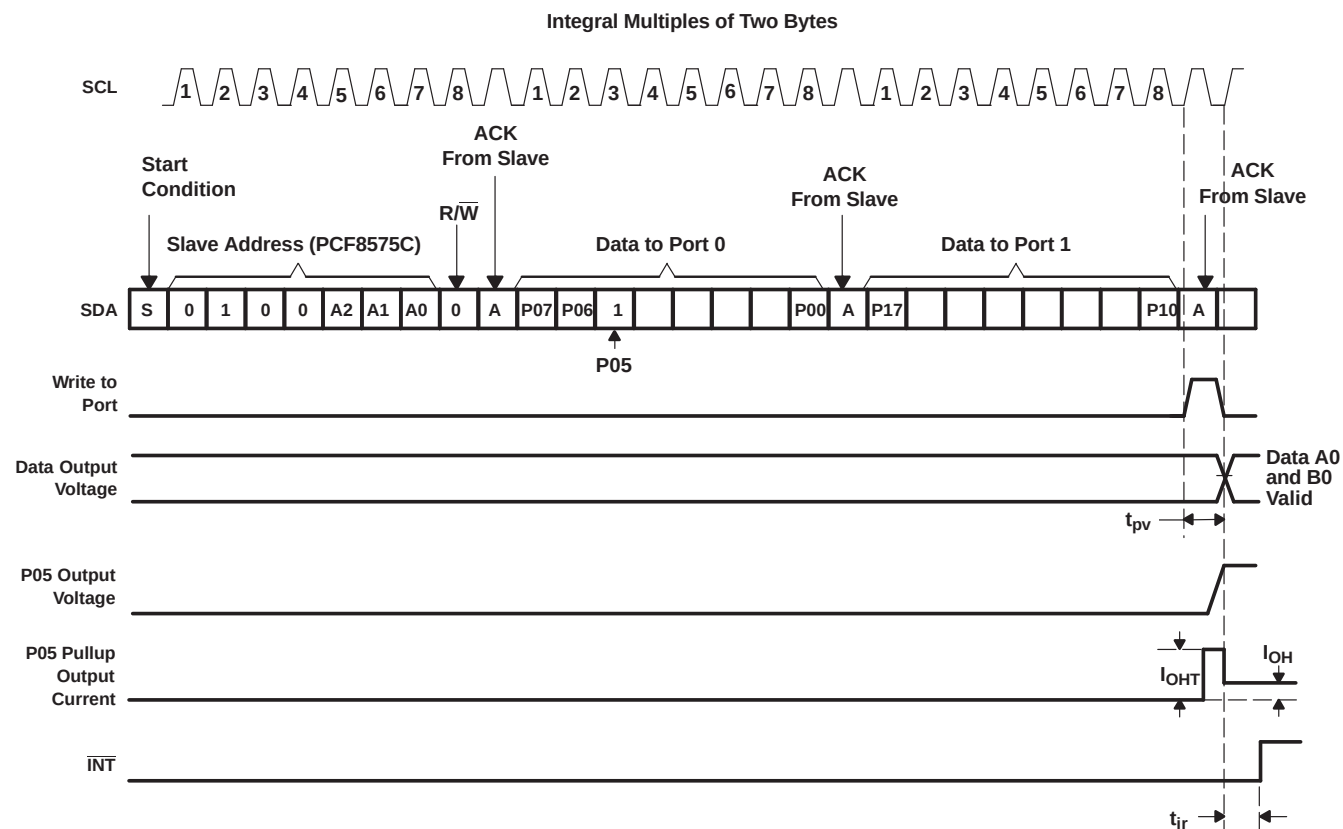
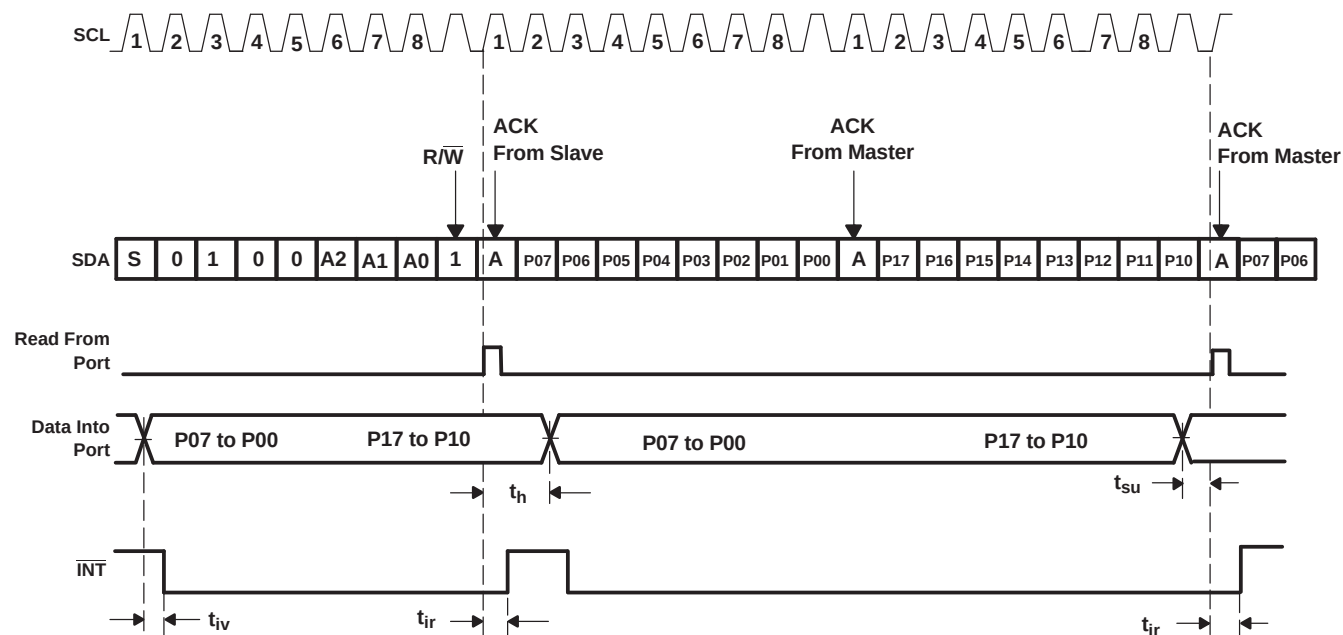


Figure 4. Write Mode (Output)



A low-to-high transition of SDA while SCL is high is defined as the stop condition (P). The transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the latest ACK phase is valid (output mode). Input data is lost.

Figure 5. Read Mode (Input)

# PCF8575C

## REMOTE 16-BIT I<sup>2</sup>C AND SMBus LOW-POWER I/O EXPANDER WITH INTERRUPT OUTPUT

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### Address Reference

| INPUTS |    |    | I <sup>2</sup> C BUS SLAVE ADDRESS |
|--------|----|----|------------------------------------|
| A2     | A1 | A0 |                                    |
| L      | L  | L  | 32 (decimal), 20 (hexadecimal)     |
| L      | L  | H  | 33 (decimal), 21 (hexadecimal)     |
| L      | H  | L  | 34 (decimal), 22 (hexadecimal)     |
| L      | H  | H  | 35 (decimal), 23 (hexadecimal)     |
| H      | L  | L  | 36 (decimal), 24 (hexadecimal)     |
| H      | L  | H  | 37 (decimal), 25 (hexadecimal)     |
| H      | H  | L  | 38 (decimal), 26 (hexadecimal)     |
| H      | H  | H  | 39 (decimal), 27 (hexadecimal)     |

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                  |                                                   | MIN                                                    | MAX                   | UNIT |
|------------------|---------------------------------------------------|--------------------------------------------------------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage range                              | –0.5                                                   | 6.5                   | V    |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>                | –0.5                                                   | V <sub>CC</sub> + 0.5 | V    |
| V <sub>O</sub>   | Output voltage range <sup>(2)</sup>               | –0.5                                                   | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current                               | V <sub>I</sub> < 0                                     | –20                   | mA   |
| I <sub>OK</sub>  | Output clamp current                              | V <sub>O</sub> < 0                                     | –20                   | mA   |
| I <sub>OK</sub>  | Input/output clamp current                        | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> | ±400                  | μA   |
| I <sub>OL</sub>  | Continuous output low current                     | V <sub>O</sub> = 0 to V <sub>CC</sub>                  | 50                    | mA   |
| I <sub>OH</sub>  | Continuous output high current                    | V <sub>O</sub> = 0 to V <sub>CC</sub>                  | –4                    | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND |                                                        | ±100                  | mA   |
| θ <sub>JA</sub>  | Package thermal impedance <sup>(3)</sup>          | DB package                                             | 63                    | °C/W |
|                  |                                                   | DBQ package                                            | 61                    |      |
|                  |                                                   | DGV package                                            | 86                    |      |
|                  |                                                   | DW package                                             | 46                    |      |
|                  |                                                   | PW package                                             | 88                    |      |
|                  |                                                   | RGE package                                            | 53                    |      |
|                  |                                                   | RHL package                                            | 43                    |      |
| T <sub>stg</sub> | Storage temperature range                         | –65                                                    | 150                   | °C   |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions

|                  |                                 | MIN                      | MAX                   | UNIT |
|------------------|---------------------------------|--------------------------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage                  | 4.5                      | 5.5                   | V    |
| V <sub>IH</sub>  | High-level input voltage        | A0, A1, A2, SDA, and SCL | 0.7 × V <sub>CC</sub> | V    |
|                  |                                 | P07–P00 and P17–P10      | 0.8 × V <sub>CC</sub> |      |
| V <sub>IL</sub>  | Low-level input voltage         | A0, A1, A2, SDA, and SCL | –0.5                  | V    |
|                  |                                 | P07–P00 and P17–P10      | –0.5                  |      |
| I <sub>OHT</sub> | P-port transient pullup current |                          | –10                   | mA   |
| I <sub>OL</sub>  | P-port low-level output current |                          | 25                    | mA   |
| T <sub>A</sub>   | Operating free-air temperature  | –40                      | 85                    | °C   |



## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        |                                       | TEST CONDITIONS                                                                         | V <sub>CC</sub>  | MIN  | TYP <sup>(1)</sup> | MAX  | UNIT |
|------------------|---------------------------------------|-----------------------------------------------------------------------------------------|------------------|------|--------------------|------|------|
| V <sub>IK</sub>  | Input diode clamp voltage             | I <sub>I</sub> = –18 mA                                                                 | 4.5 V to 5.5 V   | –1.2 |                    |      | V    |
| V <sub>POR</sub> | Power-on reset voltage <sup>(2)</sup> | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0                             | V <sub>POR</sub> |      | 1.2                | 1.8  | V    |
| I <sub>OHT</sub> | P-port transient pullup current       | High during ACK V <sub>OH</sub> = GND                                                   | 4.5 V            | –0.5 | –1                 |      | mA   |
| I <sub>OL</sub>  | SDA                                   | V <sub>OL</sub> = 0.4 V                                                                 | 4.5 V to 5.5 V   | 3    |                    |      | mA   |
|                  | P port                                | V <sub>OL</sub> = 0.4 V                                                                 | 4.5 V to 5.5 V   | 5    | 15                 |      |      |
|                  |                                       | V <sub>OL</sub> = 1 V                                                                   |                  | 10   | 25                 |      |      |
|                  | INT                                   | V <sub>OL</sub> = 0.4 V                                                                 | 4.5 V to 5.5 V   | 1.6  |                    |      |      |
| I <sub>I</sub>   | SCL, SDA                              | V <sub>I</sub> = V <sub>CC</sub> or GND                                                 | 4.5 V to 5.5 V   |      |                    | ±2   | μA   |
|                  | A0, A1, A2                            |                                                                                         |                  |      |                    | ±1   |      |
| I <sub>IHL</sub> | P port                                | V <sub>I</sub> ≥ V <sub>CC</sub> or V <sub>I</sub> ≤ GND                                | 4.5 V to 5.5 V   |      |                    | ±400 | μA   |
| I <sub>CC</sub>  | Operating mode                        | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, f <sub>SCL</sub> = 400 kHz | 5.5 V            |      | 100                | 200  | μA   |
|                  | Standby mode                          | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, f <sub>SCL</sub> = 0 kHz   |                  |      | 2.5                | 10   |      |
| ΔI <sub>CC</sub> | Supply current increase               | One input at V <sub>CC</sub> – 0.6 V,<br>Other inputs at V <sub>CC</sub> or GND         | 4.5 V to 5.5 V   |      |                    | 200  | μA   |
| C <sub>i</sub>   | SCL                                   | V <sub>I</sub> = V <sub>CC</sub> or GND                                                 | 4.5 V to 5.5 V   |      | 3                  | 7    | pF   |
| C <sub>io</sub>  | SDA                                   | V <sub>IO</sub> = V <sub>CC</sub> or GND                                                | 4.5 V to 5.5 V   |      | 3                  | 7    | pF   |
|                  | P port                                |                                                                                         |                  |      | 4                  | 10   |      |

(1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(2) The power-on reset circuit resets the I<sup>2</sup>C bus logic with V<sub>CC</sub> < V<sub>POR</sub> and sets all I/Os to logic high (with current source to V<sub>CC</sub>).

## I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6](#))

|                  |                                                          | MIN                                   | MAX | UNIT |
|------------------|----------------------------------------------------------|---------------------------------------|-----|------|
| f <sub>SCL</sub> | I <sup>2</sup> C clock frequency                         |                                       | 400 | kHz  |
| t <sub>SCH</sub> | I <sup>2</sup> C clock high time                         | 0.6                                   |     | μs   |
| t <sub>SCL</sub> | I <sup>2</sup> C clock low time                          | 1.3                                   |     | μs   |
| t <sub>SP</sub>  | I <sup>2</sup> C spike time                              |                                       | 50  | ns   |
| t <sub>Sds</sub> | I <sup>2</sup> C serial-data setup time                  | 100                                   |     | ns   |
| t <sub>Sdh</sub> | I <sup>2</sup> C serial-data hold time                   | 0                                     |     | ns   |
| t <sub>ICr</sub> | I <sup>2</sup> C input rise time                         | 20 + 0.1C <sub>b</sub> <sup>(1)</sup> | 300 | ns   |
| t <sub>ICf</sub> | I <sup>2</sup> C input fall time                         | 20 + 0.1C <sub>b</sub> <sup>(1)</sup> | 300 | ns   |
| t <sub>OCf</sub> | I <sup>2</sup> C output fall time (10-pF to 400-pF bus)  |                                       | 300 | ns   |
| t <sub>Buf</sub> | I <sup>2</sup> C bus free time between stop and start    | 1.3                                   |     | μs   |
| t <sub>Sts</sub> | I <sup>2</sup> C start or repeated start condition setup | 0.6                                   |     | μs   |
| t <sub>StH</sub> | I <sup>2</sup> C start or repeated start condition hold  | 0.6                                   |     | μs   |
| t <sub>Sps</sub> | I <sup>2</sup> C stop condition setup                    | 0.6                                   |     | μs   |
| t <sub>Vd</sub>  | Valid-data time                                          | SCL low to SDA output valid           |     | 1.2  |
| C <sub>b</sub>   | I <sup>2</sup> C bus capacitive load                     |                                       | 400 | pF   |

(1) C<sub>b</sub> = total bus capacitance of one bus line in pF

# PCF8575C

## REMOTE 16-BIT I<sup>2</sup>C AND SMBus LOW-POWER I/O EXPANDER WITH INTERRUPT OUTPUT

SCPS123C – MARCH 2005 – REVISED JULY 2006

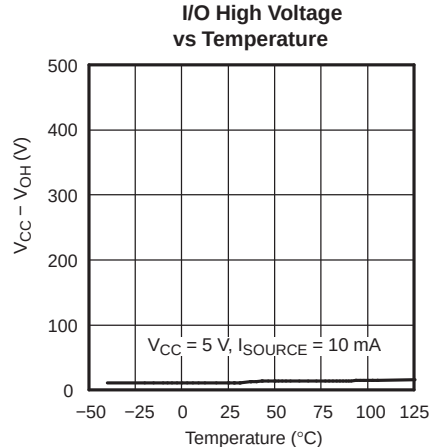
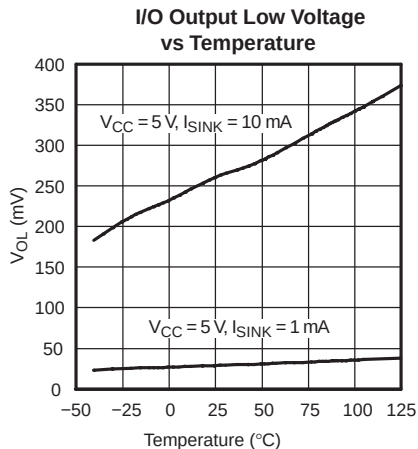
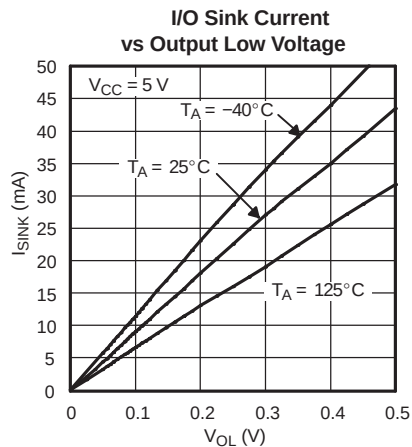
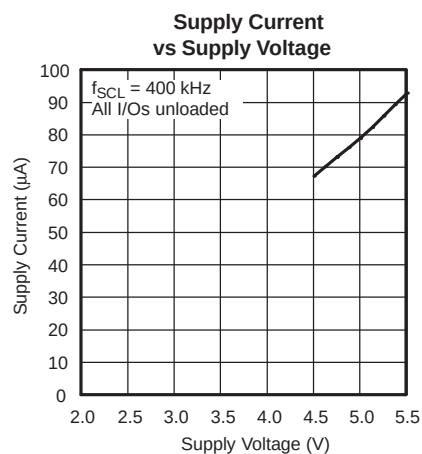
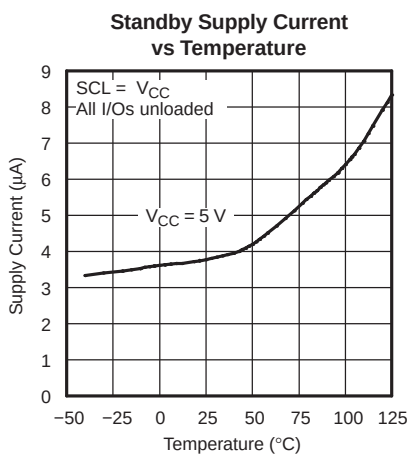
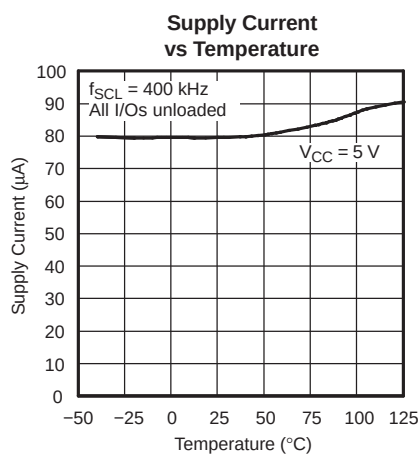
### Switching Characteristics

over recommended operating free-air temperature range,  $C_L \leq 100$  pF (unless otherwise noted) (see [Figure 7](#) and [Figure 8](#))

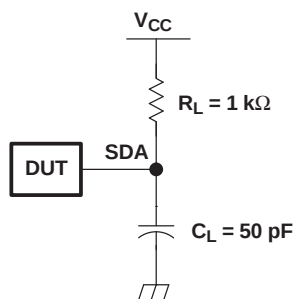
| PARAMETER |                            | FROM<br>(INPUT) | TO<br>(OUTPUT)   | MIN | MAX | UNIT    |
|-----------|----------------------------|-----------------|------------------|-----|-----|---------|
| $t_{iv}$  | Interrupt valid time       | P port          | $\overline{INT}$ |     | 4   | $\mu$ s |
| $t_{ir}$  | Interrupt reset delay time | SCL             | $\overline{INT}$ |     | 4   | $\mu$ s |
| $t_{pv}$  | Output data valid          | SCL             | P port           |     | 4   | $\mu$ s |
| $t_{su}$  | Input data setup time      | P port          | SCL              | 0   |     | $\mu$ s |
| $t_h$     | Input data hold time       | P port          | SCL              | 4   |     | $\mu$ s |

## TYPICAL OPERATING CHARACTERISTICS

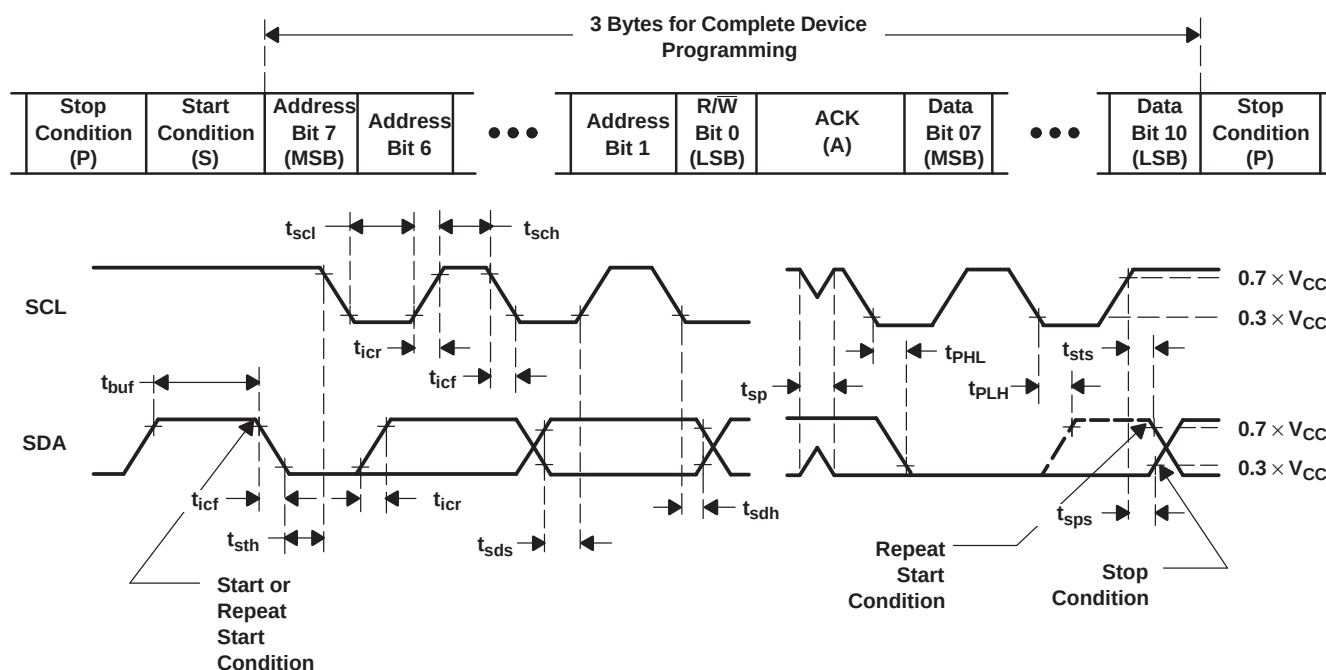
T<sub>A</sub> = 25°C (unless otherwise noted)



## PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION

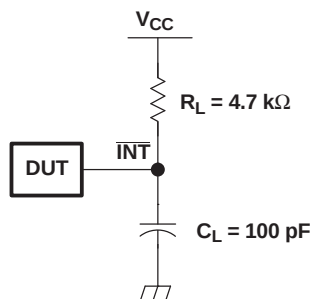


VOLTAGE WAVEFORMS

| BYTE | DESCRIPTION              |
|------|--------------------------|
| 1    | I <sup>2</sup> C address |
| 2, 3 | P-port data              |

Figure 6. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



INTERRUPT LOAD CONFIGURATION

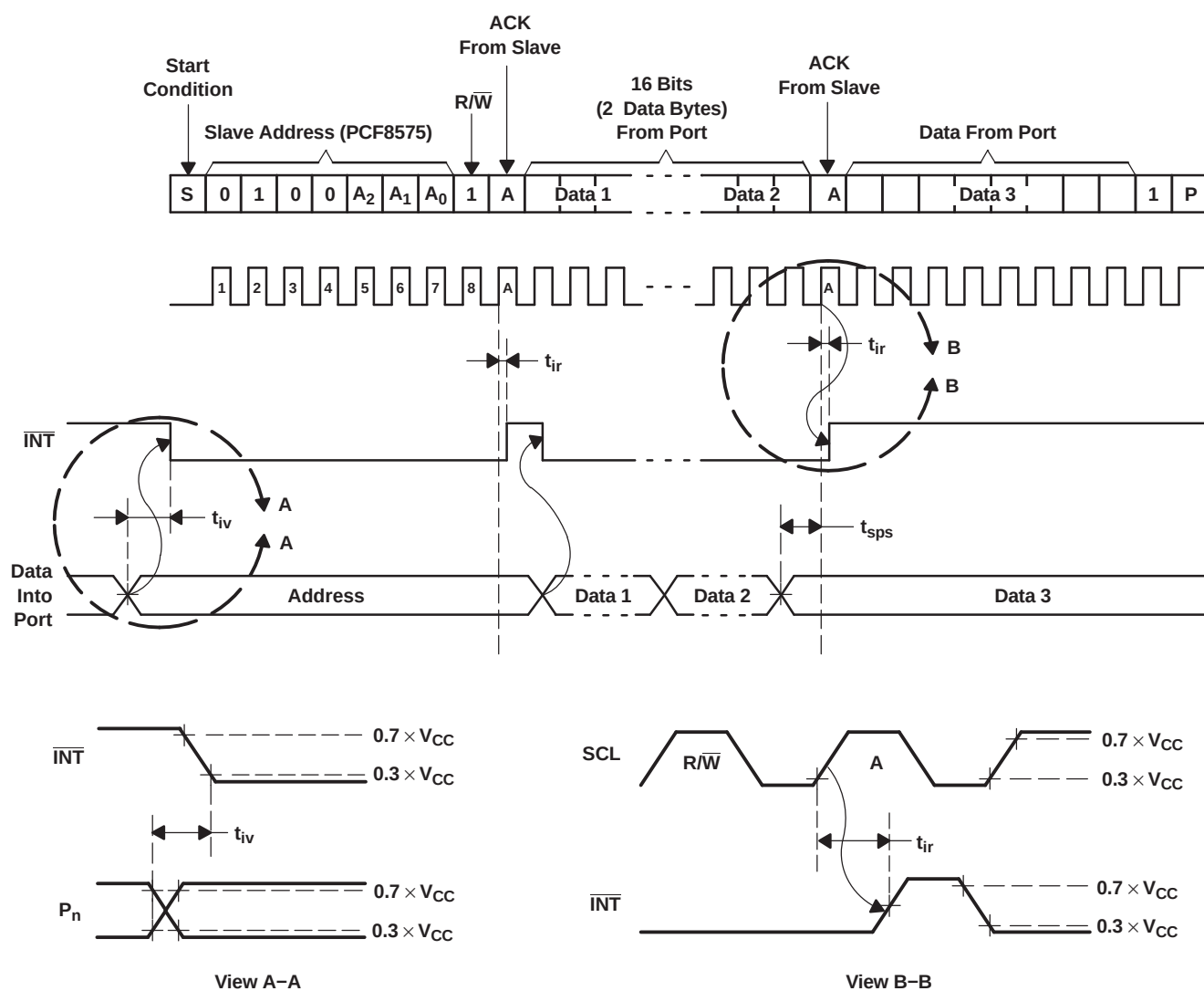
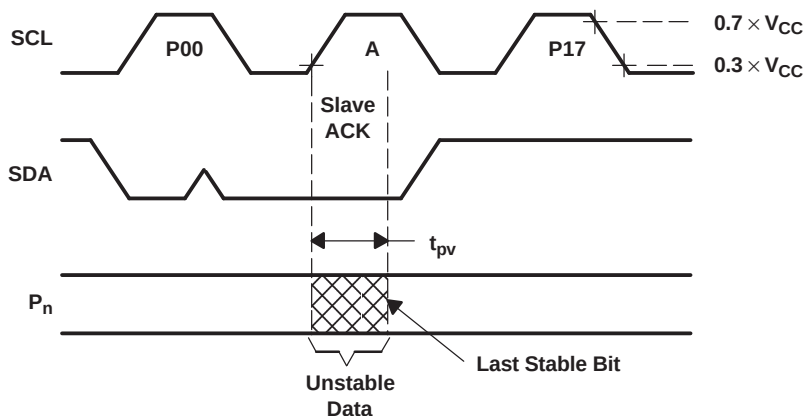
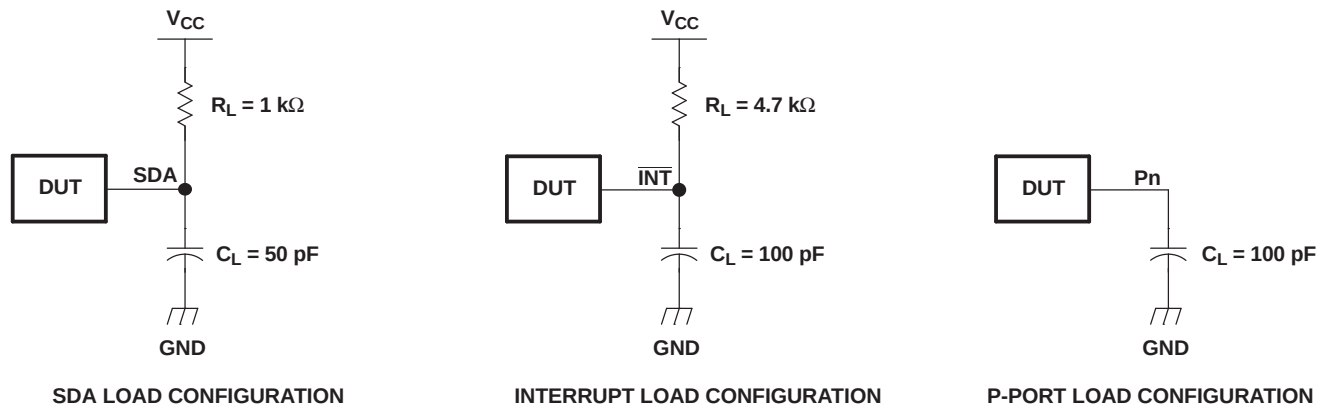
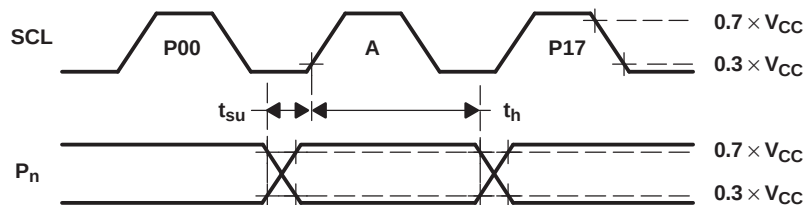


Figure 7. Interrupt Load Circuit and Voltage Waveforms

# PARAMETER MEASUREMENT INFORMATION (continued)



Write-Mode Timing (R/W = 0)



Read-Mode Timing (R/W = 1)

Figure 8. P-Port Load Circuits and Voltage Waveforms

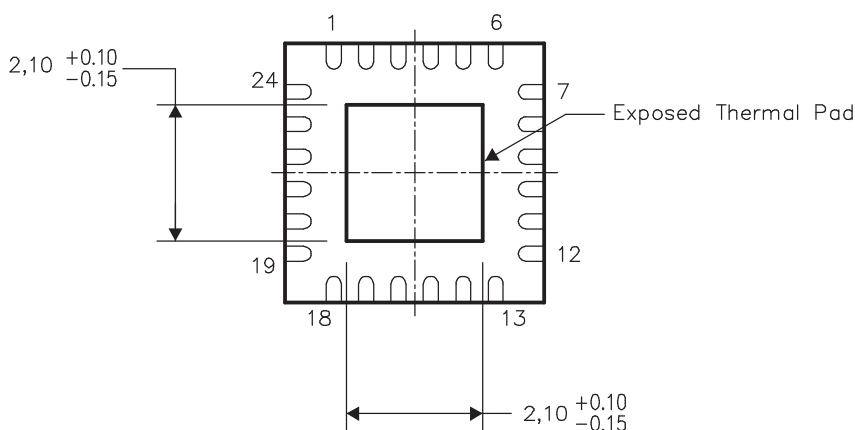
## THERMAL PAD MECHANICAL DATA RGE (S-PQFP-N24)

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

### Exposed Thermal Pad Dimensions

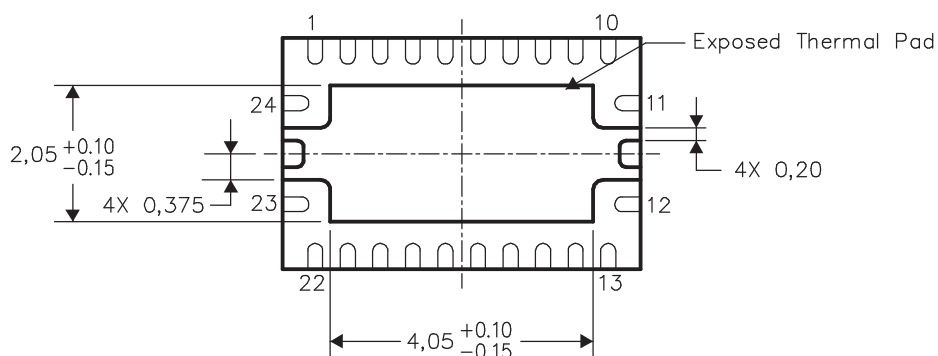
**THERMAL PAD MECHANICAL DATA**  
**RHL (S-PQFP-N24)**

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206363–3/A 01/05



**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type  | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|---------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| PCF8575CDB       | ACTIVE                | SSOP          | DB              | 24   | 60          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CDBE4     | ACTIVE                | SSOP          | DB              | 24   | 60          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CDBQR     | ACTIVE                | SSOP/<br>QSOP | DBQ             | 24   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1YEAR           |
| PCF8575CDBQRE4   | ACTIVE                | SSOP/<br>QSOP | DBQ             | 24   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1YEAR           |
| PCF8575CDBQRG4   | ACTIVE                | SSOP/<br>QSOP | DBQ             | 24   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1YEAR           |
| PCF8575CDBR      | ACTIVE                | SSOP          | DB              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CDBRE4    | ACTIVE                | SSOP          | DB              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CDGVR     | ACTIVE                | TVSOP         | DGV             | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CDGVRE4   | ACTIVE                | TVSOP         | DGV             | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CDW       | ACTIVE                | SOIC          | DW              | 24   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CDWE4     | ACTIVE                | SOIC          | DW              | 24   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CDWR      | ACTIVE                | SOIC          | DW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CDWRE4    | ACTIVE                | SOIC          | DW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CPW       | ACTIVE                | TSSOP         | PW              | 24   | 60          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CPWE4     | ACTIVE                | TSSOP         | PW              | 24   | 60          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CPWR      | ACTIVE                | TSSOP         | PW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CPWRE4    | ACTIVE                | TSSOP         | PW              | 24   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| PCF8575CRGER     | ACTIVE                | QFN           | RGE             | 24   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1YEAR           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

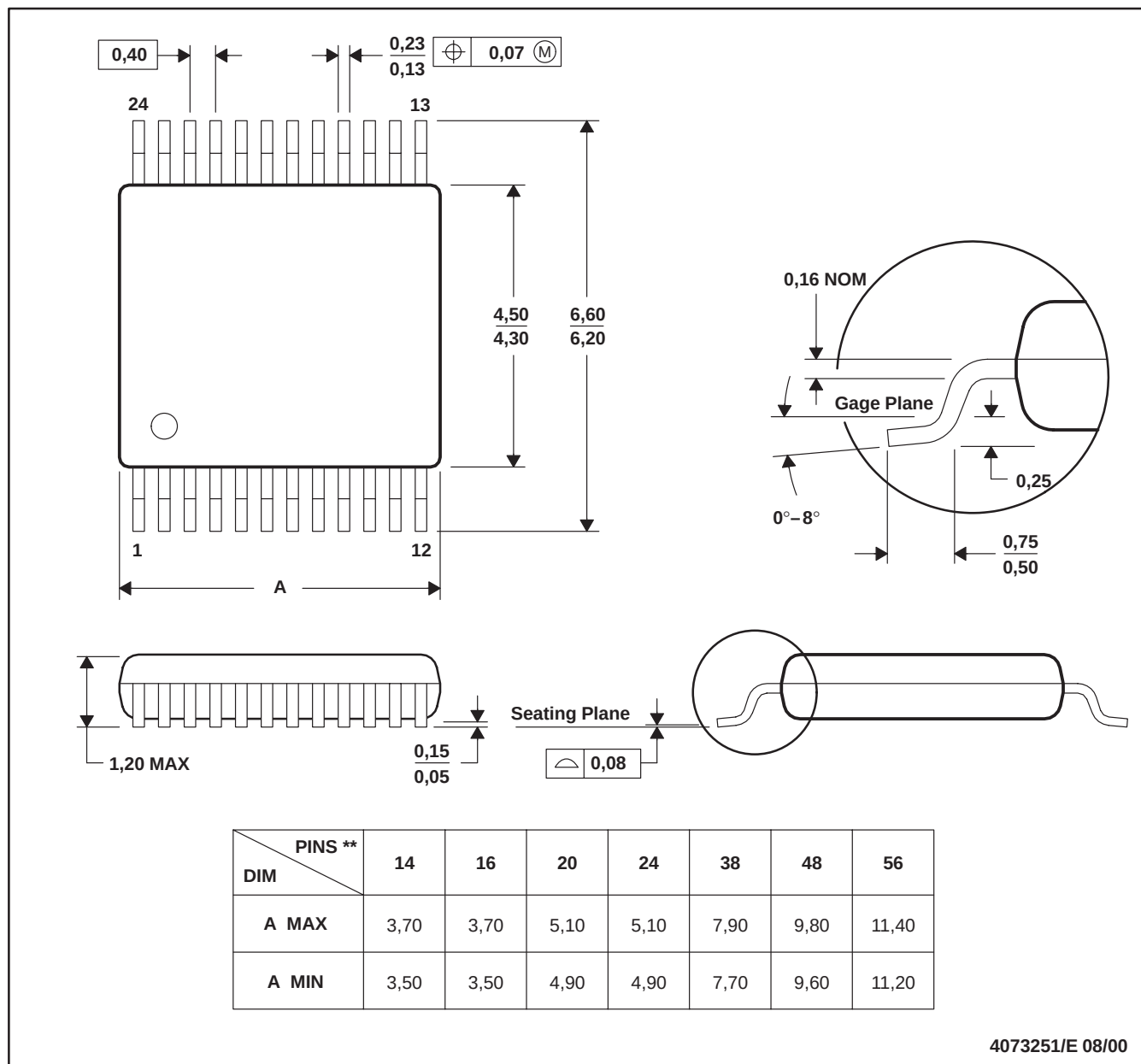
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## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

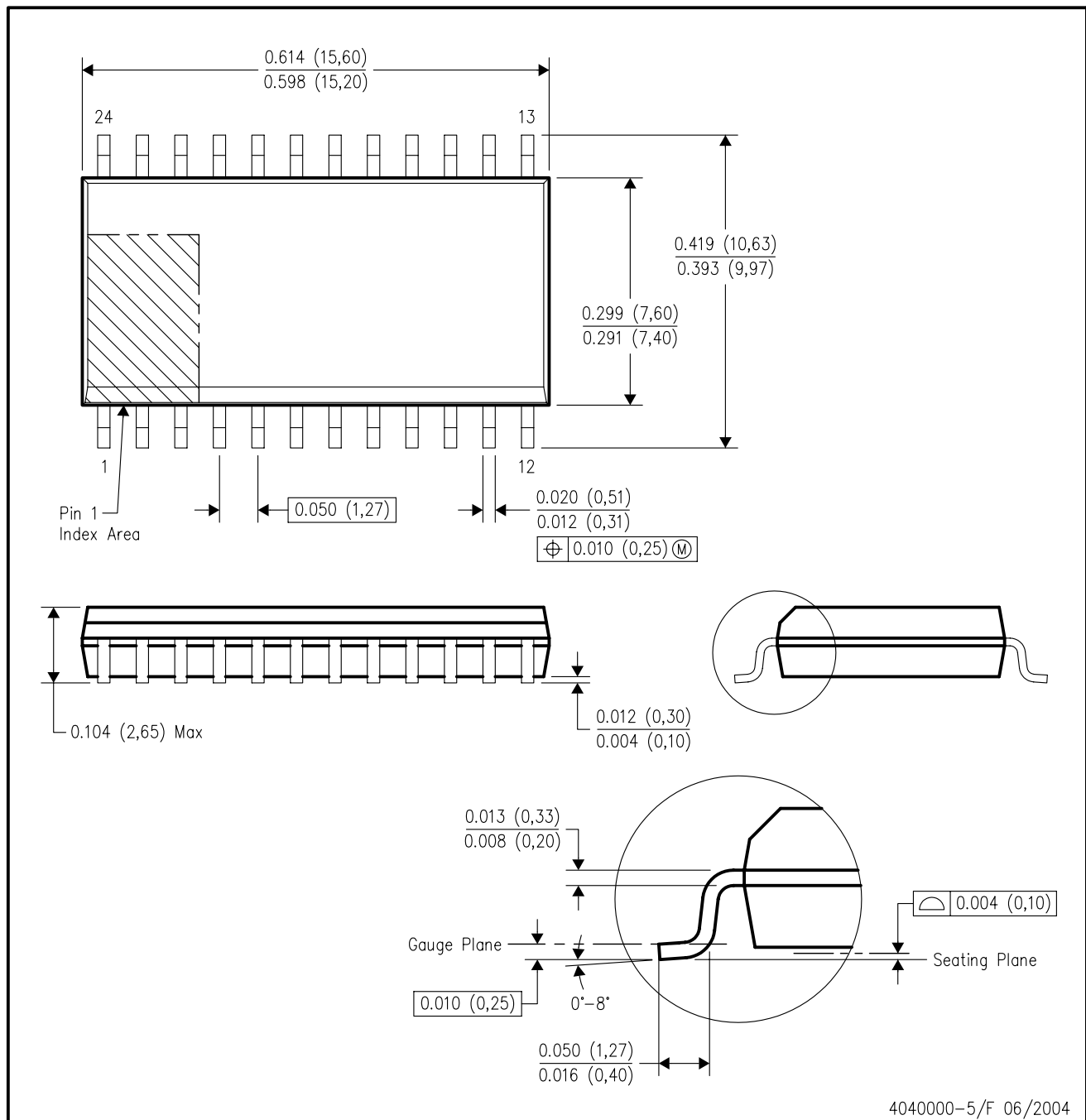
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## DW (R-PDSO-G24)

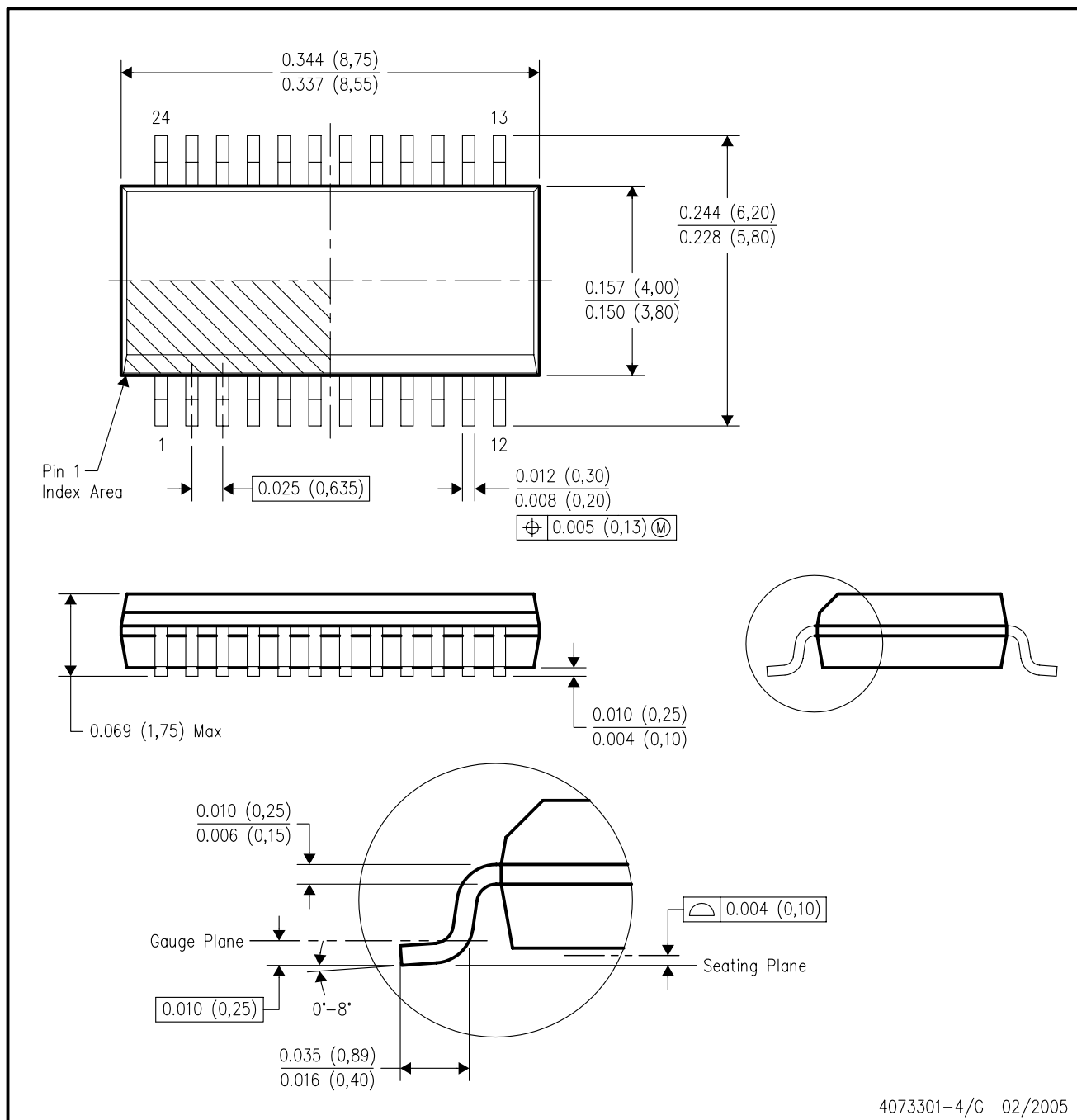
## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

## DBQ (R-PDSO-G24)

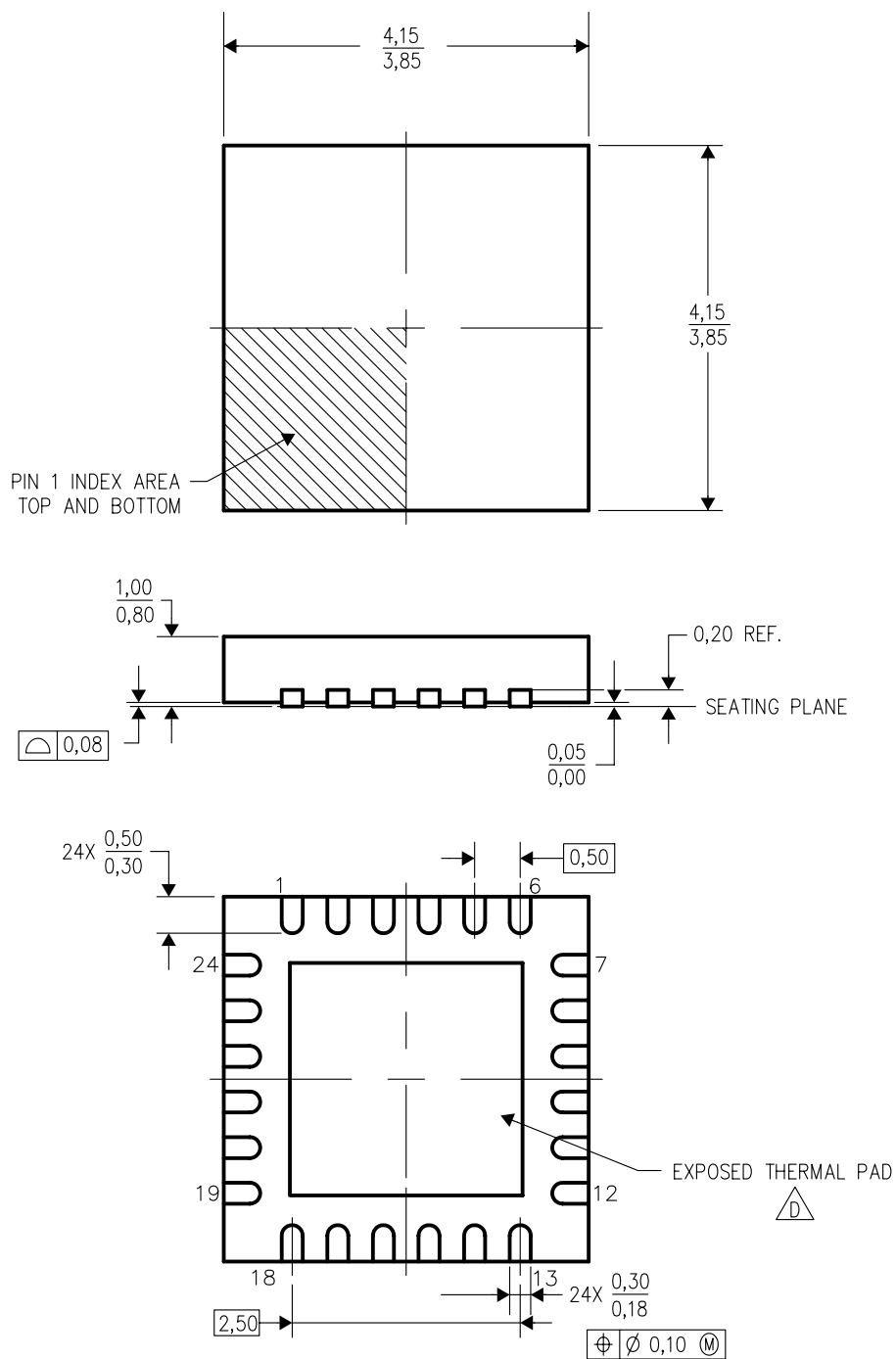
## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
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  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - Falls within JEDEC MO-137 variation AE.

RGE (S-PQFP-N24)

PLASTIC QUAD FLATPACK



4204104/C 11/04

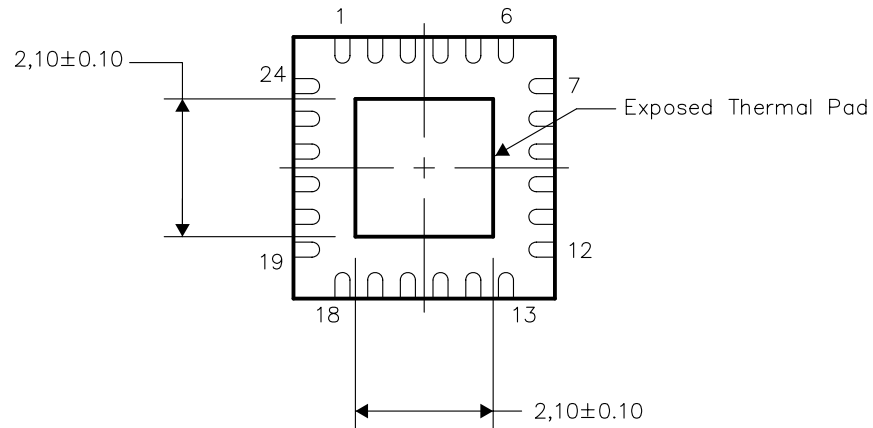
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-220.

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

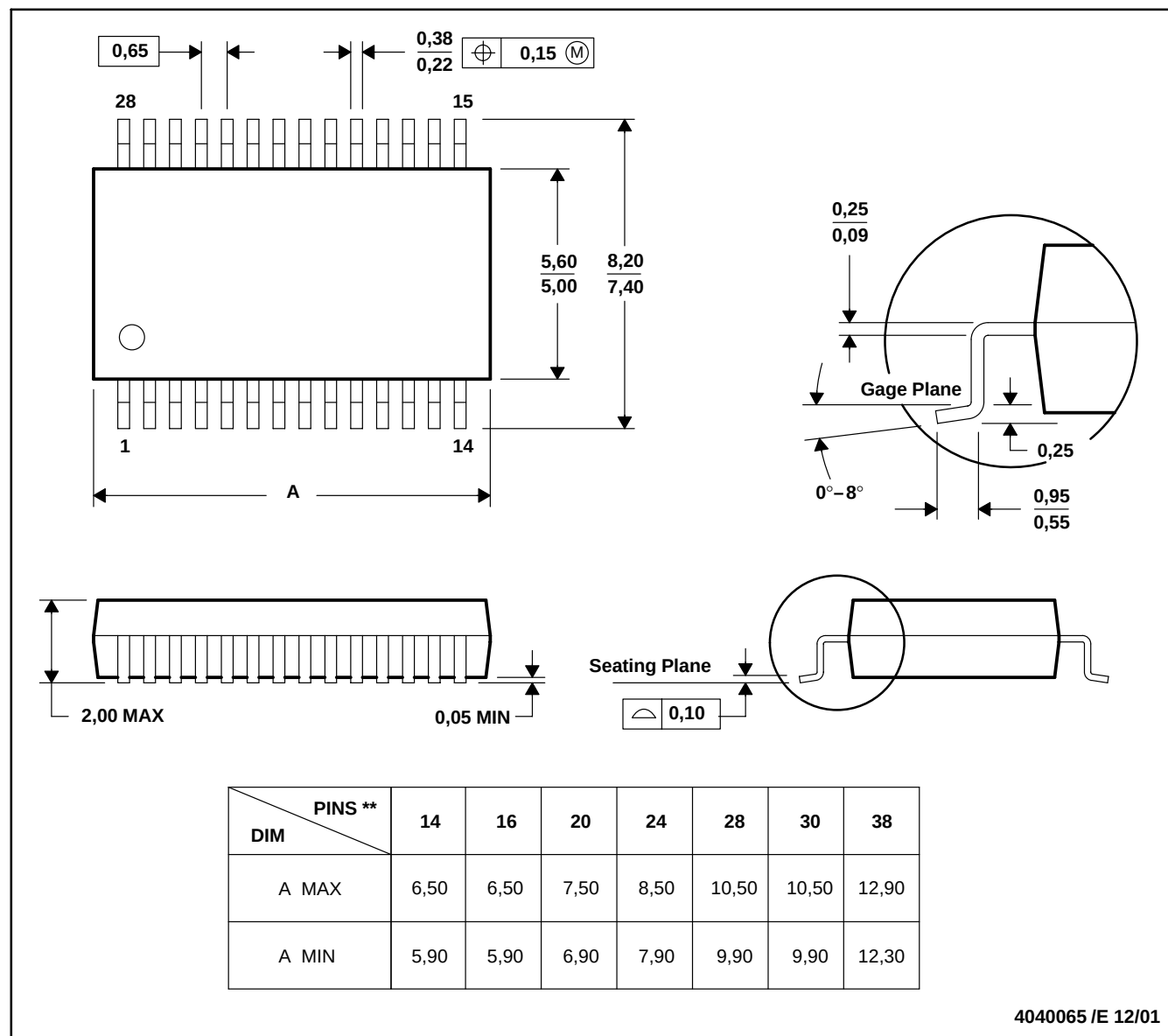
NOTE: All linear dimensions are in millimeters

## Exposed Thermal Pad Dimensions

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



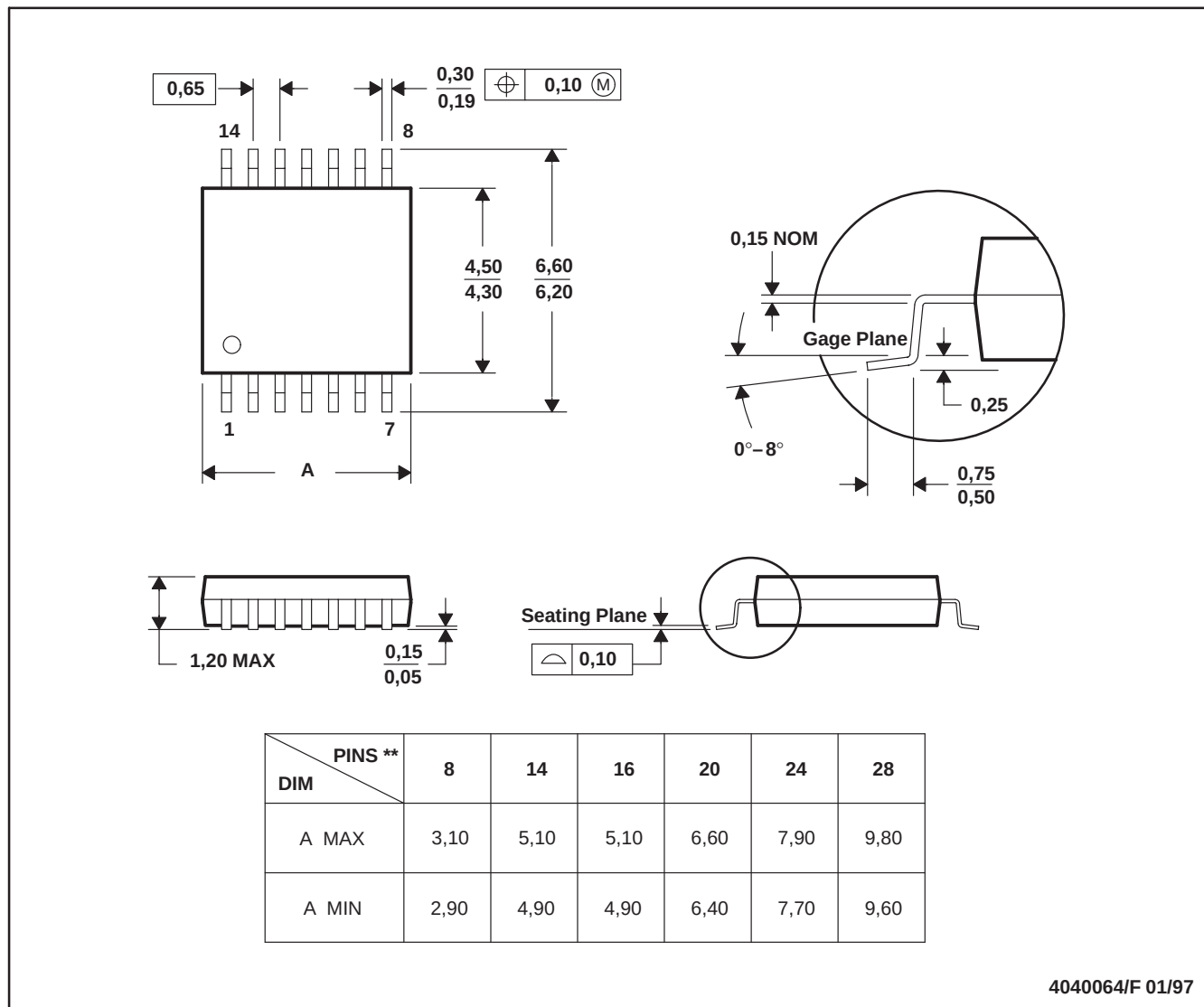
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150



## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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| Security           | <a href="http://www.ti.com/security">www.ti.com/security</a>             |
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| Wireless           | <a href="http://www.ti.com/wireless">www.ti.com/wireless</a>             |

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**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.