PI6C49S1506

High Performance Differential Fanout Buffer

Features

- 6 differential outputs with 2 banks
- User configurable output signaling standard for each bank: LVDS or LVPECL or HCSL
- Up to 1.5GHz output frequency for differential outputs
- Ultra low additive phase jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Selectable reference inputs support either single-ended or differential or Xtal
- Low skew between outputs within banks (<40ps)
- Low delay from input to output (Tpd typ. 1.5ns)
- Separate Input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- TQFP-32 package

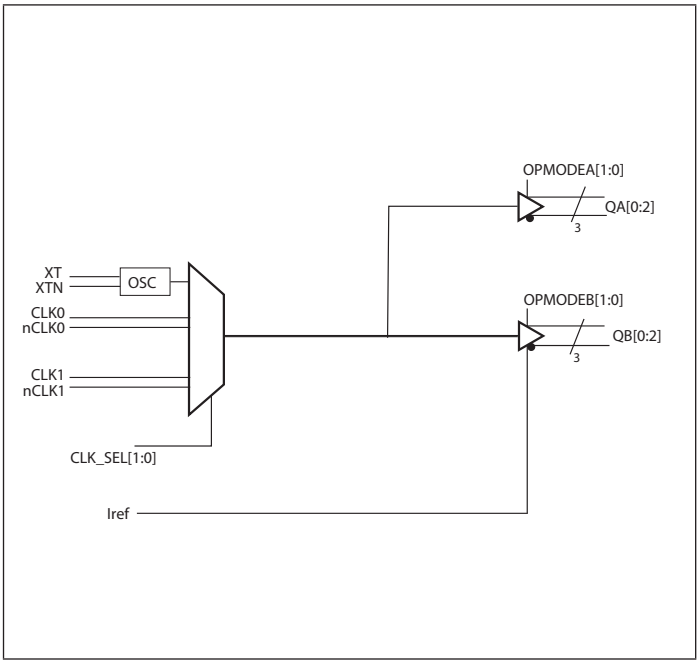
Description

The PI6C49S1506 is a high performance fanout buffer device-which supports up to 1.5GHz frequency. It also integrates a unique feature with user configurable output signaling standards on per bank basis which provide great flexibilities to users. The device also uses Pericom's proprietary input detection technique to make sure illegal input conditions will be detected and reflected by output states. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

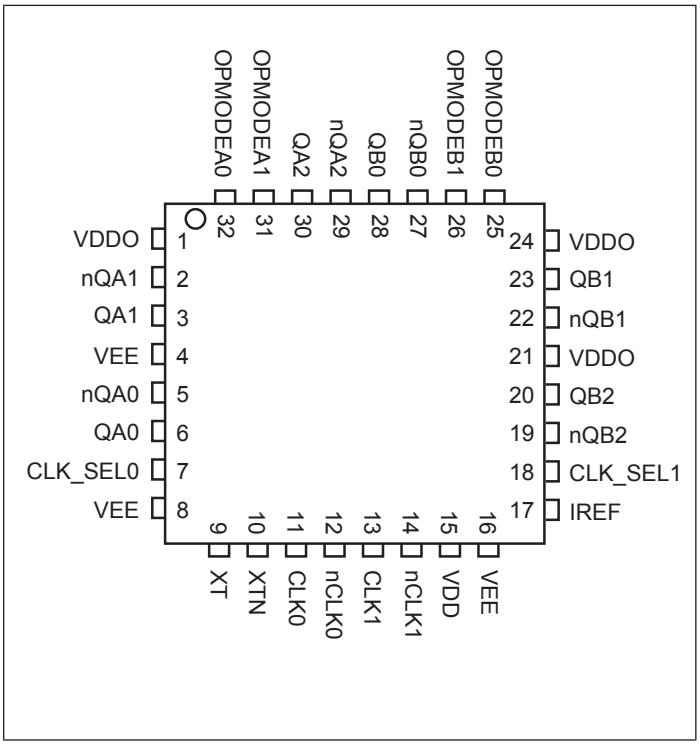
Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

Block Diagram



Pin Configuration (32-Pin TQFP)



Pinout Table

Pin #	Pin Name	Type	Description
1, 21, 24	V_{DDO}	Power	Power supply pins for outputs
2,3	nQA1 QA1	Output	Bank A differential output pair 1. Pin selectable LVPECL/LVDS/HCSL interface levels.
4, 16	V_{EE}	Power	Connect to Negative power supply
5, 6	nQA0 QA0	Output	Bank A differential output pair 0. Pin selectable LVPECL/LVDS/HCSL interface levels.
7	CLK_SEL0	Input	Input clock source selection
8	V_{EE}	Power	Negative power supply
9	XT	Input	XTAL input
10	XTN	Output	XTAL output
11, 12	CLK0	Input	Differential clock input
	nCLK0	Input	Differential clock input
13, 14	CLK1	Input	Differential clock input
	nCLK1	Input	Differential clock input
15	V_{DD}	Power	Power supply pins for device core
17	IREF	Output	Reference current
18	CLK_SEL1	Input	Input clock source selection
19, 20	QB2 nQB2	Output	Bank B differential output pair 5. Pin selectable LVPECL/LVDS/HCSL interface levels.
22, 23	nQB1 QB1	Output	Bank B differential output pair 4. Pin selectable LVPECL/LVDS/HCSL interface levels.
25	OPMODEB0	Input	Bank B output selection pin
26	OPMODEB1	Input	Bank B output selection pin
27, 28	nQB0 QB0	Output	Bank B differential output pair 3. Pin selectable LVPECL/LVDS/HCSL interface levels.
29, 30	nQA2 QA2	Output	Bank A differential output pair 2. Pin selectable LVPECL/LVDS/HCSL interface levels.
31	OPMODEA1	Input	Bank A output selection pin
32	OPMODEA0	Input	Bank A output selection pin

Function Table

Table 1: Input select function

CLK_SEL [1]	CLK_SEL [0]	Function
0	0	XTAL is the selected input
0	1	CLK0 is the selected reference input
1	X	CLK1 is the selected reference input

Table 2: Output Mode select function

OPMODEA/B [1]	OPMODEA/B [0]	Output Bank A / Bank B Mode
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Hi-Z

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....-55 to +150°C
Supply Voltage to Ground Potential (VDD) ..... -0.5 to +4.6V
Inputs (Referenced to GND) .....-0.5 to VDD+0.5V
Clock Output (Referenced to GND).....-0.5 to VDD+0.5V
Soldering Temperature (Max of 10 seconds) .....+260°C
Latch up.....200mA
ESD Protection (Input) .....2000 V min (HBM)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		3.135		3.465	V
			2.375		2.625	V
V_{DDO}	Output Supply Voltage		3.135		3.465	V
			2.375		2.625	V
I_{DD}	Core Power Supply Current				70	mA
I_{DDO}	Output Power Supply Current	All LVPECL outputs unloaded			75	
		All LVDS outputs loaded			85	
		All HCSL outputs unloaded			55	
T_A	Ambient Operating Temperature		-40		85	°C

DC Electrical Specifications - Differential Inputs

Symbol	Parameter		Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			150	uA
I_{IL}	Input Low current	Input = GND	-150			uA
C_{IN}	Input capacitance			3		PF
V_{IH}	Input high voltage				V_{DD}+0.3	V
V_{IL}	Input low voltage		-0.3			V
V_{Pk-Pk}	Input Differential Amplitude PK-PK		0.15		1.3	V
V_{CM}	Common model input voltage		GND + 0.5		V_{DD}-0.85	V

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High current	Input = V_{DD}			150	uA
I_{IL}	Input Low current	Input = GND	-150			uA
V_{IH}	Input high voltage	V_{DD}=3.3V	2.0		V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD}=3.3V	-0.3		0.8	V
V_{IH}	Input high voltage	V_{DD}=2.5V	1.7		V_{DD}+0.3	V
V_{IL}	Input low voltage	V_{DD}=2.5V	-0.3		0.7	V

DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage	V_{DD}=3.3V	2.1		2.6	V
		V_{DD}=2.5V	1.3		1.6	
V_{OL}	Output Low voltage	V_{DD}=3.3V	1.3		1.8	V
		V_{DD}=2.5V	0.5		0.8	

DC Electrical Specifications- LVDS Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage			1.433		V
V_{OL}	Output Low voltage			1.064		V
Vocm	Output common mode voltage			1.25		V
DVocm	Change in Vocm between output states				55	mV
Ro	Output impedance		85		140	Ω

DC Electrical Specifications- HCSL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High voltage		520	800		mV
V_{OL}	Output Low voltage			0	150	mV

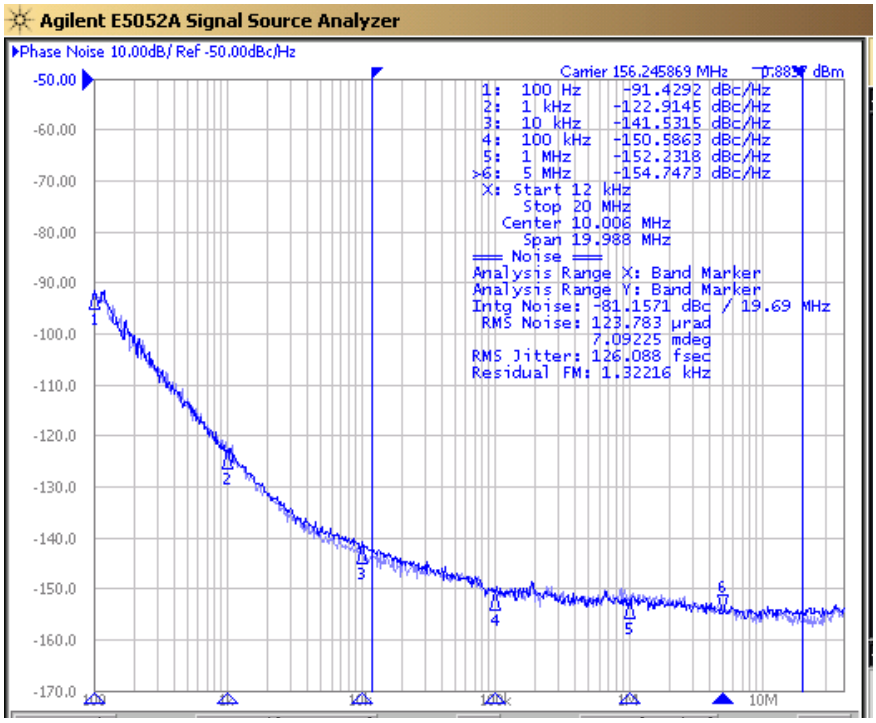
AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F_{OUT}	Clock output frequency	LVPECL, LVDS			1500	MHz
		HCSL			250	
T_r	Output rise time	From 20% to 80%		150		ps
T_f	Output fall time	From 80% to 20%		150		ps
T_{ODC}	Output duty cycle	Frequency<650MHz, LVPECL input	48		52	%
V_{PP}	Output swing Single-ended	LVPECL outputs	400			mV
		LVDS outputs, <650MHz	250			
		HCSL outputs	520			
T_j	Buffer additive jitter RMS	LVPECL and LVDS outputs		0.03	0.06	ps
		HCSL outputs		0.06	0.09	ps
V_{CROSS}	Absolute crossing voltage	HCSL	160		460	mV
DV_{CROSS}	Total variation of crossing voltage	HCSL			140	mV
T_{SK}	Output Skew	6 outputs devices, outputs in same bank, with same load, at DUT.		40		ps
T_{PD}	Propagation Delay			1500		ps
T_{OD}	Valid to HiZ			3	200	ns
T_{OE}	HiZ to valid			22	200	ns

Phase Noise Plot

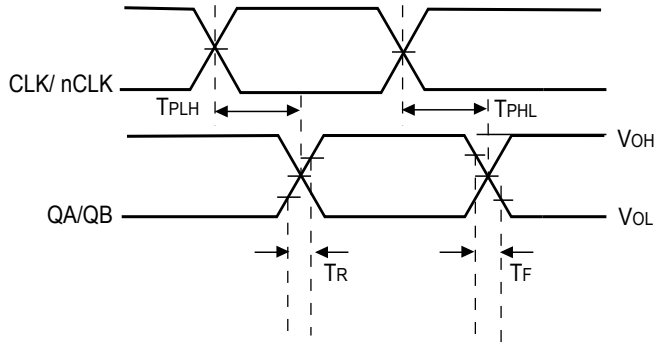
f_{OUT} = 156.25MHz

Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$ = 30fs



Propagation Delay

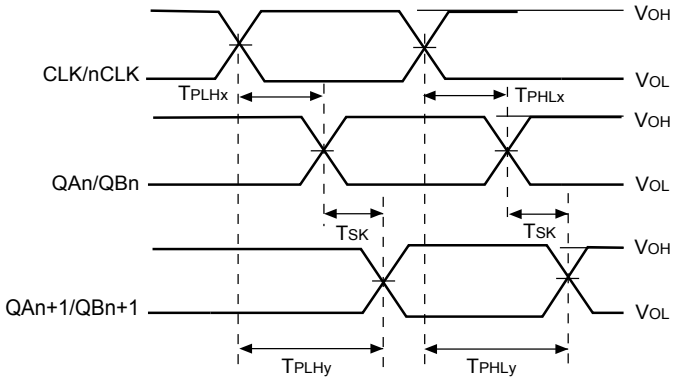
Propagation Delay T_{PD}



$T_{SK} = T_{PLH2} - T_{PLH1}$ or $T_{SK} = T_{PHL2} - T_{PHL1}$

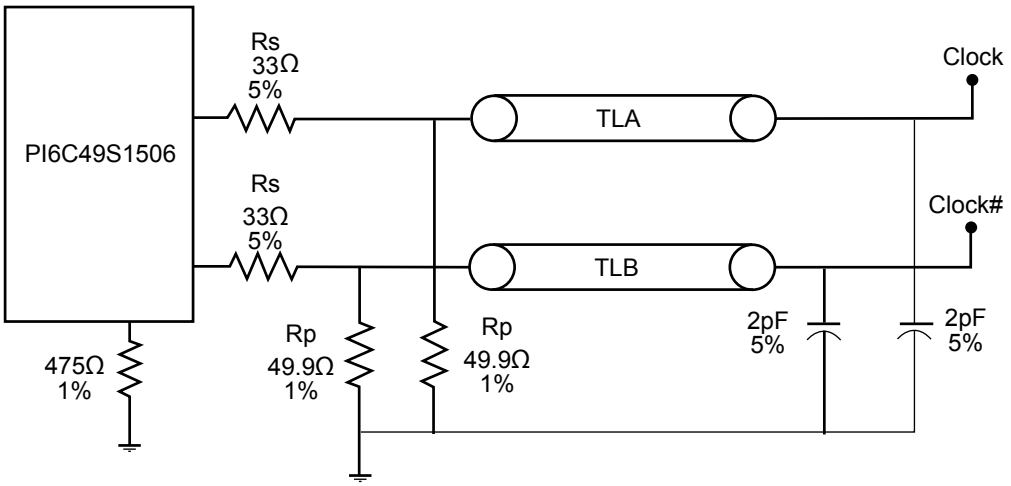
Output Skew

Output Skew T_{SK}

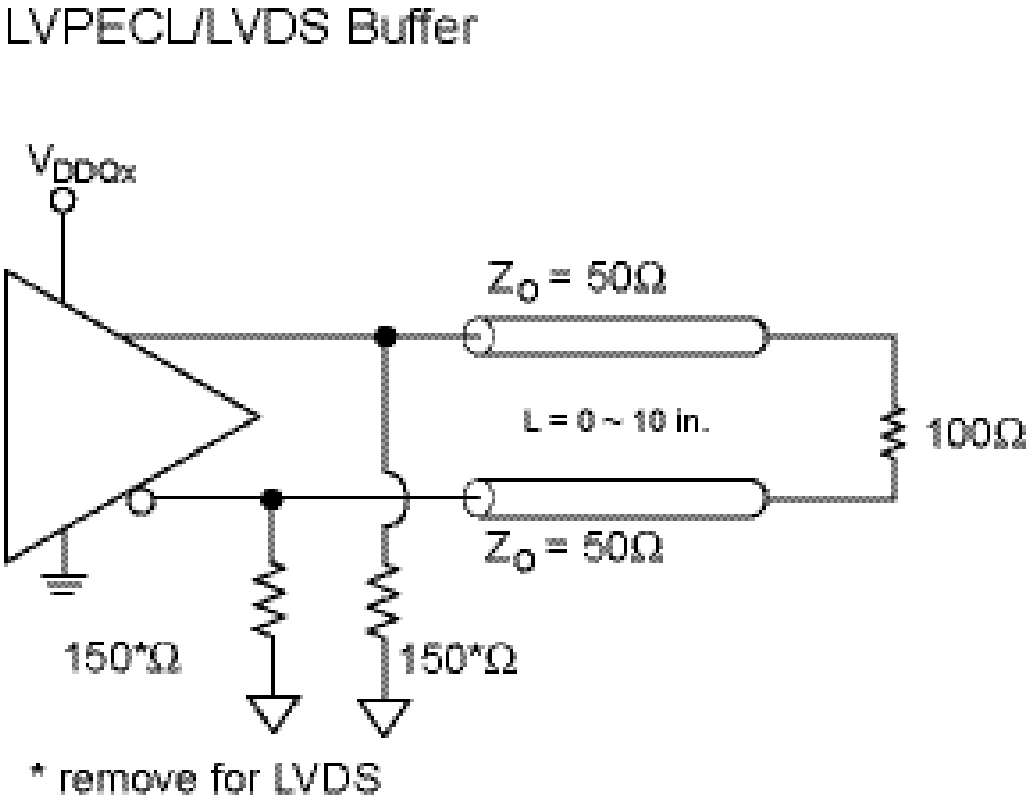


$T_{SK} = T_{PLHy} - T_{PLHx}$ or $T_{SK} = T_{PHLy} - T_{PHLx}$

Configuration Test Load Board Termination for HCSL outputs



Configuration Test Load Board Termination for LVPECL/ LVDS



Application Information

Wiring the differential input (Use CLK0) to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to postion the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R1/R2 = 0.609.

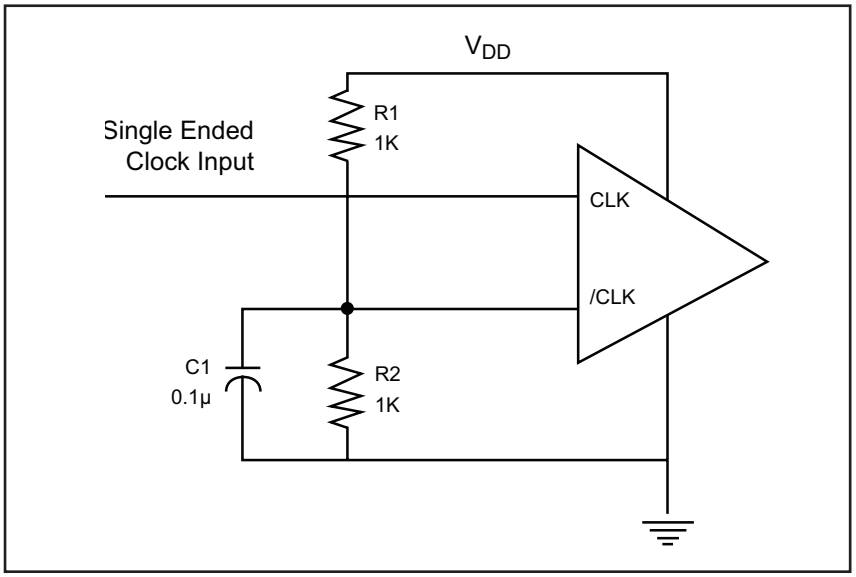
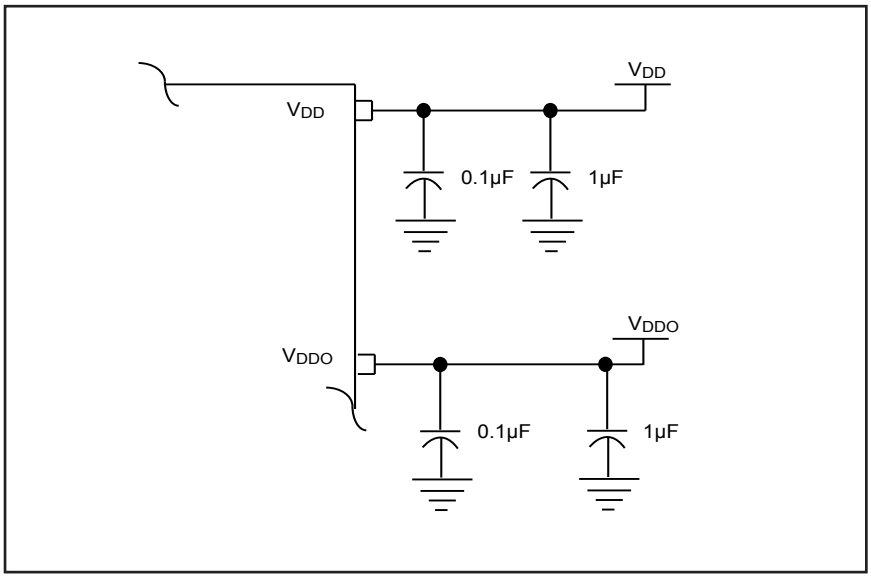


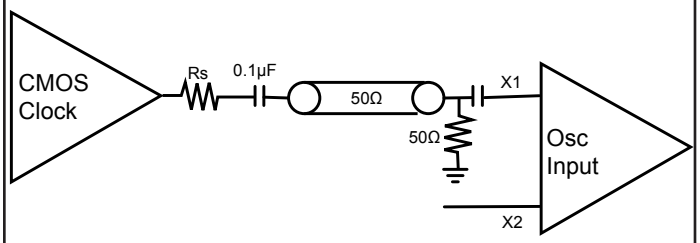
Figure 1. Single-ended input to Differential input device

Power Supply Filtering Techniques

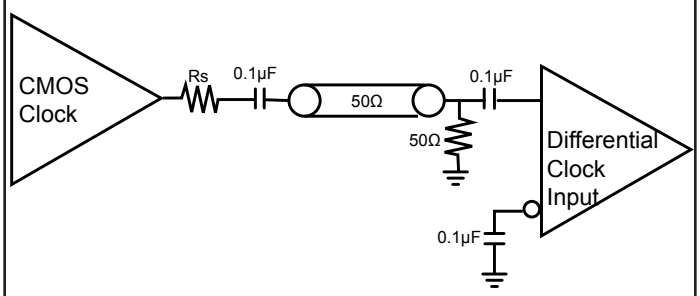
As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and 0.1µF an 1µF bypass capacitors should be used for each pin.



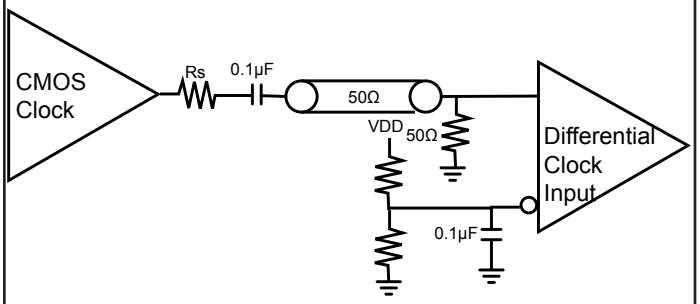
Driving X1 with a Single Ended Input



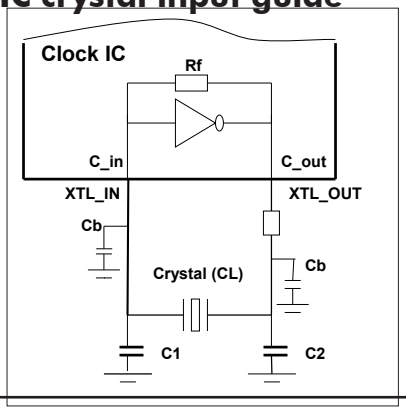
Single Ended Input, AC couple



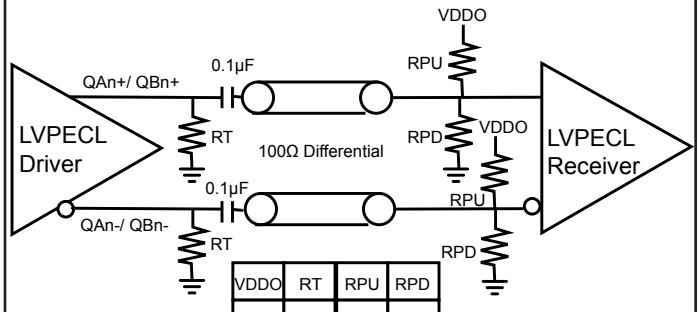
Single Ended Input, DC couple



Clock IC crystal input guide

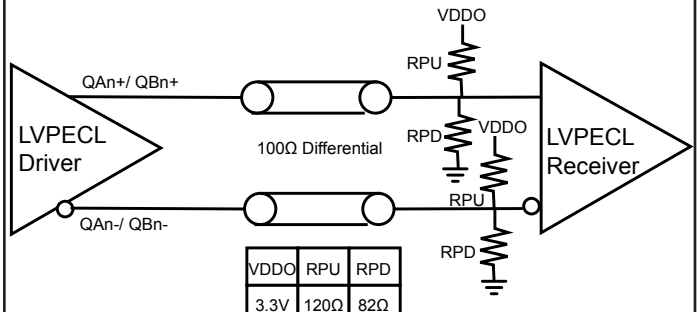


LVPECL, AC Couple, Thevenin Equivalent



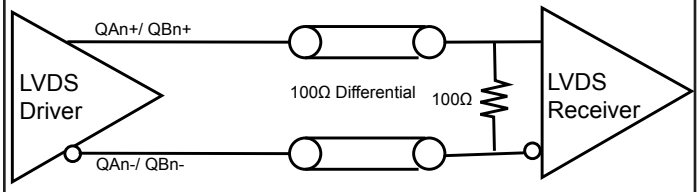
VDDO	RT	RPU	RPD
3.3V	160Ω	120Ω	82Ω
2.5V	91Ω	250Ω	62.5Ω

LVPECL, DC Couple, Thevenin Equivalent

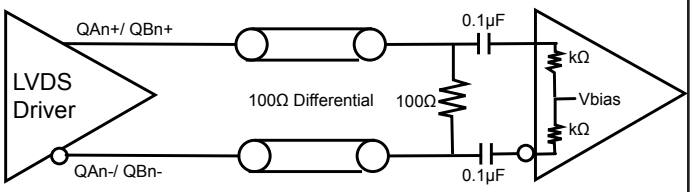


VDDO	RPU	RPD
3.3V	120Ω	82Ω
2.5V	250Ω	62.5Ω

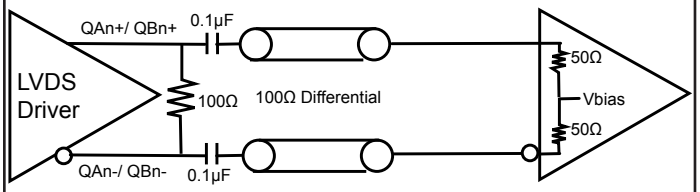
LVDS DC Couple



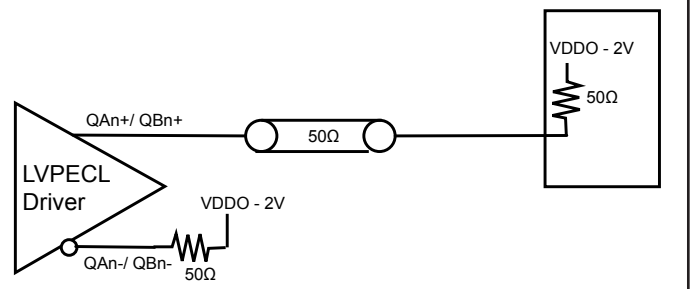
LVDS AC Couple at Load



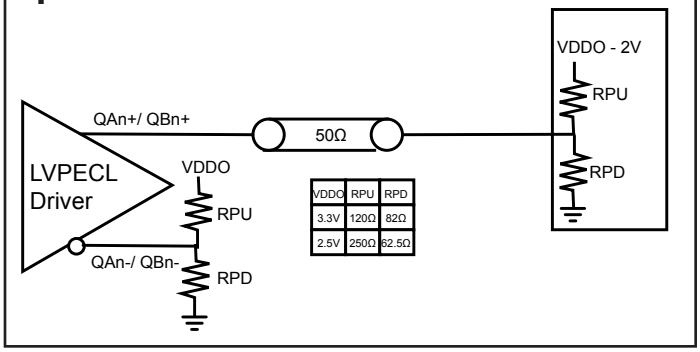
LVDS AC Couple with Internal Termination



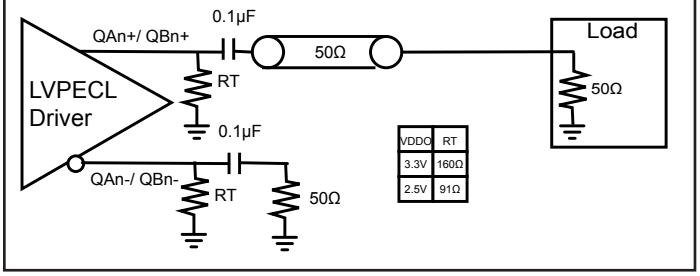
Single Ended LVPECL, DC Couple



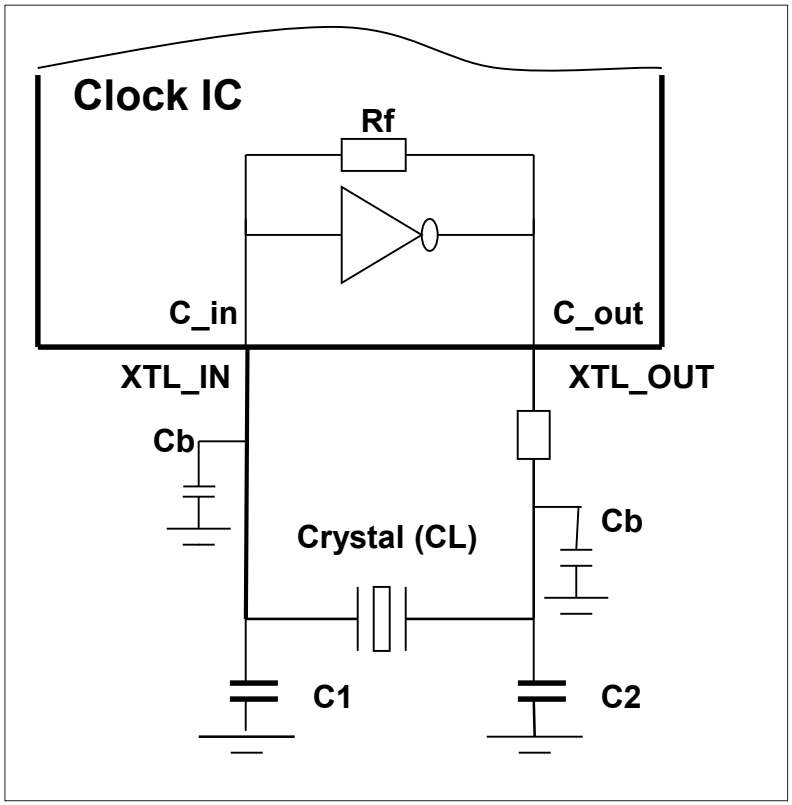
Single Ended LVPECL, DC Couple, Thevenin Equivalent



Single Ended LVPECL, AC Couple, Thevenin Equivalent



Clock IC Crystal loading cap. design guide



CL =crystal spec. loading cap.

C_in/out = (3~5pF) of IC pin cap.

Cb = PCB trace (2~4pF)

C1,C2 = load cap. of design

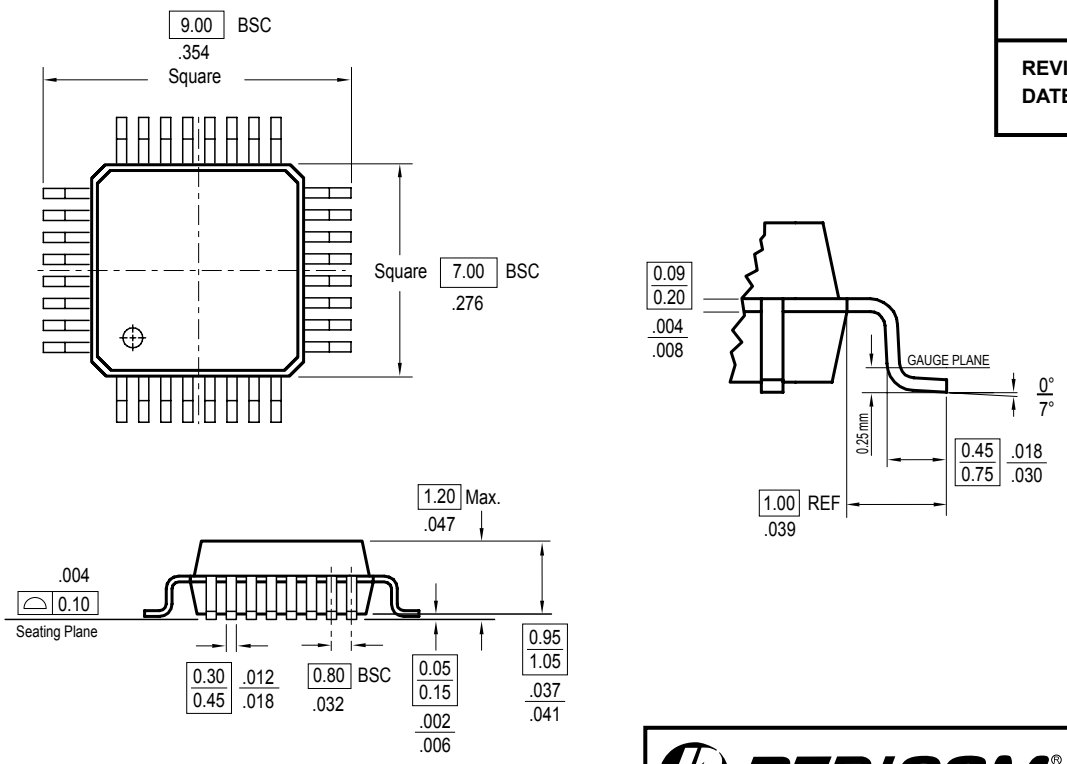
Rd = 50 to 100ohm drive level limit

Design guide: C1=C2=2 *CL - (Cb +C_in/out) to meet target +/-ppm < 20 ppm

Example1: Select CL=18 pF crystal, C1=C2=2*(18pF) – (4pF+5pF)=27pF, check datasheet too

Example2: For higher frequency crystal (=>20MHz), can use formula C1=C2=2*(CL-6), can do fine tune of C1, C2 for more accurate ppm if necessary

Packaging Mechanical:



Notes:
1. Controlling dimensions in millimeters
2. Ref.: JEDEC MS-026D/ABA
3. Package Outline Exclusive of Mold Flash and Metal Burr

DOCUMENT CONTROL NO.
PD - 1814

REVISION: C
DATE: 03/09/05

PERICOM®
Pericom Semiconductor Corporation
3545 N. 1st Street, San Jose, CA 95134
1-800-435-2335 • www.pericom.com

DESCRIPTION: 32-Pin, Thin Quad Flat Package, TQFP

PACKAGE CODE: FA

Ordering Code	Package Code	Package Type	Operating Temperature
PI6C49S1506FAIE	FA	Pb-free & Green, 32-pin TQFP	-40 °C to 85 °C

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

2. "E" denotes Pb-free and Green

3. Adding an "X" at the end of the ordering code denotes tape and Reel packaging

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- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
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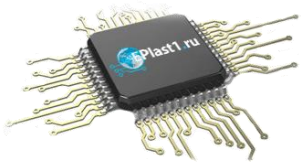
- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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