

## Differential Receiver Evaluation Boards for Amplifiers Offered in 8-Lead SOIC and MSOP Packages

### INTRODUCTION

The Analog Devices, Inc., differential receiver evaluation boards (for the MSOP and SOIC) make it easy for designers to quickly assess the performance of a particular differential receiver application circuit. The evaluation board is a bare board (that is, there are no components soldered to the board) that is very flexible and allows for several feedback configurations, common-mode and differential input terminations, reference voltage applications, and other circuit features. Most resistors and capacitors on the board are in 1206 packages.

### DEVICES COVERED

The boards are used for the [AD8129](#) and [AD8130](#).

### POWER SUPPLIES

Power is applied to the boards through J1, a Molex 0022112032 3-pin header. Pin 1 (square footprint) is for the positive supply, Pin 3 is for the negative supply, and Pin 2 is connected to the ground plane of the board. Alternatively, looped test points can be used: TP6 connects to the positive supply, TP7 connects to the negative supply, and TP8, TP9, TP10, and TP11 connect to the ground plane (see Figure 1).

The board can accommodate single and dual supplies. For single-supply operation, connect the negative supply to the ground plane.

It is very important that the power supply pins of the device under test (DUT) have decoupling circuitry. The board layout facilitates such decoupling by including footprints for a 1206 ceramic capacitor on each supply. For broadband decoupling, it is recommended that two ceramic capacitors be used: one for lower frequencies and one for higher frequencies. To use two capacitors on each supply, stack two 1206 ceramic capacitors on the same footprint. Bulk decoupling is provided by C1 and C3; 10  $\mu$ F tantalum capacitors are recommended.

### FEEDBACK NETWORKS AND INPUT/OUTPUT TERMINATIONS

Figure 1 shows the schematic for the evaluation boards. R5 and R6 compose the resistive feedback loop that can be returned to ground through R8 or to the reference voltage circuitry, VR1 and C7. Capacitor C5 and Capacitor C6 are included across the feedback resistor and gain resistor, respectively, to implement first-order frequency response shaping. C6 introduces a pole into the feedback loop, which must be compensated for by C5.

A reference voltage can be injected at Pin 4 of the DUT. Using Potentiometer VR1, which spans the power supplies, the designer can adjust the reference voltage over a wide range. C7 provides bypassing on the wiper of VR1. A test point, TP5, is provided for monitoring the reference voltage. When VR1 is used, it is important to ensure that JU3 is shorted.

To minimize parasitic summing node capacitance, the ground plane has been voided under and around Pin 5 of the DUT and the copper that connects to it.

Differential termination is provided by R3, and common-mode terminations are provided by R1 and R2. C9 and C10 allow optional input ac coupling and must be shorted across when not used. JU1 provides the means to directly monitor the differential input by using a suitable high impedance differential probe, or to directly short across the differential inputs for test purposes. Standard 0.100-inch pitch headers can be used in JU1. Alternatively, TP2 and TP3, which accommodate looped-type test points, can be used.

A source termination resistor, R7, is included on the output to facilitate driving coaxial cables and test equipment. The output signal can be monitored before the source termination resistor at TP4. Because TP4 is the direct amplifier output, any test equipment connected to TP4 adds to the capacitive load of the amplifier, thus diminishing the phase margin. Extreme care should be exercised when connecting test equipment to TP4.

### INPUT/OUTPUT CONNECTORS

The inputs and outputs have edge-mounted Subminiature A (SMA) connectors for straightforward connection to coaxial cables. Johnson Components Part Number 142-0701-801, or the equivalent, is recommended. On the inputs, TP13 and TP14 provide the option of using straight or right-angle through-hole SMA connectors.

### POWER-DOWN

Pull-up Resistor R4 and Jumper JU2 make it easy for the power-down feature of the DUT to be asserted. The recommended value for R4 is 1 k $\Omega$ . As with JU1, a 0.100-inch pitch header can be used for JU2.

### OTHER COMPONENTS

There may be application circuits where footprints for desired components are not available on the board. In these cases, the user is encouraged to use his or her ingenuity to find ways to include them.

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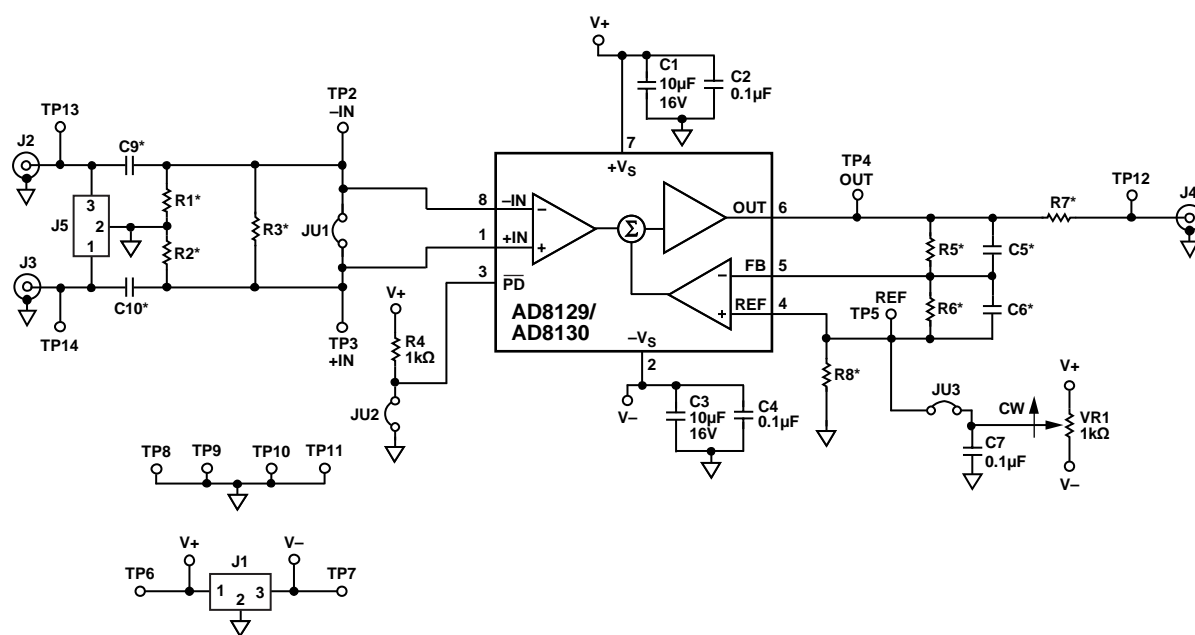
REVISION HISTORY

9/12—Rev. 0 to Rev. A

Changes to Introduction Section.....	1
Changes to Figure 2 to Figure 7 .....	4
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4/10—Revision 0: Initial Version

## EVALUATION BOARD SCHEMATIC AND ARTWORK

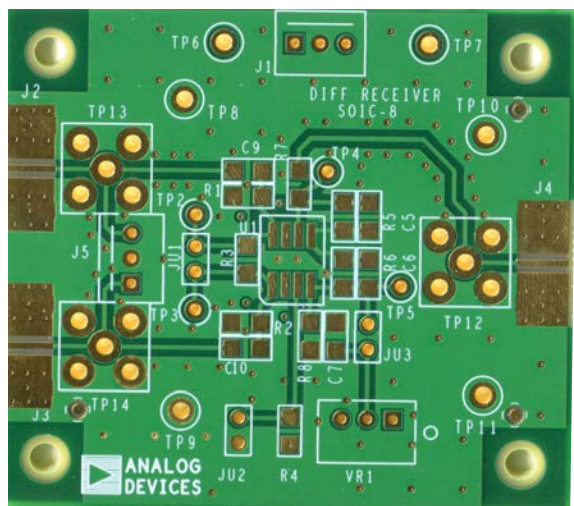


\*USER-DEFINED VALUE.

Figure 1. Differential Receiver Evaluation Board Schematic

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## SOIC EVALUATION BOARDS (R)



## NOTES

1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELLING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

Figure 2. Evaluation Board Photo, Component Side

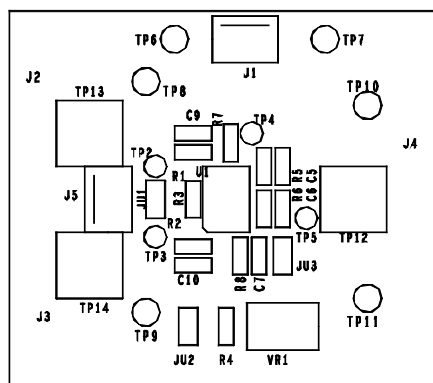


Figure 3. Assembly Drawing, Component Side

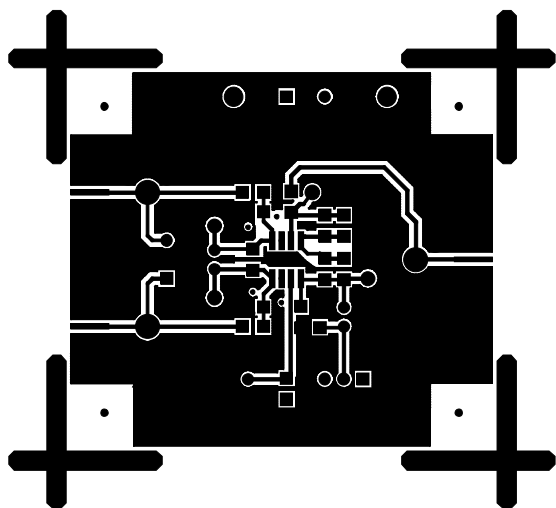


Figure 4. Board Layout Pattern, Component Side



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1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELLING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

Figure 5. Evaluation Board Photo, Circuit Side

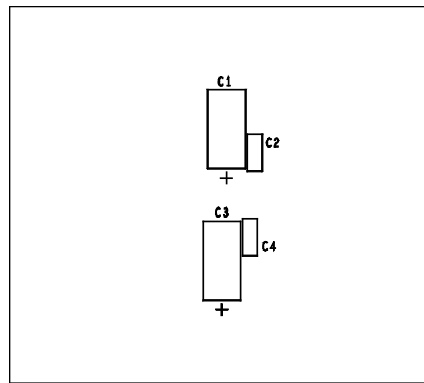


Figure 6. Assembly Drawing, Circuit Side

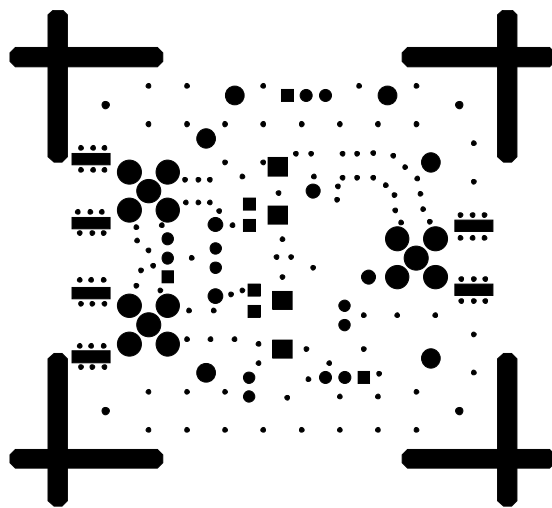
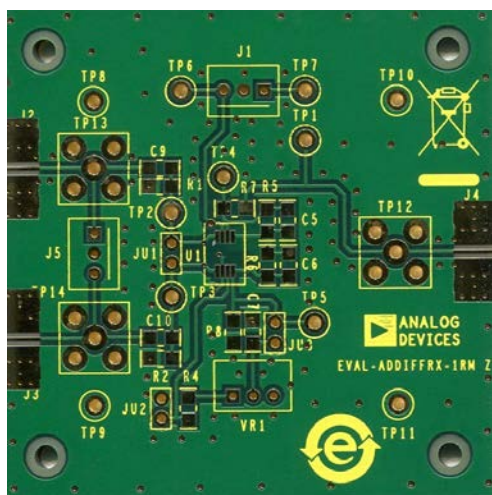


Figure 7. Board Layout Pattern, Circuit Side

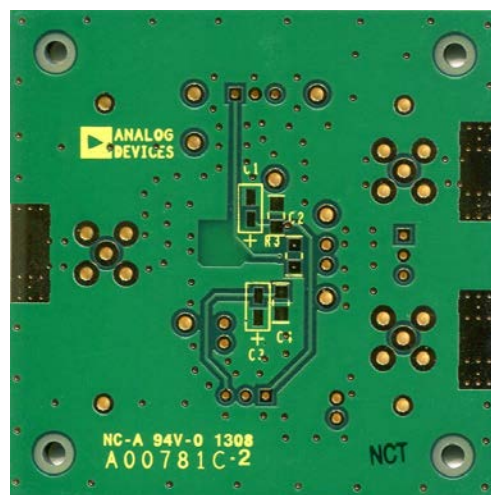
MSOP EVALUATION BOARDS (RM)



NOTES  
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELLING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

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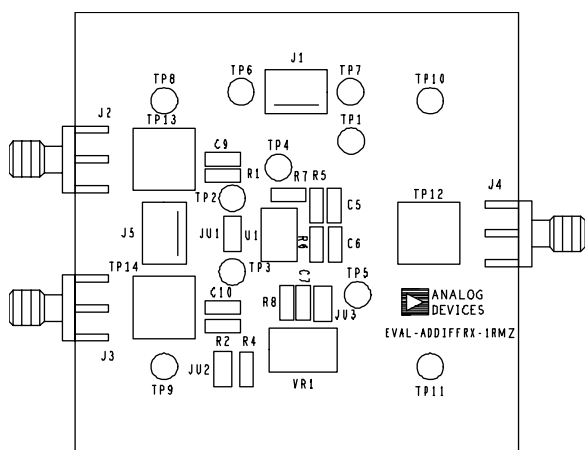
Figure 8. Evaluation Board Photo, Component Side



NOTES  
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELLING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

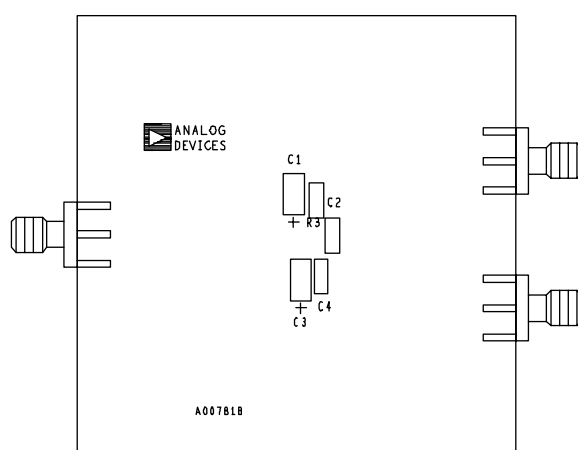
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Figure 11. Evaluation Board Photo, Circuit Side



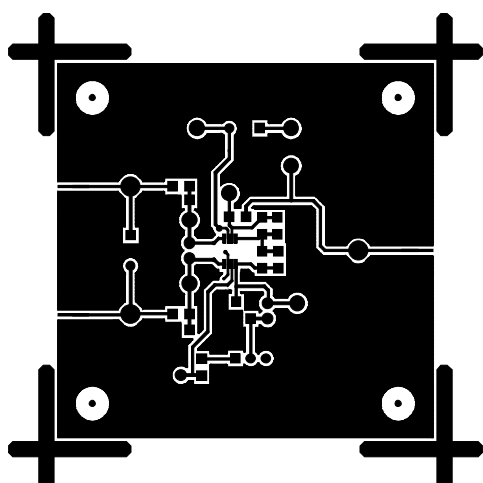
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Figure 9. Assembly Drawing, Component Side



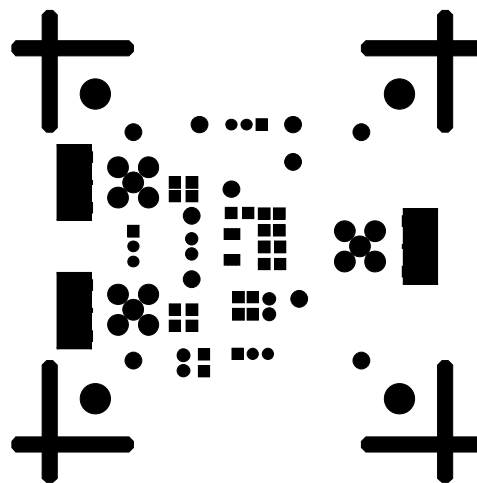
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Figure 12. Assembly Drawing, Circuit Side



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Figure 10. Board Layout Pattern, Component Side



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Figure 13. Board Layout Pattern, Circuit Side

## ORDERING INFORMATION

### BILL OF MATERIALS

Table 1.

Quantity	Reference Designator	Description	Package
1	U1	Amplifier	8-lead SOIC, 8-lead MSOP
2	C1, C3	10 $\mu$ F, capacitor	7343 (SOIC), 3216 (MSOP)
3	C2, C4, C7	0.1 $\mu$ F capacitor	1206
4	C5, C6, C9, C10	User-defined values capacitor	1206
2	J1, J5	3-pin Molex	PWR_CONN_6-9-2
7	R1, R2, R3, R5, R6, R7, R8	User-defined values resistor	1206
1	R4	1 k $\Omega$ resistor	1206
1	VR1	1 k $\Omega$ resistor	3299W
3	JU1, JU2, JU3	Jumper	BERG2
10	TP2 to TP11	Test point	TP1
3	J2, J3, J4,	SMA surface-mount technology (SMT)	SMASMT
3	TP12, TP13, TP14	SMA connector	SMACON

### RELATED LINKS

Resource	Description
<a href="#">AD8129</a>	Product Page, <a href="#">AD8129</a> Low Cost 200 MHz Differential Receiver Amplifier
<a href="#">AD8130</a>	Product Page, <a href="#">AD8130</a> Low Cost 270 MHz Differential Receiver Amplifier

## NOTES

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**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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